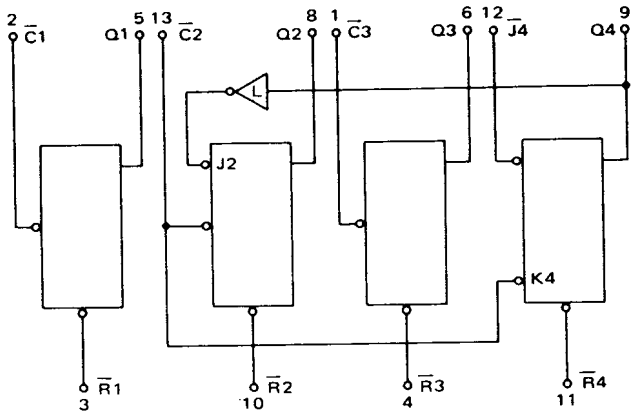
4-BIT UNIVERSAL COUNTER

# MC4323
# MC4023




$V_{CC}$ = Pin 14
GND = Pin 7

Input Loading Factor:
$\bar{J}$ = 1
$\bar{C}1$, $\bar{C}3$ = 2
$\bar{C}2$, $\bar{R}$ = 3

Output Loading Factor = 10

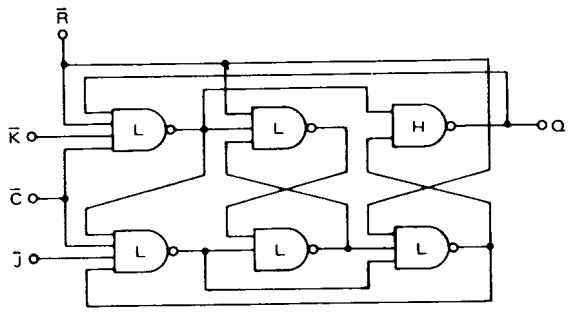
Total Power Dissipation = 200 mW typ/pkg
Propagation Delay Time = 16 ns typ/bit
Operating Frequency = 30 MHz typ

This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

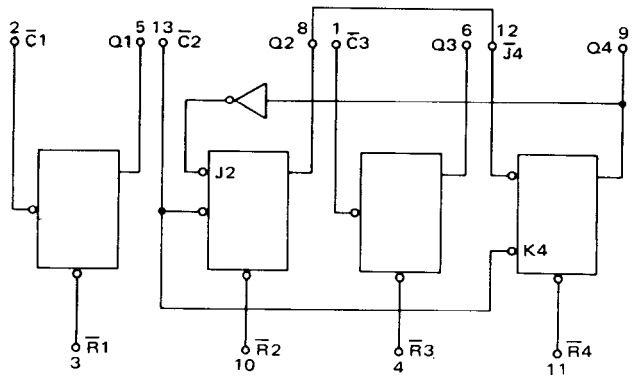
Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

## LOGIC DIAGRAM

One flip-flop shown. Only inputs shown on block diagram are present.



## COUNTING SEQUENCES




**DIVIDE BY 3**

| C̄2 | Q2 | Q4 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 0 |
| 2 | 0 | 1 |

**DIVIDE BY 4**

| C̄1 | Q1 | Q3 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 0 |
| 2 | 0 | 1 |
| 3 | 1 | 1 |

**DIVIDE BY 6**

| C̄1 | Q1 | Q2 | Q4 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |

**DIVIDE BY 12**

| C̄3 | Q3 | Q1 | Q2 | Q4 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |

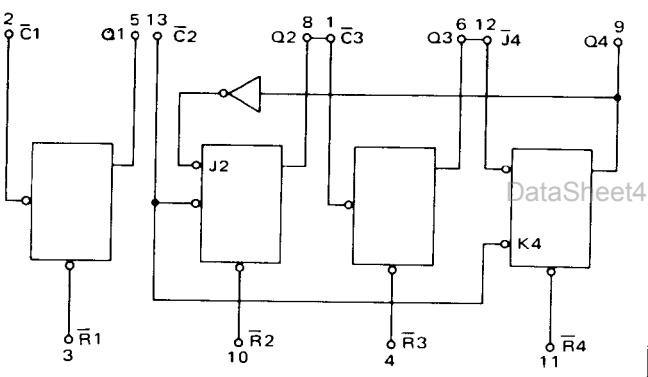
DIVIDE BY 2: Use flip-flop 1 or 3.

DIVIDE BY 3: Use flip-flops 2 and 4, connected as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 4: Use flip-flops 1 and 3; connect Q1 to C̄3. Apply the input signal to C̄1.

DIVIDE BY 6: In addition to the connection for divide by 3, connect Q1 to C̄2. Apply the input signal to C̄1.

DIVIDE BY 12: In addition to the connections for divide by 6, connect Q3 to C̄1. Apply the input signal to C̄3.




**DIVIDE BY 5**

| C̄2 | Q2 | Q3 | Q4 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |

**DIVIDE BY 8**

| C̄1 | Q1 | Q2 | Q3 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 |
| 7 | 1 | 1 | 1 |

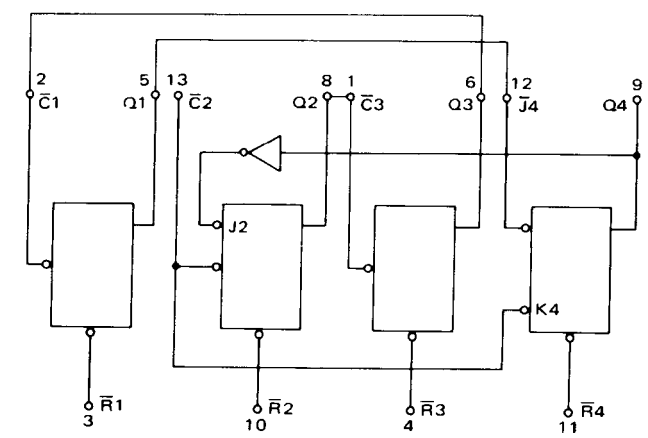
**DIVIDE BY 10**

| C̄1 | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |

DIVIDE BY 5: Connect flip-flops 2, 3, and 4 as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 8: Connect flip-flops 2 and 3 as shown for divide by 5, but do not connect Q3 to J̄4. Connect Q1 to C̄2. The input signal is applied to C̄1; the output is taken from Q3.

DIVIDE BY 10: In addition to the connections for divide by 5, connect Q1 to C̄2. Apply the input signal to C̄1.




**DIVIDE BY 9**

| C̄2 | Q2 | Q3 | Q1 | Q4 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |

DIVIDE BY 9: The input signal is applied to C̄2; the output is taken from Q4.