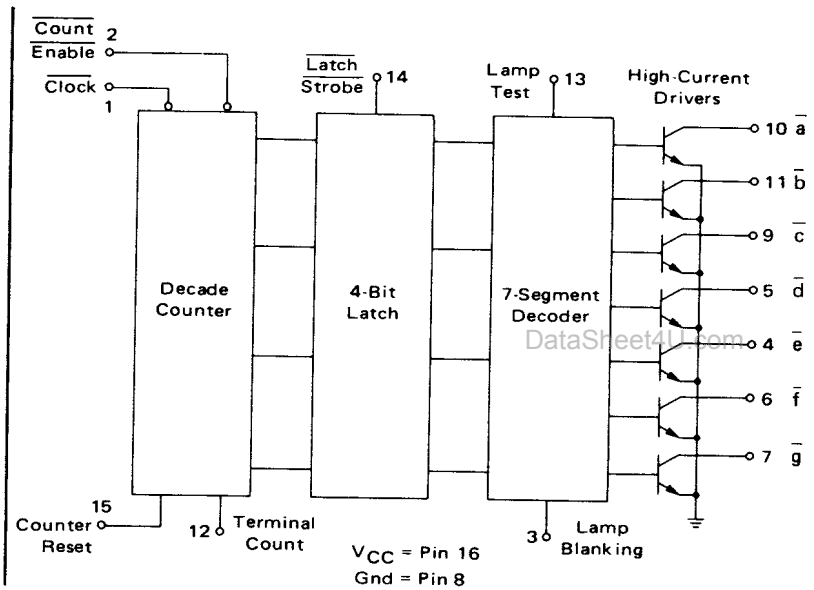
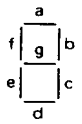
COUNTER-LATCH DECODER

MC4350
MC4050

This monolithic integrated circuit combines the functions of a binary coded decimal counter, a four-bit latch, and a seven-segment decoder/driver. Designed primarily for counting applications such as frequency counters, the circuit contains a leading zero blanking feature activated through the Reset input. For this reason the MC4350/4050 is useful in systems using automatic decimal ranging and/or automatic time base selection. A $\overline{\text{Count}}$ $\overline{\text{Enable}}$ input gates the clock input without restrictions on the clock level and without false-clocking the counter. The Terminal Count is high driving the ninth count, allowing synchronous or asynchronous counter operation when used in conjunction with the $\overline{\text{Count}}$ $\overline{\text{Enable}}$ input and external gating. The Counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. The latch section admits information while the $\overline{\text{Latch}}$ $\overline{\text{Strobe}}$ is high and latches the data on the negative edge of the strobe. The seven-segment decoder/driver provides up to 40 mA drive capability for displays requiring current sinking in the active mode. A lamp blanking input provides intensity modulation. A lamp test feature is also available.



SEGMENT IDENTIFICATION



Total Power Dissipation = 450 mW typ/package
Maximum Toggle Frequency = 40 MHz typ

FUNCTIONAL TRUTH TABLE

FUNCTION		INPUT $\overline{\text{CLOCK}}$	$\overline{\text{CE}}$	CR	$\overline{\text{LST}}$	LT	LB	OUTPUT TC	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$
Lamp Test		X	X	X	X	1	X	–	0	0	0	0	0	0	0
Lamp Blanking		X	X	X	X	0	1	–	1	1	1	1	1	1	1
Reset		X	X	1	1	0	0	0	1	1	1	1	1	1	1
$\overline{\text{Enable}}$		P	1	0	1	0	0	0	1	1	1	1	1	1	1
State Sequence	1	P1	0	0	1	0	0	0	1	0	0	1	1	1	1
	2	P2	0	0	1	0	0	0	0	0	1	0	0	1	0
	3	P3	0	0	1	0	0	0	0	0	0	0	1	1	0
	4	P4	0	0	1	0	0	0	1	0	0	1	1	0	0
	5	P5	0	0	1	0	0	0	0	1	0	0	1	0	0
	6	P6	0	0	1	0	0	0	0	1	0	0	0	0	0
	7	P7	0	0	1	0	0	0	0	0	0	1	1	1	1
	8	P8	0	0	1	0	0	0	0	0	0	0	0	0	0
	9	P9	0	0	1	0	0	1	0	0	0	0	1	0	0
	0	P10	0	0	1	0	0	0	0	0	0	0	0	0	1
	1	P11	0	0	1	0	0	0	1	0	0	1	1	1	1
	Latch	P	0	0	0	0	0	0	1	0	0	1	1	1	1

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care

FUNCTION DESCRIPTION

The MC4350/4050 is suited for driving incandescent seven-segment decimal indicators. In addition, only current limiting resistors are needed to allow driving hybrid LED's in the 2.4-volt per segment capability range with common-anode configuration. Use the MC4051 for monolithic LED arrays with common-cathode connection.

Logic "1" allows decoder to be driven directly from counter outputs. Logic "0" stores counter output data as it was immediately prior to "1" to "0" transition.

This input has no effect on the circuit if LT is at logic "1". With LT = logic "0", a logic "1" at this input turns off outputs $\bar{a}$ thru $\bar{g}$; a logic "0" allows $\bar{a}$ thru $\bar{g}$ to display normally.

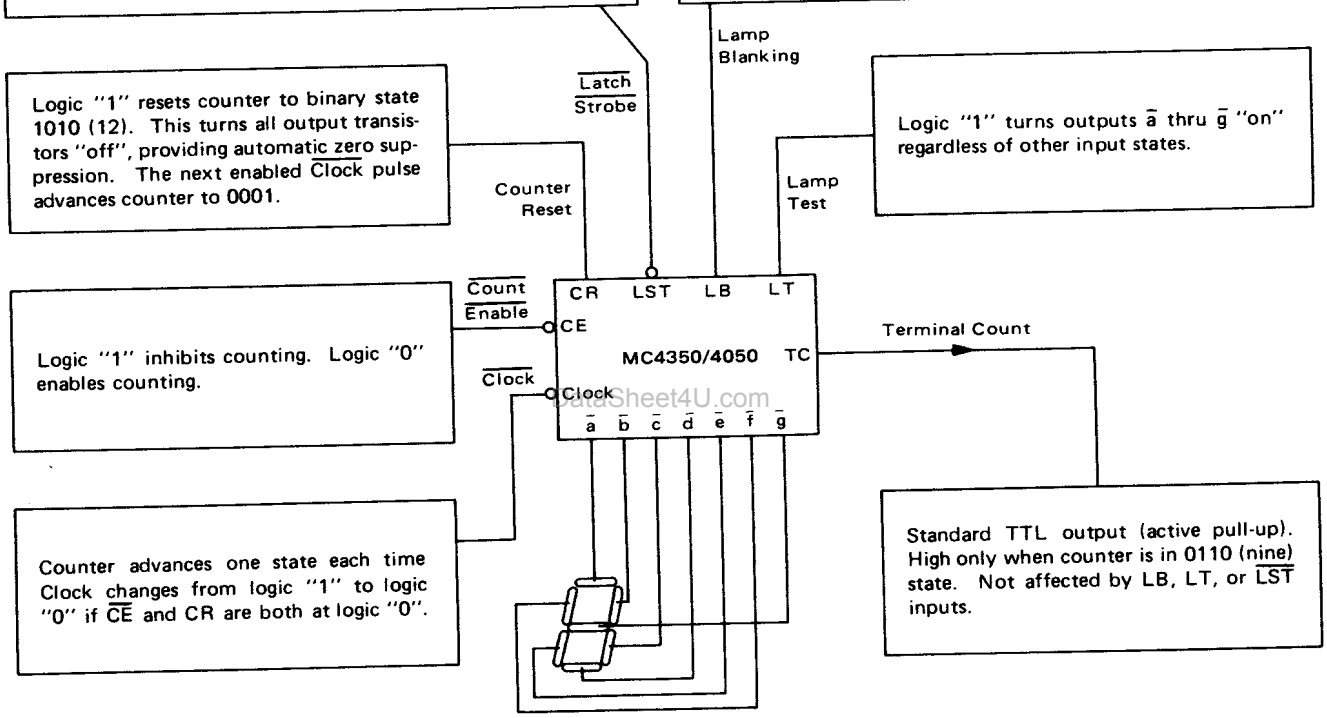
Logic "1" resets counter to binary state 1010 (12). This turns all output transistors "off", providing automatic zero suppression. The next enabled $\overline{\text{Clock}}$ pulse advances counter to 0001.

Logic "1" turns outputs $\bar{a}$ thru $\bar{g}$ "on" regardless of other input states.

Logic "1" inhibits counting. Logic "0" enables counting.

Counter advances one state each time Clock changes from logic "1" to logic "0" if $\overline{\text{CE}}$ and CR are both at logic "0".

Standard TTL output (active pull-up). High only when counter is in 0110 (nine) state. Not affected by LB, LT, or $\overline{\text{LST}}$ inputs.



OPERATING DETAILS

- $\overline{\text{Count Enable}}$ may be changed with $\overline{\text{Clock}}$ either high or low.
- Counter Reset overrides $\overline{\text{Count Enable}}$ and $\overline{\text{Clock}}$. It may be changed regardless of levels present at $\overline{\text{Count Enable}}$ and $\overline{\text{Clock}}$.
- $\overline{\text{Latch Strobe}}$, Lamp Blanking, and Lamp Test may be changed regardless of levels at $\overline{\text{Count Enable}}$, $\overline{\text{Clock}}$, and Counter Reset.
- Refer to Timing Diagram if a logic "1" to "0" transition on $\overline{\text{Clock}}$ can occur while levels are changing on $\overline{\text{Count Enable}}$ or $\overline{\text{Latch Strobe}}$, or if a logic "0" to "1" transition of Counter Reset can occur simultaneously with a "0" to "1" transition of $\overline{\text{Latch Strobe}}$.
- Tie all unused inputs to ground except for $\overline{\text{Latch Strobe}}$, which must be returned to a logic "1" level if not used.
- Outputs $\bar{a}$ thru $\bar{g}$ are open-collector transistors capable of sinking 40 mAdc with outputs low, and sustaining 8.0 Vdc minimum (15 Vdc typical) with outputs high.