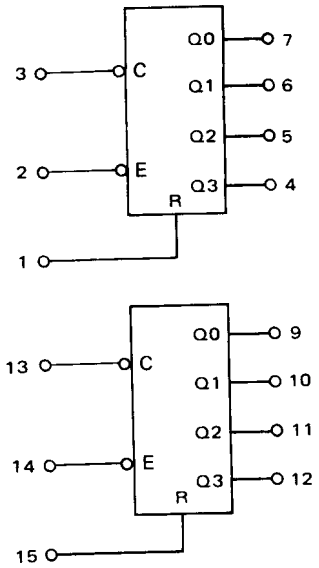
DUAL DECADE COUNTER

MC4352
MC4052

DUAL HEXADECIMAL COUNTER

MC4353
MC4053



V_{CC} = Pin 16
Gnd = Pin 8

The MC4352/4052 and MC4353/4053 consist of two independent up counters. The counters advance on the negative edge of the $\overline{\text{clock}}$ when the $\overline{\text{enable}}$ input is low. The count is held when the $\overline{\text{enable}}$ input is high. The $\overline{\text{enable}}$ input should not be taken to the high level while the $\overline{\text{clock}}$ is high, as erroneous triggering can result. A high level on the reset input places the counter in the 0000 state, overriding the $\overline{\text{clock}}$ and $\overline{\text{enable}}$ inputs. As charge control steering is utilized in this design, capacitive loading on the outputs should be kept at a minimum.

Total Power Dissipation = 350 mW typ/pkg
Maximum Toggle Frequency = 40 MHz typ

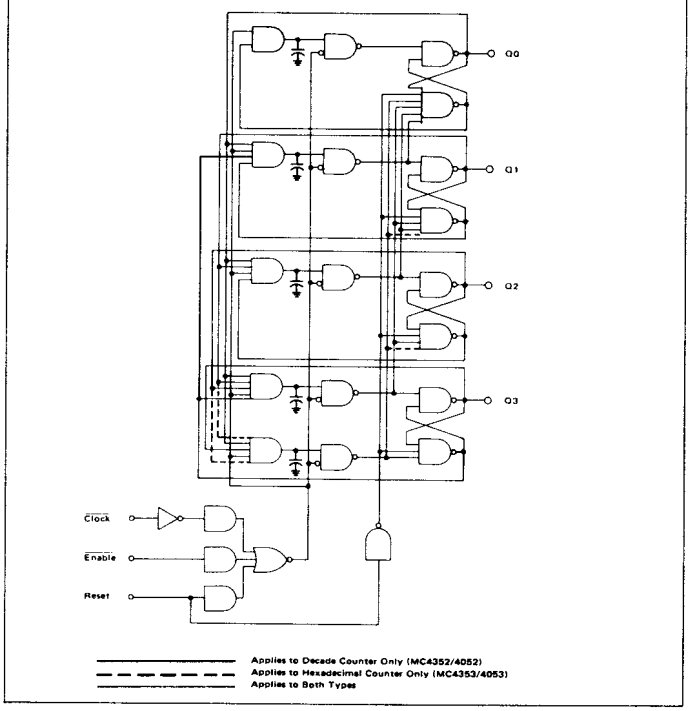
FUNCTIONAL TRUTH TABLE

INPUT			MC4352/4052 OUTPUT				MC4353/4053 OUTPUT			
R	$\overline{E}$	$\overline{C}$	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
1	X	X	0	0	0	0	0	0	0	0
0	1	P	0	0	0	0	0	0	0	0
0	0	P1	0	0	0	1	0	0	0	1
0	0	P2	0	0	1	0	0	0	1	0
0	0	P3	0	0	1	1	0	0	1	1
0	0	P4	0	1	0	0	0	1	0	0
0	0	P5	0	1	0	1	0	1	0	1
0	0	P6	0	1	1	0	0	1	1	0
0	0	P7	0	1	1	1	0	1	1	1
0	0	P8	1	0	0	0	1	0	0	0
0	0	P9	1	0	0	1	1	0	0	1
0	0	P10	0	0	0	0	1	0	1	0
0	0	P11	0	0	0	1	1	0	1	1
0	0	P12	Above Sequence Repeats				1	1	0	0
0	0	P13					1	1	0	1
0	0	P14					1	1	1	0
0	0	P15					1	1	1	1
0	0	P16					0	0	0	0
0	0	P17					0	0	0	1

Reset
Enable

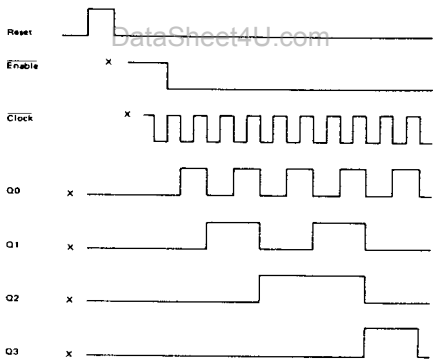
P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't Care

LOGIC DIAGRAM
(1/2 of Device Shown)

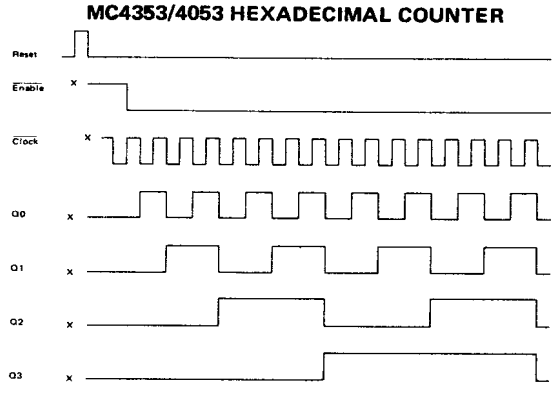


FUNCTIONAL DIAGRAMS

MC4352/4052 DECADE COUNTER



MC4353/4053 HEXADECIMAL COUNTER



X = Don't care