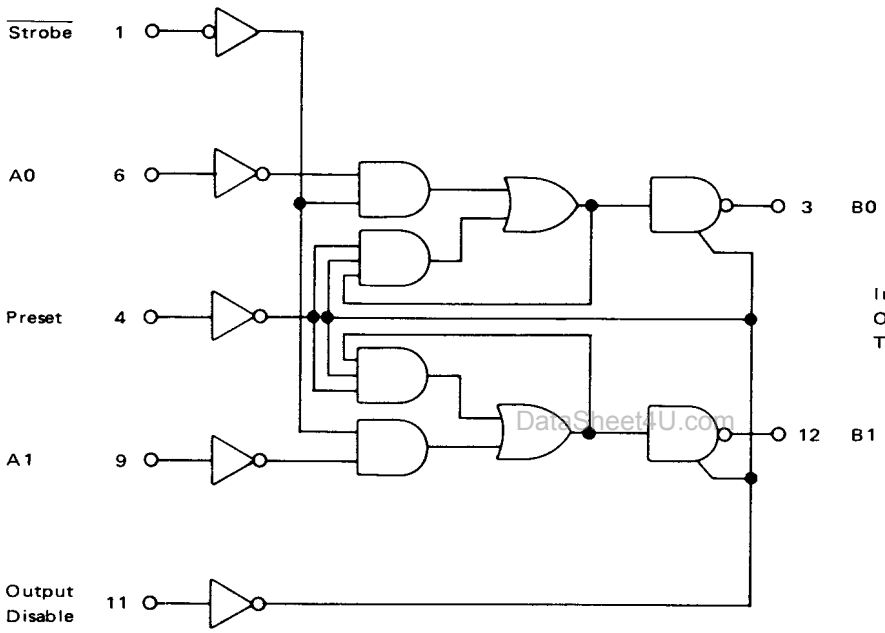
DUAL MOS-TO-TTL
LEVEL TRANSLATOR
WITH THREE-STATE OUTPUT

MC4368
MC4068

The MC4368/4068 is a dual MOS-to-TTL translator designed to sense the open-drain output current of MOS memories such as the 1103 type. The device has several features that greatly enhance system performance and reduce package count: (1) no external components are required for interfacing, (2) current rather than voltage is sensed, (3) latch capabilities are available, (4) the device has bus driver capabilities, (5) the three-state output feature allows a number of outputs to be tied together on a common data bus without sacrificing the speed of the totem pole output, and (6) only the standard TTL 5-volt power supply is required.



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 150 mW typ/pkg

A0 and A1 are current sensing inputs.

For maximum noise suppression, also connect pins 5, 8 and 10 to ground (they are internally connected to substrate).

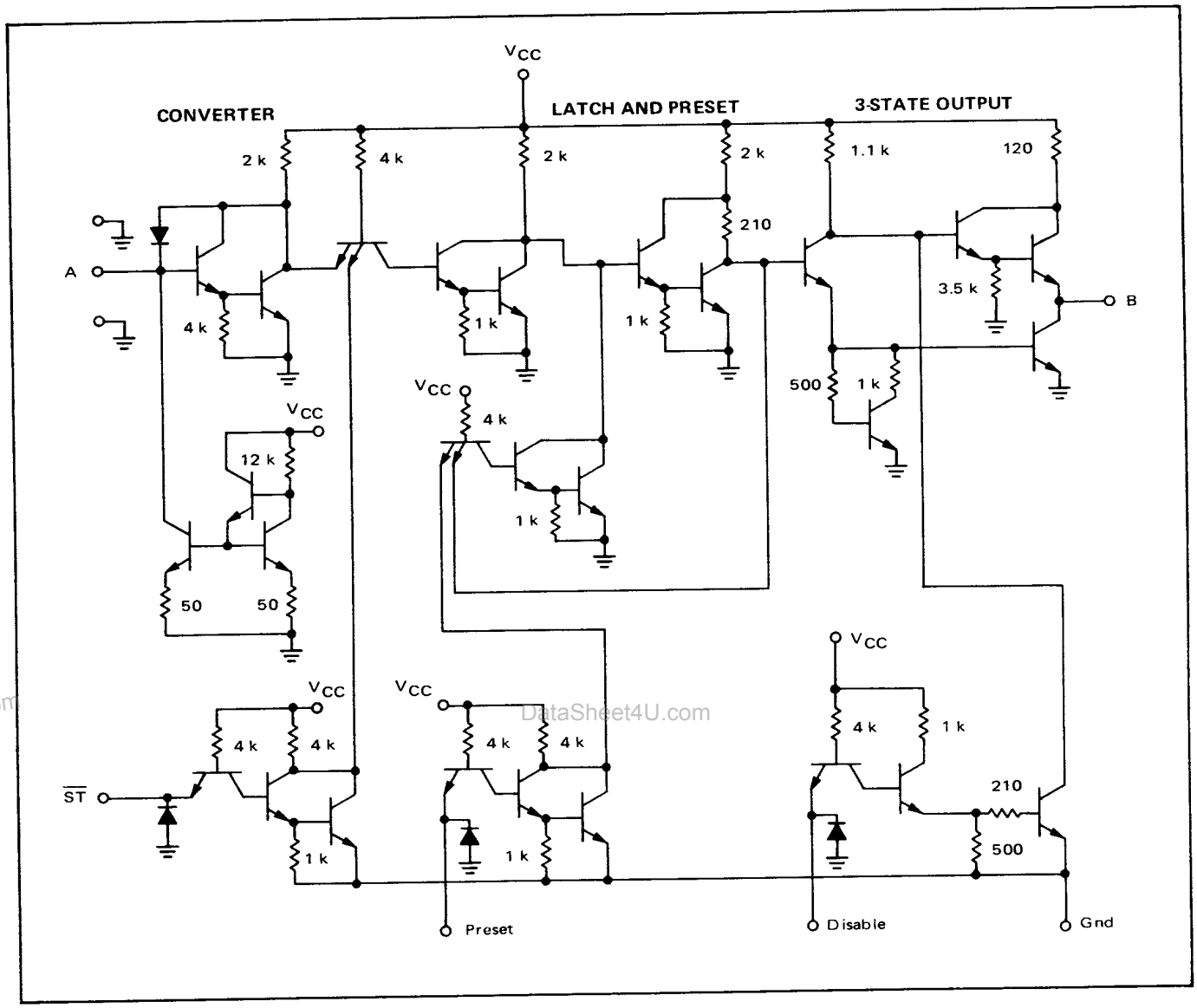
V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

DIS	$\overline{ST}$	P	A0	A1	B0	B1
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{IHT}	I_{S2}	I_{S2}	V_{OH}	V_{OH}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OH}	V_{OH}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S1}	I_{S1}	V_{OH}	V_{OH}
V_{ILT}	V_{ILT}	V_{ILT}	I_{S1}	I_{S1}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S1}	I_{S1}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OL}	V_{OL}
V_{IHT}	V_{ILT}	V_{ILT}	I_{S1}	I_{S1}	H*	H*
V_{IHT}	V_{IHT}	V_{IHT}	I_{S1}	I_{S1}	L**	L**

Ground pins 5, 7, 8, and 10.
*Outputs connected to V_{CC} thru 470 ohm resistor, H = 4.88 V min.
**Outputs connected to ground thru 220 ohm resistor, L = 55 mV max.

CIRCUIT SCHEMATIC
(1/2 of Device and Common Inputs Shown)



OPERATING CHARACTERISTICS

The MC4368/4068 is divided into three basic functions: (1) conversion of the MOS cell current to TTL voltage levels, (2) latching, and (3) coupling to the data bus.

The converter uses a darlington with negative feedback which provides a low input impedance and a fast recovery of the cell data line from noise. A fixed current logic threshold is provided by a sense amplifier arrangement. This threshold is nominally equal to one half of the minimum cell output current and is relatively unaffected by changes in temperature and power supply voltage. Ground pins are provided on each side of the current inputs. These effectively isolate the sensitive inputs from transients.

The latch contains two darlington NANDs which are ORed into another darlington. One NAND is used to strobe the converted MOS cell output into the latch and the other provides feedback for the latch and the preset function.

The latch is then coupled to the output data bus via a three-state output, which allows a number of these outputs to be tied together on a common data bus without sacrificing the speed of the totem pole output.