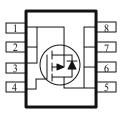
## P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r<sub>DS(on)</sub> provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$r_{\mathrm{DS(on)}} m(\Omega)$	I <sub>D</sub> (A)	
-30	$13 @ V_{GS} = -10V$	-11.5	
	$19 @ V_{GS} = -4.5V$	-9.3	





ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V <sub>DS</sub>	-30	V	
Gate-Source Voltage		V <sub>GS</sub>	±25	v	
	$T_A=25^{\circ}C$	т_	-11.5		
Continuous Drain Current <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	-9.3	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	±50		
Continuous Source Current (Diode Conduction) <sup>a</sup>		Is	-2.1	А	
	$T_A=25^{\circ}C$	D	3.1	W	
Power Dissipation <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	гD	2.3		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Case <sup>a</sup>	t <= 5 sec	$R_{\theta JC}$	25	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	t <= 5 sec	$R_{\theta JA}$	50	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

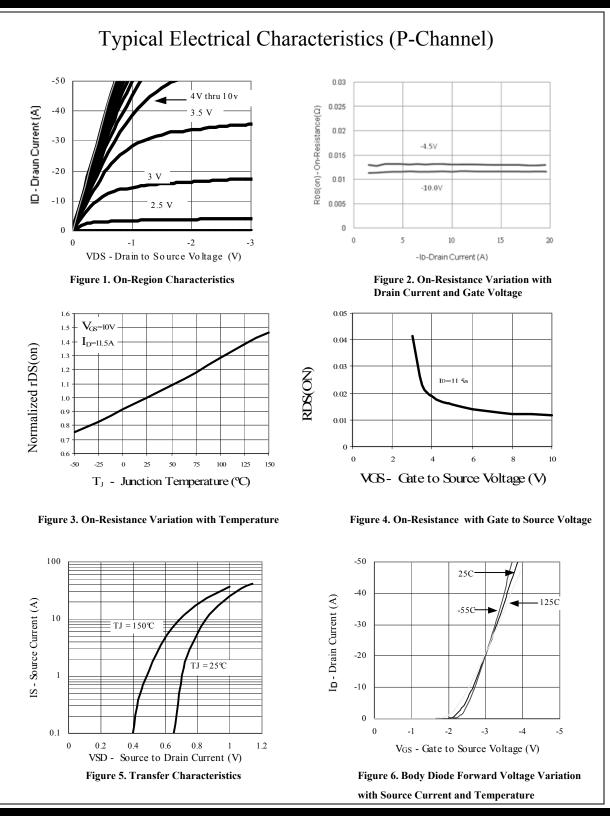
SPECIFICATIONS ( $T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
Parameter	O	T ( O	Limits			11	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS}$ = 0 V, I <sub>D</sub> = -250 uA	-30			v	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \text{ uA}$	-1			v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = ±25 V			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = -24 V, $V_{GS}$ = 0 V			-1	uA	
	500	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-5		
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS}$ = -5 V, $V_{GS}$ = -10 V	-50			А	
Drain-Source On-Resistance <sup>A</sup>	r <sub>ea</sub> ,	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -11.5 A			13	mΩ	
	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -9.3 A			19.0		
Forward Tranconductance <sup>A</sup>	9 <sub>fs</sub>	$V_{DS}$ = -15 V, I <sub>D</sub> = -11.5 A		29		S	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.5 A, V <sub>GS</sub> = 0 V		-0.8		V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -5 V, I <sub>D</sub> = -11.5 A		25		nC	
Gate-Source Charge	Q <sub>gs</sub>			11			
Gate-Drain Charge	Q <sub>gd</sub>			17			
Input Capacitance	C <sub>iss</sub>			2300			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		600		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			300			
Turn-On Delay Time	t <sub>d(on)</sub>			15			
Rise Time	t <sub>r</sub>	$V_{\text{DD}} = -15 \text{ V}, \text{ R}_{\text{L}} = 6 \ \Omega \ , \qquad \qquad \text{ID}$		13		nS	
Turn-Off Delay Time	t <sub>d(off)</sub>	= -1 A, VGEN = -10 V		100		113	
Fall-Time	t <sub>f</sub>			54			

Notes

a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .

b. Guaranteed by design, not subject to production testing.

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