MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44810

Product Preview

PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Section

SYSTEM 4
PLL TUNING CIRCUIT with 1.3 GHz PRESCALER

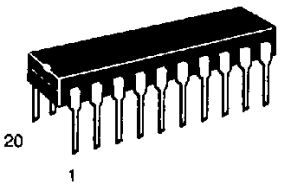
The MC44810 is a tuning circuit for TV applications. It contains a PLL section and a DAC section and is MPU controlled through the I²C Bus.

The PLL section contains all the functions required to control the VCO of a TV tuner. It generates the tuning voltage and the additional control signals (e.g. band switching voltages). The PLL section is functionally equivalent to MC44802.

The D-to-A section generates three further varactor voltages in order to feed all of the varactors of the tuner with their individually optimized control voltages (automatic tuner adjustment).

The MC44810 is manufactured on a single silicon chip using Motorola's high density bipolar MOSAIC® process (Motorola Oxide Self Aligned Implanted Circuits).

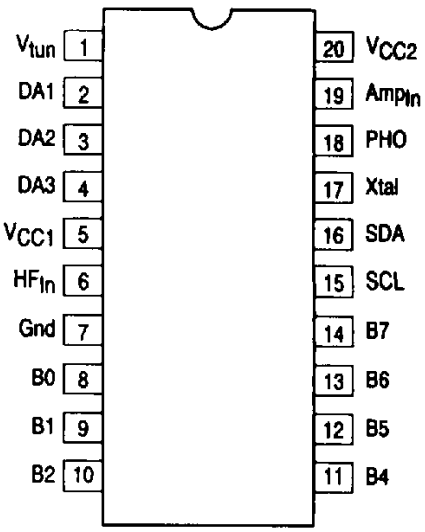
- Complete Single Chip System for MPU Control (I²C Bus)
- Selectable ÷ 8 Prescaler Accepts Frequencies Up to 1.3 GHz
- 15-Bit Programmable Divider Accepts Input Frequencies Up to 165 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (30 V)
- Seven Output Buffers: 10 mA, 12 V
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44802A
- Three 6-Bit DACs for Automatic Tuner Adjustment Allowing Use of Non-Matched Varactors
- Better Tuner Performances Through Optimum Filter Response
- Two Chip Addresses for the PLL Section and Two Different Chip Addresses for the DAC Section



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°, unless otherwise noted.)

Ratings	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	5	6.0	V
Band Buffer OFF Voltage	8 to 14	15	V
Band Buffer ON Current	8 to 14	15	mA
Op Amp Power Supply Voltage (V_{CC2})	20	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1 to 4	Continuous	sec
Storage Temperature	—	– 65 to +150	°C
Operating Temperature Range	—	0 to + 70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC44810P	0° to + 70°C	Plastic DIP
MC44810DW		SO-20L

Figure 1. Ripple Rejection - Measurement Schematic

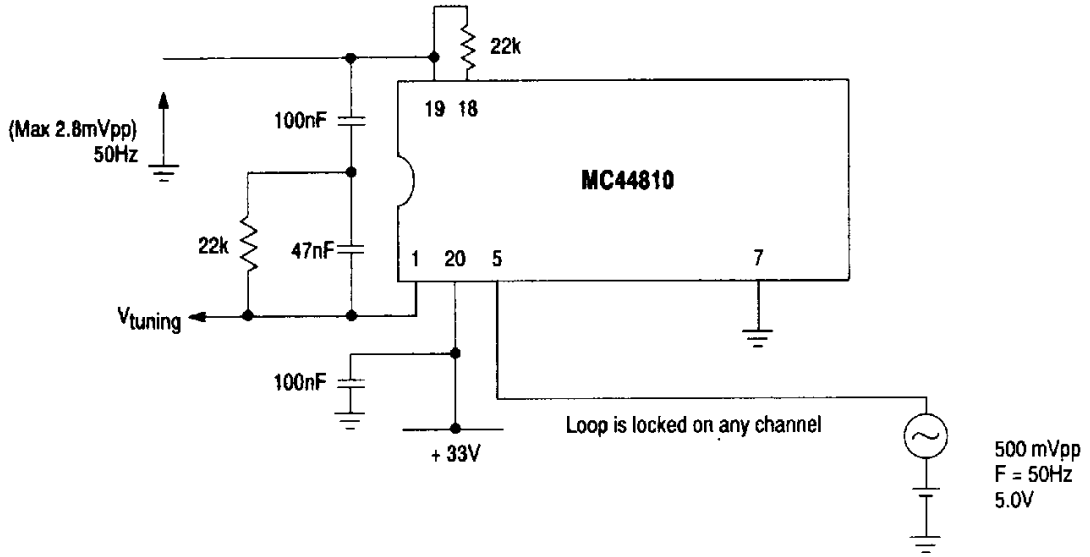
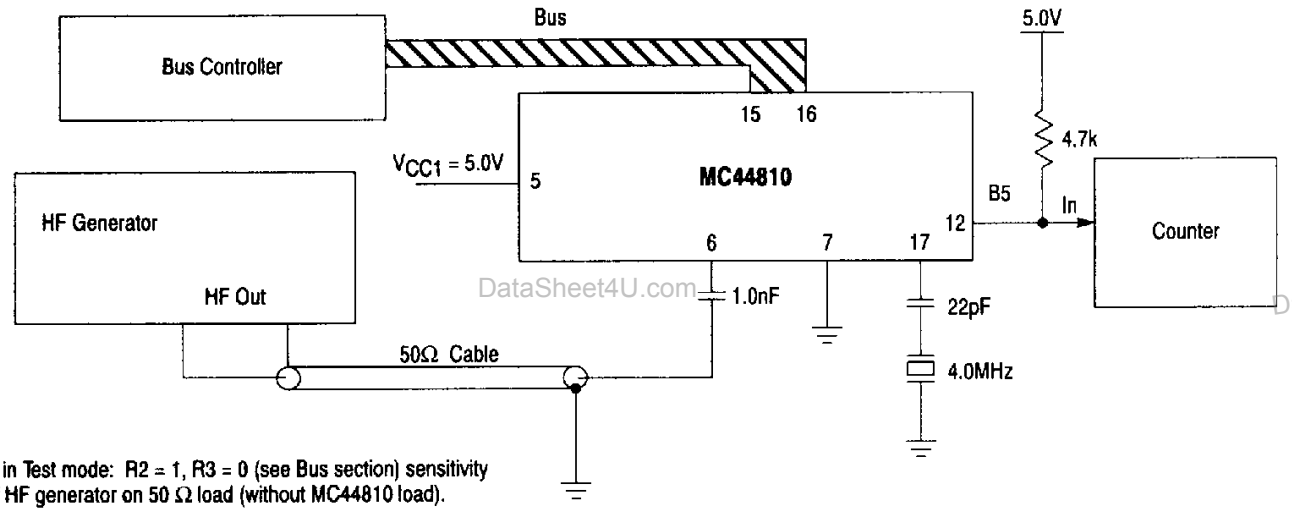


Figure 2. HF Sensitivity Test Circuit

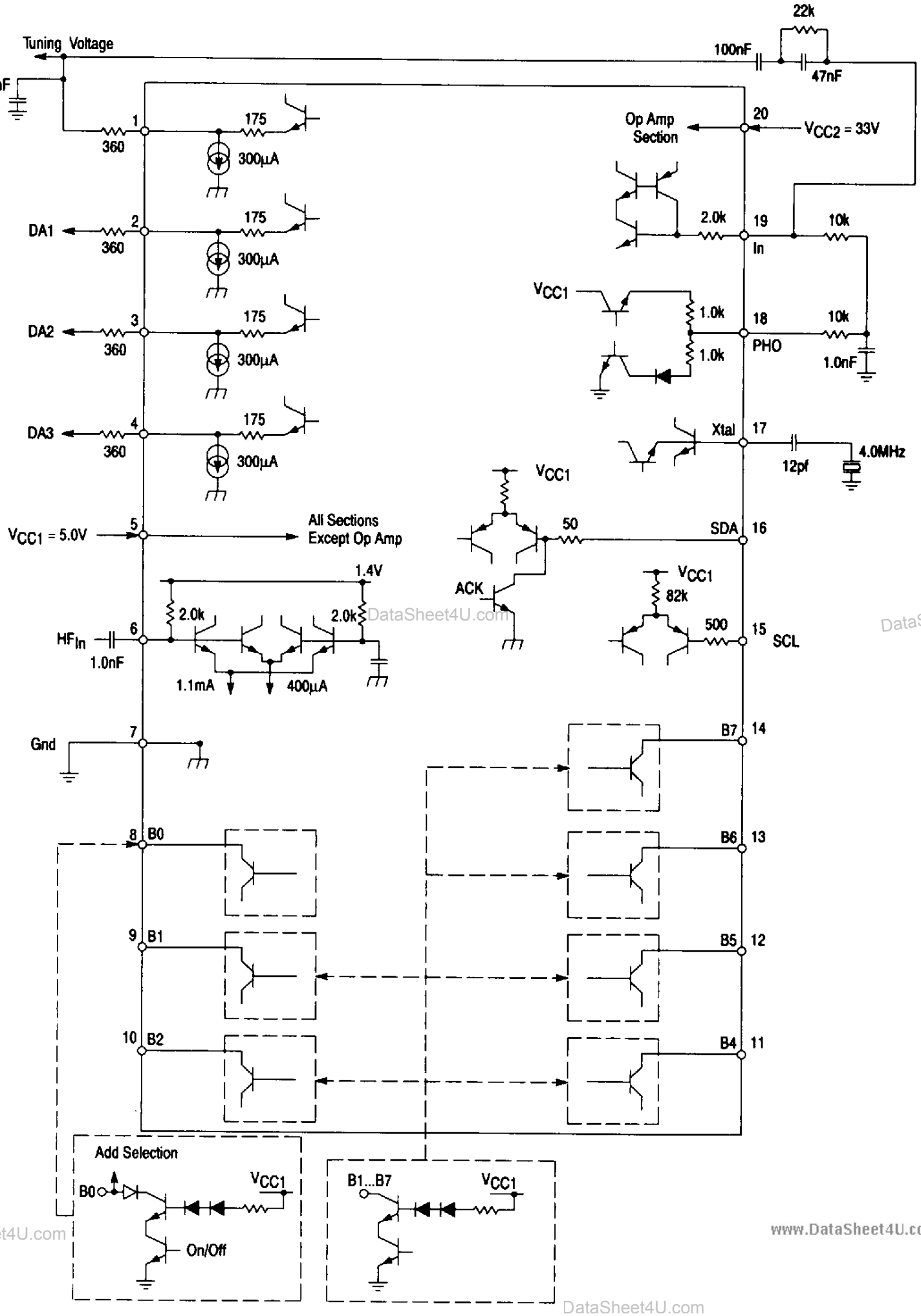


Device is in Test mode: R2 = 1, R3 = 0 (see Bus section) sensitivity is level of HF generator on 50 Ω load (without MC44810 load).

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2, 3, 4	DA1, DA2, DA3	D/A output control voltages
5	V_{CC1}	Positive supply of the circuit (except op amp)
6	HF_{In}	HF inputs from local oscillator
7	Gnd	Ground
8, 9, 10, 11 12, 13, 14	B0...B2 B4...B7	Band buffer outputs can drive up to 10 mA
15	SCL	Clock input (supplied by the microprocessor via I^2C bus)
16	SDA	Data input (I^2C bus)
17	Xtal	Crystal oscillator (typ: 4.0 MHz)
18	PHO	Phase comparator output
19	In	Negative operational amplifier input
20	V_{CC2}	Operational amplifier positive supply

Figure 3. Pin Circuit Schematic



FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of each of the internal blocks is given below.

Automatic Tuner Alignment

The circuit generates the tuning voltage through the PLL in the same way as the MC44802A. The output voltage of the D/A converters are equal to the tuning voltage plus a positive or negative offset of up to 31 steps. During the automatic alignment the PLL first locks to the appropriate frequency and then searches for the optimum values of the other varactor voltages. The digital word for each voltage value is stored in a nonvolatile memory (NVM). Hence, for each frequency point to be adjusted, three times 6 bits of information have to be stored (plus 2 bits for the DAC range).

The information stored in the NVM reflects the characteristic of the individual tuner. For this reason the NVM is preferably situated inside the tuner and is also controlled by the I2C Bus. (The NVM is also needed to store the program-channel allocation).

Figure 4. Block Diagram

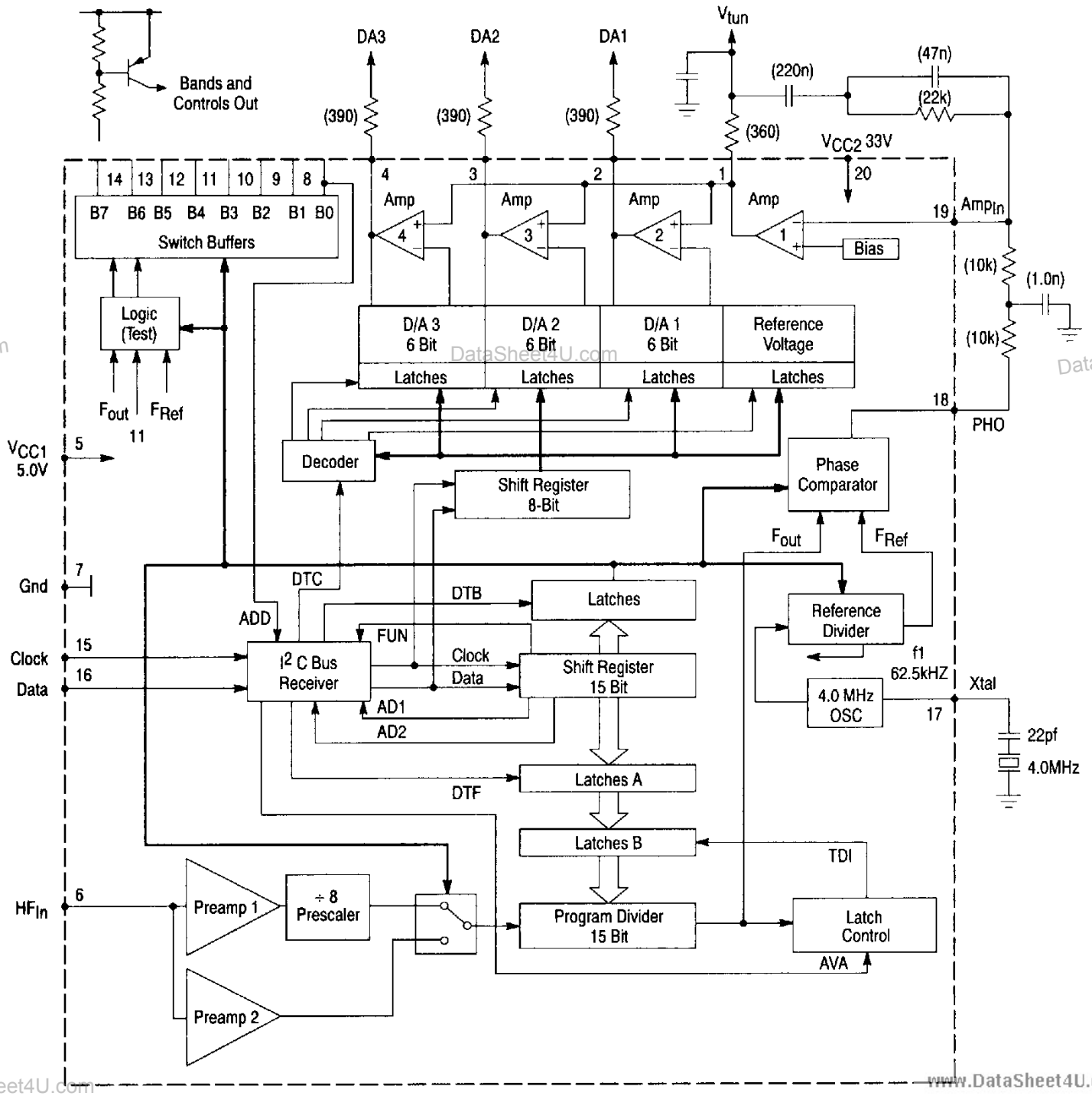
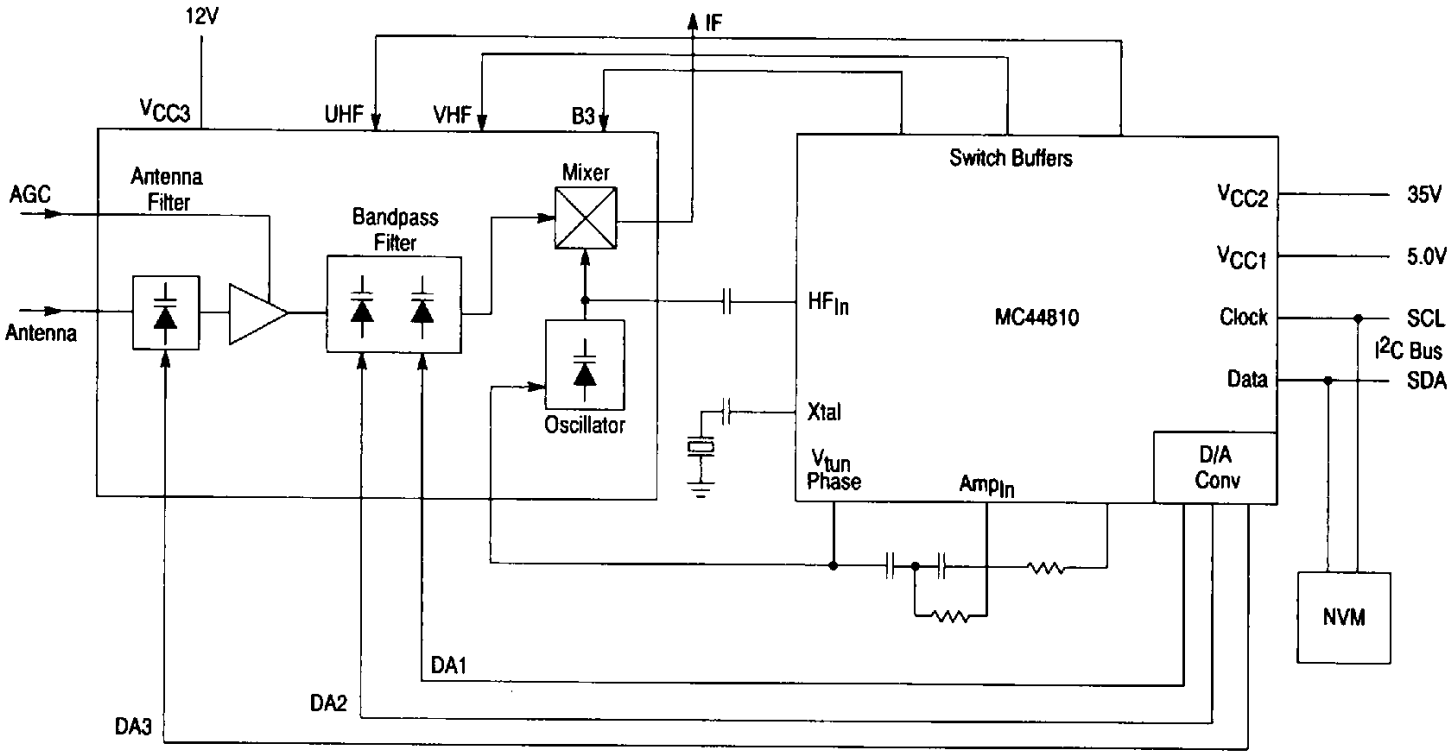


Figure 5. TV Tuner for Automatic Alignment



PLL SECTION

Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I²C Bus. The incoming information is treated in the I²C bus receiver.

Bus Protocol

1_STA	CA1	CO	BA	STO		
2_STA	CA1	FM	FL	STO		
3_STA	CA1	CO	BA	FM	FL	STO
4_STA	CA1	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA1 = Chip Address Byte of PLL Section
CO = Data Byte for Control Information
BA = Data Byte for Band Information
FM = Data Byte for Frequency Information (MSBs)
FL = Data Byte for Frequency Information (LSBs)

Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received. If three data bytes are received the third data byte is ignored. If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and third data bytes contain a function bit F. If the function bit F=0, frequency information is acknowledged and if F=1, control/band information is acknowledged.

Figure 6. Definition of Bytes

CA1_Chip Address	1	1	0	0	0	0/1	1	0	ACK
CO_Control Information	F=1	R6	T	P	R3	R2	R1	R0	ACK
BA_Band Information	B7	B6	B5	B4	X	B2	B1	B0	ACK
FM_Freq Info (with MSB)	F=0	N14	N13	N12	N11	N10	N9	N8	ACK
FL_Freq Info (with LSB)	N7	N6	N5	N4	N3	N2	N1	N0	ACK

If the address is correct (signal AD1) the information is loaded into latches.

A function bit in the first and third data byte is used to pass this data either into the latches for the programmable divider (signal DTF) or into the latches for band and control information (signal DTB). The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes.

A second string of latches is used for the data transfer into the programmable divider to inhibit the transfer during the preset operation (signal TDI, signal AVA is an internal "address valid" command).

The control and band information bits have the following functions:

Bit R0 and R1 (See Table 1) Define the reference divider division ratio. Four ratios are available.

Bit R2 and R3 (See Table 2) Are used to switch internal signals to the buffer outputs. Pin 11 and 12.

Bit R2, R6 and T (See Table 3) Are used to control the phase comparator output stage.

Bit P (See Table 6) Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

Bits B0 to B7 (See Table 7) Controls the buffers. At logic "1" the buffers are active (low).

The circuit has two PLL chip addresses. The PLL chip address is programmable by Pin 8. When Pin 8 is open or normally used as a buffer the first PLL address is selected as follows:

MSB LSB

PLL Address 1: 1 1 0 0 0 0 1 0 = C2 (octal)

When Pin 8 is at ground the 2nd address is selected.

PLL Address 2: 1 1 0 0 0 1 1 0 = C6 (octal)

Bit B4 must be "zero" when Pin 11 is used to output 62.5 kHz. Bits B4 and B5 have to be "zero" to output F_{ref} and FBY2. FBY2 is the programmable divider output frequency divided by two.

The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes. The bus receiver fulfills the standard I^2C bus specifications.

The switching levels of Clock and Data (Pins 15 and 16) are 0.5 x V_{CC1}.

Table 1

Input Data R0	Input Data R1	Reference Divider Division Ratio
0	0	2048
1	0	1024
0	1	512
1	1	256

Table 2

Input Data R2	Input Data R3	Test Outputs on Buffers Pin 11	Pin12
0	0	62.5 kHz	—
0	1	F_{Ref}	FBY2
1	0	—	—
1	1	—	—

Table 3

Input Data R2	R6	T	Output State of the Phase Comparator
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

Band Buffers – The band buffers are open collector transistors and are active "low" at Bn = 1. They are designed for 10 mA with a typical on-resistance of 70 Ω. These buffers are designed to withstand relative high output voltage in the off-state. (16 V)

B2 and B3 buffers (Pins 11 and 12) may also be used to output internal IC signals (reference frequency and programmable divider output frequency ÷ 2) for test purposes.

Buffer B2 may also be used to output a 62.5 kHz frequency from an intermediate stage of the reference divider. The bit B2 and/or B3 has to be zero if the buffers are used for these additional functions.

Buffer B0, Pin 8, is also used to select the chip address. This buffer has a higher on-voltage than the other buffers.

Programmable Divider – The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the Latches B. Latches B are loaded from Latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since Latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

N = 16384 x N14 + 8132 x N13 +...+ 4 x N2 + 2 x N1 + N0

Maximum ratio 32767, minimum ratio 17, where N0...N14 are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between Latches A and B (signal TDI) is also initiated by any start condition on the I^2C Bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N=256 or higher.

Prescaler – The prescaler has a preamp and may be bypassed (Bit P). The signal then passes through preamp 2. Table 6 shows the frequency ranges which may be synthesized with and without prescaler.

Phase Comparator – The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Operational Amplifier – The operational amplifier for the tuning voltage is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 32 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 4 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 4 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

Oscillator – The oscillator uses a 4.0 MHz crystal tied to ground through a capacitor, used in the series resonance mode. The voltage at Pin 17 "crystal" has low amplitude and low harmonic distortion.

D/A SECTION

Basic Function

The D/A section has two separate chip addresses from the PLL section. Three D-to-A converters that have a resolution of 6 bits (5 bits plus sign) are on chip. The analog output voltages are DC. The converters are buffered to the analog outputs DA1, DA2 and DA3 by operational amplifiers with an output voltage range that is equal to the tuning voltage range (about 0 V to 30 V). The op amps are arranged such that a positive or negative offset can be generated from the tuning voltage.

Data Format

The D-to-A information consists of the D/A chip address (CA2) and four data bytes. The first two bits of the data bytes are used as the function address. Thus the bytes C1, C2 and C3 contain the address for the individual converter and the 6 bits to be converted. Bit D5 is the sign (logic = 1 positive offset, logic = 0 negative offset) and the bits D0 to D4 determine the number of steps to be made as an offset from the tuning voltage. The bits S0 and S1 in the data byte RA define the step size (Vstep) and the range of the converters (see Table 4 and 5). The range is the same for all converters.

Bus Protocols

1_STA	CA2	C1	STO			
2_STA	CA2	C1	C2	STO		
3_STA	CA2	C1	C2	C3	STO	
4_STA	CA2	C1	C2	C3	RA	STO
5_STA	CA2	RA	C1	C2	C3	STO
6_STA	CA2	C1	C1	C1	C1	STO

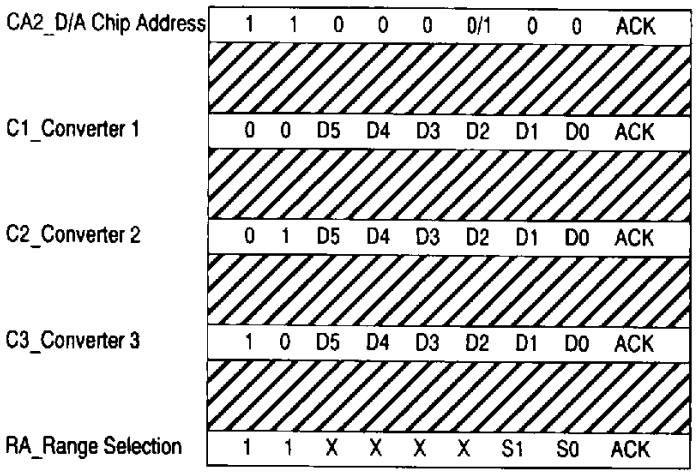
STA = Start Condition
STO = Stop Condition
CA2 = Chip Address Byte for D/A Section
C1,C2,C3 = Data Bytes for D/A Converters
RA = Data Byte for Range

The bus receiver accepts up to four data bytes in random sequences. If more than four data bytes are received, the fifth and following data bytes are ignored. The same data byte may be sent up to four times as shown in example 6.

After the chip address (CA2), up to four data bytes may be received. If more than four bytes are received the fifth and following bytes are ignored and the last acknowledged pulse is sent after the fourth data byte. The data transfer to the converters (signal DTC) is initiated each time a complete data byte is received.

Figure 7 shows some examples of the permissible bus protocols of the D-to-A section. The data bytes may be sent to the IC in random order with up to four in one sequence. The same converter may be loaded up to four times as shown in example 6 (see Bus Protocols).

Figure 7. Definition of Bytes



The D/A section has two separate chip addresses. These are programmable by Pin 8 as in the PLL section. When Pin 8 is open or normally used as a buffer, the first D/A address is selected as follows:

MSB LSB
D/A Address 1: 1 1 0 0 0 0 0 0 = C0 (octal)
When Pin 8 is at ground the second D/A address is selected.
D/A Address 2: 1 1 0 0 0 1 0 0 = C4 (octal)

Table 4. Output Voltage

VDA = Vtun ± Vstep (D0 + 2D1 + 4D2 + 8D3 + 16D4)
D5 = "1" positive sign; D5 = "0" negative sign Vtun: Tuning Voltage set by PLL Vstep: Voltage STEP (LSB) of the D/A converters

Table 5. Range Selection

Input Data S1	Input Data S0	Typ. Step Size Vstep (mV)	Guaranteed Range 31 Steps (V)
0	0	225	6.25
0	1	125	3.40
1	0	70	1.90
1	1	40	1.05

D/A Converters – The D/A converters convert 5-bit into an analog current of which the polarity is switched by the sixth bit. The reference voltage of the converters is programmed by two bits (S0, S1 of the RA-byte) to determine the scaling factor. The analog currents are then converted into voltages by means of op amps 2, 3 and 4 and the voltages are added to the tuning voltage (V_{tun}, see Figure 4) to generate the positive or negative offset.

If the data bits D0 to D5 are logic "0" the three D/A output voltages on Pins 2, 3 and 4 are equal to the tuning voltage (Pin 1) within the input offset voltages of the op amps (maximum error 0.5 LSB).

The four amplifiers have the same output characteristics with the maximum output voltage being 4.0 V lower than V_{CC2} in the worst case. The four analog outputs are short circuit protected. At power-up the D/A outputs are undetermined.

The four op amp outputs require external resistors (390 Ω) for stability.

The D/A converters are guaranteed to be monotonic with a voltage step variation of ± 0.5 LSB. The temperature stability is ± 0.5 LSB from 0° to 70°C.

Table 6

Input Data P	Prescaler Function
0	Active
1	Bypassed, Power Supply Off

Table 7

Input Data B0...B7	Band Buffers (Output State)
0	Off
1	On

Table 8. System Application (Using a 4.0 MHz Crystal)

Input Data R1	Input Data R0	Reference Divider Division Ratio	Reference Frequency (1) (Hz)	With Internal Prescaler (P=0)		Without Internal Prescaler (P=1)	
				Frequency Steps (kHz)	Max Input Frequency (MHz)	Frequency Steps (kHz)	Max Input Frequency (MHz)
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300 (2)	7.8125	165 (3)
1	1	256	15625.0	125	1300 (2)	15.625	165 (3)

(1) With 4.0 MHz Crystal (2) Limit of Prescaler (3) Limit of Programmable Divider