



# Low Power CMOS Broadband Tuner

Freescale Semiconductor's MC44S803 is a 3.3 Volt, low power, high performance, single-chip CMOS, broadband tuner. This chip offers a cost-effective, low-power solution for high-performance analog and digital TV market. This highly integrated third generation silicon tuner covers a 48 MHz to 1 GHz RF input and converts to a 30 MHz to 60 MHz IF frequency. The 861 MHz to 1 GHz frequency range is supported with reduced performance.

The single-chip broadband tuner uses a double-conversion architecture, which eliminates tracking filters and their manually aligned coils. Two IF outputs are provided to support systems with multiple demodulators (e.g. one digital demodulator and one analog TV demodulator).

The MC44S803 is designed to meet all Data Over Cable Service Interface Specification (DOCSIS), ATSC specifications for 8VSB, 64- and 256-Quadrature Amplitude Modulation (QAM) as well as the NorDig Unified 1.0.3 specifications for Coded Orthogonal Frequency Division Multiplexing (COFDM) for DVB-T.

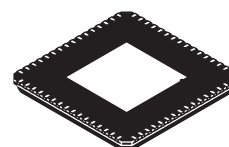
The device is available in a Pb-free 64-pin quad leadless package (QFN).

## Features

- Low power consumption (746 mW typical)
- Single 3.3 V supply operation
- Programmable power down mode with fast start-up
- Variable-gain Low-Noise Amplifier (LNA) with 40 dB gain control range
- Ability to switch between two external analog control voltages for LNA
- Two fully integrated frequency synthesizers
- Fully integrated tuned circuit Voltage Controlled Oscillators (VCOs)
- Fully integrated VCO varactors (requires only one external inductor)
- Second IF variable gain amplifier
- Flexible reference oscillator circuit (4.0 MHz to 28 MHz crystal)
- Reference oscillator buffer to drive additional tuners or modulators
- Choice of I<sup>2</sup>C or SPI interface control buses
- Internal self-diagnostic circuits
- Typical CTB of -63 dBc, CSO of -63 dBc and XMod of -55 dBc
- Typical noise figure of 7.0 dB
- Phase noise -89 dBc/Hz, typical @ 10 kHz offset

**MC44S803**

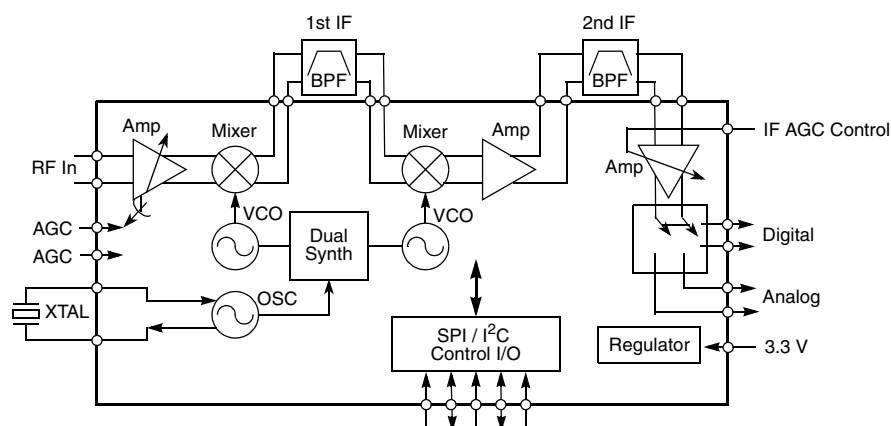
**LOW POWER CMOS  
BROADBAND TUNER**



**EP SUFFIX  
64-LEAD QFN PACKAGE  
CASE 1606-01**

## ORDERING INFORMATION

| Device     | Temp. Range  | Package | RoHS |
|------------|--------------|---------|------|
| MC44S803EP | 0°C to +85°C | 64 QFN  | yes  |

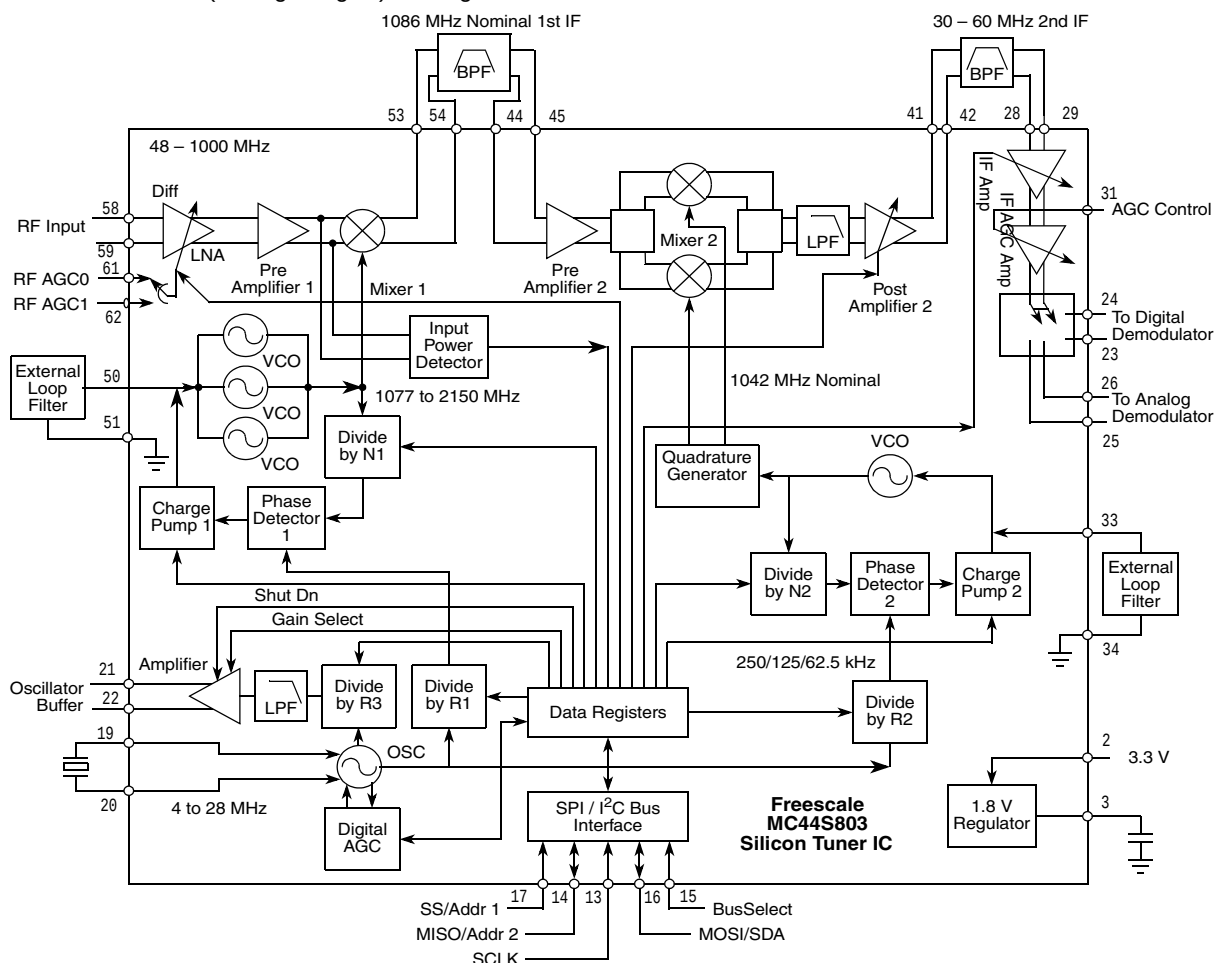


**Figure 1. MC44S803 Functional Block Diagram**

## OVERVIEW

Typical applications for the MC44S803 include cable data modems, cable TV (CATV) set-top boxes (analog & digital), computer TV tuner cards (analog & digital), analog TV sets,

digital terrestrial TV sets, digital terrestrial adapters, home DVD-R and DVR/PVR.



**Figure 2. Generation 3 CMOS Silicon Tuner IC Block Diagram**

Figure 2 shows the major sections of the MC44S803. The input frequency range is 48 MHz to 1 GHz. RF signal reception from 861 MHz to 1 GHz is supported with reduced performance. The RF input signal enters the Low Noise Amplifier (LNA) after passing through the external diplex filter. The signal is then up converted to 1086 MHz (1086 MHz is an example frequency, not a limitation or recommendation) and passed through the first IF filter. This first IF SAW can be replaced with a lower cost filter (determined by application). The filtered signal is then routed back onto the chip where it is down converted to the second IF center frequency. This is fed to the second IF channel filter. The signal enters the IC again to go through the second IF variable gain output amplifier that gets an analog AGC control voltage from the demodulator.

The output can be switched between two output ports. This provides support for systems with multiple demodulators (e.g. one digital demodulator and one analog TV demodulator).

Many of the amplifiers in the IC have programmable gain to balance the gain budget for a given application. Amplifier

gains are typically set as part of the initialization sequence at power up, then do not need to be changed after that. All programming and configuration control is accomplished via an industry standard I<sup>2</sup>C or SPI interface bus.

Additional features of the MC44S803 include:

- 3.3 V  $\pm 5\%$  single supply operation
- Internal 1.8 V tracking regulator
- High linearity and reduced current
- Reduced gain roll off at high frequencies
- 40 dB gain control range in LNA, digitally or analog voltage controlled.
- 36 dB gain control range in IF, analog voltage controlled.
- Ability to switch between two control voltages for use with digital and analog demodulators
- Fully integrated VCO varactors (only one VCO inductor required)
- Reference crystal frequency range from 4.0 to 28 MHz

## PIN DESCRIPTION

Table 1 lists the pin out of the MC44S803. In addition to the 64 leads, there is a grounding pad on the bottom of the package, which is soldered to the PCB.

**Table 1. Pin Descriptions (Listed by Pin Number)**

| Pin Number | Signal Name     | Description                                                                               |
|------------|-----------------|-------------------------------------------------------------------------------------------|
| 1          | VCO1RegByp      | Bypass for VCO 1 Reg., No Connect (Recommended)                                           |
| 2          | V <sub>DD</sub> | 3.3 Volt, VCO1 power supply, (Bypass caps should return to pin 64, V <sub>SS</sub> RBias) |
| 3          | VCO1Cap         | Bypass Cap for VCO 1 (Return cap to pin 64, V <sub>SS</sub> RBias)                        |
| 4          | VCO1LCRtn       | Return for VCO 1c Inductor                                                                |
| 5          | VCO1LC          | Inductor for VCO 1c                                                                       |
| 6          | VCO1LBRtn       | Return for VCO 1b Inductor                                                                |
| 7          | VCO1LB          | Inductor for VCO 1b                                                                       |
| 8          | VCO1LARtn       | Return for VCO 1a Inductor                                                                |
| 9          | VCO1LA          | Inductor for VCO 1a                                                                       |
| 10         | TestP           | Test Pin Plus                                                                             |
| 11         | TestM           | Test Pin Minus                                                                            |
| 12         | V <sub>DD</sub> | 3.3 Volt, SPI power supply                                                                |
| 13         | SClk            | Serial Clock                                                                              |
| 14         | MISO_Adr2       | MISO / Address bit 2. (Internal pull-up for "1"; Ground for "0")                          |
| 15         | BusSel          | SPI/I2C Bus Select. (Internal pull-up for "1"; Ground for "0")                            |
| 16         | SDA_MOSI        | SDA / MOSI                                                                                |
| 17         | SS_Adr1         | Slave Select / Address bit 1. (Internal pull-up for "1"; Ground for "0")                  |
| 18         | V <sub>DD</sub> | 3.3 Volt, OSC power supply                                                                |
| 19         | Xtal2           | Crystal Input 2                                                                           |
| 20         | Xtal1           | Crystal Input 1                                                                           |
| 21         | RefOutP         | Ref. Osc. Buffer In/Output Plus                                                           |
| 22         | RefOutM         | Ref. Osc. Buffer In/Output Minus                                                          |
| 23         | DigiFOM         | Digital IF Out Minus                                                                      |
| 24         | DigiFOP         | Digital IF Out Plus                                                                       |
| 25         | AnIFOP          | Analog IF Out Plus                                                                        |
| 26         | AnIFOM          | Analog IF Out Minus                                                                       |
| 27         | V <sub>DD</sub> | 3.3 Volt, IF AGC power supply                                                             |
| 28         | IFAGCInM        | IF AGC Amplifier Input Minus (Internally cap coupled)                                     |
| 29         | IFAGCInP        | IF AGC Amplifier Input Plus (Internally cap coupled)                                      |
| 30         | AnTest          | Analog Test Pin                                                                           |

**Table 1. Pin Descriptions (Listed by Pin Number)**

| Pin Number | Signal Name     | Description                                                                                               |
|------------|-----------------|-----------------------------------------------------------------------------------------------------------|
| 31         | 2ndIFAGC        | Second IF AGC Control.                                                                                    |
| 32         | V <sub>DD</sub> | 3.3 Volt, Synth 2 power supply                                                                            |
| 33         | LF2             | Loop Filter 2                                                                                             |
| 34         | LF2Rtn          | V <sub>SS</sub> RefVCO2. Return for Loop Filter 2                                                         |
| 35         | VCO2RegByp      | Bypass for VCO 2 Reg., No Connect (Recommended)                                                           |
| 36         | V <sub>DD</sub> | 3.3 Volt, V <sub>DD</sub> VCO2 power supply. (Bypass cap should return to pin 34 V <sub>SS</sub> RefVCO2) |
| 37         | VCO2Cap         | Bypass Cap for VCO 2. (Return cap to pin 34 V <sub>SS</sub> RefVCO2)                                      |
| 38         | VCO2L1          | Inductor for VCO 2                                                                                        |
| 39         | VCO2L2          | Return for VCO 2 Inductor                                                                                 |
| 40         | V <sub>DD</sub> | 3.3 Volt, IF AMP power supply                                                                             |
| 41         | IFampOP         | IF Amplifier Output Plus                                                                                  |
| 42         | IFampOM         | IF Amplifier Output Minus                                                                                 |
| 43         | V <sub>SS</sub> | V <sub>SS</sub> IF AMP                                                                                    |
| 44         | PreMix2InM      | Mixer 2 Preamp Input Minus                                                                                |
| 45         | PreMix2InP      | Mixer 2 Preamp Input Plus                                                                                 |
| 46         | V <sub>DD</sub> | 3.3 Volt, M2IF power supply                                                                               |
| 47         | NC              | No Internal Connection                                                                                    |
| 48         | NC              | No Internal Connection                                                                                    |
| 49         | V <sub>DD</sub> | 3.3 Volt, Synth 1 power supply                                                                            |
| 50         | LF1             | First LO Loop Filter                                                                                      |
| 51         | LF1Rtn          | V <sub>SS</sub> Ref VCO1. Return for Loop Filter 1                                                        |
| 52         | V <sub>DD</sub> | 3.3 Volt, Mixer 1 power supply                                                                            |
| 53         | Mix1OP          | First Mixer Output Plus                                                                                   |
| 54         | Mix1OM          | First Mixer Output Minus                                                                                  |
| 55         | LNABias         | LNA Bias                                                                                                  |
| 56         | V <sub>DD</sub> | 3.3 Volt, LNA power supply                                                                                |
| 57         | LNAInPL         | Inductor for RF In Plus                                                                                   |
| 58         | LNAInP          | RF Input Plus                                                                                             |
| 59         | LNAInM          | RF Input Minus                                                                                            |
| 60         | LNAInML         | Inductor for RF In Minus                                                                                  |
| 61         | FEAGC_A         | FE AGC Control A                                                                                          |
| 62         | FEAGC_B         | FE AGC Control B                                                                                          |
| 63         | RBias           | Bias Setting Resistor                                                                                     |
| 64         | RBiasRtn        | Return for RBias                                                                                          |
| 65         | Gnd_Pad         | Ground pad on bottom of package                                                                           |

## ELECTRICAL SPECIFICATIONS

**Table 2. Absolute Maximum Ratings**

Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute maximum rated conditions is not implied.

| Characteristic            | Symbol    | Min  | Max            | Units |
|---------------------------|-----------|------|----------------|-------|
| Supply Voltage            | $V_{DD}$  | -0.3 | +3.6           | V     |
| Any Input Voltage         | $V_{in}$  | -0.3 | $V_{DD} + 0.3$ | V     |
| Storage Temperature Range | $T_{stg}$ | -65  | +150           | °C    |

**Table 3. General Specifications**

| Characteristic                                   | Symbol | Min  | Units |
|--------------------------------------------------|--------|------|-------|
| ESD Protection (Machine Model)                   | MM     | 200  | V     |
| ESD Protection (Human Body Model) <sup>(1)</sup> | HBM    | 2000 | V     |
| Latch-Up Immunity                                | LU     | 200  | mA    |

1. MIL STD 883C method 3015-7.

**Table 4. Recommended Operating Conditions**

| Characteristic      | Symbol   | Min    | Typ  | Max    | Units |
|---------------------|----------|--------|------|--------|-------|
| Supply Voltage      | $V_{DD}$ | +3.135 | +3.3 | +3.465 | V     |
| Ambient Temperature | $T_A$    | 0      | —    | +85    | °C    |

**Table 5. Typical DC Power Consumption**

| Power Mode           | Supply (V) | Power (mW) | CTB (dBc) | CSO (dBc) | XMOD (dBc) |
|----------------------|------------|------------|-----------|-----------|------------|
| Low (−3 dBmV Attack) | 3.3        | 746        | -59       | -58       | -55        |
| High (0 dBmV Attack) | 3.3        | 1040       | -63       | -63       | -55        |

Table 6 specifies the tuner performance with low power settings for the reference design shown in Figure 30, which includes the applicable filtering. Note that this tuner can be operated in an extended frequency band of 861 MHz to 1000 MHz. In this extended band, Gain Variation and Noise Figure specs increase 1.0 dB.

### TEST CONDITIONS:

- $V_{DD} = 3.3$  V
- $T_A = 25^\circ\text{C}$
- Second IF = 44 MHz
- RF Frequency Range = 57 to 861 MHz

| Parameter | Atten | Pre Amp1 | Mix1 | Pst Amp2 | IF Amp |
|-----------|-------|----------|------|----------|--------|
| Gain      | 0 dB  | Nom      | —    | 8.3 dB   | 6.0 dB |
| Power     | —     | Low      | Low  | Low      | Low    |

**Table 6. Tuner Performance (Low Power Settings)**

Data for VCC = 3.3V, 25C RFAGC for minimum attenuation = 2.0V

| Parameter                                                                            | Min           | Typ  | Max  | Units  |      |
|--------------------------------------------------------------------------------------|---------------|------|------|--------|------|
| Supply Current — Low power mode                                                      | —             | 211  | —    | mA     |      |
| Supply Current — All blocks shutdown                                                 | —             | 12   | 14   | mA     |      |
| Noise Figure Channel 57 MHz                                                          | —             | 6.8  | 8.0  | dB     |      |
| Noise Figure Channel 861 MHz                                                         | —             | 7.5  | 8.5  | dB     |      |
| Noise Figure Channel 1000 MHz                                                        | —             | 8.2  | 9.3  | dB     |      |
| Conversion Gain — All max settings                                                   | 57 MHz        | 88   | 91   | 95     | dB   |
|                                                                                      | 861 MHz       | 84   | 87   | 91     | dB   |
|                                                                                      | 1000 MHz      | 83   | 86   | 90     | dB   |
| Conversion Gain — All min settings                                                   | 57 MHz        | 80   | 84   | 87     | dB   |
|                                                                                      | 861 MHz       | 76   | 80   | 83     | dB   |
|                                                                                      | 1000 MHz      | 75   | 79   | 82     | dB   |
| Gain Variation — Variation in Gain for one tuner over 57MHz-861MHz                   | —             | 4.2  | —    | dB     |      |
| IF Gain Flatness — within any channel                                                | —             | —    | ±0.5 | dB     |      |
| RF AGC Range                                                                         | —             | 40   | —    | dB     |      |
| IF AGC Range 0.5 V to 3.3 V                                                          | —             | 36   | —    | dB     |      |
| Spurious at Input Terminals:                                                         | 5 to 42 MHz   | —    | —    | -59    | dBmV |
|                                                                                      | 54 to 861 MHz | —    | —    | -55    | dBmV |
| Spurious at Output Terminals                                                         | —             | -65  | —    | dBc    |      |
| 2nd IF Image Rejection (Tuner board uses an external 1st IF SAW for image rejection) | 64            | —    | —    | dB     |      |
| Distortions with -3 dBmV AGC Attack Point (99 Channels)                              | —             | —    | —    | —      |      |
| Beats within the output                                                              | —             | -57  | -49  | dBc    |      |
| Cross-Modulation Ratio                                                               | —             | -55  | -47  | dBc    |      |
| Composite Second Order (CSO)                                                         | —             | -58  | -54  | dBc    |      |
| Composite Triple Beat (CTB)                                                          | —             | -59  | -54  | dBc    |      |
| Phase Noise @ 1 kHz                                                                  | —             | -92  | —    | dBc/Hz |      |
| Phase Noise @ 10 kHz                                                                 | —             | -89  | —    | dBc/Hz |      |
| Phase Noise @ 100 kHz                                                                | —             | -100 | —    | dBc/Hz |      |
| Phase Noise @ 1 MHz                                                                  | —             | -128 | —    | dBc/Hz |      |

Table 7 specifies the tuner performance with high power settings for the reference design shown in Figure 30, which includes the applicable filtering. Note that this tuner can be operated in an extended frequency band of 861 MHz to 1000 MHz. In this extended band, Gain Variation and Noise Figure specs increase 1.0 dB.

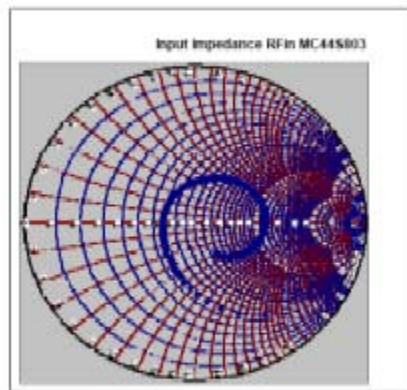
**TEST CONDITIONS:**

- $V_{DD} = 3.3 \text{ V}$
- $T_A = 25^\circ\text{C}$
- Second IF = 44 MHz
- RF Frequency Range = 57 to 861 MHz

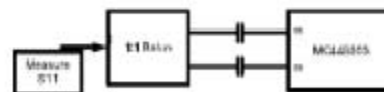
| Parameter | Atten | Pre Amp1 | Mix1 | Pst Amp2 | IF Amp |
|-----------|-------|----------|------|----------|--------|
| Gain      | 0 dB  | Nom      | —    | 8.3 dB   | 6.0 dB |
| Power     | —     | Nom      | High | Nom      | Nom    |

**Table 7. Tuner Performance (High Power Settings)**Data for  $V_{CC} = 3.3$  V, 25°C, RFAGC for minimum attenuation = 2.0 V

| Parameter                                                          | Min                          | Typ  | Max  | Units  |      |
|--------------------------------------------------------------------|------------------------------|------|------|--------|------|
| Supply Current — Nominal power mode                                | —                            | 315  | —    | mA     |      |
| Supply Current — All blocks shutdown                               | —                            | 12   | 14   | mA     |      |
| Noise Figure Channel 57 MHz                                        | —                            | 6.6  | 7.5  | dB     |      |
| Noise Figure Channel 861 MHz                                       | —                            | 8.2  | 9.0  | dB     |      |
| Noise Figure Channel 1000 MHz                                      | —                            | 9.0  | 10.0 | dB     |      |
| Conversion Gain — All max settings                                 | 57 MHz                       | 88   | 91   | 95     | dB   |
|                                                                    | 861 MHz                      | 84   | 87   | 91     | dB   |
|                                                                    | 1000 MHz                     | 83   | 86   | 90     | dB   |
| Conversion Gain — All min settings                                 | 57 MHz                       | 80   | 84   | 87     | dB   |
|                                                                    | 861 MHz                      | 76   | 80   | 83     | dB   |
|                                                                    | 1000 MHz                     | 75   | 79   | 82     | dB   |
| Gain Variation — Variation in Gain for one tuner over 57MHz-861MHz | —                            | 4.2  | —    | dB     |      |
| IF Gain Flatness — within any channel                              | —                            | —    | ±0.5 | dB     |      |
| RF AGC Range                                                       | —                            | 40   | —    | dB     |      |
| IF AGC Range 0.5 V to 3.3 V                                        | —                            | 36   | —    | dB     |      |
| Spurious at Input Terminals:                                       | —                            | —    | —    |        |      |
|                                                                    | 5 to 42 MHz                  | —    | —    | -59    | dBmV |
|                                                                    | 54 to 861 MHz                | —    | —    | -55    | dBmV |
| Spurious at Output Terminals                                       | —                            | -60  | —    | dBc    |      |
| 2nd IF Image Rejection                                             | 64                           | —    | —    | dB     |      |
| Distortions with 0 dBmV AGC Attack Point                           | —                            | —    | —    | —      |      |
|                                                                    | Beats within the output      | —    | -59  | -52    | dBc  |
|                                                                    | Cross-Modulation Ratio       | —    | -56  | -52    | dBc  |
|                                                                    | Composite Second Order (CSO) | —    | -66  | -54    | dBc  |
|                                                                    | Composite Triple Beat (CTB)  | —    | -63  | -57    | dBc  |
| Distortions with -3 dBmV AGC Attack Point                          | —                            | —    | —    | —      |      |
|                                                                    | Beats within the output      | —    | -60  | -52    | dBc  |
|                                                                    | Cross-Modulation Ratio       | —    | -61  | -57    | dBc  |
|                                                                    | Composite Second Order (CSO) | —    | -66  | -58    | dBc  |
|                                                                    | Composite Triple Beat (CTB)  | —    | -66  | -62    | dBc  |
| Phase Noise @ 1 kHz                                                | —                            | -92  | —    | dBc/Hz |      |
| Phase Noise @ 10 kHz                                               | —                            | -89  | —    | dBc/Hz |      |
| Phase Noise @ 100 kHz                                              | —                            | -100 | —    | dBc/Hz |      |
| Phase Noise @ 1 MHz                                                | —                            | -128 | —    | dBc/Hz |      |



| S11 Impedance |    |      |
|---------------|----|------|
| MHz           | R  | I    |
| 10            | 33 | -j39 |
| 50            | 35 | -j1  |
| 100           | 38 | j10  |
| 200           | 43 | j24  |
| 500           | 95 | j40  |
| 800           | 97 | -j33 |
| 1000          | 59 | -j24 |



RFinput Impedance and Measurement Circuit

Figure 3. RFinput Impedance MC44S803 Drawing

## DIGITAL INTERFACE

The digital control interface has the capability to interface with Serial Peripheral Interface (SPI) or I<sup>2</sup>C buses. Five pins are shared between the two buses. A Bus Select pin, (BusSel), as shown in Table 8, is used to determine which bus will be used. The BUSSEL pin has an internal pull-up resistor. For a logic one the pin may be left open and for a logic zero it should be connected to ground.

For the I<sup>2</sup>C bus, two pins are used to select one of four I<sup>2</sup>C addresses. This allows up to four tuners on the same bus for applications that use multiple tuners. The two pins used for the I<sup>2</sup>C bus are the Clock and Data pins. The data pin is bi-directional. The SPI bus uses four pins: Slave Select (SS), Serial Clock (SCLK), Master Out Slave In (MOSI), and Master In Slave Out (MISO). Data is read from the part through the MISO pin. For multiple tuner application using the SPI interface, each device shares the Clock, MOSI and MISO lines. Each device is supplied its own Slave Select line. The Slave Select and MISO pins for the SPI share the same pins as the two address lines for the I<sup>2</sup>C bus. Internally, the two buses share the same Control, Data, and Shift registers that interface with each section of the IC.

**Table 8. Interface Bus Selection**

| Bus Select Pin | Interface Standard |
|----------------|--------------------|
| 0              | SPI                |
| 1              | I <sup>2</sup> C   |

### SERIAL PERIPHERAL INTERFACE (SPI) OPERATION

A 24-bit shift register is used to shift data in and out of the device. The input data stream is clocked on the rising edge of SCLK into a shift register with the MSB first. If more than 24 bits are clocked in only the last 24 bits inputted are

recognized. If less than 24 bits are required, only the required bits need to be clocked in. No back filling is required. The output data stream is clocked out of the shift register on the falling edge of SCLK with the MSB first. The bus master samples the MISO line on the rising edge of SCLK. Every SPI operation is both a read and a write operation, since the data is input on one pin and output on a different pin. Read data out while clocking data in. The data stored in the shift register is loaded into one of the appropriate registers after the rising edge of SS. The 4 LSBs are the Control Register Address Bits.

### I<sup>2</sup>C OPERATION

The same 24-bit shift register is used to shift data in and out of the part. The input data stream is clocked in on the rising edge of SCLK into the shift register with the MSB first. The IC Address and R/W bit are sent first. This allows the IC to determine if it is the device that is being communicated with. After that, 24 bits are clocked in to control the IC. If less than 24 bits are required, then 16 or 8 bits could be used. In other words, commands can be sent in 1, 2, or 3 byte increments depending on the requirements for the particular control register you are writing to. Data can be read back from the IC in 1, 2, or 3 byte increments also. The Master controls the clock line, whether writing to the part or reading from it. After each byte that is sent, the device that receives it sends an acknowledge bit. The output data stream is clocked out of the shift register on the falling edge of SCLK and valid on the rising edge, with the MSB first. The data stored in the shift register is loaded into one of the appropriate registers after the Stop Condition is sent. The 4 LSBs are the Control Register Address Bits.



## READ OPERATION PROTOCOL

The following flowchart is provided to show the steps required to read out a particular Data Register. Note that when using the SPI interface, since there are separate lines for data in (MOSI) and data out (MISO), each SPI operation

is both a read and a write operation. But the data being read out is not affected by the command that is actively being written to the IC. The command doesn't take effect until the SPI operation is completed.

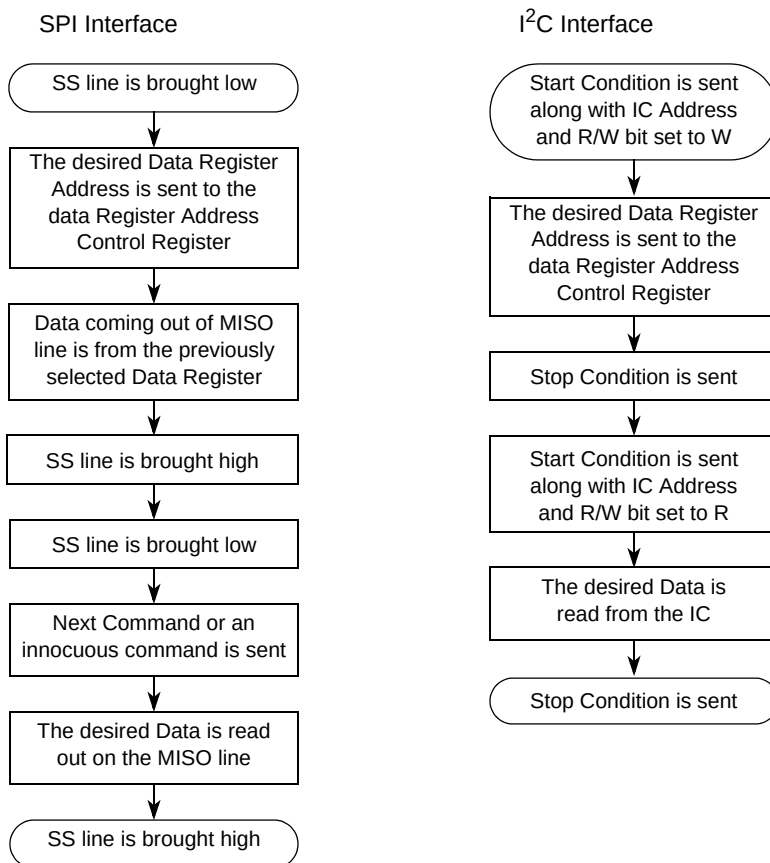


Figure 4. Read Operation Protocol

## ADDRESSES

There are three type of addresses referred to in this document.

### I<sup>2</sup>C DEVICE ADDRESS

Since the I<sup>2</sup>C bus is a two-wire bus that does not have a separate select line, each IC on the bus has a unique address. This address is sent each time an IC is communicated with. The address is the first seven bits that are sent to the IC. The eighth bit sent is the R/W bit, it determines whether the master will read from or write to the IC. Five fixed bits and two pin selectable bits set the address of this IC. Address bit 2 is set with the MISO/Addr2 pin. Address bit 1 is set with the SS/Addr1 pin.

Table 9. I<sup>2</sup>C IC Address

| MSB        |   |   |   |   |   |   | LSB |
|------------|---|---|---|---|---|---|-----|
| IC Address |   |   |   |   |   |   |     |
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | R/W |
| 1          | 1 | 0 | 0 | 0 | X | X | X   |

### CONTROL REGISTER ADDRESS

Each command that is sent to the IC is stored in its corresponding Control Register. The Control Register Address specifies which command is being sent.

### DATA REGISTER ADDRESS

There are 16 registers for data that can be read from the IC. The Data Register Address specifies which register is read during the next read operation. The address of the desired data register is stored in the Control Register called Data Register Address.

## DIGITAL INTERFACE TIMING

### SPI TIMING

SPI buses can have one of four serial clock phase and polarity combinations. Freescale microcontrollers should be configured using CPOL = 0 and clock phase, CPHA = 0. See the product documentation for more information. A clock polarity of 0 simply means that the slave samples MOSI line and master samples MISO line on the rising edge of the SCLK. A clock phase of 0 means that the first edge on the SCLK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. MOSI and MISO transition on the falling edge of SCLK.

The MISO pin has an open drain output that is pulled up by an external resistor. This allows multiple tuners to share the same MISO line. The output from the MISO line can be disabled by programming the SO bit of the Reset/SO Enable register to 0. The MISO line is disabled at power up and reset.

The first bit out of MISO is repeated. For 24 bits clocked out, the last three bits are fixed as 110.

The SPI/I<sup>2</sup>C interface lines are 5.0 V tolerant. Therefore, they can be pulled up to 5.0 V if that is required to interface with the microprocessor in a given application.

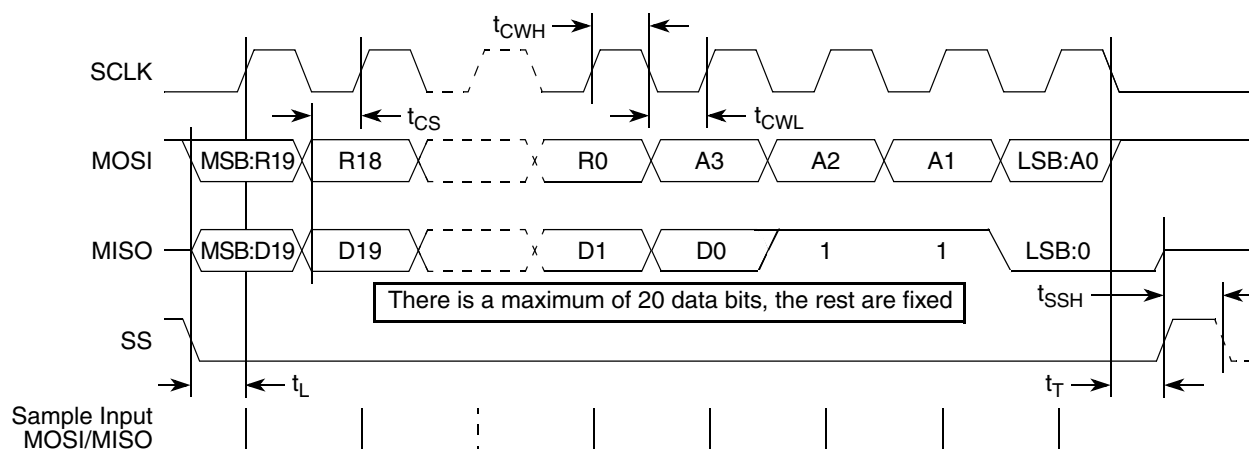


Figure 5. SPI Timing Diagram

Table 10. SPI Interface Bus Specifications

See Figure 5 for timing references.

| Characteristic <sup>(1)</sup>      | Symbol     | Min | Typ | Max | Units |
|------------------------------------|------------|-----|-----|-----|-------|
| Low Level Output Voltage           | $V_{OL}$   | —   | —   | 0.4 | V     |
| High Level Input Voltage           | $V_{IH}$   | 2.3 | —   | —   | V     |
| Low Level Input Voltage            | $V_{IL}$   | —   | —   | 1.0 | V     |
| Absolute Maximum Input Voltage     | $V_{IN}$   | —   | —   | 5.5 | V     |
| SCLK Frequency                     | $f_{SCLK}$ | —   | —   | 2.0 | MHz   |
| Data to Clock Set Up Time          | $t_{CS}$   | —   | —   | —   | ns    |
| Clock Pulse Width High             | $t_{CWH}$  | —   | —   | —   | ns    |
| Clock Pulse Width Low              | $t_{CWL}$  | —   | —   | —   | ns    |
| Leading, SS Falling to SCK Rising  | $t_L$      | —   | —   | —   | ns    |
| Trailing, SCK Falling to SS Rising | $t_T$      | —   | —   | —   | ns    |
| SS Pulse Width High                | $t_{SSH}$  | —   | —   | —   | ns    |

1. Unless otherwise noted;  $V_{DD} = 3.3$  Vdc,  $V_{SS} = GND = 0$  Vdc,  $0 < T_A < 85^\circ\text{C}$ .

## INTER-IC (I<sup>2</sup>C) INTERFACE TIMING

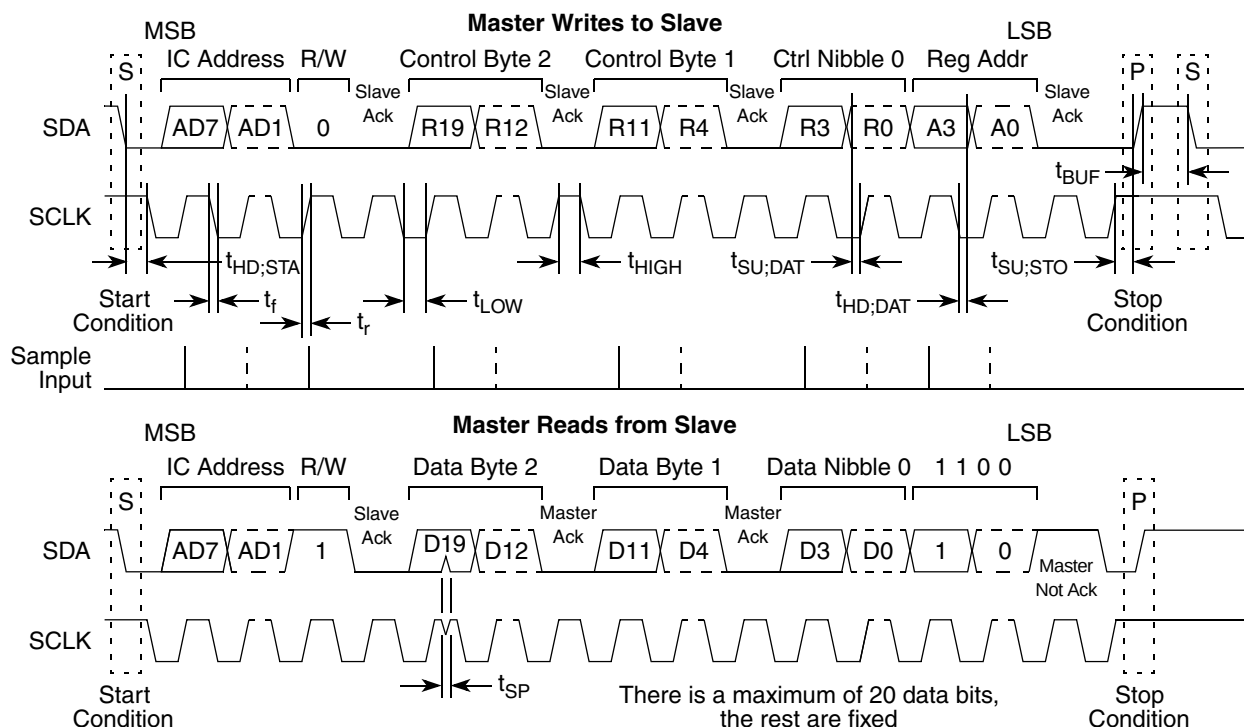


Figure 6. I<sup>2</sup>C Timing Diagram

Table 11. I<sup>2</sup>C Interface Bus Specifications

| Parameter                                                                                  | Symbol       | Min.                          | Max.                | Units   |
|--------------------------------------------------------------------------------------------|--------------|-------------------------------|---------------------|---------|
| Low Level Output Voltage<br>$V_{DD} > 2.0\text{ V}$<br>$V_{DD} < 2.0\text{ V}$             | $V_{OL}$     | 0<br>0                        | 0.4<br>$0.2 V_{DD}$ | V       |
| High Level Input Voltage                                                                   | $V_{IH}$     | $0.7 V_{DD}$                  | $V_{DDmax}+0.5$     | V       |
| Low Level Input Voltage                                                                    | $V_{IL}$     | -0.5                          | $0.3 V_{DD}$        | V       |
| Absolute Max Input Voltage                                                                 | —            | —                             | 5.0                 | V       |
| Hysteresis of Schmitt Trigger Inputs<br>$V_{DD} > 2.0\text{ V}$<br>$V_{DD} < 2.0\text{ V}$ | $V_{hys}$    | $0.05 V_{DD}$<br>$0.1 V_{DD}$ | —<br>—              | V       |
| Capacitance for each I/O Pin <sup>(1)</sup>                                                | $C_{in}$     | —                             | 10                  | pF      |
| Pulse Width of Spikes Filtered Out                                                         | $t_{SP}$     | 0                             | 50                  | nS      |
| SCLK Frequency                                                                             | $f_{SCLK}$   | 0                             | 800                 | kHz     |
| Hold Time Start Condition                                                                  | $t_{HD;STA}$ | 500                           | —                   | ns      |
| Set-Up Time for Repeated Start                                                             | $t_{SU;STA}$ | 500                           | —                   | ns      |
| Data Set-Up Time                                                                           | $t_{SU;DAT}$ | 100                           | —                   | ns      |
| Data Hold Time                                                                             | $t_{HD;DAT}$ | 0                             | —                   | ns      |
| Set-Up Time for Stop Condition                                                             | $t_{SU;STO}$ | 500                           | —                   | ns      |
| Low Period of the SCLK Clock                                                               | $t_{LOW}$    | 0.6                           | —                   | $\mu$ S |
| High Period of the SCLK Clock                                                              | $t_{HIGH}$   | 0.6                           | —                   | $\mu$ S |
| Rise Time of both SDA and SCLK                                                             | $t_r$        | $20 + 0.1C_b$                 | 300                 | ns      |
| Fall Time of both SDA and SCLK                                                             | $t_f$        | $20 + 0.1C_b$                 | 300                 | ns      |
| Bus Free Time between Stop and Start                                                       | $t_{BUF}$    | 200                           | —                   | ns      |

1.  $C_b$  = total capacitance of one bus line in pF.

## CONTROL REGISTER DEFINITIONS

Each Control Register controls a different area of the IC. The description of each register follows.

written to is a function of the Control Register Address Bits. These are the 4 LSBs, A3 to A0.

### CONTROL REGISTER FORMAT

There is a set of control registers that are programmed to tune and adjust the IC. Which particular control register is

| MSB                   |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    | LSB          |    |    |    |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|
| R19                   | R18 | R17 | R16 | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |
| Control Register Bits |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    | Address Bits |    |    |    |

Figure 7. Control Register Format

Table 12. Control Register Address Map

| Register Function        | Address Bits |    |    |    | Control Reg. CR-x |
|--------------------------|--------------|----|----|----|-------------------|
|                          | A3           | A2 | A1 | A0 |                   |
| Power Down               | 0            | 0  | 0  | 0  | 0                 |
| Reference Oscillator     | 0            | 0  | 0  | 1  | 1                 |
| Reference Dividers       | 0            | 0  | 1  | 0  | 2                 |
| Mixer & Reference Buffer | 0            | 0  | 1  | 1  | 3                 |
| Reset/Serial Out         | 0            | 1  | 0  | 0  | 4                 |
| LO 1                     | 0            | 1  | 0  | 1  | 5                 |
| LO 2                     | 0            | 1  | 1  | 0  | 6                 |
| Circuit Adjust           | 0            | 1  | 1  | 1  | 7                 |
| Test                     | 1            | 0  | 0  | 0  | 8                 |
| Digital Tune             | 1            | 0  | 0  | 1  | 9                 |
| LNA AGC                  | 1            | 0  | 1  | 0  | 10                |
| Data Register Address    | 1            | 0  | 1  | 1  | 11                |

### POWER DOWN REGISTER (CR-0)

The Power Down Register allows various circuits to be powered down to save power when not in use. A 1 written to any of the control bits power down the corresponding circuit. Conversely, a 0 written to any of the control bits powers up the corresponding circuit. The reset state for all bits is 1. After DC power is applied or software reset, the IC is powered up

by writing 0s to all desired bits. The interface bus circuits are never powered down because they are needed in order to power the IC back up. One should wait at least 20 millisecond between the time that the IC is powered up through this command and performing a digital tune of the VCOs. This time will allow the reference oscillator to stabilize.

| MSB        |            |      |         |         |          |          |     |     |     |          |      |        |     |          |      |        |     |      |      | LSB          |    |    |             |
|------------|------------|------|---------|---------|----------|----------|-----|-----|-----|----------|------|--------|-----|----------|------|--------|-----|------|------|--------------|----|----|-------------|
| R19        | R18        | R17  | R16     | R15     | R14      | R13      | R12 | R11 | R10 | R9       | R8   | R7     | R6  | R5       | R4   | R3     | R2  | R1   | R0   | A3           | A2 | A1 | A0          |
| 1          | 1          | 1    | 1       | 1       | 1        | 1        | 1   | 1   | 1   | 1        | 1    | 1      | 1   | 1        | 1    | 1      | 1   | 1    | 0    | 0            | 0  | 0  | Reset State |
| IF Pwr Det | RF Pwr Det | Buf2 | Ref Osc | AGC Amp | Reserved | Reserved | IF2 | IF1 | LNA | Reserved | Mix1 | Synth2 | CP2 | Reserved | VCO2 | Synth1 | CP1 | Buf1 | VCO1 | Address Bits |    |    |             |

Figure 8. Power Down Register Format

**Table 13. Power Down Bit Table**

| Bit | Mnemonic   | Function                        |
|-----|------------|---------------------------------|
| 0   | VCO 1      | Voltage Controlled Oscillator 1 |
| 1   | Buf1       | VCO 1 Buffer                    |
| 2   | CP1        | Charge Pump 1                   |
| 3   | Synth1     | Synthesizer 1                   |
| 4   | VCO 2      | Voltage Controlled Oscillator 2 |
| 5   | Reserved   | Reserved                        |
| 6   | CP2        | Charge Pump 2                   |
| 7   | Synth2     | Synthesizer 2                   |
| 8   | Mix1       | First Mixer                     |
| 9   | Reserved   | Reserved                        |
| 10  | LNA        | Low Noise Amplifier             |
| 11  | IF1        | First IF                        |
| 12  | IF2        | Second IF                       |
| 13  | Reserved   | Reserved                        |
| 14  | Reserved   | Reserved                        |
| 15  | AGC Amp    | AGC Amplifier                   |
| 16  | Ref Osc    | Reference Oscillator            |
| 17  | Buf2       | VCO 2 Buffer                    |
| 18  | RF Pwr Det | RF Power Detector               |
| 19  | IF Pwr Det | IF Power Detector               |

**REFERENCE OSCILLATOR REGISTER (CR-1)**

The Reference Oscillator register contains bits that affect the operation of the reference oscillator. There is only one bit that needs to be changed. That bit is **Osc Sel**. This should be set according to the table below. All other bits should be kept at their reset values with the exception of the start up sequence.

The start up programming sequence is as follows:

CR1 = 10 11xx xxxx 0001    Crystal Oscillator Register

CR0 = Power down register (typically program all circuits to power up with:  
0000 0000 0010 0000 0000 0000)

Wait 10mS before issuing next CR1 command

CR1 = 10 01xx xxxx 0001    (second CR1 command)

Wait 20mS between the second CR1 command and a CR9 command. (Other registers can be written during this 20mS wait period.)

CR9 (prescaler)

CR9 command for L01 auto tune

CR9 command for L02 auto tune

Note: The crystal oscillator needs to be operating before the CR9 registers are written.

| MSB     |         |    |    |    |    |    |    |    |    | LSB          |    |    |    | Reset State |
|---------|---------|----|----|----|----|----|----|----|----|--------------|----|----|----|-------------|
| R9      | R8      | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0       | 0       | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0  | 0  | 1  |             |
| Osc Sel | Ref Osc |    |    |    |    |    |    |    |    | Address Bits |    |    |    |             |

Figure 9. Reference Oscillator Register Format

Table 14. Oscillator Sel Bit

| Crystal Frequency  | Osc Sel |
|--------------------|---------|
| 4.0 MHz to <16 MHz | 0       |
| 16 MHz to 28 MHz   | 1       |

#### PROGRAMMABLE R1 & R2 REFERENCE DIVIDERS REGISTER (CR-2)

Selects the First and Second LO reference frequencies, which are divided down from the crystal frequency by the divide ratios specified by the respective Divider Ratio bits. The **Ref Buf En** bit enables the reference buffers for LO1 and

LO2. In normal operation, this bit is programmed to 1. The Reference Dividers are actually R+1 dividers, therefore the number to program into this register for R1 Divide Ratio and R2 Divide Ratio must be one less than the desired divide ratio.

| MSB             |     |     |     |     |            |                 |    |    |    |    |    |    |    |    | LSB          |    |    |    |             |
|-----------------|-----|-----|-----|-----|------------|-----------------|----|----|----|----|----|----|----|----|--------------|----|----|----|-------------|
| R14             | R13 | R12 | R11 | R10 | R9         | R8              | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0               | 0   | 0   | 0   | 1   | 1          | 0               | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0            | 0  | 1  | 0  | Reset State |
| R1 Divide Ratio |     |     |     |     | Ref Buf En | R2 Divide Ratio |    |    |    |    |    |    |    |    | Address Bits |    |    |    |             |

Figure 10. Reference Divider Register Format

#### REFERENCE BUFFER REGISTER (CR-3)

The BufIOP and BufIOM pins output a buffered reference oscillator signal. The oscillator frequency can be changed by the R3 divider before it exits the BufIO pins. The R3 divider

does not effect which frequency the tuner is tuned to. In addition, the gain of the sine wave buffer can be selected. If Buf Gain bit is 1 then the buffer is at full gain, if it is 0 it is at half gain.

| MSB      |     |          |     |          |     |    |                         |          |           |         |       |       |                 |    |    | LSB |    |    |    | Reset State  |  |  |  |
|----------|-----|----------|-----|----------|-----|----|-------------------------|----------|-----------|---------|-------|-------|-----------------|----|----|-----|----|----|----|--------------|--|--|--|
| R15      | R14 | R13      | R12 | R11      | R10 | R9 | R8                      | R7       | R6        | R5      | R4    | R3    | R2              | R1 | R0 | A3  | A2 | A1 | A0 |              |  |  |  |
| 1        | 1   | 1        | 1   | 1        | 1   | 1  | 0                       | 0        | 1         | 0       | 0     | 0     | 0               | 0  | 0  | 0   | 0  | 1  | 1  |              |  |  |  |
| R        | R   | R        | R   | R        | R   | R  | Buf I/O                 | Buf Gain | Tri State | Osc Scr | Mux 4 | Mux 3 | R3 Divide Ratio |    |    |     |    |    |    |              |  |  |  |
| Reserved |     | Reserved |     | Reserved |     |    | Sine Wave Buffer Output |          |           |         |       |       |                 |    |    |     |    |    |    | Address Bits |  |  |  |

Figure 11. Reference Buffer Register

**Table 15. R3 Divide Ratio**

| Divide Ratio | R2 | R1 | R0 |
|--------------|----|----|----|
| 1            | 0  | 0  | 0  |
| 2            | 1  | 0  | 0  |
| 4            | 1  | 0  | 1  |
| 6            | 1  | 1  | 0  |
| 8            | 1  | 1  | 1  |

**Table 16. Sine Wave Buffer Configuration**

| Condition | R8 | R7 | R6 | R5 | R4 | R3 | R2 |
|-----------|----|----|----|----|----|----|----|
|-----------|----|----|----|----|----|----|----|

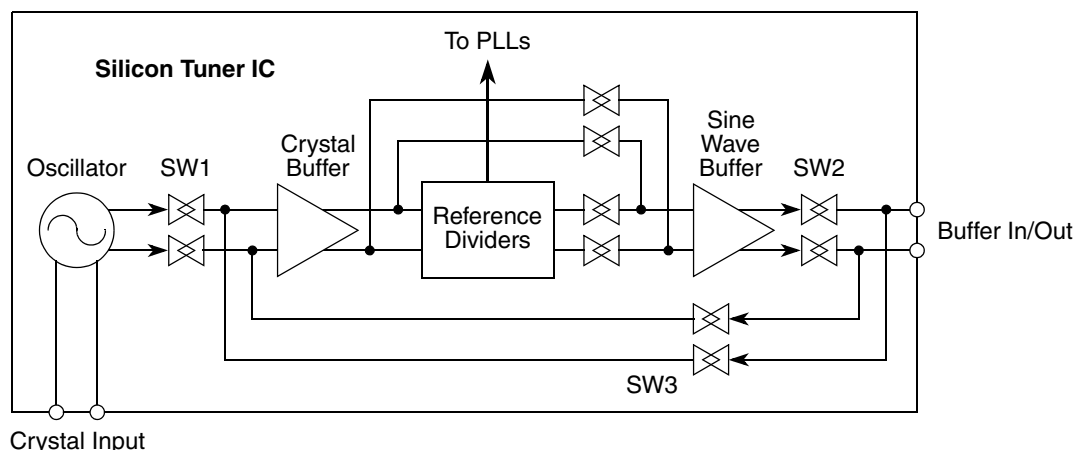
The Reference switches allow the Buffer In/Out pins to be reconfigured so that a second tuner can be driven from the crystal of a first tuner. The block diagram in Figure 12 shows where the switches are located. Programming a 1 to **Buf I/O**

**Table 16. Sine Wave Buffer Configuration (continued)**

|                                      |   |                     |   |   |   |   |   |
|--------------------------------------|---|---------------------|---|---|---|---|---|
| Normal Crystal Op                    | 0 | 0                   | 1 | 0 | 0 | 0 | 0 |
| Pass Thru Crystal Freq               | 0 | Note <sup>(1)</sup> | 0 | 0 | 0 | 1 | 0 |
| Divide by 2, 4, 6, 8, or 10          | 0 | Note <sup>(1)</sup> | 0 | 0 | 1 | 0 | 1 |
| Reverse Path for Osc Source          | 1 | 0                   | 1 | 1 | 0 | 0 | 0 |
| Pass Ref Osc Directly to Buffer Pins | 1 | 0                   | 1 | 0 | 0 | 0 | 0 |

1. Depends on Amplitude 0 = Low Gain, 1 = High Gain

and **Buf Scr** routes the divided oscillator signal out the Buf I/O pins. A 0 allows the crystal from another tuner to drive this tuner. See the Reference Oscillator section for more information on multi tuner configurations.



**Figure 12. Reference Oscillator Buffer**

#### RESET/SERIAL OUT REGISTER (CR-4)

The Reset/Serial Out Register consists of a 2-bit latch. The part will be in reset when a logic "1" is written to the **RS** bit location. **The part will be in reset until a logic "0" is written to the RS bit location.** The serial data format is shown below. This register or the power on reset (POR) circuitry

output will initiate reset. The Reset States of registers is indicated where applicable.

Writing a logic "1" to the **SO** bit location will activate the MISO port. The part will disable the MISO port upon a reset. This only affects SPI operation not I<sup>2</sup>C operation. **SC** is always programmed to 0.

| MSB |    |    |              |    |    |    | LSB         |
|-----|----|----|--------------|----|----|----|-------------|
| R2  | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0   | 0  | 0  | 0            | 1  | 0  | 0  | Reset State |
| SC  | SO | RS | Address Bits |    |    |    |             |

**Figure 13. Reset/Serial Out Register Format**

Table 17. Reset State Table

| State        | RS |
|--------------|----|
| Not In Reset | 0  |
| In Reset     | 1  |

Table 18. SO Setup Register Table

| S0 | Function    |             |
|----|-------------|-------------|
| 0  | SO Disabled | Reset State |
| 1  | SO Active   |             |

**LOCAL OSCILLATOR 1 REGISTER (CR-5)**

The N1 divider consists of a 12 bit N counter. The range of N1 values is from 2 to 4097. The serial data format is shown

in Table 19. This N divider is actually an N+2 divider. In other words, the bits that are programmed into the register are 2 less than what is calculated for the given frequency.

| MSB        |     |    |    |    |    |    |    |    |    |    |    | LSB          |    |    |    |             |
|------------|-----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|-------------|
| R11        | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0          | 0   | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0            | 1  | 0  | 1  | Reset State |
| N11        | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | Address Bits |    |    |    |             |
| N1 Counter |     |    |    |    |    |    |    |    |    |    |    |              |    |    |    |             |

Figure 14. LO 1 Register Format

Table 19. 12 Bit N Counter Control Bits (N1)

| N Counter Value | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |             |
|-----------------|-----|-----|----|----|----|----|----|----|----|----|----|----|-------------|
| 2               | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |             |
| *               | *   | *   | *  | *  | *  | *  | *  | *  | *  | *  | *  | *  |             |
| 421             | 0   | 0   | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | Reset State |
| *               | *   | *   | *  | *  | *  | *  | *  | *  | *  | *  | *  | *  |             |
| 4097            | 1   | 1   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |             |

**Counter Value Functions (N1)**

The First LO Frequency is a function of reference frequency and the N1 and R1 dividers as described in the  $F_{VCO1}$  equation.

$$F_{VCO1} = N1 * F_{OSC} / R1$$

Where:

- $F_{VCO1}$ : Output frequency of the first voltage controlled oscillator (VCO1)

- N1: Value of control bits for 15 bit programmable N1 counter. (N1-2 is actually programmed into register)
- $F_{OSC}$ : Output frequency of the reference frequency oscillator. (Example:  $F_{OSC} = 4.0$  MHz)
- R1: Divide ratio of first programmable reference counter.
- $F_{REF1}$ : Reference Frequency for First LO.  $F_{REF1} = F_{OSC} / R1$ . (R1-1 is actually programmed into Reference Dividers register)

**LOCAL OSCILLATOR 2 REGISTER (CR-6)**

The N2 divider consists of a 15 bit N counter. The range of N2 values is from 2 to 32769. The serial data format is shown

in Table 20. This N divider is actually an N+2 divider. In other words, the bits that are programmed into the register are 2 less than what is calculated for the given frequency.

| MSB        |     |     |     |     |    |    |    |    |    |    |    |    |    |    | LSB          |    |    |    |             |
|------------|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|-------------|
| R14        | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0          | 0   | 1   | 0   | 0   | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 0            | 1  | 1  | 0  | Reset State |
| N14        | N13 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | Address Bits |    |    |    |             |
| N2 Counter |     |     |     |     |    |    |    |    |    |    |    |    |    |    |              |    |    |    |             |

Figure 15. LO 2 Register Format



**Table 20. 15 Bit N Counter Control Bits (N2)**

| N Counter Value | N14 | N15 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |             |
|-----------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-------------|
| 2               | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |             |
| *               | *   | *   | *   | *   | *   | *  | *  | *  | *  | *  | *  | *  | *  | *  | *  |             |
| 4310            | 0   | 0   | 1   | 0   | 0   | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | Reset State |
| *               | *   | *   | *   | *   | *   | *  | *  | *  | *  | *  | *  | *  | *  | *  | *  |             |
| 32769           | 1   | 1   | 1   | 1   | 1   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |             |

### Counter Value Functions (N2)

The Second LO Frequency is a function of reference frequency and the N2 and R2 dividers as described in the  $F_{VCO2}$  equation.

$$F_{VCO2} = N2 * F_{OSC} / R2$$

Where:

- $F_{VCO2}$ : Output frequency of the second voltage controlled oscillator (VCO2)
- N2: Value of control bits for 15 bit programmable N2 counter. (N2-2 is actually programmed into register)

- $F_{OSC}$ : Output frequency of the reference frequency oscillator. (Example:  $F_{OSC} = 4.0$  MHz)
- R2: Divide ratio of second programmable reference counter.
- $F_{REF2}$ : Reference Frequency for Second LO.  
 $F_{REF2} = F_{OSC} / R2$ . (R2-1 is actually programmed into Reference Dividers register)

### CIRCUIT ADJUST REGISTER (CR-7)

The Circuit Adjust Register provides gain and power adjustments to various circuits.

| MSB            |              |              |          |            |      |      |           |         |             |                        |          |          |                       |          |    |          | LSB          |    |    |    |             |
|----------------|--------------|--------------|----------|------------|------|------|-----------|---------|-------------|------------------------|----------|----------|-----------------------|----------|----|----------|--------------|----|----|----|-------------|
| R16            | R15          | R14          | R13      | R12        | R11  | R10  | R9        | R8      | R7          | R6                     | R5       | R4       | R3                    | R2       | R1 | R0       | A3           | A2 | A1 | A0 |             |
| 0              | 0            | 0            | 0        | 0          | 0    | 0    | 0         | 1       | 1           | 1                      | 1        | 1        | 1                     | 0        | 1  | 1        | 0            | 1  | 1  | 1  | Reset State |
| CLIF           | CLRF         | LP5          | Reserved | LP3        | LPB2 | LPB1 | LPB0      | S1      | G7          | G6                     | Reserved | Reserved | G3                    | Reserved | G1 | Reserved | Address Bits |    |    |    |             |
| IF Detec tor   | RF Detec tor | IF AGC Amp   |          | Post Amp 2 | Mix1 |      | Pre Amp 1 | Out Sel | IF Amp Gain | Post Amp 2 Gain Adjust |          |          | Pre Amp 1 Gain Adjust |          |    |          |              |    |    |    |             |
| Clear Detector |              | Power Adjust |          |            |      |      |           |         |             |                        |          |          |                       |          |    |          |              |    |    |    |             |

**Figure 16. Circuit Adjust Register Format**

The **G7** and **G6** bits give a limited amount of gain control to Second IF Amplifier. This gain adjustment is not intended for AGC control but as a way to easily adjust the gain distribution within the tuner. Table 21 shows the affect of the **IF Amp Gain** bits.

**Table 21. IF Amp Gain**

| IF Amp Gain | G7 | G6 |             |
|-------------|----|----|-------------|
| 6.0 dB      | 0  | 0  |             |
| 12 dB       | 0  | 1  |             |
| 18 dB       | 1  | 0  |             |
| 20 dB       | 1  | 1  | Reset State |

In a similar manner, **G3** adjusts the gain of the Post Amplifier 2 as shown in Table 22.

**Table 22. Post Amp 2 Gain**

| Post Amp 2 Gain | G3 |             |
|-----------------|----|-------------|
| 6.0 dB          | 0  |             |
| 8.3 dB          | 1  | Reset State |

The **G1** bit adjusts the gain of Pre Amplifier 1 as shown in Table 23.

**Table 23. Pre Amp 1 Gain**

| Pre Amp 1 Gain | G1 |             |
|----------------|----|-------------|
| Nominal        | 0  |             |
| +1.0 dB        | 1  | Reset State |

The Power Adjust bits put their respective amplifiers into Low Power mode, which consumes half the power. For bits **LP3** and **LP5** a 1 puts the amplifier in low power mode and a 0 puts it in nominal mode. For bit **LPB0** a 0 puts Pre Amp 1 in a low power mode and a 1 puts it in nominal mode.

Table 24 shows the settings for bits **LPB2** and **LBP1** for adjusting the power level of Mixer 1.

**Table 24. Mixer 1 Power Adjust**

| Mixer 1 Power | LPB2 | LBP1 | Reset State |
|---------------|------|------|-------------|
| Low           | 0    | 0    |             |
| Nominal       | 0    | 1    |             |
| Middle        | 1    | 0    |             |
| High          | 1    | 1    |             |

The **S1**, Output Select, routes the signal to one of the two Second IF output paths as shown in Table 25.

**Table 25. Output Select**

| State        | S1 | Reset State |
|--------------|----|-------------|
| Analog Port  | 0  |             |
| Digital Port | 1  |             |

**CLRF** and **CLIF** bits clear the RF and IF detector respectively. The peak detectors continue to record the peak levels that they see until they are cleared and a new measurement starts. To clear the detector, write a 1 to **CLRF** or **CLIF**. Then write a 0 to **CLRF** or **CLIF** to bring the detector out of the clear state. The detector will then operate in a “max hold” mode where it continually records the highest peak that it sees.

## TEST REGISTER (CR-8)

The Test Register controls the various self test modes and directs test signals to the test pins.

| MSB  |              |             |      |          |      |     |     |     |    |              |                 |     |     |     |                 |     |     |     | LSB          |    |    |    |             |
|------|--------------|-------------|------|----------|------|-----|-----|-----|----|--------------|-----------------|-----|-----|-----|-----------------|-----|-----|-----|--------------|----|----|----|-------------|
| R18  | R17          | R16         | R15  | R14      | R13  | R12 | R11 | R10 | R9 | R8           | R7              | R6  | R5  | R4  | R3              | R2  | R1  | R0  | A3           | A2 | A1 | A0 |             |
| 0    | 0            | 0           | 0    | 0        | 0    | 0   | 0   | 0   | 0  | 0            | 1               | 0   | 1   | 1   | 1               | 0   | 1   | 1   | 1            | 0  | 0  | 0  | Reset State |
| T6   | RL           | RE          | T5   | AB       | T4   | T3  | T2  | T1  | T0 | GP           | TB3             | TB2 | TB1 | TB0 | TA3             | TA2 | TA1 | TA0 |              |    |    |    |             |
| Test | Reg Test Low | Reg Test En | Test | Func Sel | Test |     |     |     |    | Gen Purp Out | Test Pin Func B |     |     |     | Test Pin Func A |     |     |     | Address Bits |    |    |    |             |

**Figure 17. Test Register Format**

**RE – Regulator Test Enable:** Enables the internal regulator testing.

**RL – Regulator Test Low:** Determines if High Voltage Test = 0 or Low Voltage Test = 1 is tested when test is enabled.

Test bits: **T6:T0** are always programmed to 0.

The **Test Pin Function** bits control which signal is sent to the test pin. The test pin has a user selectable function that is used to monitor internal signals for test and development. The **TB3:TB0** and **TA3:TA0** are used to select the function. The **Func Sel:AB** bit is use to choose between function list A (0) shown in Table 26 and function list B (1) shown in Table 27. In normal operation, the **Test Pin Func** bits should be set to the Disable mode, which is the reset state. Or, the lock status could be routed to a microprocessor input for monitoring. When the PLL lock detect logic signal is sent to the test pin, a high state indicates PLL in lock.

The **Gen Purp Out** bit can be routed out the test pin. The test pin could then be used as a logic output to control an external circuit. The state of the logic output would then be changed by programming **Gen Purp Out**.

**Table 26. Test Pin Function List A**

| Test Function # | TA3 | TA2 | TA1 | TA0 | Test Pin Function A             |             |
|-----------------|-----|-----|-----|-----|---------------------------------|-------------|
| 0               | 0   | 0   | 0   | 0   | PLL2 Lock Detect                |             |
| 1               | 0   | 0   | 0   | 1   | Not Used                        |             |
| 2               | 0   | 0   | 1   | 0   | VCO 1 Out                       |             |
| 3               | 0   | 0   | 1   | 1   | General Purpose Output 1        |             |
| 4               | 0   | 1   | 0   | 0   | Power On Reset Bar              |             |
| 5               | 0   | 1   | 0   | 1   | PLL1 & PLL2 Lock Detect         |             |
| 6               | 0   | 1   | 1   | 0   | VCO 1 in Range                  |             |
| 7               | 0   | 1   | 1   | 1   | PLL1 Lock Detect                |             |
| 8               | 1   | 0   | 0   | 0   | R1 Ref Divider Out, $\div 2$    |             |
| 9               | 1   | 0   | 0   | 1   | PLL2 Prog Divider Out, $\div 2$ |             |
| 10              | 1   | 0   | 1   | 0   | VCO 1 Divided by 64 Out         |             |
| 11              | 1   | 0   | 1   | 1   | Disable = Low                   | Reset State |
| 12              | 1   | 1   | 0   | 0   | PLL1&2 LD & VCO1&2 In Range     |             |
| 13              | 1   | 1   | 0   | 1   | Phase Detect 1 Down Test        |             |
| 14              | 1   | 1   | 1   | 0   | Phase Detect 2 Down Test        |             |
| 15              | 1   | 1   | 1   | 1   | Reserved                        |             |

**Table 27. Test Pin Function List B**

| Test Function # | TB3 | TB2 | TB1 | TB0 | Test Pin Function B                |             |
|-----------------|-----|-----|-----|-----|------------------------------------|-------------|
| 0               | 0   | 0   | 0   | 0   | Reserved                           |             |
| 1               | 0   | 0   | 0   | 1   | VCO 2 Out                          |             |
| 2               | 0   | 0   | 1   | 0   | Not Used                           |             |
| 3               | 0   | 0   | 1   | 1   | Reserved                           |             |
| 4               | 0   | 1   | 0   | 0   | Sinewave Buffer                    |             |
| 5               | 0   | 1   | 0   | 1   | Reserved                           |             |
| 6               | 0   | 1   | 1   | 0   | VCO 2 In Range                     |             |
| 7               | 0   | 1   | 1   | 1   | PLL2 Lock Detect                   |             |
| 8               | 1   | 0   | 0   | 0   | R2 Reference Divider Out, $\div 2$ |             |
| 9               | 1   | 0   | 0   | 1   | PLL1 Prog Divider Out, $\div 2$    |             |
| 10              | 1   | 0   | 1   | 0   | VCO 2 Divided by 64 Out            |             |
| 11              | 1   | 0   | 1   | 1   | Disable = Low                      | Reset State |
| 12              | 1   | 1   | 0   | 0   | Phase Detect 1 Up Test             |             |
| 13              | 1   | 1   | 0   | 1   | Phase Detect 2 Up Test             |             |
| 14              | 1   | 1   | 1   | 0   | Reserved                           |             |
| 15              | 1   | 1   | 1   | 1   | Reserved                           |             |

## DIGITAL TUNE MODULE (CR-9)

CR-9 is unique in that CR-9 register data is latched with the crystal clock while all other registers are latched with the SPI/I2C clock. Therefore, the crystal oscillator must be running before data is written to CR-9.

The Digital Tune module is a state machine that controls the capacitors in the VCOs for both VCO 1 and VCO 2. This is used as a coarse tune adjustment for the VCO frequency.

The Digital Tune Module is controlled through five registers. In addition to the normal control register address, it uses an additional three address bits (DT Address) to access one of the five Digital Tune registers. There is also a **RW** bit that determines which register is read back; 1 = Read and 0 = Write. The following diagrams show a description of the registers.

| MSB   |       |       |       |       |       |      |      |      |      |      |      |      |      |      |            |    |     |     |     | LSB          |    |    |    |             |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------------|----|-----|-----|-----|--------------|----|----|----|-------------|
| R19   | R18   | R17   | R16   | R15   | R14   | R13  | R12  | R11  | R10  | R9   | R8   | R7   | R6   | R5   | R4         | R3 | R2  | R1  | R0  | A3           | A2 | A1 | A0 |             |
|       | 0     | 0     | 0     | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0          | 0  | 0   | 0   | 0   | 1            | 0  | 0  | 1  | Reset State |
| DC 15 | DC 14 | DC 13 | DC 12 | DC 11 | DC 10 | DC 9 | DC 8 | DC 7 | DC 6 | DC 5 | DC 4 | DC 3 | DC 2 | DC 1 | DC 0       | RW | DA2 | DA1 | DA0 | Address Bits |    |    |    |             |
|       |       |       |       |       |       |      | Rst  |      |      |      |      |      | XOd  |      | DT Address |    |     |     |     |              |    |    |    |             |

Figure 18. Digital Tune Register: XO Prescale Format

**Rst.** Writing a 1 to this bit will cause all Tune Request bits to clear, the count registers will clear, and the tuning state machine will return to idle state. To resume normal operation, first clear this bit and then proceed. This bit is for abnormal error recovery situations and should normally not be required.

**XOd.** This field is used to specify a pre-scale value. It is set according to what the crystal oscillator frequency is. Refer to the following table. This allows the count of the VCO cycles to exceed 2000 in the lowest VCO frequency case and be less than 8000 in the highest VCO frequency case.

Table 28. Prescaler Selection

| Crystal Freq                                  | Prescale | XOd1 | XOd0 | VCO Counting Time |
|-----------------------------------------------|----------|------|------|-------------------|
| $4.0 \text{ MHz} \leq x < 4.2 \text{ MHz}$    | 1        | 0    | 0    | 15 XO clocks      |
| $4.2 \text{ MHz} \leq x < 8.2 \text{ MHz}$    | 2        | 0    | 1    | 30 XO clocks      |
| $8.2 \text{ MHz} \leq x < 16.5 \text{ MHz}$   | 4        | 1    | 0    | 60 XO clocks      |
| $16.5 \text{ MHz} \leq x \leq 28 \text{ MHz}$ | 8        | 1    | 1    | 120 XO clocks     |

| MSB   |       |       |                     |       |       |      |      |      |      |      |      |      |      |      |            |    |      |      |      | LSB          |    |    |    |             |
|-------|-------|-------|---------------------|-------|-------|------|------|------|------|------|------|------|------|------|------------|----|------|------|------|--------------|----|----|----|-------------|
| R19   | R18   | R17   | R16                 | R15   | R14   | R13  | R12  | R11  | R10  | R9   | R8   | R7   | R6   | R5   | R4         | R3 | R2   | R1   | R0   | A3           | A2 | A1 | A0 |             |
| 0     | 0     | 0     | 0                   | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0          | 0  | 0    | 0    | 1    | 1            | 0  | 0  | 1  | Reset State |
| DC 15 | DC 14 | DC 13 | DC 12               | DC 11 | DC 10 | DC 9 | DC 8 | DC 7 | DC 6 | DC 5 | DC 4 | DC 3 | DC 2 | DC 1 | DC 0       | RW | DA 2 | DA 1 | DA 0 | Address Bits |    |    |    |             |
|       | MT1   | AT1   | LO1 Reference Count |       |       |      |      |      |      |      |      |      |      |      | DT Address |    |      |      |      |              |    |    |    |             |

Figure 19. Digital Tune Register: LO1 Reference Register Format

| MSB   |       |       |                     |       |       |      |      |      |      |      |      |      |      |      |            |    |      |      |      | LSB          |    |    |    |             |
|-------|-------|-------|---------------------|-------|-------|------|------|------|------|------|------|------|------|------|------------|----|------|------|------|--------------|----|----|----|-------------|
| R19   | R18   | R17   | R16                 | R15   | R14   | R13  | R12  | R11  | R10  | R9   | R8   | R7   | R6   | R5   | R4         | R3 | R2   | R1   | R0   | A3           | A2 | A1 | A0 |             |
| 0     | 0     | 0     | 0                   | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0          | 0  | 0    | 1    | 0    | 1            | 0  | 0  | 1  | Reset State |
| DC 15 | DC 14 | DC 13 | DC 12               | DC 11 | DC 10 | DC 9 | DC 8 | DC 7 | DC 6 | DC 5 | DC 4 | DC 3 | DC 2 | DC 1 | DC 0       | RW | DA 2 | DA 1 | DA 0 | Address Bits |    |    |    |             |
|       | MT2   | AT2   | LO2 Reference Count |       |       |      |      |      |      |      |      |      |      |      | DT Address |    |      |      |      |              |    |    |    |             |

Figure 20. Digital Tune Register: LO2 Reference Register Format

**MT1** and **MT2**. The Manual Tune request bits will initiate a Manual Tune cycle for LO1 and LO2, respectively. The Manual Tune cycle will count the selected VCO frequency and put the result in the LO1 or LO2 Result Count register. The Manual Tune bit will be automatically cleared when the count is finished. This is really just a way to measure the current frequency.

**AT1** and **AT2**. The Auto Tune request bits will initiate an Automatic Tune cycle for LO1 and LO2 respectively. Upon completion of the Auto Tune cycle, this bit will automatically clear. After the Auto Tune cycle is completed the coarse tuning is finished.

The **LO1** and **LO2 Reference Count** is used to tell the Auto Tune cycle what frequency to tune to. It is not needed for a Manual Tune request. Write the respective reference count at the same time as setting **AT1** or **AT2**. The following equation is used to determine the reference count.

$$\text{Reference Count} = (15 * XOd * F) / (2 * XO)$$

Where: F = desired VCO frequency in MHz

XO = crystal frequency in MHz

XOd = XOdvider = 1, 2, 4, or 8 as specified in the XO Prescaler register.

| MSB   |       |       |       |                  |       |      |      |      |      |      |      |      |      |      |      |            |     |     |     | LSB          |    |    |    |             |
|-------|-------|-------|-------|------------------|-------|------|------|------|------|------|------|------|------|------|------|------------|-----|-----|-----|--------------|----|----|----|-------------|
| R19   | R18   | R17   | R16   | R15              | R14   | R13  | R12  | R11  | R10  | R9   | R8   | R7   | R6   | R5   | R4   | R3         | R2  | R1  | R0  | A3           | A2 | A1 | A0 |             |
| 0     | 0     | 0     | 0     | 0                | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0          | 0   | 1   | 1   | 1            | 0  | 0  | 1  | Reset State |
| DC 15 | DC 14 | DC 13 | DC 12 | DC 11            | DC 10 | DC 9 | DC 8 | DC 7 | DC 6 | DC 5 | DC 4 | DC 3 | DC 2 | DC 1 | DC 0 | RW         | DA2 | DA1 | DA0 | Address Bits |    |    |    |             |
|       |       |       |       | LO1 Result Count |       |      |      |      |      |      |      |      |      |      |      | DT Address |     |     |     |              |    |    |    |             |

Figure 21. Digital Tune Register: LO1 Result Count (Read Only) Register Format

| MSB   |       |       |       |                  |       |      |      |      |      |      |      |      |      |      |      |            |     |     |     | LSB          |    |    |    |             |
|-------|-------|-------|-------|------------------|-------|------|------|------|------|------|------|------|------|------|------|------------|-----|-----|-----|--------------|----|----|----|-------------|
| R19   | R18   | R17   | R16   | R15              | R14   | R13  | R12  | R11  | R10  | R9   | R8   | R7   | R6   | R5   | R4   | R3         | R2  | R1  | R0  | A3           | A2 | A1 | A0 |             |
| 0     | 0     | 0     | 0     | 0                | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0          | 1   | 0   | 0   | 1            | 0  | 0  | 1  | Reset State |
| DC 15 | DC 14 | DC 13 | DC 12 | DC 11            | DC 10 | DC 9 | DC 8 | DC 7 | DC 6 | DC 5 | DC 4 | DC 3 | DC 2 | DC 1 | DC 0 | RW         | DA2 | DA1 | DA0 | Address Bits |    |    |    |             |
|       |       |       |       | LO2 Result Count |       |      |      |      |      |      |      |      |      |      |      | DT Address |     |     |     |              |    |    |    |             |

Figure 22. Digital Tune Register: LO2 Result Count (Read Only)

## LNA AGC REGISTER (CR-10)

The variable gain LNA (Low Noise Amplifier) is used to provide automatic gain control (AGC) at the RF frequency. The gain is varied with an external analog control voltage or digitally via the interface bus using **G5:G0**. The Control bits **AGC An Dig** bit determines if either analog or digital control is controlling the AGC. There are two RF AGC control pins,

**FEAGC\_A** and **FEAGC\_B**. This facilitates having the tuner connected to both analog and digital demodulators as found in many set-top boxes, thus eliminating the need for an external switch and its controls. The **AGC Sel** bit controls which of these pins are used. Figure 23 shows the LNA AGC register format.

| MSB      |     |       |         |      |             |          |            |          |          |          |          |       |     |            |    |    |    |    |    | LSB          |    |    |    | Reset State |
|----------|-----|-------|---------|------|-------------|----------|------------|----------|----------|----------|----------|-------|-----|------------|----|----|----|----|----|--------------|----|----|----|-------------|
| R19      | R18 | R17   | R16     | R15  | R14         | R13      | R12        | R11      | R10      | R9       | R8       | R7    | R6  | R5         | R4 | R3 | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 0        | 0   | 0     | 0       | 1    | 0           | 0        | 0          | 0        | 0        | 0        | 0        | 0     | 0   | 0          | 1  | 1  | 1  | 1  | 0  | 1            | 0  | 1  | 0  |             |
| B2       | B1  | At0   | AGC Sel | LNA0 | AGC Read En | Atten En | AGC An Dig | HL GR En | Reserved | Reserved | Reserved | At2   | At1 | G5         | G4 | G3 | G2 | G1 | G0 | Address Bits |    |    |    |             |
| LNA Bias |     | Atten |         |      |             |          |            |          |          |          |          | Atten |     | Normal AGC |    |    |    |    |    |              |    |    |    |             |

Figure 23. LNA AGC Register Format

There is a programmable attenuator between the LNA and Mixer 1. To control this attenuator set **At2**, **At1**, and **At0** as shown in the Table 29 below. When the attenuator is set to a value greater than 0 dB, the **HL GR En** bit and **Atten En** bit is set high. This fixed gain adjustment has less of an affect on noise figure than setting the LNA gain while still improving distortion performance by limiting the levels hitting the first mixer.

Table 29. Attenuator Control

| Attenuation | Attn En | HL GR En | At 2 | At1 | At0 |
|-------------|---------|----------|------|-----|-----|
| 0 dB        | 0       | 0        | 1    | 1   | 0   |
| 1.1 dB      | 1       | 1        | 1    | 1   | 1   |
| 2.2 dB      | 1       | 1        | 0    | 1   | 0   |
| 3.2 dB      | 1       | 1        | 0    | 1   | 1   |
| 4.1 dB      | 1       | 1        | 1    | 0   | 0   |
| 4.8 dB      | 1       | 1        | 1    | 0   | 1   |
| 5.6 dB      | 1       | 1        | 0    | 0   | 0   |
| 6.3 dB      | 1       | 1        | 0    | 0   | 1   |

Digital control, bits **G5:G0** are used to set the LNA gain. Values range from 0 maximum gain to 63 minimum gain. When using analog control the gain bits are not set. However, the equivalent gain setting can be read back from the part. The **AGC Read En** bit allows reading back of the RF AGC setting. A 1 for this bit allows read back. This feature allows the tuner to report back where the demodulator has set the AGC gain. Note that when reading back this register, bits **G2:G0** are inverted.

Table 30. RF AGC Control

| Type of Control | AGC Sel | AGC AnDig | Gain Bits |
|-----------------|---------|-----------|-----------|
|                 |         |           | G5:G0     |
| Digital         | X       | 0         |           |
| FEAGC_A         | 1       | 1         | X:X       |
| FEAGC_B         | 0       | 1         | X:X       |

The **LNA0** bit changes the dc output bias of the LNA. The **LNA Bias** bits, **B2:B1**, control the bias voltage in the LNA. Table 31 shows how these bits should normally be programmed. When reading the Regulator Test Data register, **LNA0** should be set to 0; otherwise, the LNA regulator test will fail.

Table 31. LNA Bias Control

| LNA0 | LNA Bias Bits |
|------|---------------|
|      | B2:B1         |
| 1    | 01            |

## DATA ADDRESS REGISTER (CR-11)

The Data Address Register sets the address of the data register to be read back during the next read from the IC. See Read Operations Protocol section for more detail as to how this is used. The default Data Address corresponds to the LNA AGC register (CR 10).

| MSB          |    |    |    | LSB          |    |    |    |             |
|--------------|----|----|----|--------------|----|----|----|-------------|
| R3           | R2 | R1 | R0 | A3           | A2 | A1 | A0 |             |
| 1            | 0  | 1  | 0  | 1            | 0  | 1  | 1  | Reset State |
| D3           | D2 | D1 | D0 | Address Bits |    |    |    |             |
| Data Address |    |    |    |              |    |    |    |             |

**Figure 24. Data Address Register Format**

### DATA REGISTER DEFINITIONS

There are 16 Data Registers that can be read back from the IC. The 1011 Control Register (Data Register Address) controls which of these Data Registers will be read out of the IC during the next read operation. To select the desired Data

Register this address register first needs to be set. Then on the next read operation the desired data will be available.

The Data Register Format is shown in Figure 25.

| MSB                |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    | LSB |    |    |    |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----|----|----|----|
| D19                | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3  | D2 | D1 | D0 |
| Data Register Bits |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |     |    |    |    |

**Figure 25. Data Register Format**

Below is the Data Register Address Map that shows the function of each Data Register. The first 12 Data Registers read back the contents of the 12 Control Registers. They

have the same format as their corresponding Control Register. The rest of the registers display various status and self-diagnostic data.

**Table 32. Data Register Address Map**

| Register Function     | Address Bits |    |    |    |
|-----------------------|--------------|----|----|----|
| D19 – D0              | A3           | A2 | A1 | A0 |
| Power Down            | 0            | 0  | 0  | 0  |
| Reference Oscillator  | 0            | 0  | 0  | 1  |
| Reference Dividers    | 0            | 0  | 1  | 0  |
| Reference Buffer      | 0            | 0  | 1  | 1  |
| Reset/Serial Out      | 0            | 1  | 0  | 0  |
| LO 1                  | 0            | 1  | 0  | 1  |
| LO 2                  | 0            | 1  | 1  | 0  |
| Circuit Adjust        | 0            | 1  | 1  | 1  |
| Test                  | 1            | 0  | 0  | 0  |
| Digital Tune          | 1            | 0  | 0  | 1  |
| LNA AGC               | 1            | 0  | 1  | 0  |
| Data Register Address | 1            | 0  | 1  | 1  |
| Regulator Test        | 1            | 1  | 0  | 0  |
| VCO Test              | 1            | 1  | 0  | 1  |
| LNA Gain/Input Power  | 1            | 1  | 1  | 0  |
| ID Bits               | 1            | 1  | 1  | 1  |

## REGULATOR TEST DATA REGISTER (REGTEST)

The regulator comparator test compares the internal regulator voltages to reference voltages. A low voltage and high voltage test can be run. The type of test is determined by the **Reg Test Low** bit in the Test register. When **Reg Test Low** is High the low voltage test is run. When **Reg Test Low** is Low the high voltage test is run. In addition, to run either

test the **Reg Test En** bit in the Test register needs to be set high. In normal operation, when this test isn't being run, program the **Reg Test En** bit to 0. A failure of a Low test indicates the voltage is too low. For the low test, a 1 indicates correct operation. Similarly, a High test failure indicates the voltage is too high, but a 0 indicates correct operation.

| MSB                 |      |     |        |          |      |     |        |      |          |     |      |    |    |    |    | LSB |    |    |    |
|---------------------|------|-----|--------|----------|------|-----|--------|------|----------|-----|------|----|----|----|----|-----|----|----|----|
| D19                 | D18  | D17 | D16    | D15      | D14  | D13 | D12    | D11  | D10      | D9  | D8   | D7 | D6 | D5 | D4 | D3  | D2 | D1 | D0 |
| Reserved            | Buf1 | CP1 | Synth1 | Reserved | Buf2 | CP2 | Synth2 | Quad | Reserved | LNA | 1.8V |    |    |    |    |     |    |    |    |
| Regulator Test Bits |      |     |        |          |      |     |        |      |          |     |      |    |    |    |    |     |    |    |    |

Figure 26. Regulator Test Register Format

Table 33. Regulator Test Register Field Description

|     | Bit # | Circuit         | Bit Name |
|-----|-------|-----------------|----------|
| LSB | 0-6   | Reserved        |          |
|     | 7     | 1.8 V Regulator | 1.8 V    |
|     | 8     | Low Noise Amp   | LNA      |
|     | 9     | Reserved        |          |
|     | 10    | Reserved        |          |
|     | 11    | Reserved        | Reserved |
|     | 12    | Synthesizer 2   | Synth2   |
|     | 13    | Charge Pump 2   | CP2      |
|     | 14    | VCO Buffer 2    | BUF2     |
|     | 15    | Reserved        |          |
|     | 16    | Synthesizer 1   | Synth1   |
|     | 17    | Charge Pump 1   | CP1      |
|     | 18    | VCO Buffer 1    | BUF1     |
| MSB | 19    | Reserved        |          |

## VCO TEST REGISTER (VCOTEST)

The VCO test shows the results of various VCO tests including: first and second VCO tuning ranges and, first and second LO lock status.

| MSB           |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    | LSB |    |    |    |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----|----|----|----|
| D19           | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3  | D2 | D1 | D0 |
| RH1           | RL1 | RH2 | RL2 | LD1 | LD2 |     |     |     |     |    |    |    |    |    |    |     |    |    |    |
| VCO Test Bits |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |     |    |    |    |

Figure 27. VCO Test Register Format



**Table 34. VCO Test Register Field Description**

|     | Bit #  | Description            | Bit Name | Pass |
|-----|--------|------------------------|----------|------|
| LSB | 0 - 13 | Reserved               |          |      |
|     | 14     | Lock Detect LO2        | LD2      | 1    |
|     | 15     | Lock Detect LO1        | LD1      | 1    |
|     | 16     | VCO2 Out of Range Low  | RL2      | 0    |
|     | 17     | VCO2 Out of Range High | RH2      | 1    |
|     | 18     | VCO1 Out of Range Low  | RL1      | 0    |
| MSB | 19     | VCO1 Out of Range High | RH1      | 1    |

#### CURRENT LNA GAIN DATA REGISTER (LNAGain)

This register holds the current LNA gain setting in the 6 MSBs of the register. When controlled by an external analog control, the analog voltage is converted to a digital word using an analog to digital converter (ADC). The resulting value is contained in **LNA Gain Bits**. The **AGC**

**Read En** bit, in the LNA AGC register, must be set to 1 in order to allow reading back of the RF AGC setting. Note that when reading back this register, bits **G2:G0** are inverted. Also note that when in the analog mode, the readings for levels corresponding to 0 through 9 are all read back as 9.

| MSB           |     |     |     |     |     |        |     |     |        |    |    | LSB |    |    |    |    |    |    |    |
|---------------|-----|-----|-----|-----|-----|--------|-----|-----|--------|----|----|-----|----|----|----|----|----|----|----|
| D19           | D18 | D17 | D16 | D15 | D14 | D13    | D12 | D11 | D10    | D9 | D8 | D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| G5            | G4  | G3  | G2  | G1  | G0  | P2     | P1  | P0  | P2     | P1 | P0 |     |    |    |    |    |    |    |    |
| LNA Gain Bits |     |     |     |     |     | RF Pwr |     |     | IF Pwr |    |    |     |    |    |    |    |    |    |    |

**Figure 28. LNA Gain Register Format**

The **RF Pwr** bits contain the reading from the broadband power detector at the input of the IC. This is a broadband power detector that senses the total power at the input of the IC. It can be used to optimize performance of the front end by adjusting the AGC algorithm in case of high total input power. The **IF Pwr** bits contain the reading from the power detector at the second IF. It also is used to optimize performance.

**Table 35. IF Power Detector Levels**

|         | Level | P2 | P1 | P0 | Peak mV |
|---------|-------|----|----|----|---------|
| Highest | 4     | 1  | 0  | 0  | 1271    |
|         | 5     | 1  | 0  | 1  | 1113    |
|         | 7     | 1  | 1  | 1  | 994     |
|         | 6     | 1  | 1  | 0  | 881     |
|         | 2     | 0  | 1  | 0  | 800     |
|         | 3     | 0  | 1  | 1  | 700     |
|         | 1     | 0  | 0  | 1  | 629     |
| Lowest  | 0     | 0  | 0  | 0  | < 629   |

**Table 36. RF Power Detector Levels**

|         | Level | P2 | P1 | P0 | Peak mV |
|---------|-------|----|----|----|---------|
| Highest | 4     | 1  | 0  | 0  | 992     |
|         | 5     | 1  | 0  | 1  | 824     |
|         | 7     | 1  | 1  | 1  | 699     |
|         | 6     | 1  | 1  | 0  | 627     |
|         | 2     | 0  | 1  | 0  | 518     |
|         | 3     | 0  | 1  | 1  | 441     |
|         | 1     | 0  | 0  | 1  | 370     |
| Lowest  | 0     | 0  | 0  | 0  | < 370   |

The **CLRF** and **CLIF** bits of the Circuit Adjust register (CR-7), change the response time of RF and IF detectors, respectively. When set to instantaneous mode (1), the corresponding detector reads the instantaneous voltage peak. When set to normal mode (0), the input signals are integrated over a short period of time. This gives a more consistent reading. When there are many input signals, they add or subtract together on an instantaneous bases, so in the instantaneous mode there is more variation in detector readings than is typically desired. In either mode, a number

of readings should be taken and averaged. One needs to remember that the detector readings are Gray coded, so they need to be decoded before they are averaged. For the normal mode a minimum of 5 readings should be averaged. In instantaneous mode at least 32 readings should be averaged.

### IDENTIFICATION REGISTER (IDBITS)

These Identification (ID) bits are fixed for each mask revision. See Table 37 for the ID bit values.

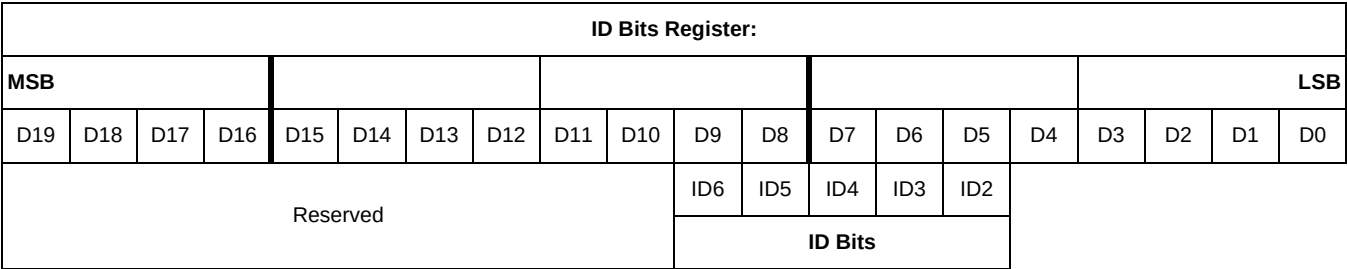


Figure 29. ID Register Format

Table 37. ID Register Bits

|     | Bit # | Description | Bit Value |
|-----|-------|-------------|-----------|
| LSB | 0-4   | Reserved    |           |
|     | 5     | ID Bit 2    | 0         |
|     | 6     | ID Bit 3    | 0         |
|     | 7     | ID Bit 4    | 1         |
|     | 8     | ID Bit 5    | 0         |
|     | 9     | ID Bit 6    | 1         |
| MSB | 10-19 | Reserved    |           |

## APPLICATIONS INFORMATION — SAMPLE SYSTEM DESIGN

Figure 30 shows a simplified block diagram for a sample system design. Note that the upstream and downstream frequency bands overlap. These are the limits of the frequency ranges. The actual bands are adjusted based on the target application.

Performance specifications (as previously listed in Table 6) dealing with overall tuner performance apply to the sample system design, since it includes the necessary filters.

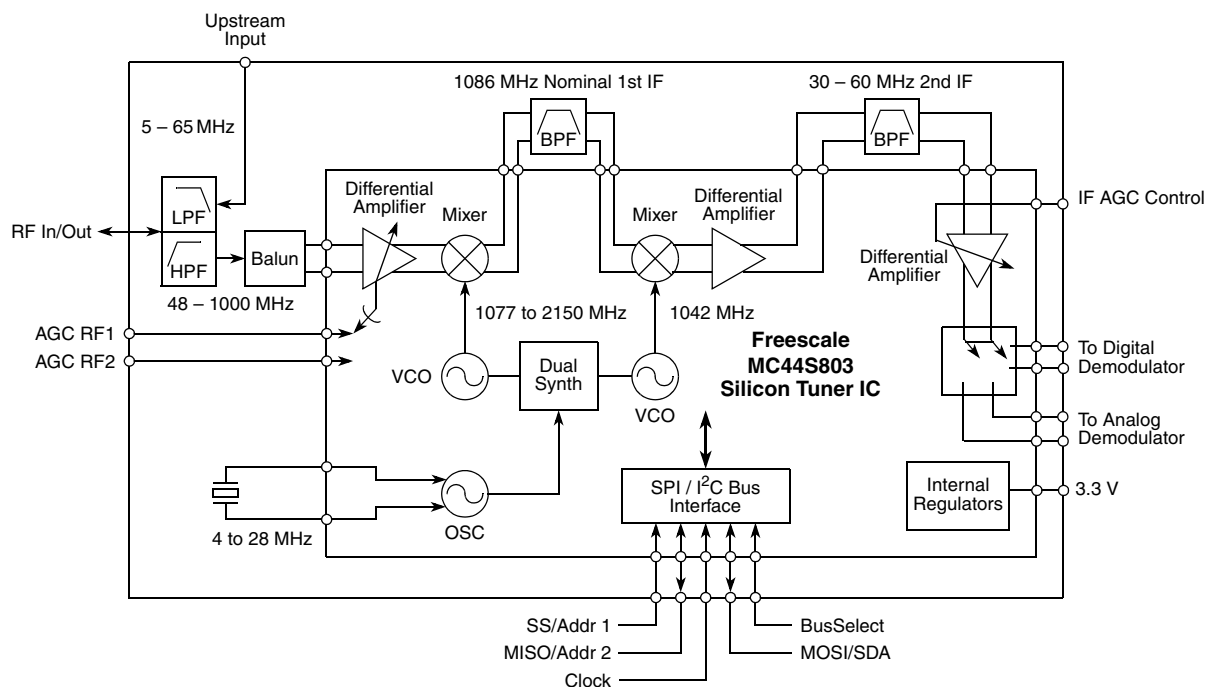


Figure 30. MC44S803 Silicon Tuner Sample System Design Block Diagram

## SECOND IF

The Second IF consists of the on chip amplifiers that boost the signal level so that it is high enough for the tuner to be directly connected to the demodulator. The output of Post Amp 2 is routed off chip through the channel SAW and back on chip to the second IF amplifiers. A switch is provided to route the signal to either a digital or an analog demodulator for settop box applications. The performance at the analog and digital IF output ports are identical. The IF Amplifier gain has some level of programmability. This is not intended for

Automatic Gain Control (AGC), but as a way to optimize the gain distribution. It is envisioned that this gain would be fixed at a certain level for the particular application. Since typical analog demodulators have a high range of AGC control built into them, the IF AGC control voltage will need to be fixed at some level when using these demodulators. When using a digital demodulator, the AGC control voltage is fed from the digital demodulator. This is usually a filtered PWM signal.

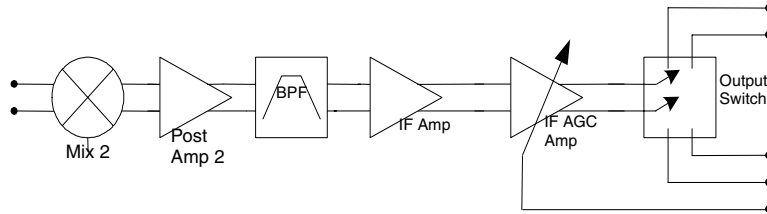


Figure 31. Second IF

Table 38. Second IF Amplifier Performance

| Parameter                          | Typ.               | Unit |
|------------------------------------|--------------------|------|
| Post Amplifier 2 Gain Settings     | 6.0 or 8.3         | dB   |
| IF Amplifier Gain Settings         | 6.0, 12, 18, or 20 | dB   |
| IF AGC Amplifier Gain at 0.5 V AGC | 36                 | dB   |
| IF AGC Amplifier Gain at 3.3 V AGC | 0                  | dB   |

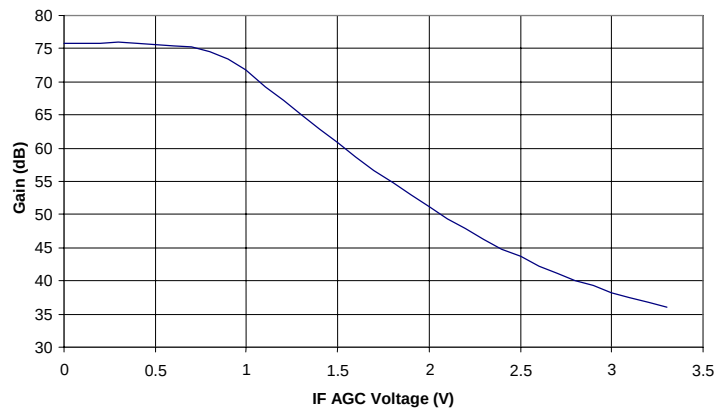


Figure 32. Tuner Gain versus IF AGC Voltage

## REFERENCE OSCILLATOR

The integrated reference oscillator requires an external crystal. The oscillator circuit is designed to accept a crystal in the frequency range of 4.0 MHz to 28 MHz.

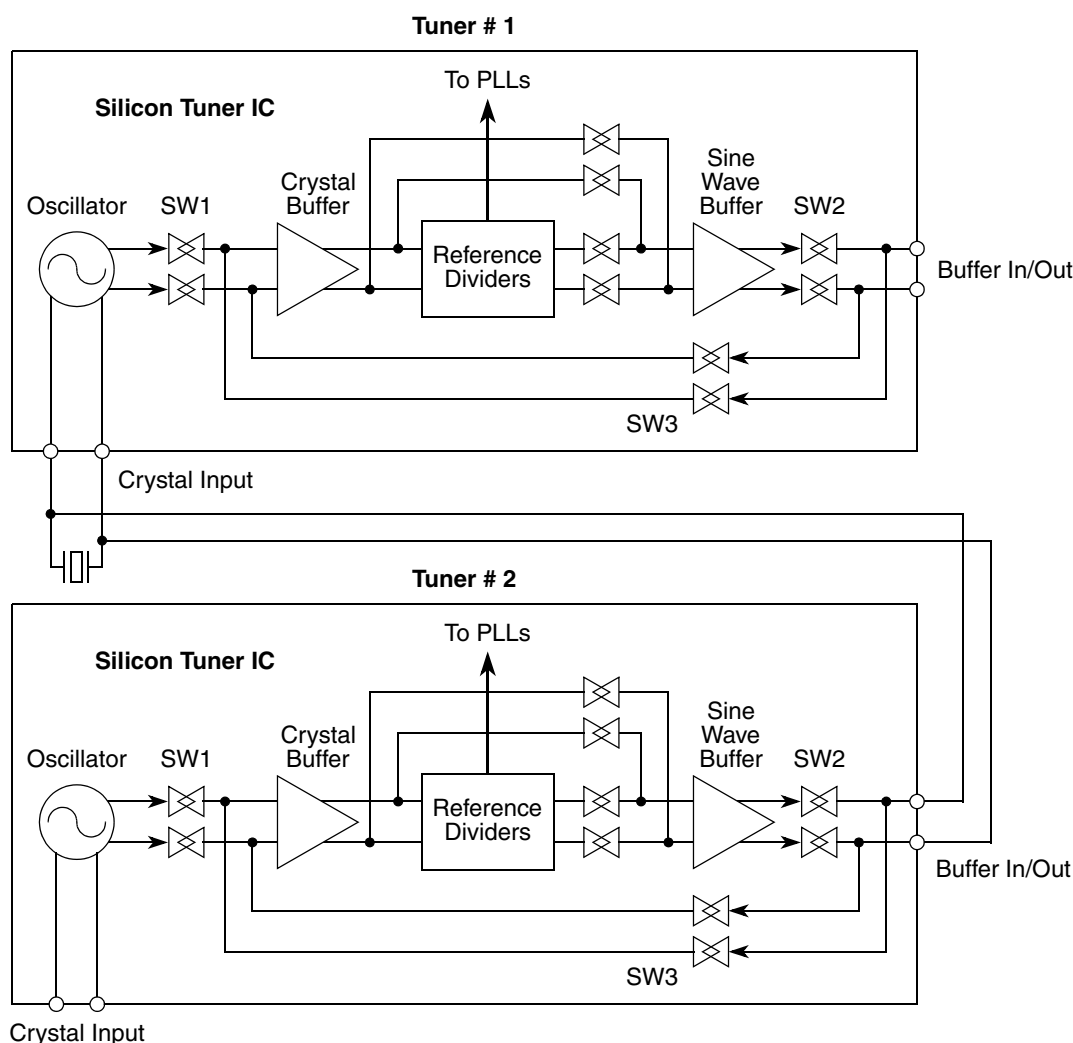
The oscillator drives the reference dividers for LO1 and LO2. Additionally, it goes through a Divide-By-R3 stage. Possible divider ratios are 1, 2, 4, 6, 8, or 10. For divide by 1, the signal is routed around the divider. The signal passes through a low pass filter to produce a sine wave. It is then buffered internally and output at pins BufIOP and BufIOM so that it can be used to drive other ICs such as an audio-video modulator in a settop box. If no other ICs are driven from this oscillator, nothing should be connected to BufIOP and BufIOM. The IC can be programmed to shut down the oscillator buffer if it is not used. It is enabled at power up and on reset.

In dual tuner applications, one crystal can drive two tuners, as shown in the following figures. This saves cost and

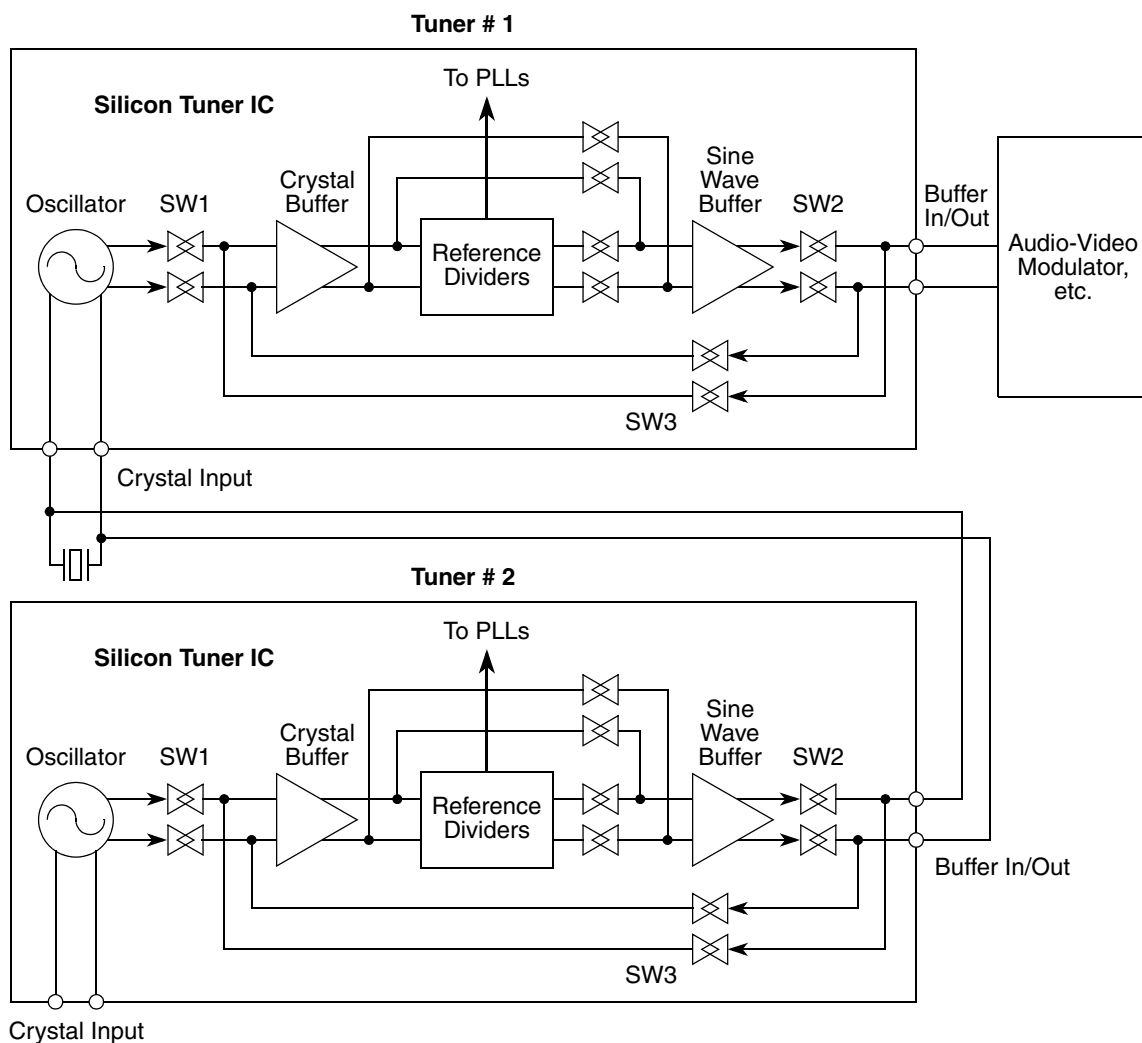
eliminates spur problems due to having multiple frequencies that are very close to each other but not exactly the same. In this case, the second tuner is connected up to the same crystal but fed into the Buffer In/Out pins. Internal switches of the second tuner are programmed to feed this signal to the Crystal Buffer. The internal switches of the first tuner are programmed to feed the output of the Sine Wave Buffer to a modulator or other IC. The other switches shown are to allow for a divide by 1 state.

**Table 39. Switch States**

|             | BufI/O bit | SW1    | SW2    | SW3    |
|-------------|------------|--------|--------|--------|
| Reset State | 0          | Closed | Closed | Open   |
| Tuner #1    | 0          | Closed | Closed | Open   |
| Tuner #2    | 7          | Open   | Open   | Closed |



**Figure 33. Two Receivers Sharing One Crystal**



**Figure 34. Two Receivers and Modulator Sharing One Crystal**

The CMOS Broadband Tuner IC is designed to work with a crystal meeting the crystal specifications shown in Table 40. Of course the frequency tolerance will be application specific. Look at the specification for the demodulator that you intend to use with the tuner for frequency tolerance that it needs to capture signal. Internal load capacitance is 10 pF, typical PC board stray capacitance is 3.0 or 4.0 pF.

**Table 40. Crystal Specifications**

|                  |                           |
|------------------|---------------------------|
| Frequency        | 4.0 MHz to 28 MHz         |
| Drive Level      | 500 $\mu$ W               |
| Load Capacitance | 13 pF                     |
| Resistance       | 10 Ohms typ, 100 Ohms max |

## TYPICAL APPLICATION CONFIGURATIONS

Figure 35 and Figure 36 are block diagrams that show how the Silicon Tuner is used in multiple applications.

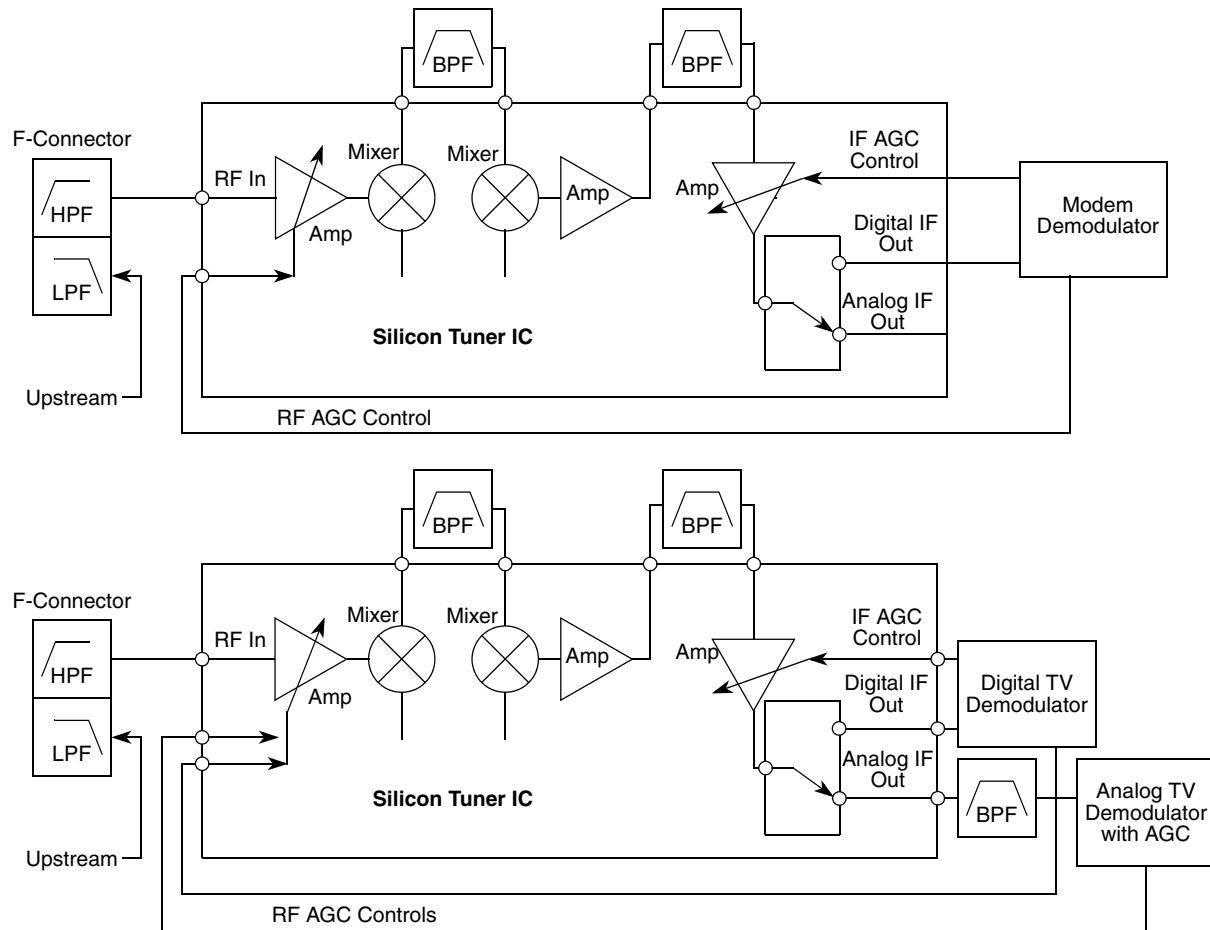


Figure 35. Modem and Digital/Analog Settop Box Using Silicon Tuner

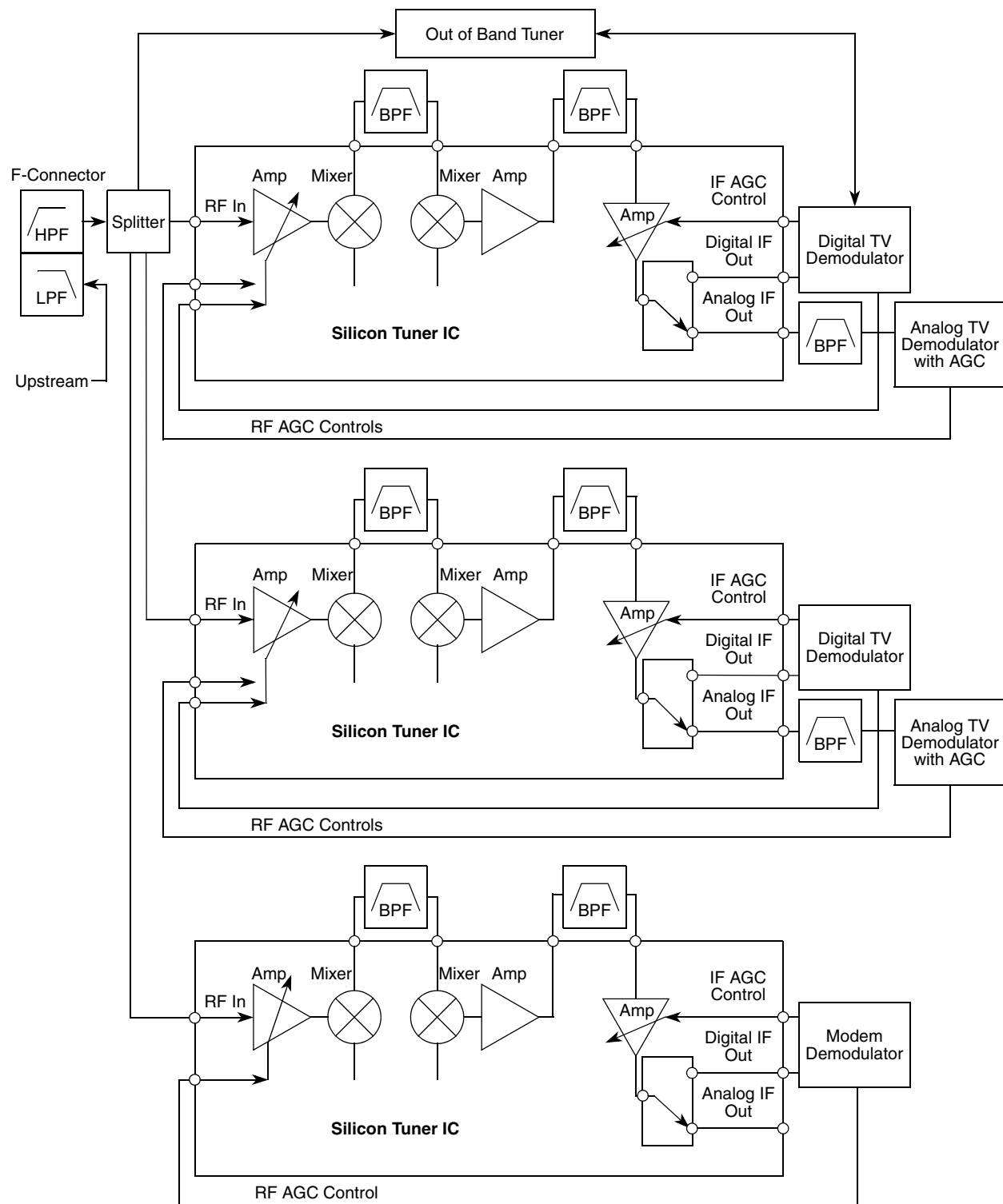


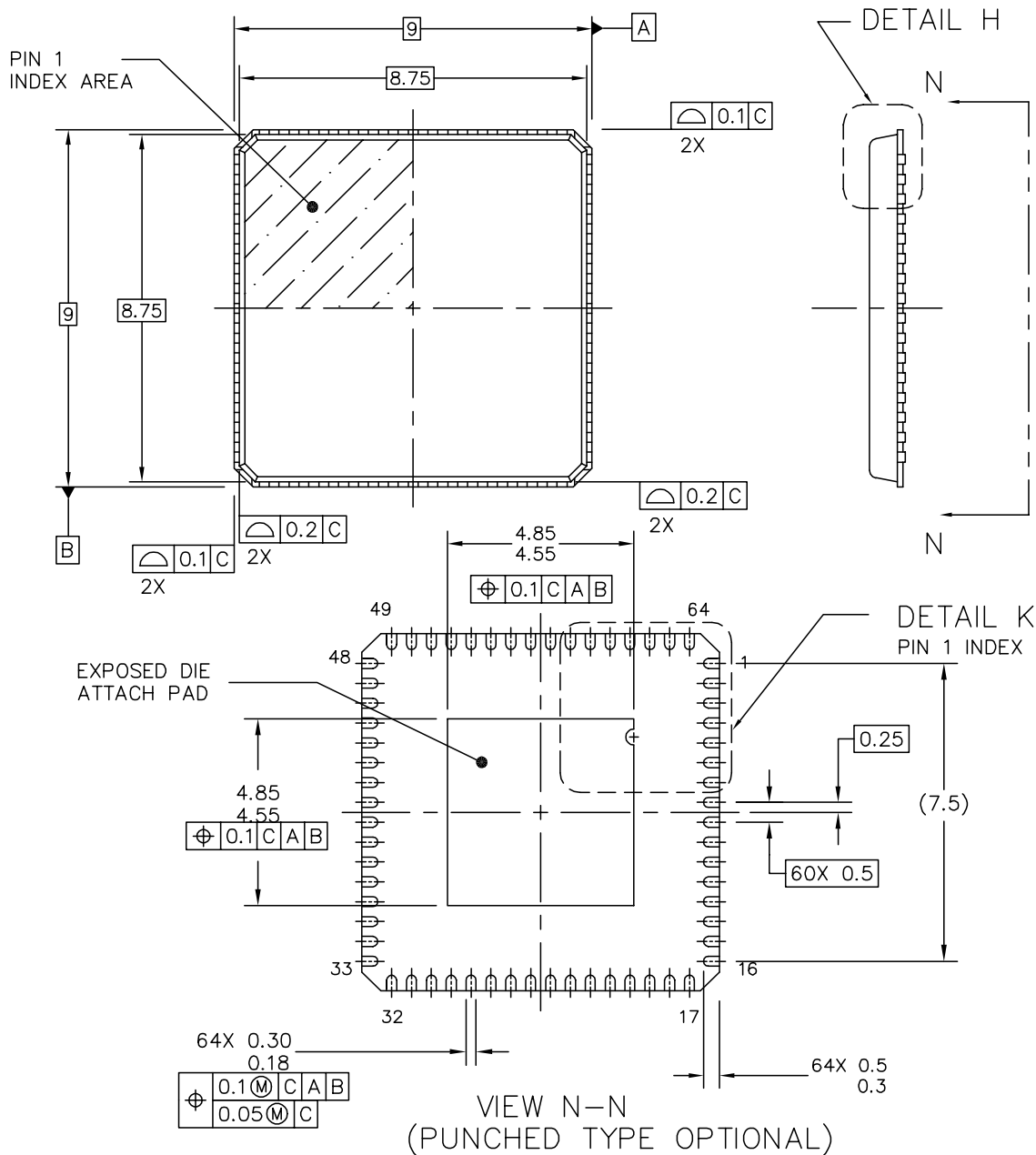
Figure 36. Settop Box or Media Gateway with Two Digital/Analog TV Tuners and Broadband Modem Tuner



## PACKAGE DIMENSIONS

This IC package is in a Pb-free 64 pin Quad Leadless Package (QFN) with a grounding pad on the bottom of the package. The QFN is similar to a QFP except the leads wrap

around the edge of the package rather than the gull wing style used on the QFP. The grounding pad is intended to be soldered to the PCB during normal reflow operation.

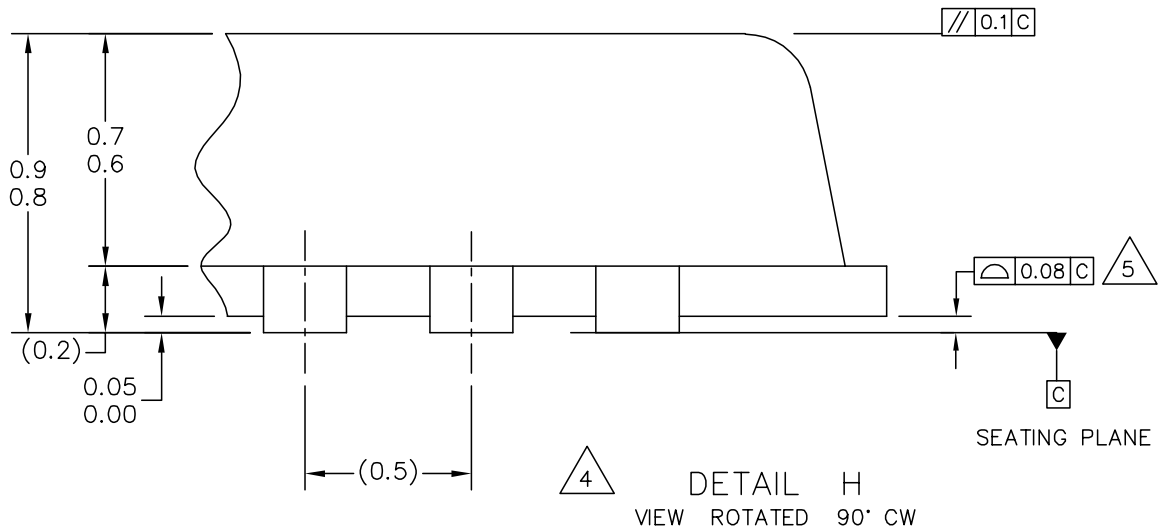
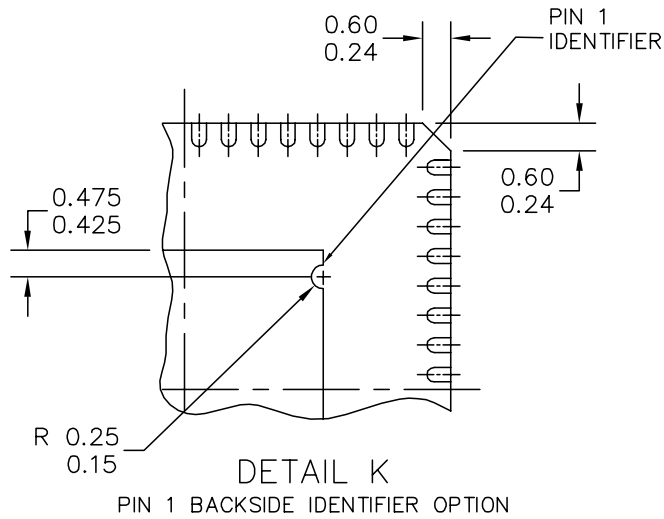


|                                                                                                       |                           |                            |
|-------------------------------------------------------------------------------------------------------|---------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                               | <b>MECHANICAL OUTLINE</b> | PRINT VERSION NOT TO SCALE |
| TITLE: THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>64 TERMINAL, 0.5 PITCH (9 X 9 X 1) | DOCUMENT NO: 98ARS10519D  | REV: 0                     |
|                                                                                                       | CASE NUMBER: 1606-01      | 29 SEP 2005                |
|                                                                                                       | STANDARD: NON-JEDEC       |                            |

PAGE 1 OF 3

MC44S803

## PACKAGE DIMENSIONS



|                                                         |                                                                                                       |  |                            |             |
|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------|--|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. | <b>MECHANICAL OUTLINE</b>                                                                             |  | PRINT VERSION NOT TO SCALE |             |
|                                                         | TITLE: THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>64 TERMINAL, 0.5 PITCH (9 X 9 X 1) |  | DOCUMENT NO: 98ARS10519D   | REV: 0      |
|                                                         |                                                                                                       |  | CASE NUMBER: 1606-01       | 29 SEP 2005 |
|                                                         | STANDARD: NON-JEDEC                                                                                   |  |                            |             |

PAGE 2 OF 3

**CASE 1606-01**  
**ISSUE 0**  
**64-LEAD QFN PACKAGE**

## PACKAGE DIMENSIONS

### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HP-VFQFP-N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
6. MINIMUM GAP BETWEEN METAL SHOULD BE 0.2 mm.

|                                                                                                       |                           |                            |             |
|-------------------------------------------------------------------------------------------------------|---------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                               | <b>MECHANICAL OUTLINE</b> | PRINT VERSION NOT TO SCALE |             |
| TITLE: THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>64 TERMINAL, 0.5 PITCH (9 X 9 X 1) | DOCUMENT NO: 98ARS10519D  |                            | REV: 0      |
|                                                                                                       | CASE NUMBER: 1606-01      |                            | 29 SEP 2005 |
|                                                                                                       | STANDARD: NON-JEDEC       |                            |             |

PAGE 3 OF 3

**CASE 1606-01  
ISSUE 0  
64-LEAD QFN PACKAGE**

**MC44S803**

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.