MOTOROLA

MC54/74F85

4-BIT MAGNITUDE COMPARATOR

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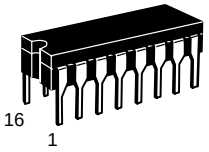
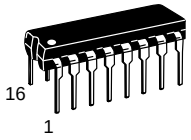
FAST™ SCHOTTKY TTL

The MC54/74F85 is a 4-Bit Magnitude Comparator which compares two 4-Bit words (A_0-A_3, B_0-B_3), A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes; the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($0_{A > B}$), "A less than B" ($0_{A < B}$), "A equal to B" ($0_{A = B}$). Three Expander Inputs, $I_{A > B}$, $I_{A < B}$, $I_{A = B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A < B} = I_{A > B} = L$, $I_{A = B} = H$. For serial (ripple) expansion the $0_{A > B}$, $0_{A < B}$ Outputs are connected respectively to the $I_{A > B}$ and $I_{A = B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to applications section of data sheet for high speed method of comparing large words.

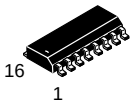
- High Impedance NPN Base Inputs for Reduced Loading (20 μA in HIGH and LOW States)
- Magnitude Comparison of any Binary Words
- Serial or Parallel Expansion Without Extra Gating
- ESD > 4000 Volts



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

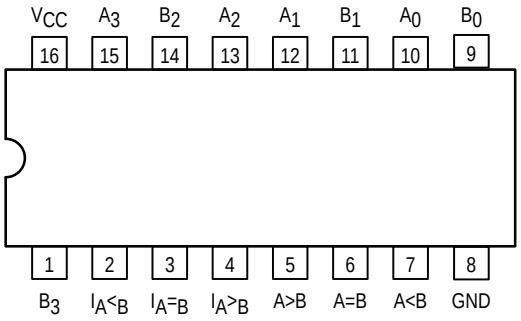


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

CONNECTION DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

FUNCTION TABLE

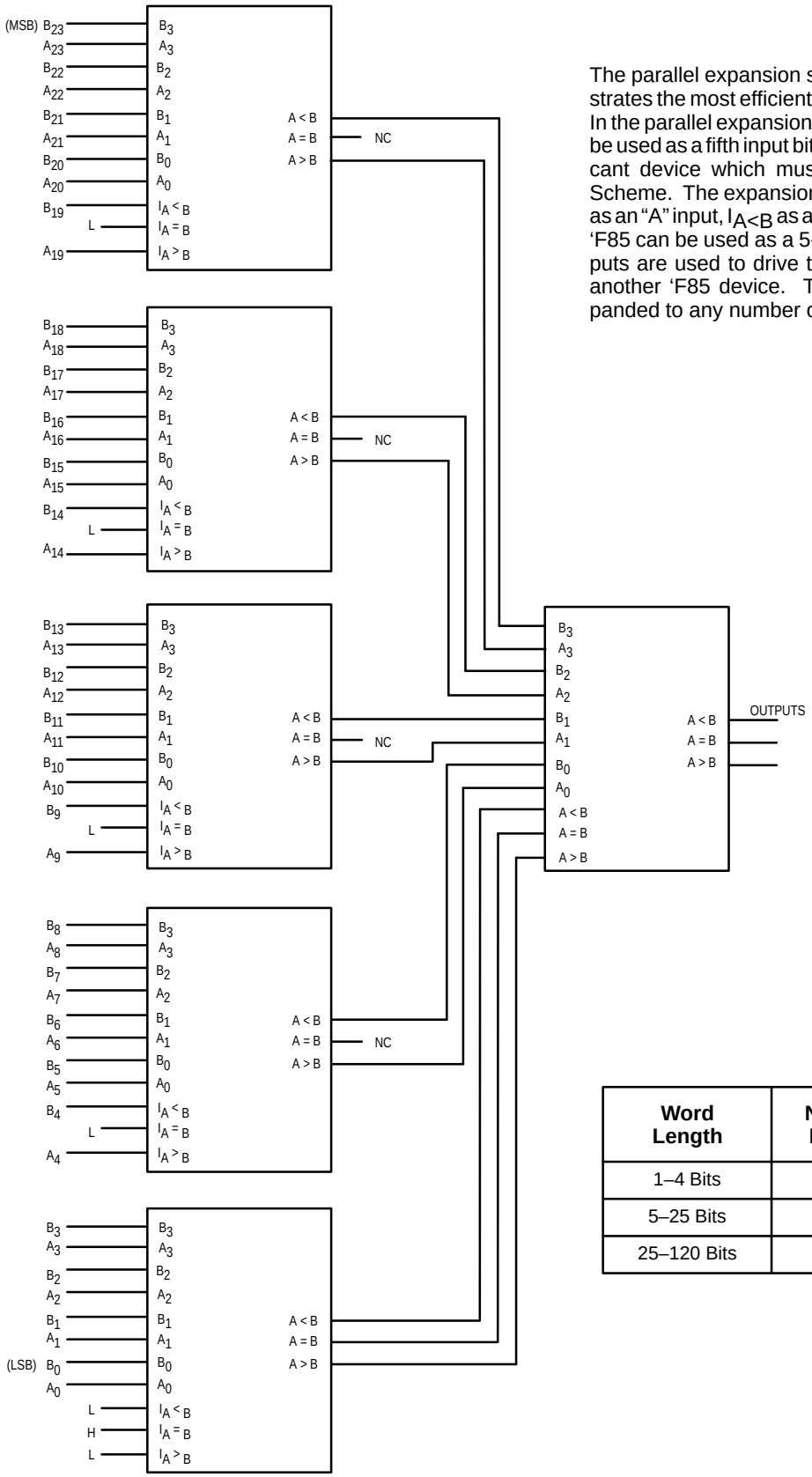
Comparing Inputs				Expansion Inputs			Outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OH} = –1.0 mA	V_{CC} = 4.50 V
		74	2.7					V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA, V_{CC} = MIN	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = 0 V, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				–20	µA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Total Supply Current HIGH V_{IN} = HIGH				50	mA	V_{CC} = MAX	
	LOW $A_n = B_n = I_{A-B}$ = GND: $I_{A>B} = I_{A<B}$ = 4.5 V				54			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.



The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the Serial Scheme. The expansion inputs are used by labelling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ low. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

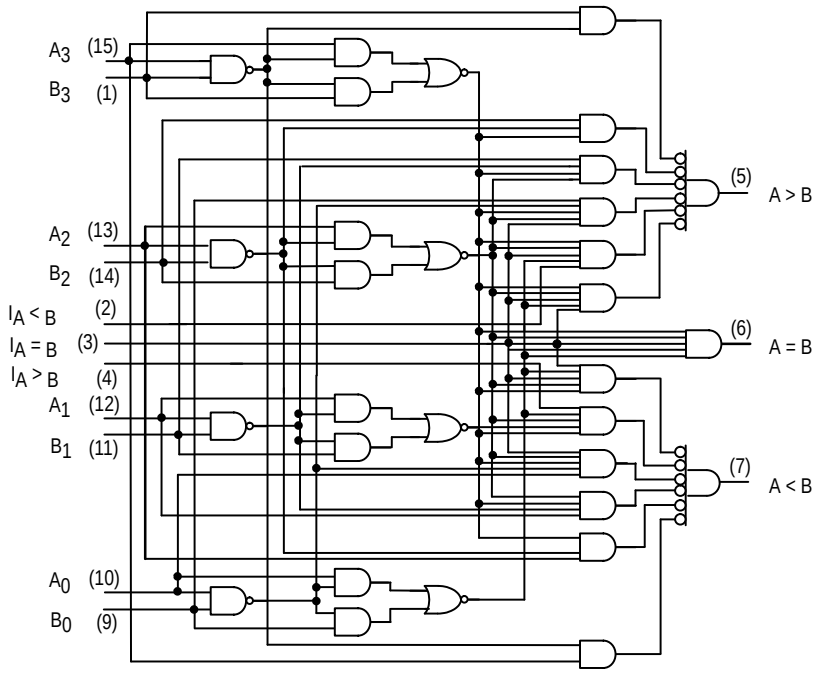
Word Length	Number of Packages	Typical Speeds 74F
1–4 Bits	1	12 ns
5–25 Bits	2–6	22 ns
25–120 Bits	8–31	34 ns

Figure 1. Comparison of Two 24-Bit Words

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF		54F T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		74F T_A = 0°C to + 70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		Unit
		Min	Max	Min	Max	Min	Max	
t_{PLH}	A or B Input to	6.0	11	5.5	14	5.5	13	ns
t_{PHL}	A < B, A > B Output	6.0	14	5.5	16.5	5.5	15.5	
t_{PLH}	A or B Input to	5.5	11.5	5.0	15	5.0	14	ns
t_{PHL}	A = B Output	7.0	14	6.5	15.5	6.5	14.5	
t_{PLH}	$I_{A<B}$ and $I_{A=B}$ Input	3.0	7.5	2.5	10	2.5	9.0	ns
t_{PHL}	to A>B Output	3.0	9.0	2.5	11	2.5	10	
t_{PLH}	$I_{A=B}$ Input to	2.5	7.0	2.0	10	2.0	9.0	ns
t_{PHL}	A = B Output	3.5	10	2.5	13	2.5	12	
t_{PLH}	$I_{A>B}$ and $I_{A=B}$ Input	3.0	8.0	3.0	10.5	3.0	9.5	ns
t_{PHL}	to A<B Output	3.0	9.0	2.0	10.5	2.0	9.5	

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B, and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15 ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram