MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC245A

Advance Information

Octal 3-State Noninverting Bus Transceiver

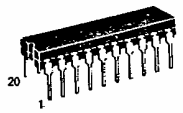
High-Performance Silicon-Gate CMOS

The MC54/74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

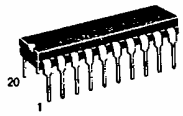
The HC245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC245A performs functions similar to those of the HC640A and the HC643A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-02

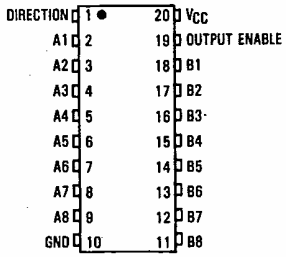
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

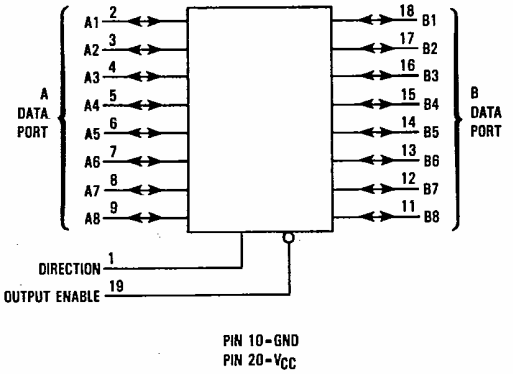
MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

T_A = −55° to 125°C for all packages.

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 10 = GND
PIN 20 = V_{CC}

FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin 1 or 19	±20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC}=2.0 V	0	1000	ns
	(Figure 1)	V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\| \leq 20\ \mu A$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\| \leq 20\ \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \leq 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \leq 6.0$ mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \leq 7.8$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \leq 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \leq 6.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \leq 7.8$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{in}=V_{IL} or V_{IH} V_{out}=V_{CC} or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance (Pin 1 or Pin 19)	—	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	—	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V_{CC} = 5.0 V 40	pF

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

SWITCHING WAVEFORMS

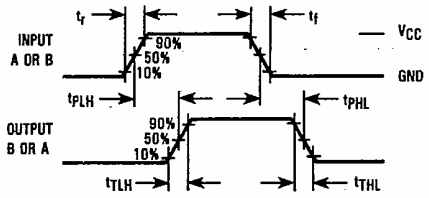


Figure 1

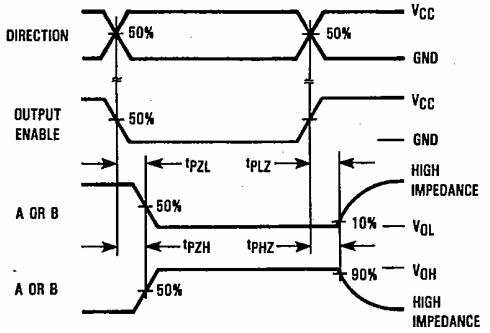
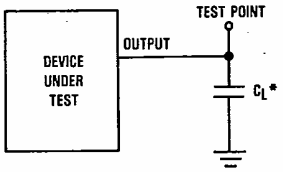
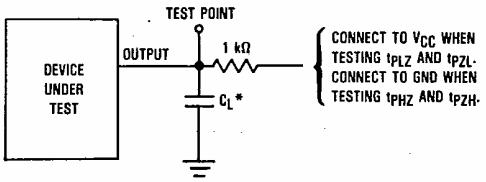


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM