3W Stereo Audio Power Amplifier with Advanced DC Volume Control

General Description

The MC6019 is a stereo audio power amplifier that drives 3 W/channel of continuous RMS power into a 3-W load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME Terminal, Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

Features

- Advanced DC Volume Control With 2-dB Steps from -40 dB to 20 dB
  Fade Mode
  Maximum Volume Setting for SE Mode
  Adjustable SE Volume Control Referenced to BTL Volume Control
- 3 W Into 3-Ω Speakers
- Stereo Input MUX
- Differential Inputs

Applications

- PDVD
- Notebook PC
- LCD Monitors
- Pocket PC

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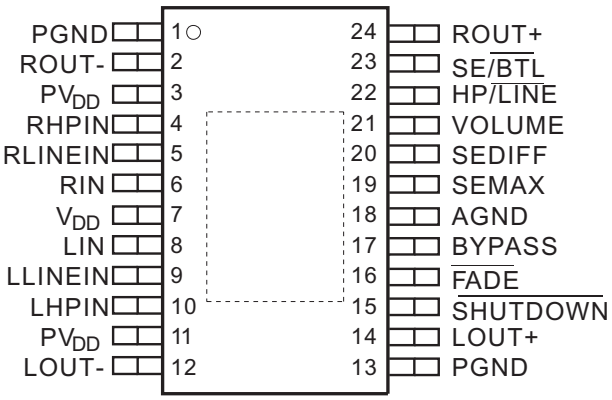
Pin Configuration



(TOP VIEW)

Pin Function

TERMINAL NAME	NO.	I/O	DESCRIPTION
PGND	1, 13	-	Power ground
LOUT-	12	O	Left channel negative audio output
PV_{DD}	3, 11	-	Supply voltage terminal for power stage
LHPIN	10	I	Left channel headphone input, selected when HP/LINE is held high
LLINEIN	9	I	Left channel line input, selected when HP/LINE is held low
LIN	8	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
V_{DD}	7	-	Supply voltage terminall
RIN	6	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
RLINEIN	5	I	Right channel line input, selected when HP/LINE is held low
RHPIN	4	I	Right channel headphone input, selected when HP/LINE is held high
ROUT-	2	O	Right channel negative audio output
ROUT+	24	O	Right channel positive audio output
$\overline{\text{SHUTDOWN}}$	15	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
$\overline{\text{FADE}}$	16	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal.
BYPASS	17	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
AGND	18	-	Analog power supply ground
SEMAX	19	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to V_{DD}.
SEDIFF	20	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to V_{DD}.
VOLUME	21	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}.
HP/ $\overline{\text{LINE}}$	22	I	Input MUX Control. When logic high,RHPIN and LHPIN input are selected, When logic low, RLINEIN and LLINEIN inputs are selected.
SE/ $\overline{\text{BTL}}$	23	I	Output MUX Control. When this termind is high,SE outputs are selected, When this termind is low, BTL outputs are selected.
LOUT+	14	O	Left channel positive audio output

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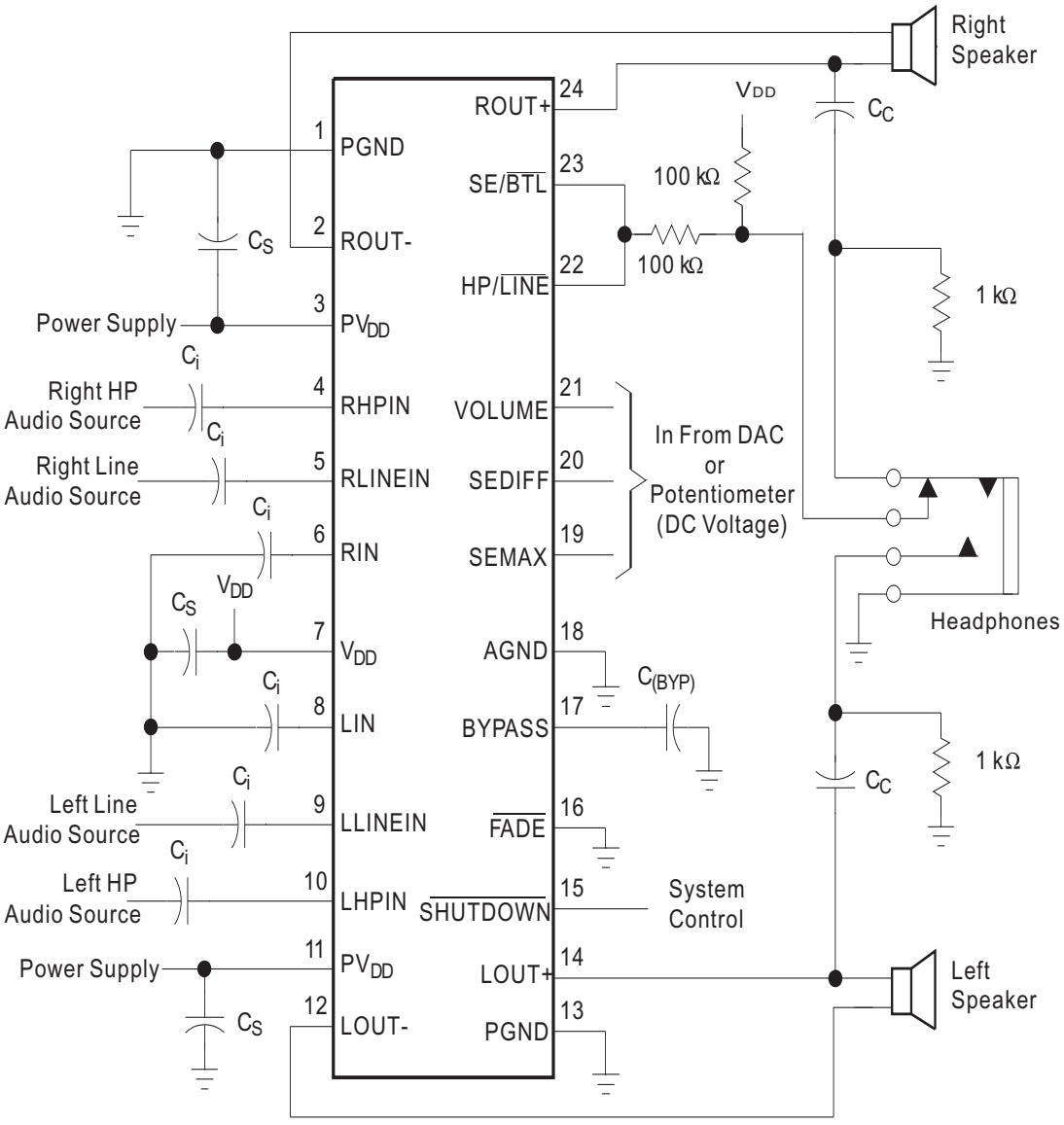
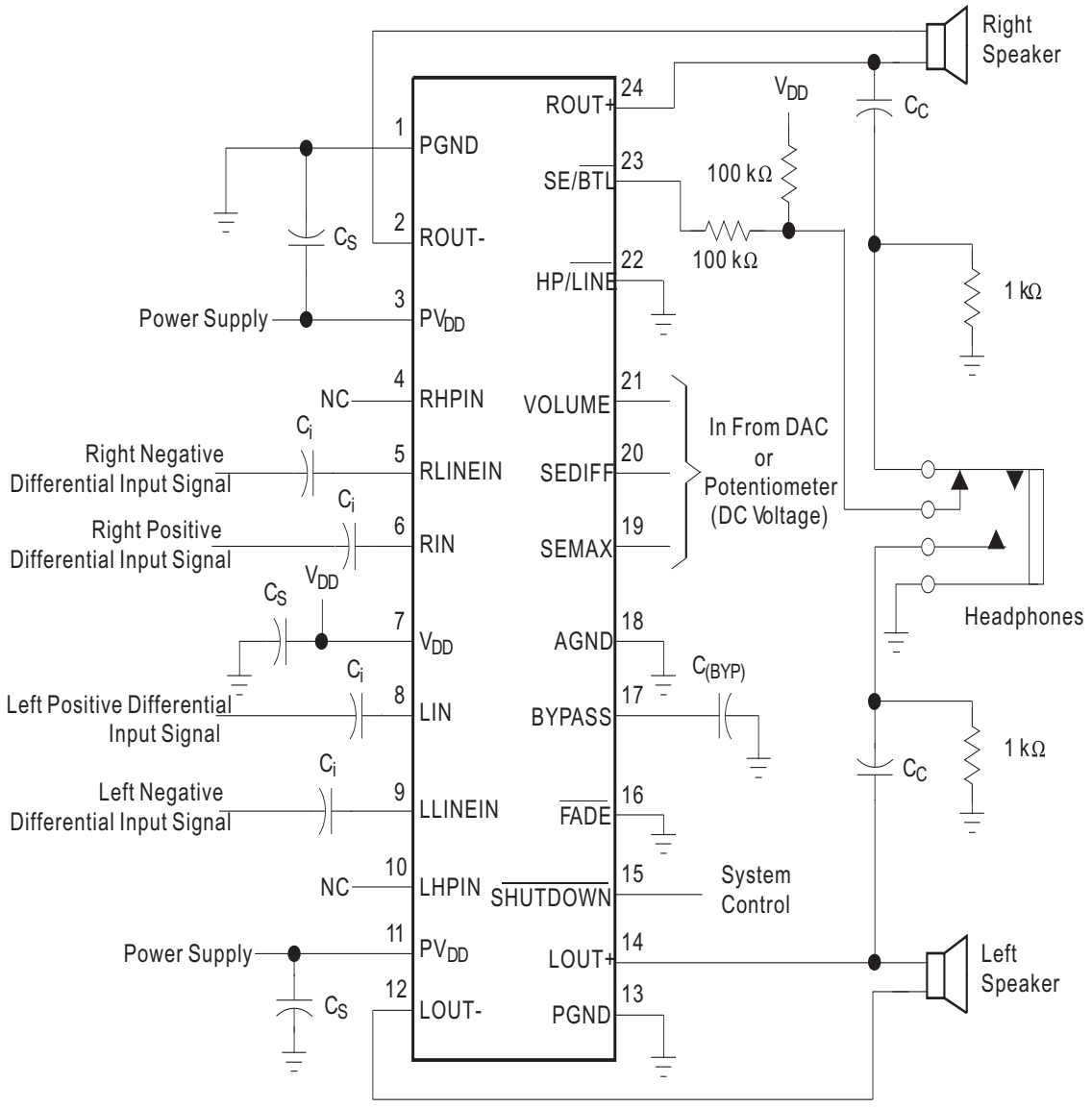
Typical Application 1



Application Circuit Using Single-Ended Inputs and Input MUX

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

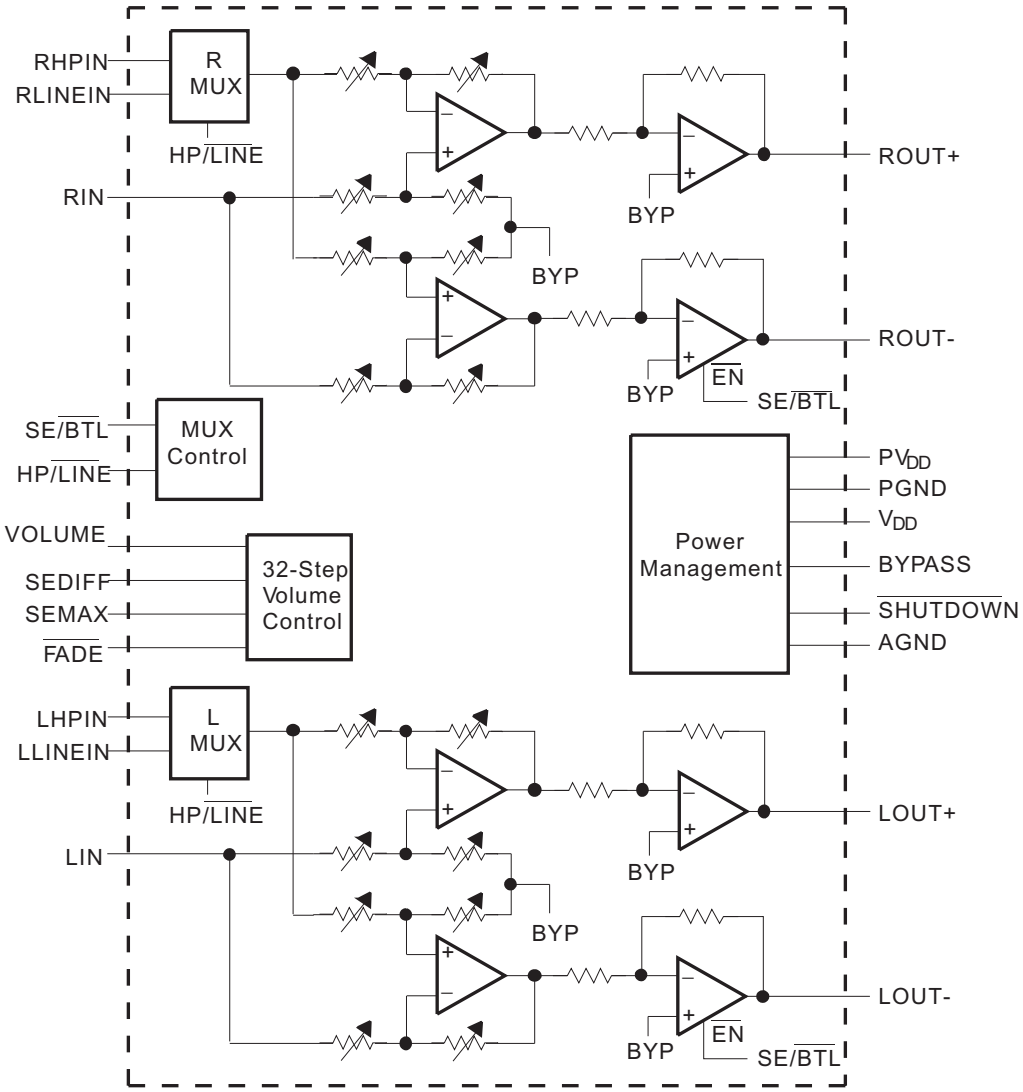
Typical Application 2



Application Circuit Using Differential Inputs

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Block Diagram



NOTE: All resistor wipers are adjusted with 32step volume control.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Absolute Maximum Ratings

	Item	UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}	-0.3V to 6 V
V_I	Input voltage	-0.3V to V_{DD}+0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	-40°C to 85°C
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150 °C
	Lead temperature 1,6mm (1/16inch) from case for 10seconds	260°C

Recommended Operating Conditiions

Item			MIN	MAX	UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}		4.0	5.5	V
V_{IH}	High-level input voltage	SE/$\overline{BTL}$,HP/$\overline{LINE}$,$\overline{FADE}$	0.8× V_{DD}		V
		$\overline{SHUTDOWN}$	2		V
V_{IL}	Low-level input voltage	SE/$\overline{BTL}$,HP/$\overline{LINE}$,$\overline{FADE}$		0.6× V_{DD}	V
		$\overline{SHUTDOWN}$		0.8	V
T_A	Operating free-air temperature		-40	85	°C

Thermal Information [2]

Symbol	Description	Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient	43	°C/W
θ_{JC}	Thermal Resistance-Junction to Case	10	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
MC6019	TSSOP28	MC6019 XXXX	13''	12mm	2500 units

ESD Susceptibility

ESD Susceptibility-HBM ---------- 2kV
ESD Susceptibility-MM ---------- 200V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.
2. The ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan,and the PCB is a 2-layer,5-inch square area with 2oz copper thickness.

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Electrical Characteristics

T_A = 25°C, V_{DD} = PV_{DD} = 5.5 V (unless otherwise noted)

PARAMETER		TESTCONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage(measured differentially)	V_{DD} = 5.5V, Gain= 0 dB, SE/$\overline{BTL}$ = 0 V			30	mV
		V_{DD} = 5.5V, Gain= 20 dB, SE/$\overline{BTL}$ = 0 V			50	mV
PSRR	Powersupply rejection ratio	V_{DD} = PV_{DD} = 4.0V to 5.5V	-42	-70		dB
$\lvert I_{IH} \rvert$	High-level input current(SE/$\overline{BTL}$,$\overline{FADE}$,HP/$\overline{LINE}$ $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5V, V_I = V_{DD} = PV_{DD}			1	A
$\lvert I_{IL} \rvert$	Low-level input current (SE/$\overline{BTL}$,$\overline{FADE}$,HP/$\overline{LINE}$ $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5V, V_I = 0 V			1	A
I_{DD}	Supply current, no load	V_{DD} = PV_{DD} = 5.5V, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V	6.0	7.5	9.0	mA
		V_{DD} = PV_{DD} = 5.5V, SE/$\overline{BTL}$ = 5 V, $\overline{SHUTDOWN}$ = 2 V	3.0	5	6	
I_{DD}	Supply current,max power into a 3-Ω load	V_{DD} = 5 V = PV_{DD}, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V, R_L = 3Ω, P_O = 2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0.0V		1	20	A

Operating Characteristics

T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 3 W, Gain = 6 dB (unless otherwise noted)

PARAMETER		TESTCONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD= 1%, f = 1 kHz			2		W
		THD= 10%, f = 1 kHz, V_{DD} = 5.5V			3		
THD+N	Total harmonic distortion+ noise	P_O = 1 W, R_L = 8 Ω , f = 20 Hz to 20 kHz			<0.4%		
V_{OH}	High-level output voltage	R_L = 8 Ω, Measured between output and V_{DD}				700	mV
V_{OL}	Low-level output voltage	R_L = 8 Ω, Measured between output and GND				400	mV
$V_{(Bypass)}$	Bypass voltage (Nominally V_{DD}/2)	Measured at pin17, No load, V_{DD} = 5.5V		2.65	2.75	2.85	V
B_{OM}	Maximum output power bandwidth	THD= 5%			>20		kHz
	Supply ripple rejection ratio	f = 1 kHz, Gain= 0 dB, $C_{(BYP)}$= 0.47 F	BTL		-63		dB
			SE		-57		dB
	Noise output voltage	f = 20 Hz to 20kHz, Gain= 0 dB, $C_{(BYP)}$= 0.47 F	BTL		36		V_{RMS}
Z_I	Input impedance (see Figure26)	VOLUME=5.0V			14		kΩ

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Table 1. DC Volume Control (BTL Mode, V_{DD} = 5 V)(1)

VOLUME(PIN21)		GAIN OF AMPLIFIER (Typ)
FROM(V)	TO (V)	
0.00	0.26	-85(2)
0.33	0.37	-40
0.44	0.48	-38
0.56	0.59	-36
0.67	0.70	-34
0.78	0.82	-32
0.89	0.93	-30
1.01	1.04	-28
1.12	1.16	-26
1.23	1.27	-24
1.35	1.38	-22
1.46	1.49	-20
1.57	1.60	-18
1.68	1.72	-16
1.79	1.83	-14
1.91	1.94	-12
2.02	2.06	-10
2.13	2.17	-8
2.25	2.28	-6(2)
2.36	2.39	-4
2.47	2.50	-2
2.58	2.61	0
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20(2)

(1) For other values of VDD, scale the voltage values in the table by a factor of VDD/5.
(2) Tested in production. Remaining gain steps are specified by design.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Table 2. DC Volume Control (SE Mode, V_{DD} = 5 V)(1)

SE_VOLUME= VOLUME- SEDIFFor SEMAX		GAIN OF AMPLIFIER (Typ)
FROM(V)	TO (V)	
0.00	0.26	-85(2)
0.33	0.37	-46
0.44	0.48	-44
0.56	0.59	-42
0.67	0.70	-40
0.78	0.82	-38
0.89	0.93	-36
1.01	1.04	-34
1.12	1.16	-32
1.23	1.27	-30
1.35	1.38	-28
1.46	1.49	-26
1.57	1.60	-24
1.68	1.72	-22
1.79	1.83	-20
1.91	1.94	-18
2.02	2.06	-16
2.13	2.17	-14
2.25	2.28	-12
2.36	2.39	-10
2.47	2.50	-8
2.58	2.61	-6(2)
2.70	2.73	-4
2.81	2.83	-2
2.92	2.95	0(2)
3.04	3.06	2
3.15	3.17	4
3.26	3.29	6(2)
3.38	3.40	8
3.49	3.51	10
3.60	3.63	12
3.71	5.00	14

(1) For other values of VDD, scale the voltage values in the table by a factor of VDD/5.
(2) Tested in production. Remaining gain steps are specified by design.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Typical Operating Characteristics

Total Harmonic Distortion + Noise (BTL) vs Frequency

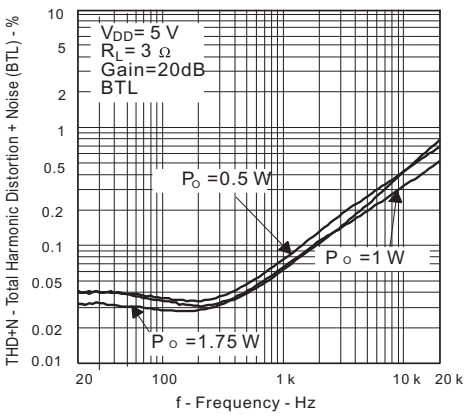


Figure 1

Total Harmonic Distortion + Noise (BTL) vs Frequency

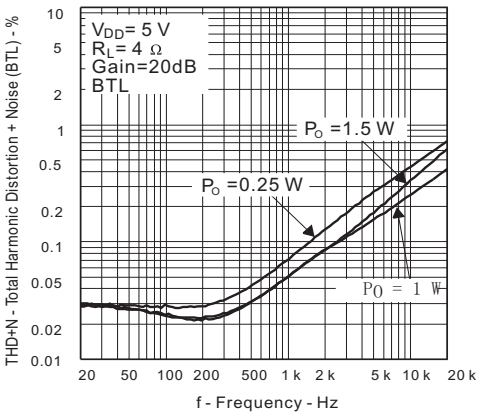


Figure 2.

Total Harmonic Distortion + Noise (BTL) vs Frequency

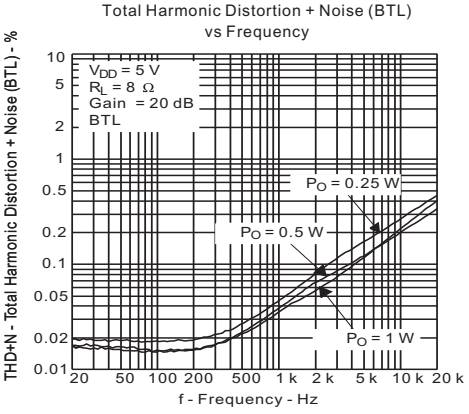


Figure3.

Total Harmonic Distortion + Noise (SE) vs Frequency

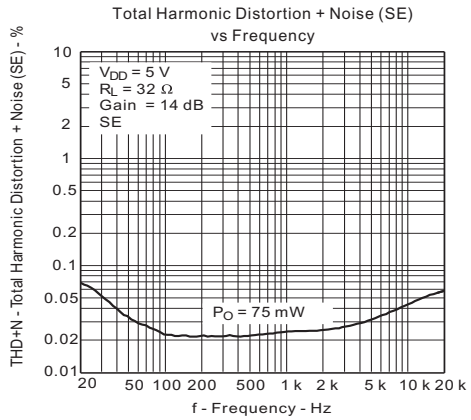


Figure4.

Total Harmonic Distortion + Noise (SE) vs Frequency

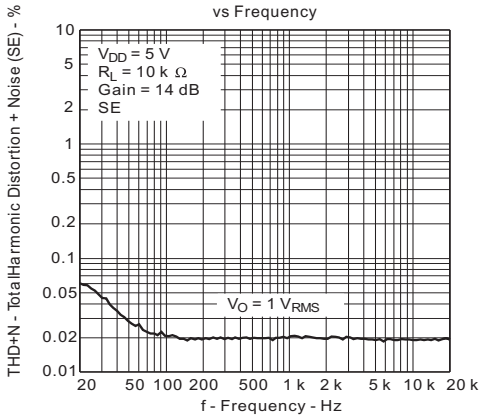


Figure5.

Total Harmonic Distortion + Noise (BTL) vs Frequency

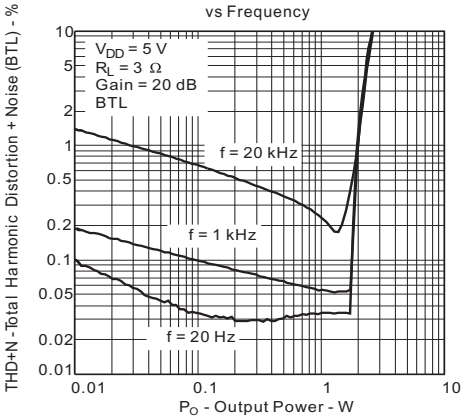


Figure6.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Typical Operating Characteristics (Continued)

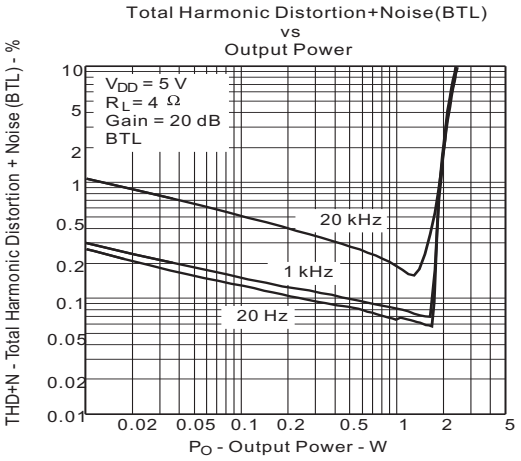


Figure7.

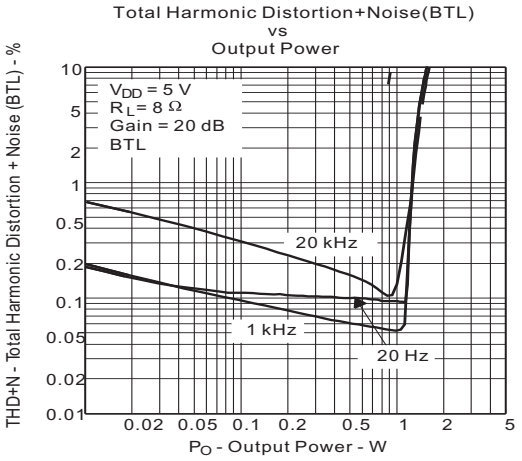


Figure8.

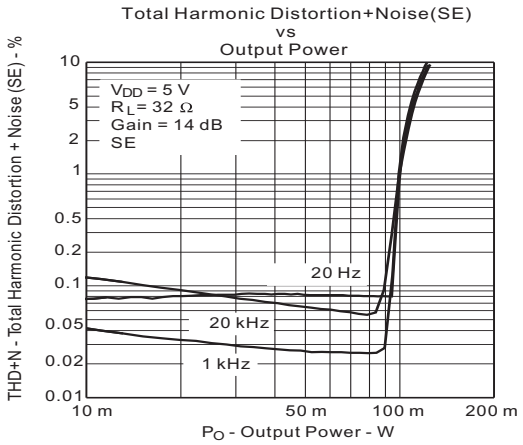


Figure9.

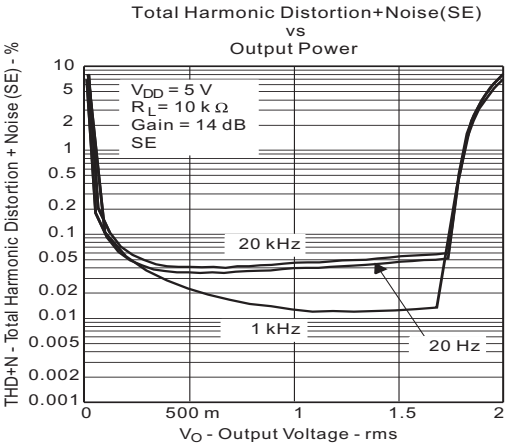


Figure10.

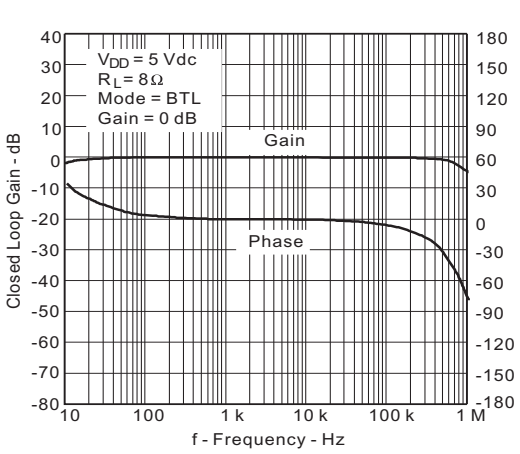


Figure11.

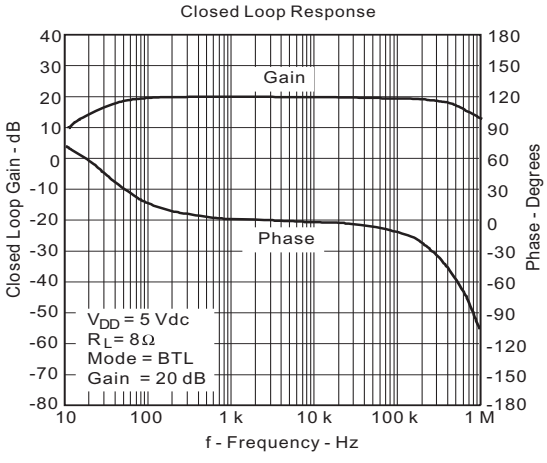


Figure12.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Typical Operating Characteristics (Continued)

Supply Current vs Free-air Temperature

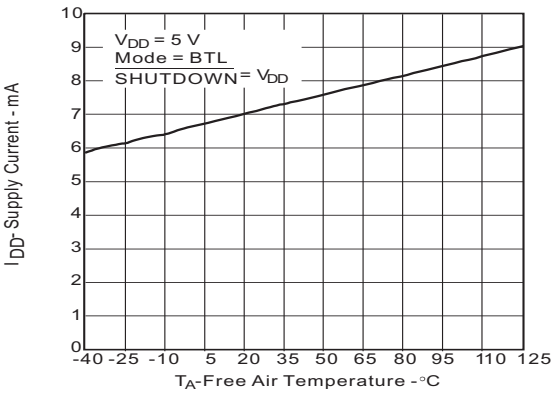


Figure13.

Supply Current vs Supply Voltage

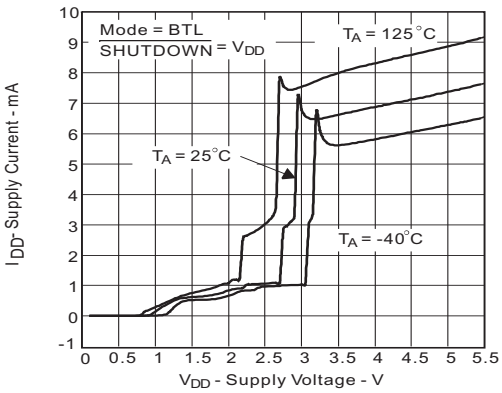


Figure14.

Supply Current vs Supply Voltage

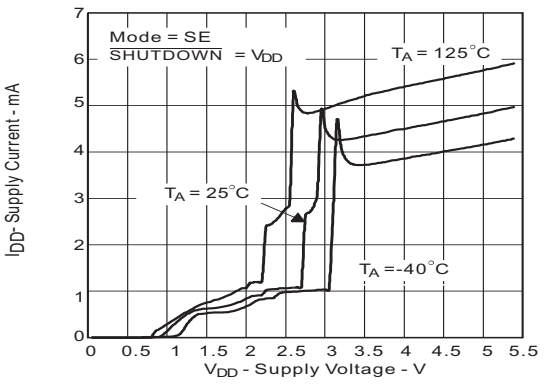


Figure15.

Supply Current vs Supply Voltage

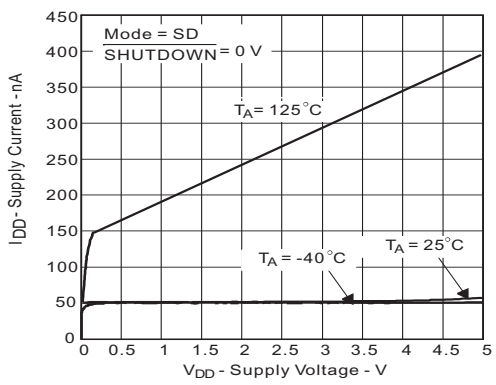


Figure16.

Power Dissipation(per channel) vs Output Power

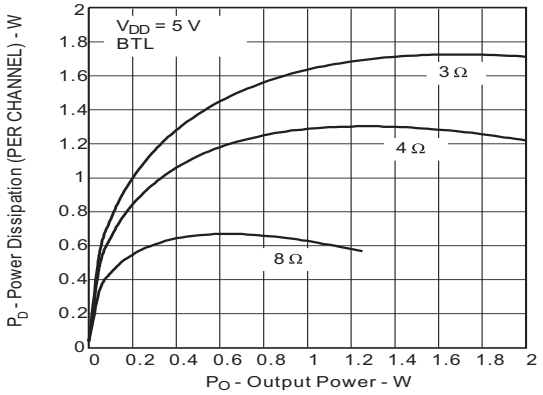


Figure 17.

Power Dissipation(per channel) vs Output Power

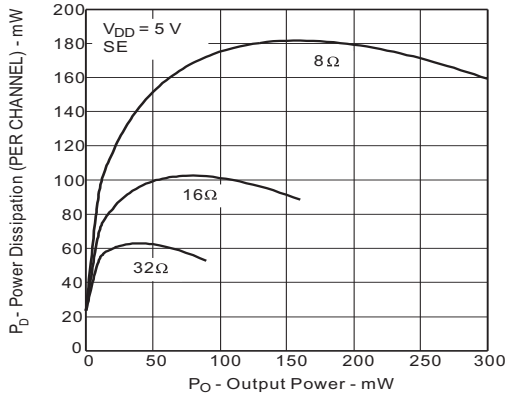


Figure18.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Typical Operating Characteristics (Continued)

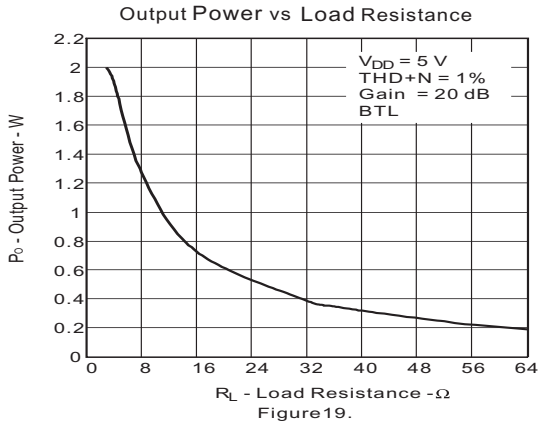


Figure19.

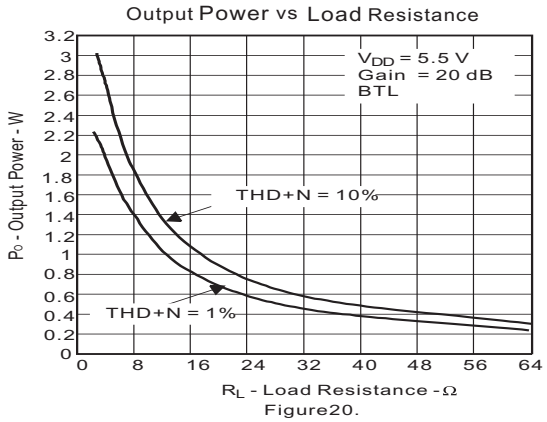


Figure20.

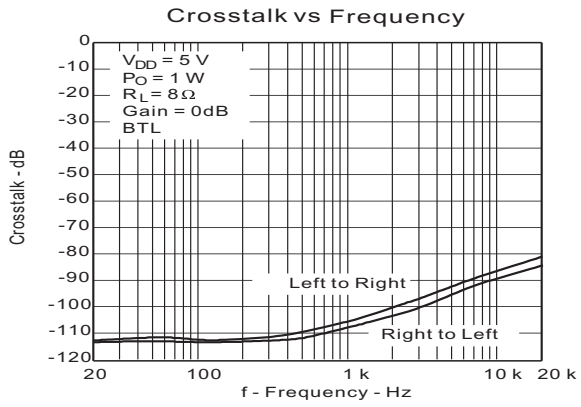


Figure21.

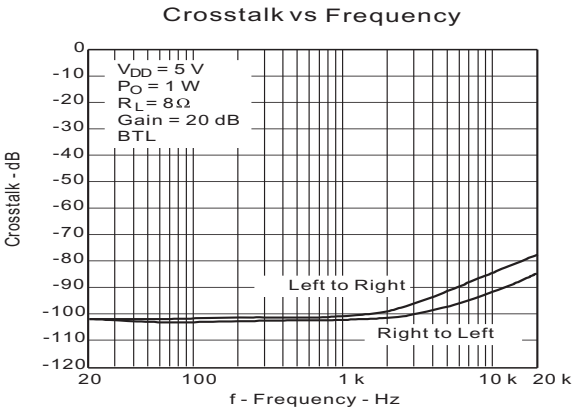


Figure22.

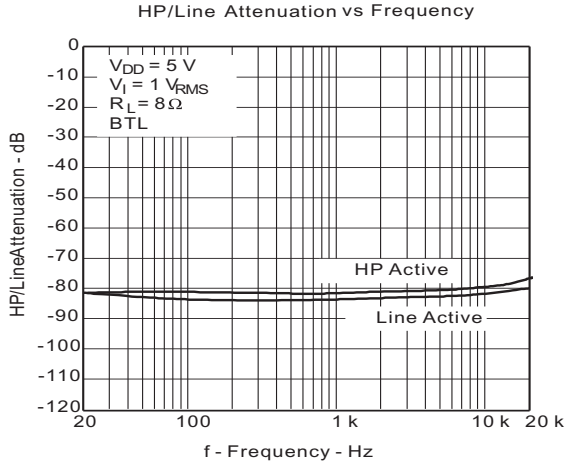


Figure23.

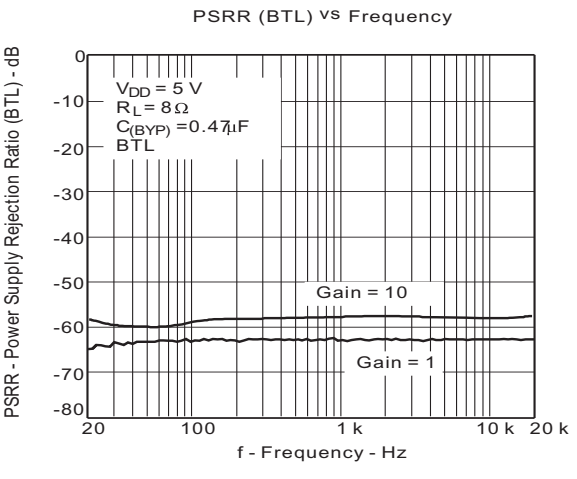


Figure24.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Typical Operating Characteristics (Continued)

PSRR(SE) vs Frequency

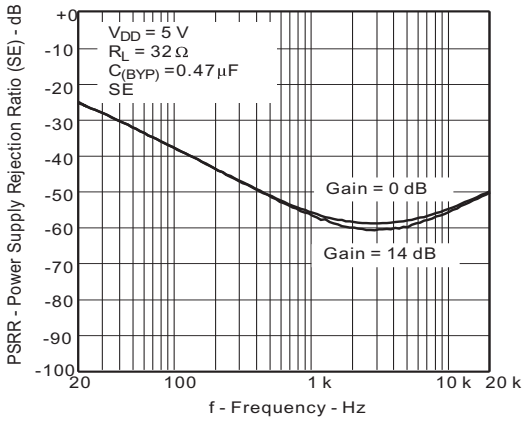


Figure25.

Input Impedance vs BTL Gain

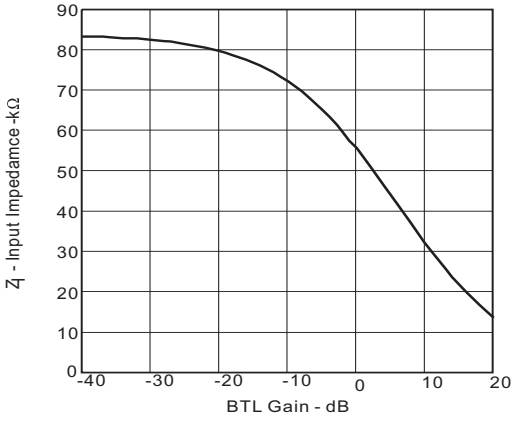


Figure26.

Output Noise Voltage vs Frequency

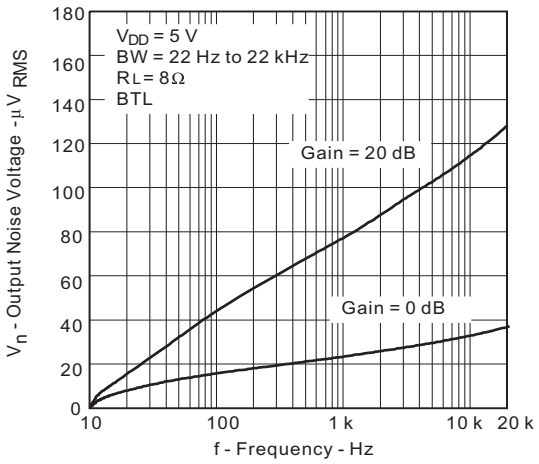


Figure27.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Application Information

SE/BTL Operation

The ability of the MC6019 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the MC6019, two separate amplifiers drive OUT+ and OUT-. The SE/BTL input controls the operation of the follower amplifier that drives LOUT- and ROUT-. When SE/BTL is held low, the amplifier is on and the MC6019 is in the BTL mode. When SE/BTL is held high, the OUT- amplifiers are in a high output impedance state, which configures the MC6019 as an SE driver from LOUT+ and ROUT+ I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/BTL input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 28. The trip level for the SE/BTL input can be found in the *recommended operating conditions* table.

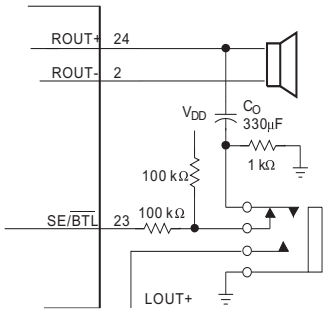


Figure 28. Resistor Divider Network Circuit

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kW/1-kW divider pulls the SE/BTL input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/BTL input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (Co) into the headphone jack.

HP/$\overline{\text{LINE}}$ Operation

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure 28. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/BTL pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.
When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 3 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

$\overline{\text{FADE}}$ Operation

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.
When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (VIL) or logic high (VIH) can be found in the *recommended operating conditions* table.
When a logic low is applied to the $\overline{\text{FADE}}$ pin and a logic low is then applied on the $\overline{\text{SHUTDOWN}}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown.For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from thehighest gain, or 31 steps, and multiplying by the time per step, or 34 ms.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of $V_{DD}/2$ to ground. This time is dependent on the value of the bypass capacitor. For a 0.47-µF capacitor that is used in the application diagram in *Typical application1*, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-µF capacitor, or 1 second. Figure 28 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode.The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$, the gain increases in 2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequence. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 29 below is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the FADE pin does not change the power-up sequence. Upon a power-up condition, the MC6019 begins in the lowest gain settingand steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

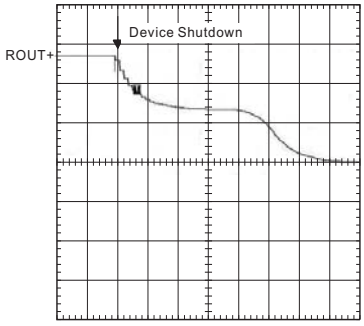


Figure 29. Shutdown Sequence in the Fade-on Mode

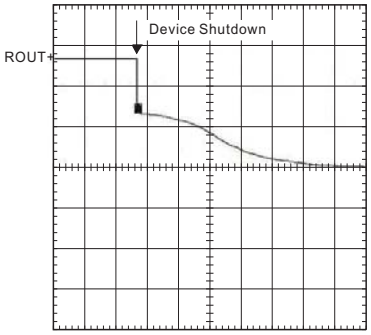


Figure 30. Shutdown Sequence in the Fade-off Mode

Shutdown Modes

The MC6019 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal shouldbe held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs tomute and the amplifier to enter a low-current state, I_{DD} = 20 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 3. HP/LINE, SE/BTL, and Shutdown Functions

INPUTS(1)			AMPLIFIER STATE	
$\overline{\text{HP/LINE}}$	$\overline{\text{SE/BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Inputs should never be left unconnected.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Volume, SEDIFF, AND SEMAX Operation

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceedV_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD} = 5 V. For a different V_{DD}, the values in the table scale linearly. If V_{DD} = 4 V, multiply all the voltages in the table by 4 V/5 V, or 0.8.

The MC6019 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF= 0 V, the difference between the BTL gain and the SE gain is 6 dB. Refer to the section labeled bridged-tied load versus single-ended load for an explanation on why the gain in BTL mode is 2x that of single-ended mode,or 6dB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20 dB, the gain in the headphone channel is fixed at 14 dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 31. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD} = 5 V. The values must be scaled for other values of V_{DD}.

Table 1 and Table 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction.

The trip point, where the gain actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 32. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

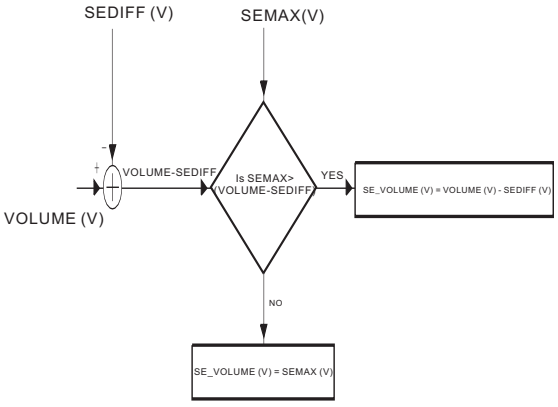


Figure 31. Block Diagram of SE Volume Control

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

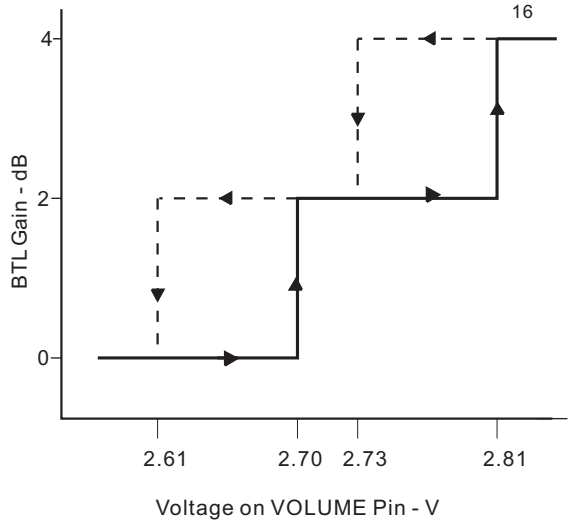


Figure 32. DC Volume Control Operation

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency also changes by over six times.

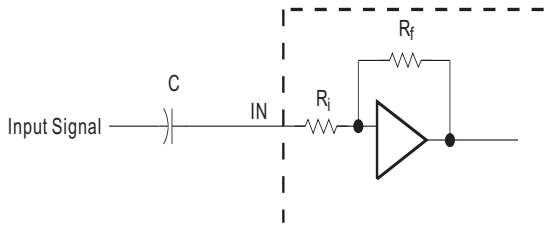


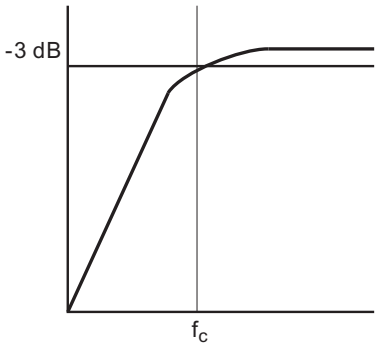
Figure 33. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 26.
The -3-dB frequency can be calculated using Equation 1.

$$f_{-3dB} = \frac{1}{2\pi C R_i} \qquad (1)$$

INPUT CAPACITOR, Ci

In the typical application an input capacitor (Ci) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, Ci and the input impedance of the amplifier (Ri) form a high-pass filter with the corner frequency determined in Equation 2.



$$C_i = \frac{1}{2\pi R_i C_i} \qquad (2)$$

The value of Ci is important to consider as it directly affects the bass (low frequency) performance of the circuit.Consider the example where Ri is 70 kW and the specification calls for a flat-bass response down to 40 Hz.Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi R_i f_c} \qquad (3)$$

In this example, Ci is 56.8 nF, so one would likely choose a value in the range of 56 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Power Supply Decoupling, C(S)

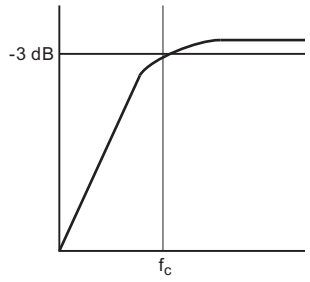
The MC6019 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

Midrail Bypass Capacitor, C(BYP)

The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.
Bypass capacitor ($C_{(BYP)}$) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for Ci. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

Output Coupling Capacitor, C(C)

In the typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.



$$f_{c(high)} = \frac{1}{2\pi R_i C_i} \qquad (4)$$

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads vary from 3Ω ,4 Ω, 8 Ω, 32Ω , 10 kΩ, and 47 kΩ . Table 4 summarizes the frequency response characteristics of each configuration.

R_L	$C_{(C)}$	LOWEST FREQUENCY
3 Ω	330 F	161Hz
4 Ω	330 F	120Hz
8 Ω	330 F	60Hz
32 Ω	330 F	15Hz
10,000 Ω	330 F	0.05Hz
47,000 Ω	330 F	0.01Hz

Table 4. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

As Table 4 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate,headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Using LOW-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal)capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of thisresistance, the more the real capacitor behaves like an ideal capacitor.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Bridged-tied Load vs Single-ended LOAD

Figure 34 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The MC6019 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 X´ $V_{O(PP)}$ into the power equation,where voltage is squared, yields 4´ the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(rms)}^2}{R_L} \qquad (5)$$

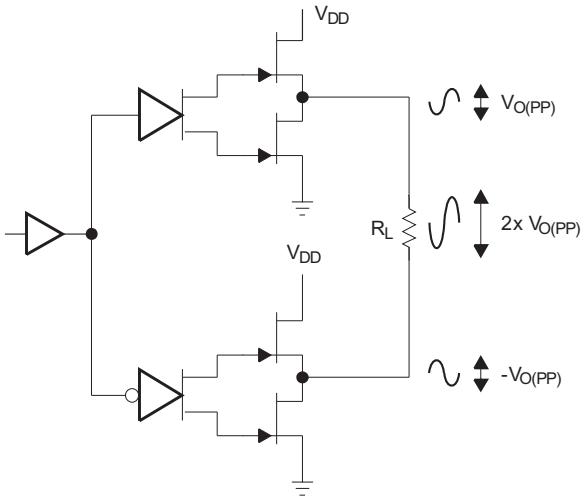


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-W speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to Increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offsetvoltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

$$F_{(c)} = \frac{1}{2\pi R_L C_C} \qquad (6)$$

For example, a 68-µF capacitor with an 8Ω - speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

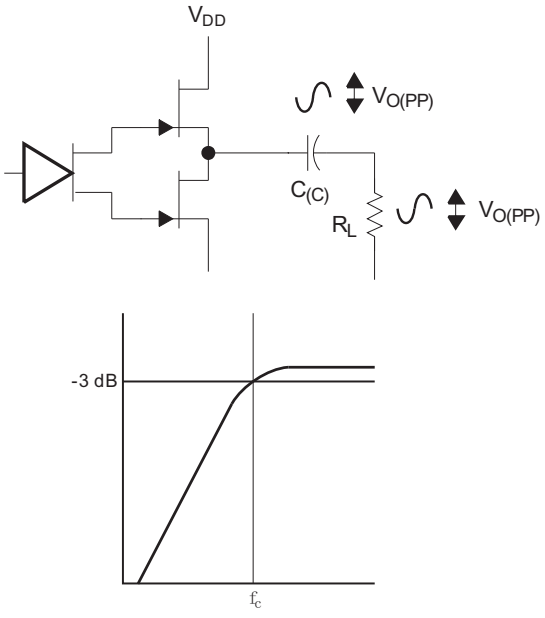


Figure 35. Single-Ended Configuration and Frequency Response

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4´ the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 35), the load is driven from the primary amplifier output for each channel (OUT+).The amplifier switches single-ended operation when the SE/BTL terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier's gain by 6 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output.The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.
An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 36).

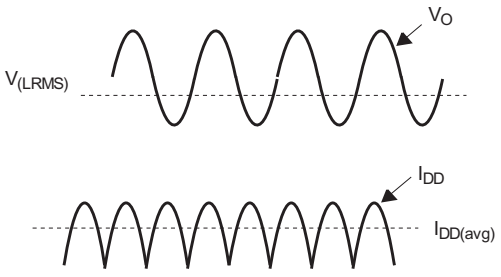


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different.Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform.The following equations are the basis for calculating amplifier efficiency.

Efficiency of a BTL amplifier $= \frac{P_L}{P_{SUP}}$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} + \frac{V_P}{\sqrt{2}},$$

Therefore,

$$P_L = \frac{V_P^2}{2R_L} \text{ and } P_{SUP} = V_{DD}\, I_{DD}avg$$

$$\text{and } I_{DD}avg = \frac{1}{\Pi}\int_0^{\Pi} \frac{V_P}{R_L} \sin(t)\, dt$$

$$= \frac{1}{\Pi} x \frac{V_P}{R_L} [\cos(t)]_0^{\Pi} = \frac{2V_P}{\Pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\Pi\, R_L} \qquad (7)$$

substituting PL and PSUP into Equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\, R_L}}{\frac{2\, V_{DD} V_P}{\Pi\, R_L}} = \frac{\Pi V_P}{4 V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\Pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}}$$

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

PL = Power delivered to load
PSUP = Power drawn from power supply
VLRMS = RMS voltage on BTL load
RL = Load resistance

V_P = Peak voltage on BTL load
I_{DDavg} = Average current drawn from the power supply
V_{DD} = Power supply voltage
h_{BTL} = Efficiency of a BTL amplifier (8)

Table 5 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 5. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47 (1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

Crest Factor and Thermal Considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the MC6019 data sheet, one can see that when the MC6019 is operating from a 5-V supply into a 3-Ω speaker, that 4-W peaks are available.Use equation 9 to convert watts to dB.

$$PdB=10\ \mathrm{Log}\ \frac{P_W}{P_{ref}}=10\mathrm{Log}\ \frac{4W}{1W}=6dB \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

· 6 dB - 15 dB = -9 dB (15-dB crest factor)
· 6 dB - 12 dB = -6 dB (12-dB crest factor)
· 6 dB - 9 dB = -3 dB (9-dB crest factor)
· 6 dB - 6 dB = 0 dB (6-dB crest factor)
· 6 dB - 3 dB = 3 dB (3-dB crest factor)

To convert dB back into watts use equation 10.

$$Pw=10^{PdB/10}\ X\ P_{ref}$$

= 63 mW (18-db crest factor)
= 125 mW (15-db crest factor)
= 250 mW (12-db crest factor)
= 500 mW (9-db crest factor)
= 1000 mW (6-db crest factor)
= 2000 mW (3-db crest factor) (10)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for theamplifier system. Comparing the worst case, which is 2 W of continuous power output with a 3-dB crest factor,against 12-dB and 15-dB applications significantly affects maximum ambient temperature ratings for the system.Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the MC6019 andmaximum ambient temperatures is shown in Table 6.

3W Stereo Audio Power Amplifier with Advanced DC Volume Control

Table 6. MC6019 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2W(3dB)	1.7	-3 C
4	1W(6dB)	1.6	6 C
4	500mW(9dB)	1.4	24 C
4	250mW(12dB)	1.1	51 C
4	125mW(15dB)	0.8	78 C
4	63mW(18dB)	0.6	96 C

Table 7. MC6019 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250mW(3-dB crest factor)	0.55	100 C
2.5	1000mW(4-dB crest factor)	0.62	94 C
2.5	500mW(7-dB crest factor)	0.59	97 C
2.5	250mW(10-dB crest factor)	0.53	102 C

The maximum dissipated power (PD(max)) is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating PD(max) may be used for an 8-W application.

$$Pd(max) = \frac{2V^2_{DD}}{\Pi^2 R_L} \quad (11)$$

However, in the case of a 3-Ω load, the PD(max) occurs at a point well above the normal operating power level.The amplifier may therefore be operated at a higher ambient temperature than required by the PD(max) formula for a 3-Ω load.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. Use equation 12 to convert this to Q_{JA}.

$$Q_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45℃/W \quad (12)$$

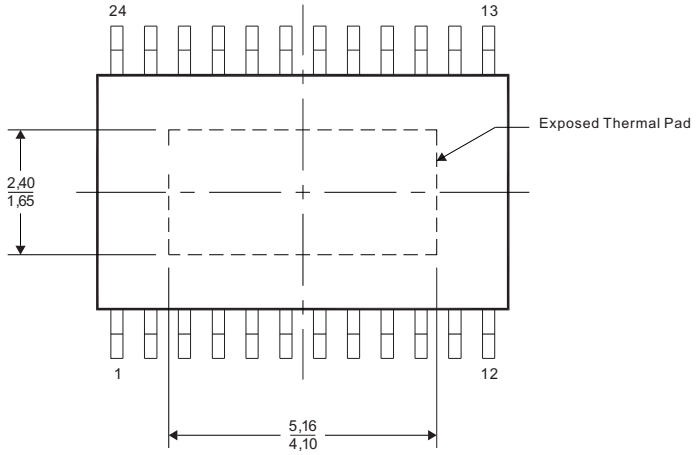
To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Given Q_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13. The maximum recommended junction temperature for the MC6019 is 150°C.The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A Max = T_J Max - Q_{JA} P_D \quad (13)$$
$$= 150 - 45(0.6X2) = 96°C \text{ (15-dB crest factor)}$$

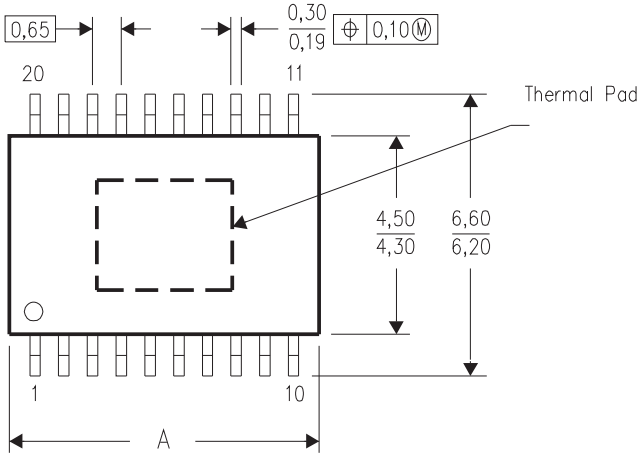
Table 6 and Table 7 show that some applications require no airflow to keep junction temperatures in the specified range. The MC6019 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 6 and Table 7 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers increases the thermal performance by increasing amplifier efficiency.

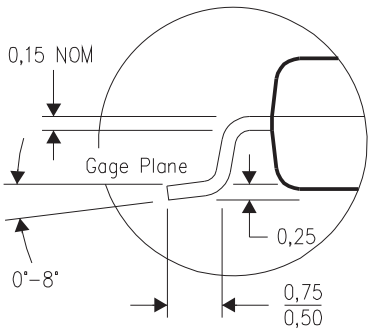
3W Stereo Audio Power Amplifier with Advanced DC Volume Control

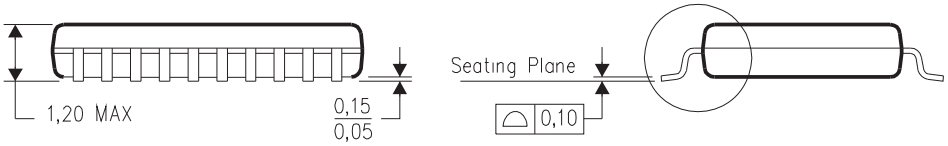
Package Information



Top View







DIM \ PINS	14	16	20	24	28
A MAX	5.10	5.10	6.60	7.90	9.80
A MIN	4.90	4.90	6.40	7.70	9.60