MOTOROLA

MC6805K2
MC6805K3

Product Preview

8-BIT MICROCOMPUTER UNITS WITH SERIAL PERIPHERAL INTERFACE AND TWO TIMERS

The MC6805K2/MC6805K3 microcomputer units are members of the M6805 Family of low-cost single-chip microcomputers. These 8-bit microcomputers contain a CPU, on-chip clock, ROM, EEPROM, RAM, I/O, two timers, one programmable prescaler, and a serial peripheral interface. These units are designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set.

HARDWARE FEATURES

- 32 Bidirectional TTL I/O Lines
  - Eight CMOS I/O Compatible
  - Eight LED I/O Compatible
  - Eight Open Drain (Software Control)
- User ROM: MC6805K2 – 2K Bytes
  MC6805K3 – 3.6K Bytes
- 96 Bytes of User RAM, 16 Bytes on Standby via V_{STBY} Pin
- 128 Bytes of User EEPROM with Write/Erase Latches
- Self-Check Mode
- Serial Peripheral Interface
- Zero-Crossing Detect/Interrupt
- Two Cascadable 8-Bit Timers with 7-Bit Software Programmable Prescaler, Data Modulus Latch, and Capture Latch
- Auxiliary Counter with "Watchdog" Reset Feature
- 5-Volt Single Supply
- Two External Interrupts

SOFTWARE FEATURES

- 10 Powerful Addressing Modes
- Byte Efficient Instruction Set with True Bit Manipulation, Bit Test, and Branch Instructions
- Single Instruction Memory Examine/Change
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Register/Flags
- User Callable Self-Check Subroutines
- Complete Development System Support on EXORciser, EXORset, and HDS-200

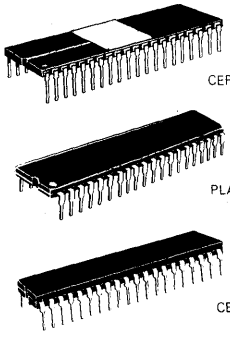
USER SELECTABLE OPTIONS

- Eight Bidirectional I/O Lines with TTL or TTL/CMOS Interface Option
- Crystal or Low-Cost Resistor Oscillator Option
- Low Voltage Inhibit Option
- Vectored Interrupts: Timer/SPI, Software, and External
- Eight Byte Standby RAM Option

HMOS

(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

8-BIT MICROCOMPUTERS



L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

S SUFFIX
CERPID PACKAGE
CASE 734

PIN ASSIGNMENT

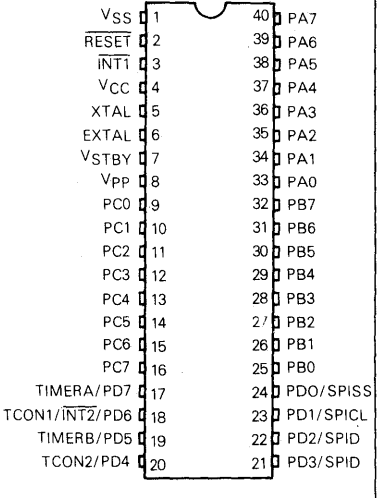
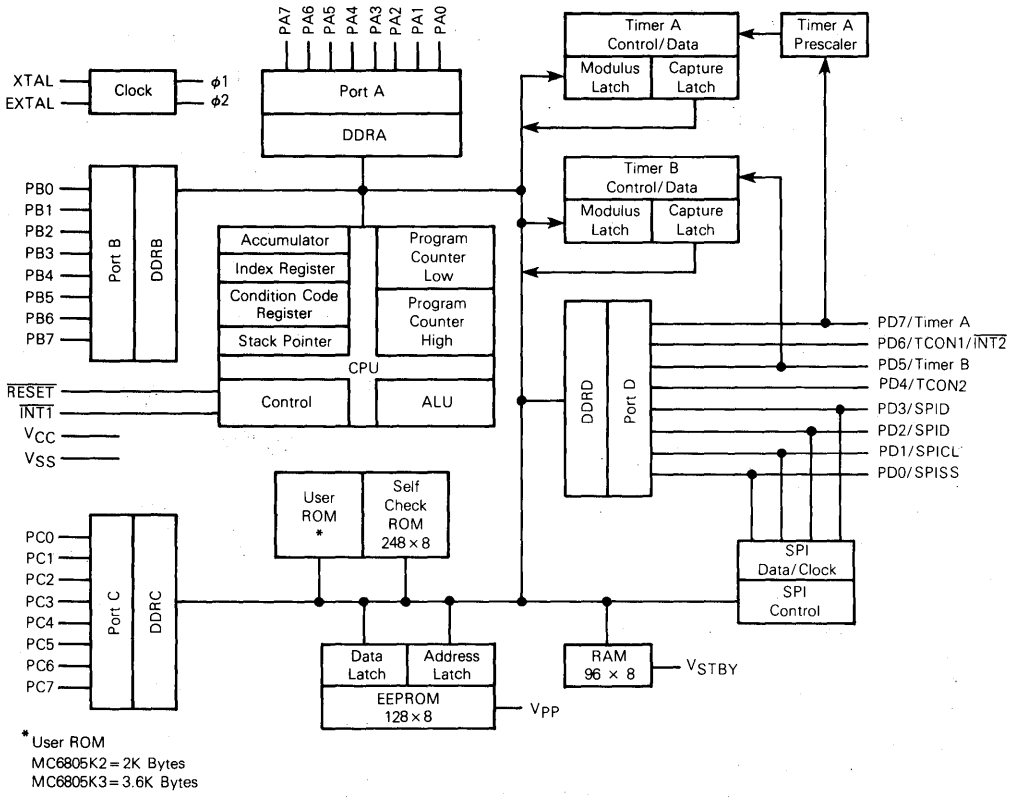
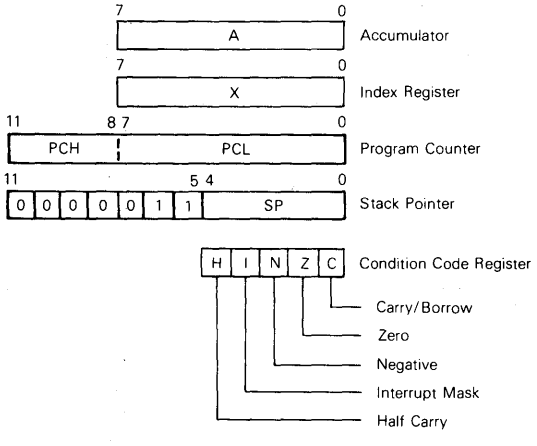


FIGURE 1 — BLOCK DIAGRAM



*User ROM
MC6805K2 = 2K Bytes
MC6805K3 = 3.6K Bytes

FIGURE 2 — PROGRAMMING MODEL



SIGNAL DESCRIPTION

The input and output signals for the MC6805K2 and MC6805K3 microcomputer units (MCUs) are described in the following paragraphs.

V_{CC}, V_{SS}, AND V_{STBY}

Power is supplied to the MCUs using these pins. V_{CC} provides the 5.0 volt ±5% power supply connection, V_{SS} is the ground connection, and V_{STBY} is the standby RAM power connection.

$\overline{INT1}$

This pin provides the capability for asynchronously applying an external interrupt to the MCU. Zero-crossing detection capability is provided on this pin.

XTAL AND EXTAL

These pins provide control input for the on-chip clock oscillator circuit. A crystal or a capacitor-resistor network, depending on the user selectable manufacturing mask option, can be connected to these pins to provide a system clock source with various stability/cost tradeoffs.

V_{PP}

This pin is used to supply programming voltage (21 volts) to the EEPROM in the program mode. It should be connected to V_{CC} during normal operation.

TIMER A/PD7 — TIMER B/PD5

These pins allow an external input to be used to decrement the internal timers.

$\overline{RESET}$

This pin allows resetting of the MCU by an external source.

INPUT/OUTPUT PORTS (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7)

Ports A, B, and C are programmable as either inputs or outputs under software control of the data direction registers. All ports are CMOS and TTL input compatible and TTL output compatible.

MEMORY

As shown in Figure 3, the MC6805K2 and MC6805K3 microcomputers are capable of addressing 4096 bytes of memory space with their program counters. The MCUs have implemented 2048 bytes of ROM including eight interrupt vectors, 248 bytes of self-check ROM, 96 bytes of user RAM, 128 bytes of EEPROM, and 17 bytes of port I/O, control, data, and status registers. The user ROM is split into two areas. One area is the main memory (locations $700 to $EFF). The last eight user ROM locations, $FF8 to $FFF, are for the interrupt vectors.

The MCUs reserve the first 17 memory locations for I/O and hardware features. These locations are used for the ports, the port data direction registers, the timers, the miscellaneous register, the serial peripheral interface, and the EEPROM program control. Of the 96 RAM bytes, 31 ($061 through $07F) are shared with the stack area. The stack must be used with care when data shares the stack area. The lower sixteen bytes of RAM, between $20 and $2F, are powered through the V_{STBY} pin.

The shared stack area is used during the processing of an interrupt or subroutine calls, to save the contents of the CPU state. Since the register contents are pushed onto the stack, the stack pointer decrements during pushes. The low order byte (PCL) of the program counter is stacked first; then the high order four bits (PCH) are stacked. This ensures that the program counter is loaded correctly during pulls from the stack, since the stack pointer increments when it pulls data from the stack. A subroutine call results in only the program counter (PCL, PCH) contents being pushed onto the stack; the remaining CPU registers are not pushed (see Figure 4).

FIGURE 3 — MEMORY MAP

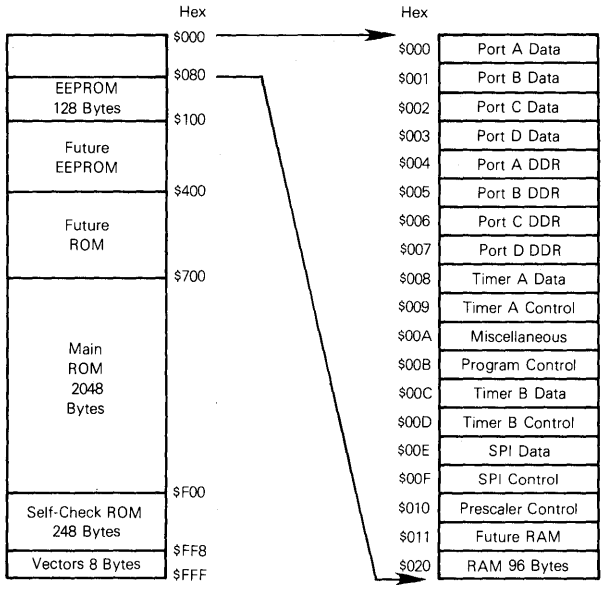
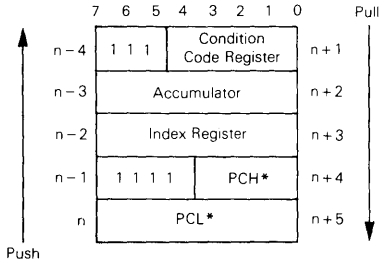


FIGURE 4 — INTERRUPT STACKING DIAGRAM



*For subroutine calls, only PCL and PCH are stacked.