MC68704P2

Technical Summary

HMOS Microcomputer Unit

MC68704P2 HMOS (high-density NMOS) microcomputer unit (MCU) is an EPROM member of the M6804 Family of microcomputers. User programmable EPROM allows program changes and lower volume applications. This feature further heightens the versatility of an MCU whose design-ability to process 8-bit variables, one bit at a time, already makes it tremendously cost effective.

This technical summary contains limited information on the MC68704P2. For detailed information, refer to the advanced information data sheet for the MC6804J1, MC6804J2, MC6804P2, and MC68704P2 8-bit microcomputers, (MC6804J1/D) or to the *M6804 MCU Manual* (DLE404/D).

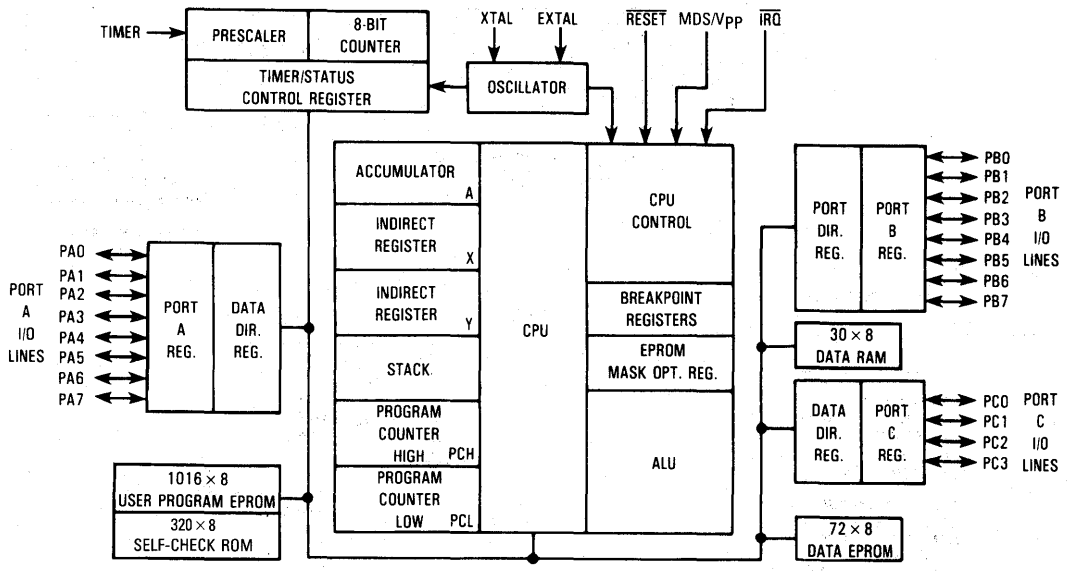
Major hardware and software features of the MC68704P2 MCU are:

- On-Chip Clock Generator
- I/O and Registers Mapped in Data Space Memory
- Software Programmable 8-Bit Timer with 7-Bit Prescaler
- Single Instruction Memory Examine/ Change
- MC6804J1/J2/P2 Emulation
- 1088 Bytes of EPROM
- True Bit Manipulation
- Bit Test and Branch Instruction
- Breakpoint and Mask Option Registers
- Self-Check
- Conditional Branches
- Timer Pin is Software Programmable as Event Counter or Timer Output
- MC68HC04P2/P3 Pin Compatibility
- 32 Bytes of RAM

User selectable options are:

- Mask Selectable Edge- or Level-Sensitive Interrupt Pin
- Push-Pull or Open-Drain Interface Ports

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIGNAL DESCRIPTION

V_{CC} AND V_{SS}

Power is supplied to the microcomputer using these two pins. V_{CC} is +5 volts (±0.5 V) power, and V_{SS} is ground.

$\overline{IRQ}$

This pin provides the capability for asynchronously applying an external interrupt to the microcomputer.

EXTAL AND XTAL

These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor/capacitor combination, or an external signal is connected to these pins to provide a system clock. Selection is made through the mask option register (MOR). The different clock generator options are shown in Figure 1, along with crystal specifications.

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Internal Clock Options

The crystal oscillator start-up time is a function of many variables. To ensure rapid oscillator start-up, neither the crystal characteristics nor load capacitances should exceed recommendations. When using the on-board oscillator, the MCU should remain in a reset condition, with the $\overline{RESET}$ pin voltage below V_{IRES+}, until the oscillator has stabilized at its operating frequency. See Figure 2 for resistor/capacitor oscillator options.

TIMER

The TIMER pin can be configured to operate in either the input or output mode. As input, this pin is connected to the prescaler input and serves as the timer clock. As output, the timer pin reflects the contents of the DOUT bit of the timer status/control register, the last time the TMZ bit was logic high.

$\overline{RESET}$

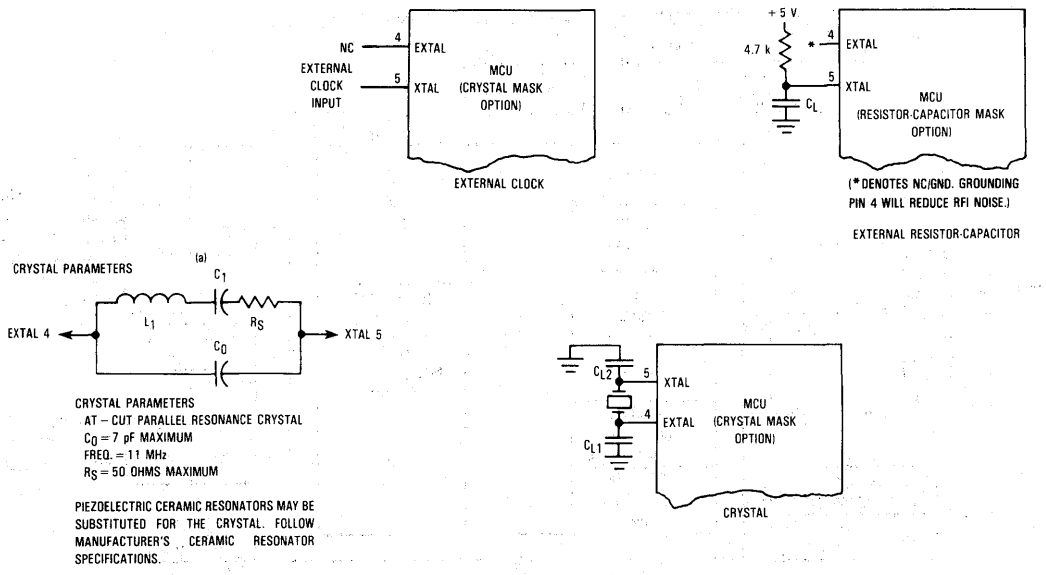
The $\overline{RESET}$ pin is used to restart the processor to the beginning of a program. The program counter is loaded with the address of the restart vector. This should be a jump instruction to the first instruction of the main program. Together with the MDS pin, the $\overline{RESET}$ pin selects the operating mode of the MCU.

MDS/V_{PP}

The mode select (MDS) pin places the MCU into special operating modes. When this pin is logic high at the exit of the reset state, the decoded state of PA6 and PA7 is latched to determine the operating mode. This choice can be either the single-chip, self-check, or EPROM programming. However, if MDS is logic low at the end of the reset state, the single-chip operating mode is automatically selected. No external diodes, switches, transistors, etc. are required for single-chip mode selection. This pin is raised to V_{PP} voltage to program the EPROM.

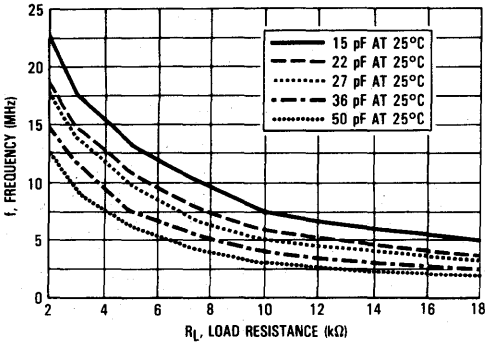
INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC3)

These 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmable as

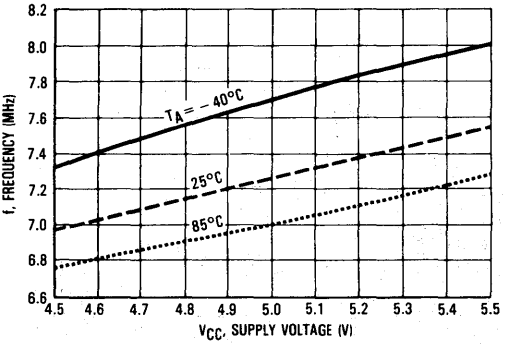


NOTE: Keep crystal leads and circuit connections as short as possible.

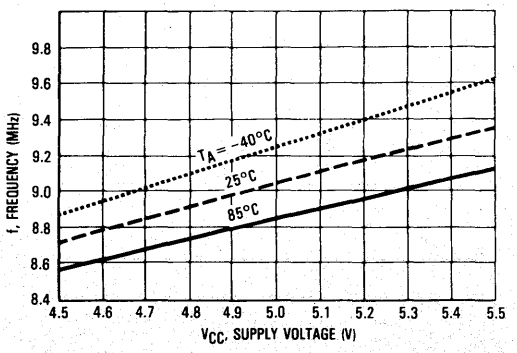
Figure 1. Clock Generator Options and Crystal Parameters



(a) TYPICAL FREQUENCY VS RESISTANCE



(b) TYPICAL FREQUENCY VARIATIONS @ $C_L = 15$ pF, 10 kΩ



(c) TYPICAL FREQUENCY VARIATIONS @ $C_L = 50$ pF, 3 kΩ

Figure 2. Typical Frequency Selection for Resistor/Capacitor Oscillator Options

either inputs or outputs under software control of the data direction registers.

PROGRAMMING

INPUT/OUTPUT PROGRAMMING

There are 20 input/output pins. All pins of each port are programmable as inputs or outputs under the control of the data direction registers (DDR).

The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output, or a logic zero for input, as shown in Figure 3. When the registers are programmed as outputs, the latched data is readable regardless of the logic levels at the output pin due to output loading.

All the I/O pins are LSTTL compatible as both inputs and outputs. In addition, all three ports may use either or both of two output options: open drain or push-pull.

Any write to a port writes to all of its data bits even though the port DDR may be set to input. This can be used as a tool to initialize the data registers and avoid undefined outputs. However, care must be exercised when using read-modify-write instructions. The data read corresponds to the pin level if the DDR is an input or to the latched output data when the DDR is an output.

The 20 bidirectional lines may be configured by port to be the standard configuration, push-pull, or open drain. Port B outputs are LED compatible.

Port Data Registers ($00, $01, $02)

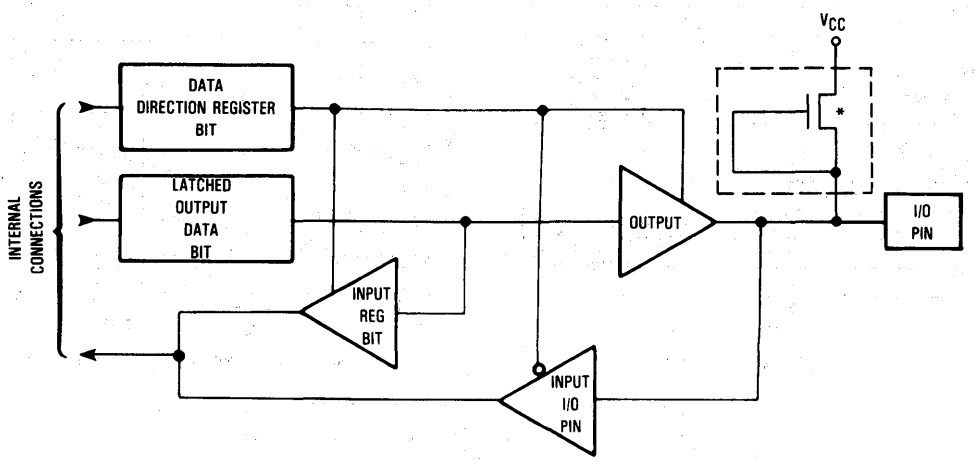
The port data registers are not initialized on reset. These registers should be initialized before changing the DDR bits to avoid undefined levels.

Port A ($00) and Port B ($01)

7	6	5	4	3	2	1	0

Port C ($02)

7	6	5	4	3	2	1	0
X	X	X	X				



DATA DIRECTION REGISTER BIT	OUTPUT DATA BIT	OUTPUT STATE	INPUT TO MCU
1	0	0	0
1	1	1	1
0	X	HI-Z	PIN

*For CMOS option transistor acts as resistor (approximately 40 kΩ) to V_{CC}.
For LSTTL/open-drain options transistor acts as low current clamping diode to V_{CC}.

Figure 3. Typical I/O Port Circuitry

With regard to Port C only, the four MSB bits are unused. These bits are "don't care" (X) bits when written to but are always logic high when read.

Port Data Direction Registers ($04, $05, $06)

Port DDRs configure the port pins as either outputs or inputs. Each port pin can be programmed individually to be an input or an output. A zero in the pin's corresponding DDR bit programs it as an input; a logic one programs it as an output. On reset, all the DDRs are initialized to a logic zero state to put the ports in the input mode.

Port A ($04) and Port B ($05)

7	6	5	4	3	2	1	0

Port C ($06)

7	6	5	4	3	2	1	0
X	X	X	X				

With regard to Port C only, the four MSB bits are unused. These bits are "don't care" (X) bits when written to but are always logic high when read.

MEMORY

The MCU memory map (Figure 4) consists of 4352 bytes of addressable memory and I/O register locations. This MCU has three separate memory spaces: program space, data space, and stack space.

The MCU is capable of addressing 4096 bytes of program space memory with its program counter and 256 bytes of data space memory with its instructions. Program space memory includes self-check ROM, program EPROM, self-check vectors (mask ROM), user program vectors (EPROM), and reserved memory locations.

A non-accessible subroutine stack space RAM is provided. This stack space consists of a last-in-first-out (LIFO) register. This register is used with inherent addressing to stack the return address for subroutines and interrupts.

Indirect X and Y register locations $80 and $81 are generally used as pointers for such tasks as indirect addressing to data space locations. Short direct addressing allows access to the four data space addresses $80-$83 with single byte opcodes. The operations allowed are increment, decrement, load, and store. Data space locations $82 and $83 can be used for 8-bit counter locations.

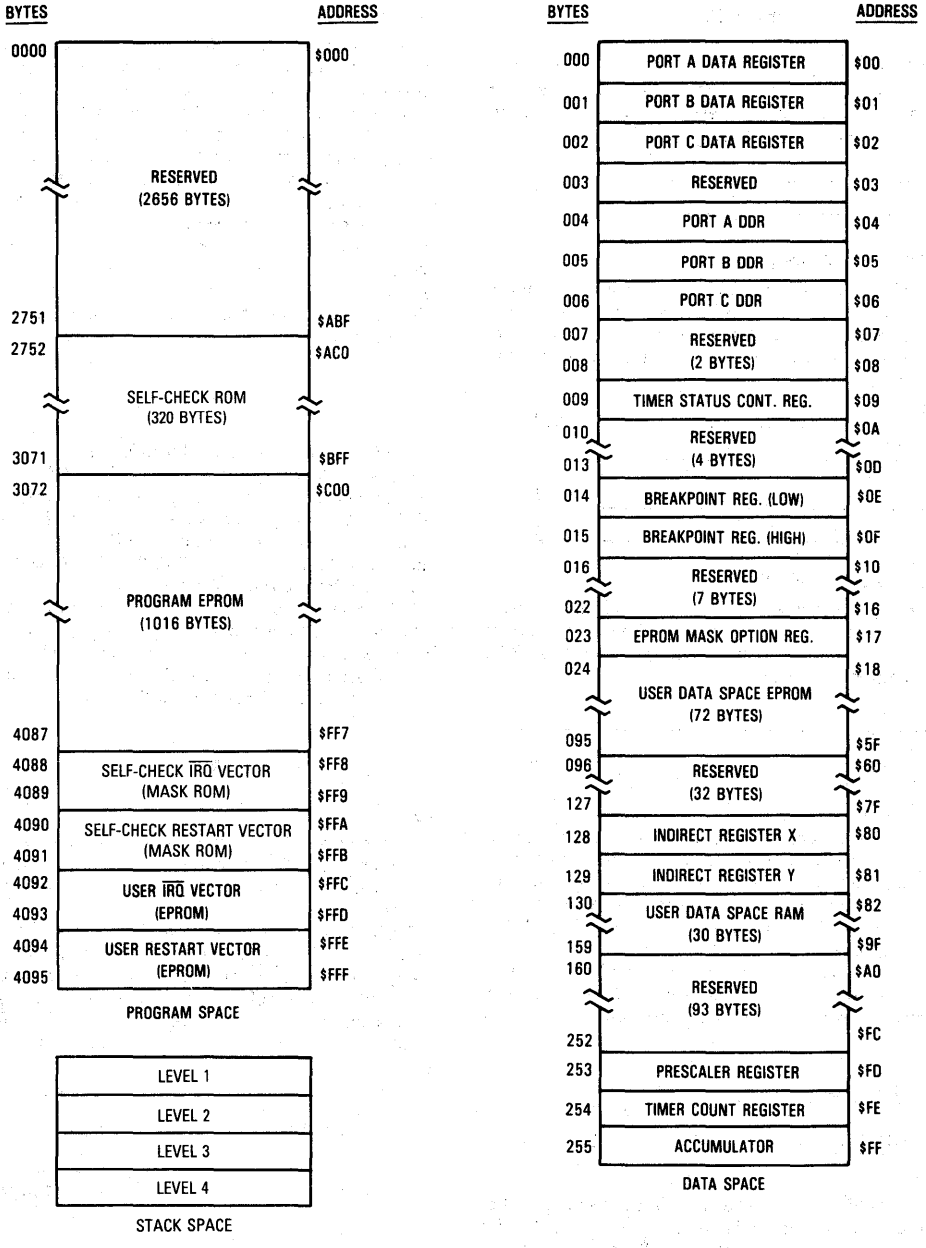


Figure 4. Memory Map

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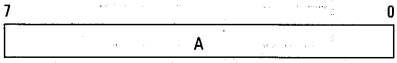
REGISTERS

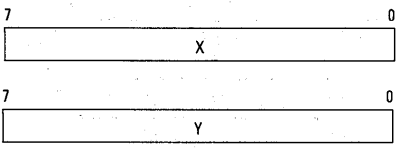
ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



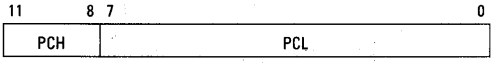
INDIRECT REGISTERS (X,Y)

These two registers are used to maintain pointers to other memory locations in data space. They are used in the register-indirect addressing mode and can be accessed with the direct, indirect, short direct, or bit set/clear modes.



PROGRAM COUNTER (PC)

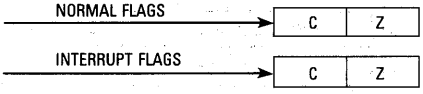
The program counter is a 12-bit register that contains the address of the next byte to be fetched from program space. The program counter is contained in low byte (PCL) and high nibble (PCH).



FLAGS (C,Z)

The first flag, the carry (C) bit, is set on a carry or borrow out of the arithmetic logic unit (ALU). It is cleared if the arithmetic operation does not result in a carry or borrow. The C bit is also set to the value of the bit tested in a bit test instruction. It participates in the rotate left (ROLA) instruction, as well.

The second flag, the zero (Z) bit, is set if the result of the last arithmetic or logic operation was equal to zero. Otherwise, it is cleared. Bit test instructions do not affect the Z bit.



There are two sets of these flags. One set is for interrupt processing (interrupt mode flags). The other set is for normal operations (program mode flags). When an interrupt occurs, a context switch is made from the program flags to the interrupt flags. An RTI forces the context switch back. While in either mode, only the flags for that mode are available. A context switch does not affect the value of the C or Z bits. Both sets of flags are cleared by $\overline{\text{RESET}}$.

STACK

A last-in-first-out (LIFO) stack is incorporated in the MCU that eliminates the need for a stack pointer. This non-accessible subroutine stack space is implemented in separate RAM, 12-bits wide. Whenever a subroutine call or interrupt occurs, the contents of the PC are shifted into the top register of the stack. At the same time, the top register is shifted one level deeper. This happens to all registers, with the bottom register falling out of the stack.

Whenever a return from subroutine or interrupt occurs, the top register is shifted into the PC and all lower registers are shifted one level higher. The stack RAM is four levels deep. If the stack is pulled more than four times with no pushes, then the address that was stored in the bottom level of the stack is shifted into the PC.

SELF CHECK

The MCU implements two forms of internal check: self check and the verify mode phase of EPROM programming. Self check performs an extensive functional check of the MCU using a signature analysis technique. For information on the verify mode in EPROM programming, see application note, *MC68704P2 8-Bit EPROM Microcomputer Programming Module* (AN-942).

Self-check mode is selected by holding the MDS and PA7 pins logic high and the PA6 pin logic low as $\overline{\text{RESET}}$ goes low to high. Monitoring the self-check mode's stages for successful completion requires external circuitry, see Motorola's *M6804 MCU Manual* (DLE404/D).

RESET

$\overline{\text{RESET}}$

All resets of the MC68704P2 are caused by the external reset input ($\overline{\text{RESET}}$). A reset can be achieved by pulling the $\overline{\text{RESET}}$ pin to logic low for a minimum of 96 oscillator cycles.

During reset, a delay of 96 oscillator cycles is needed before allowing the $\overline{\text{RESET}}$ input to go high. If power is being applied, $\overline{\text{RESET}}$ must be held low long enough for the oscillator to stabilize and then provide the 96 clocks. Connecting a capacitor and resistor to the $\overline{\text{RESET}}$ input, as shown in Figure 5 below typically provides sufficient delay.

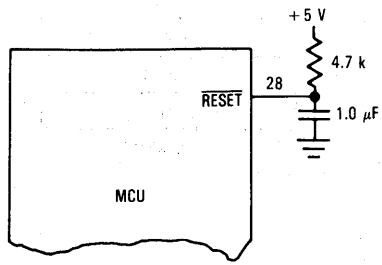


Figure 5. Powerup $\overline{\text{RESET}}$ Delay Circuit

INTERRUPT

The MCU can be interrupted by applying a logic low signal to the $\overline{IRQ}$ pin. However, a bit in the mask option register (MOR) determines whether the falling edge or the actual low level of the $\overline{IRQ}$ pin is sensed to indicate an interrupt.

EDGE-SENSITIVE OPTION

When the $\overline{IRQ}$ pin is pulled low, the internal interrupt request latch is set. Prior to each instruction fetch, this interrupt request latch is tested. If its output is low, an interrupt sequence is initiated at the end of the current instruction, provided the interrupt mask is cleared. Figure 6 contains a flowchart that illustrates both the reset and interrupt sequences.

The interrupt sequence consists of one cycle during which:

the interrupt request latch is cleared,

the interrupt mode flags are selected,

the program counter (PC) is saved on the stack,

the interrupt mask is set, and

The $\overline{IRQ}$ vector jump address is loaded into the PC.

The $\overline{IRQ}$ vector jump address is $FFC-$FFD in the single-chip mode and $FF8-$FF9 in the self-check mode. The contents of these locations are not decoded as an address to which the PC should jump. Instead, they are decoded like any other EPROM program word. So, it is essential that the vector contents specify a JMP instruction in addition to the starting address of the interrupt service routine. If required, this routine should save the values of the accumulator and the X and Y registers, since these values are not stored on the stack.

Internal processing of the interrupt continues until a return from interrupt (RTI) instruction is processed. During RTI the interrupt mask is cleared and the program mode flags are selected. The next instruction of the program is then fetched and executed.

When the interrupt was initially detected and the interrupt sequence started, the interrupt request latch was cleared so that the next interrupt could be detected. These steps occurred even as the first interrupt was being serviced. However, even though the second interrupt edge set the interrupt request latch during the first interrupt's processing, the second interrupt's sequence can not begin until completion of the interrupt service routine for the first interrupt. Completion of an interrupt service rou-

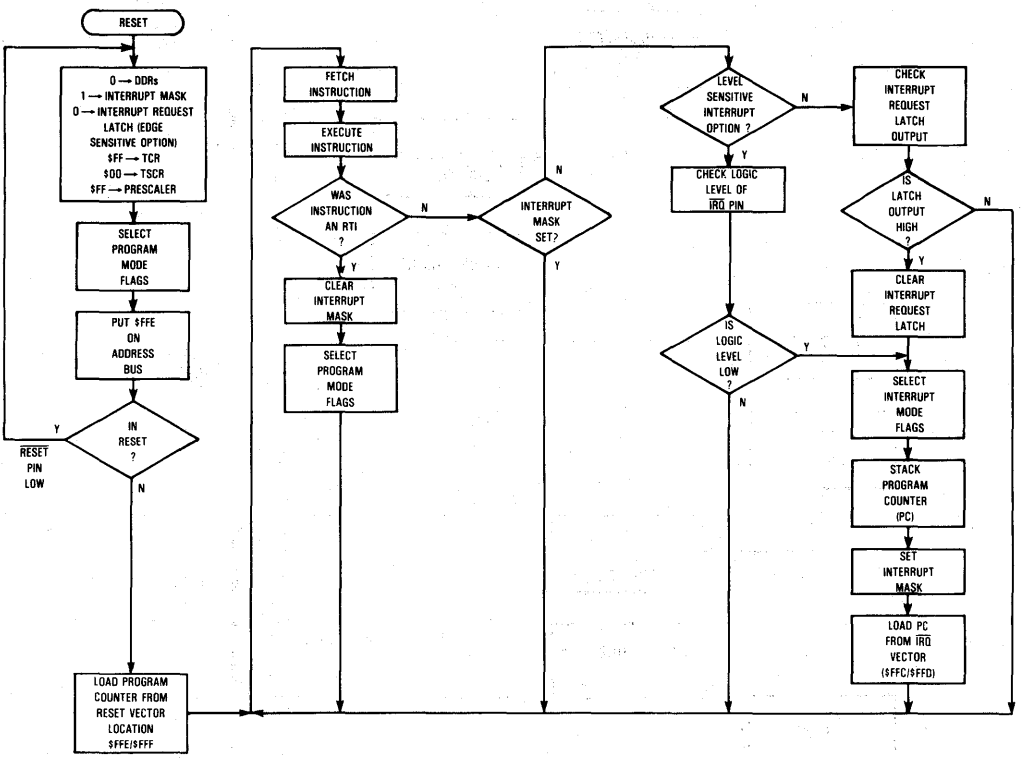


Figure 6. Reset and Interrupt Flowchart

tine is always accomplished using an RTI instruction to return to the main program. The interrupt mask, which is not directly available to the programmer, is cleared during the last cycle of the RTI instruction.

LEVEL-SENSITIVE OPTION

Actual operation of the level-sensitive and edge-sensitive options are similar. However, the level-sensitive option does not have an interrupt request latch. Since there is no interrupt request latch, the logic level of the $\overline{IRQ}$ pin is checked to detect the interrupt. Also, in the interrupt sequence there is no need to clear the interrupt request latch. These differences are shown in Figure 6.

POWERUP AND TIMING

During the powerup sequence, the interrupt mask is closed. This precludes any false interrupts. The PC is also loaded with the appropriate restart vector (jump instruction).

To open the interrupt mask, the user should do a JSR to an initialization subroutine that ends with an RTI instead of an RTS. The RTI opens the interrupt mask. Typical $\overline{RESET}$ and $\overline{IRQ}$ processes and their relationship to the interrupt mask are shown in Figure 7.

Maximum interrupt response time is six machine cycles. This includes five cycles for the longest instruction plus one for stacking the PC and switching flags.

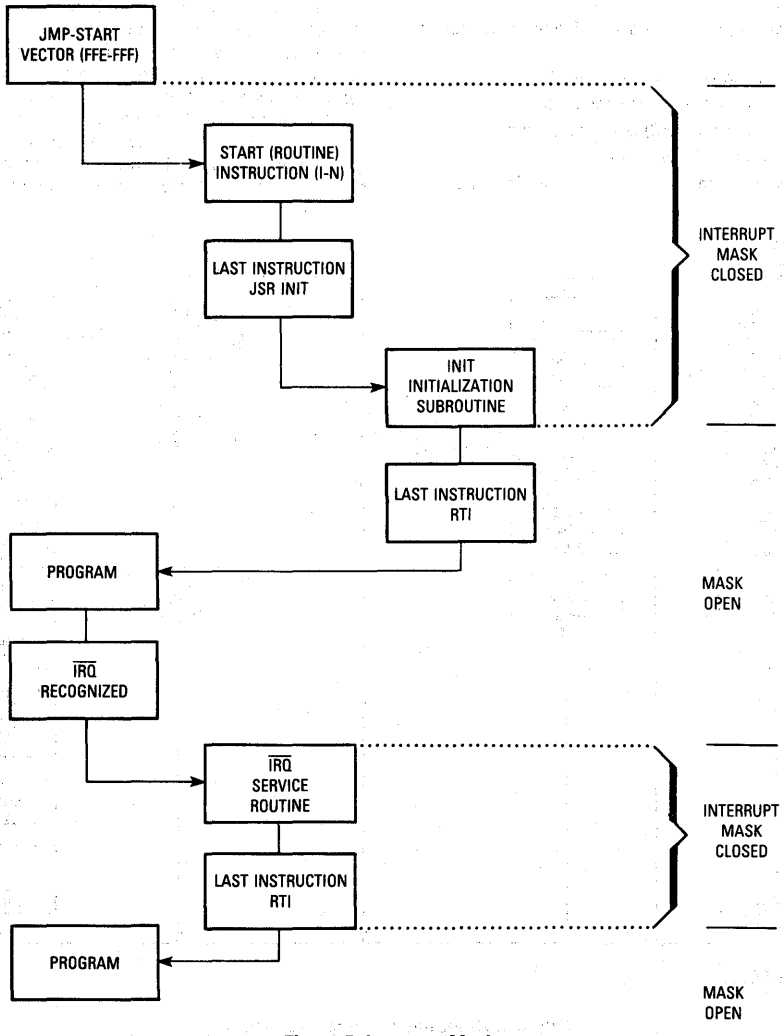
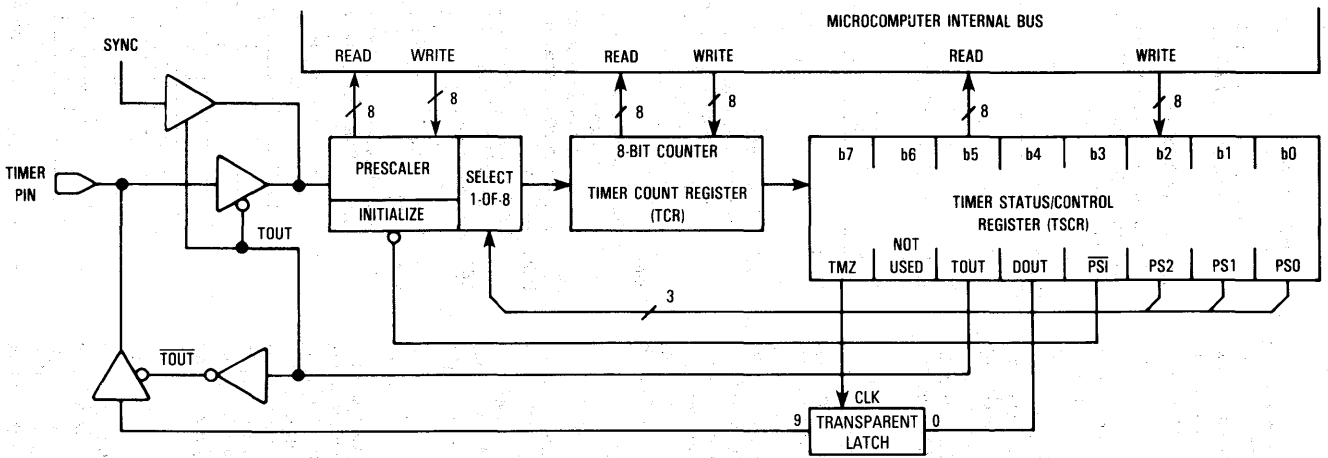


Figure 7. Interrupt Mask



TIMER PIN STATUS

TOUT	PRESCALER CLOCK	TIMER PIN
0	TIMER PIN	INPUT MODE
1	SYNC	OUTPUT MODE

Figure 8. Timer Block Diagram

TIMER

A block diagram of the MC68704P2 timer circuitry is shown in Figure 8. The timer logic in the MCU is comprised of a simple 8-bit counter called the timer counter. This counter is decremented by a 7-bit prescaler at a rate determined by the timer status/control register (TSCR).

PRESCALER

The prescaler is a 7-bit counter used to extend the maximum interval of the overall timer. This counter is clocked by a signal from the TIMER pin or by the internal sync pulse. It divides the frequency received by some factor to create the prescaler output. The factor by which the TIMER pin signal is divided is called the prescaler tap. The value of this tap is selected by three bits of the TSCR (PS0-PS2). These bits control the division of the prescaler input within the range of divide-by-2^0, to divide-by-2^7.

TIMER COUNTER

The timer counter, which may be read or loaded under program control, is decremented from a maximum value of 256 toward zero by the prescaler output. Both are decremented on rising clock edges.

The prescaler register and timer count register are readable and writeable. A write to either one will take precedence over the normal counter function. For example, if a value is written to the timer count register, and this write and a decrement-to-zero occur at the same time, the write takes precedence. TSCR bit one (TMZ) is not set until the next timer time out.

TIMER PIN

The TIMER pin may be programmed as either an input or an output. Its status depends on the value of TSCR bit 5 (TOUT). This relationship is shown in the TIMER pin status section of Figure 8. The frequency of the internal clock applied to the TIMER pin must be less than t_{byte}, which is (f_{osc}/48).

TIMER INPUT MODE

In the timer input mode, TOUT is logic zero and the TIMER pin is connected directly to prescaler input. So, the prescaler is clocked by the signal from the TIMER pin. The prescaler divides the TIMER pin clock input by the prescaler tap. The prescaler output then clocks the 8-bit timer count register. When this register is decremented to zero, it sets TSCR bit one (TMZ). This TMZ bit can be tested under program control to tell when the counter register has reached zero.

TIMER OUTPUT MODE

In the output mode, the TIMER pin is output. TOUT is a logic one. The prescaler is clocked by the internal sync pulse. This pulse is a divide-by-48 of the internal oscillator (f_{osc}/48). From this point on, operation is similar to that described for the input mode. However, in the output mode, once the prescaler decrements the timer counter to zero, the high TMZ bit state allows TSCR bit 4 (DOUT) to become direct input to the TIMER pin.

NOTE

TMZ is normally set to logic one when TCR decrements to zero and the timer times out. However, it may be set by a write of $00 to the timer counter or by a write to bit 7 of TSCR.

TIMER COUNT REGISTER ($FE)

The timer count register reflects the current count in the internal 8-bit counter. The register is the counter and can be read or written.

7							0
MSB							LSB
RESET:							
1	1	1	1	1	1	1	1

TIMER STATUS/CONTROL REGISTER (TSCR) ($09)

7	6	5	4	3	2	1	0
TMZ	—	TOUT	DOUT	$\overline{PSI}$	PS2	PS1	PS0
RESET:							
0	0	0	0	0	0	0	0

TMZ — Timer zero
- 1 = Timer count register has reached the all zero's state since the last time the TMZ bit was read
- 0 = This bit is cleared by a read of the TSCR if TMZ is read as logic one

Bit 6
- Not used by this register

TOUT — Timer output
- 1 = Output mode is selected for the timer
- 0 = Input mode is selected for the timer

DOUT — Data output
- Latched data at this bit is sent to the TIMER pin when both the TMZ and TOUT bits are logic high.

$\overline{PSI}$ — Prescaler initialize
- 1 = Prescaler begins to decrement
- 0 = Prescaler is initialized and counting is inhibited

PS0 — PS2
- These bits are used to select the prescaler tap. The coding of the bits is shown below:

PS2	PS1	PS0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

It is recommended that MVI or loading and storing instructions be used when changing bit values in the TSCR. Read-modify-write instructions can cause the TMZ to assume an unexpected state.

During reset, the TSCR is set to all zeroes; the TIMER pin is in the high impedance input mode; and DOUT LATCH is forced to a logic high. At the same time, PS0-PS2 coding sets the prescaler tap at divide-by-one, and bit 3 initializes the prescaler.

TIMER PRESCALER REGISTER ($FD)

The timer prescaler register reflects the current count of the 7-bit prescaler. This register is the prescaler counter and can be read or written.

6						0
MSB						LSB
RESET:						
1	1	1	1	1	1	1

EPROM

BREAKPOINT REGISTERS

The breakpoint registers are used as a program debugging aid. To enable the breakpoint registers:

— The MDS pin must be pulled high using a 300 ohm resistor to +5 volts.

— In the Port A I/O register, both PA6 and PA7 pins must be pulled low using a 10 kilohm resistor to ground.

A breakpoint address is written into address registers ARL and ARH by the user. The lower eight bits of the breakpoint address (A0-A7) are written into the ARL. The upper four bits (A8-A11) are written into the ARH.

Breakpoint Address Register Low (ARL) ($0E)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
RESET:							
0	0	0	0	0	0	0	0

A7-A0
Breakpoint address bits A7 through A0.

Breakpoint Address Register High (ARH) ($0F)

7	6	5	4	3	2	1	0
X	X	X	X	A11	A10	A9	A8
RESET:							
0	0	0	0	0	0	0	0

A11-A8
Breakpoint address bits A11 through A8.

NOTE

ARL must be written after writing to ARH.

ARL and ARH are concatenated to form the breakpoint address. When the processor fetches an instruction having the same address as the breakpoint address, the MDS pin goes logic low for one machine cycle. This operation does not alter program flow.

MASK OPTION REGISTER (MOR) ($17)

The MC68704P2 uses the EPROM MOR during emulation to select the clock/oscillator, port, and interrupt request edge- and level-sensitive triggering options available on the MC6804J1/J2/P2 devices. The mask option register is not affected by $\overline{\text{RESET}}$.

7	6	5	4	3	2	1	0
OSC	X	PORT A	X	PORT B	PORT C	$\overline{\text{IRQ}}$	X

OSC — The oscillator option bit
1 = Resistor/capacitor mode of operation
0 = Crystal mode of operation
The crystal mode is selected in the EPROM programming mode, regardless of the state of OSC.

PORT A — Port A output selection bit
1 = Open drain output mode
0 = Three-state output mode

PORT B — Port B output selection bit
1 = Open drain output mode
0 = Three-state output mode

PORT C — Port C output selection bit
1 = Open drain output mode
0 = Three-state output mode

$\overline{\text{IRQ}}$ — Interrupt request bit
1 = Level-sensitive triggering input mode
0 = Edge-sensitive triggering input mode

Bits 6, 4, and 0
Not used in this register

Emulation

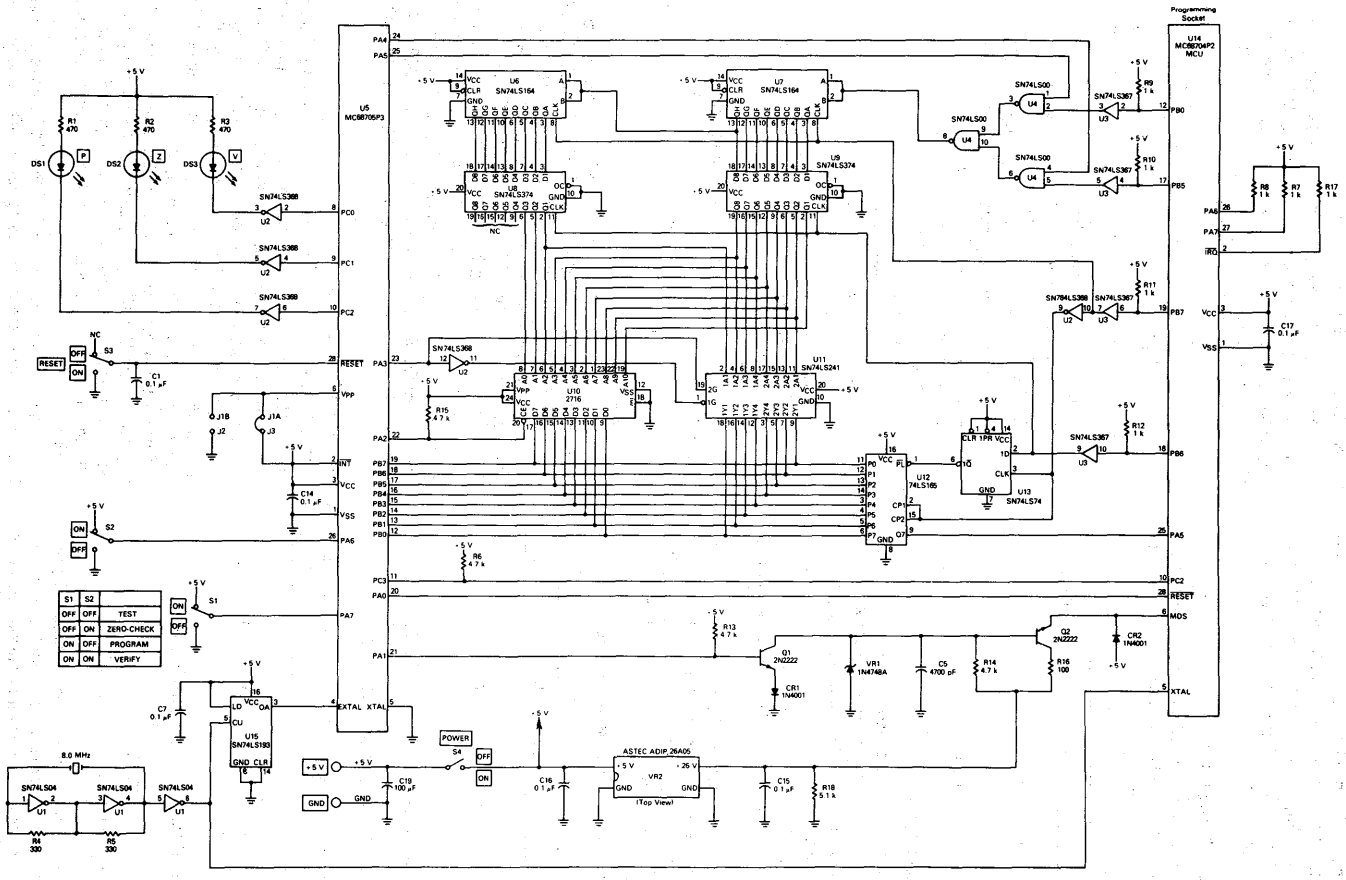
The MC68704P2 MCU internal EPROM can be programmed to emulate either the MC6804J1, MC6804J2, or the MC6804P2 MCU device. While the M6805 Family of EPROM MCUs have an on-chip bootstrap-loader program stored in mask ROM, the MC68704P2 does not. Additional programming hardware and software are required to program this MCU EPROM. For more specific information regarding the programming and erasing of the MCU EPROM; see application note, *MC68704P2 8-Bit EPROM Microcomputer Programming Module* (AN-942).

Emulation Limitations

This EPROM MCU is designed to emulate the functions of the MC6804J1/J2/P2 devices as closely as possible. Limitations to this capability pertain to the CMOS pullup option, execution out of data space, and packaging pin assignments of the MCU being emulated. The limitations do not apply to the timing, execution speed, or functionality of the MCU being emulated.

This MCU cannot emulate the CMOS pullup option. To implement the CMOS option, external 40 kilohm pullup resistors are connected to the specific I/O port signal lines. All other options are available through correct use of the MOR bytes.

It was necessary that the PC of this MCU have access to both the program and data space EPROM because of the implementation of the MCU programming hardware. Therefore, the MC68704P2 will execute code out of the



Notes:
1. Pins 1, 8, and 15 connected to GND for devices U2 and U3.
2. Pin 16 connected to +5 V for devices U2 and U3.
3. Pin 7 connected to GND, and pin 14 connected to +5 V for devices U1 and U4.

Figure 9. Programming Module Schematic

data space EPROM ($18-$5F). This anomaly is not permitted on the MC6804J1/J2/P2 ROM devices. When planning on operating ROM patterns from this EPROM MCU, the programmer should not use data space as extra program space.

The MC6804J1/J2 devices are packaged in 20-pin dual-in-line (DIL). The MC6804P2 and the MC68704P2 devices are packaged in 28-pin DIL packages. Device pin assignments must be adhered to. When emulating a 20-pin MCU with this EPROM MCU, all unused pins (PA0-PA3, PC0-PC3) should be grounded externally through a 10 kilohm resistor. This allows the MC68704P2 to emulate the software execution exactly as it would occur on the 20-pin device.

EPROM ERASING

This MCU EPROM is erased by exposure to a high intensity ultraviolet light (UV) with a wavelength of 2537 Angstrom. The recommended dosage is 15Ws/cm^2, (UV intensity at EPROM surface/area to be erased). UV lamps should be used without filters. The MC68704P2 should be positioned about one inch from the UV source. The duration of the exposure is a function of the radiant strength of the individual UV source.

EPROM PROGRAMMING HARDWARE

The MC68704P2 programming module, shown in Figure 9, is used to program the MC68704P2 MCU EPROM. To do this, the module requires a 2K EPROM of the 2716 type, a +5 Vdc power supply, and either a MC68705P3 or MC6805P2 MCU as the module MCU. For more specific information regarding the hardware and procedures necessary to program the MC68704P2; see either the advanced information data sheet for MC6804J1, MC6804J2, MC6804P2, and MC68704P2 8-bit microcomputers (MC6804J1/D) or application note, *MC68704P2 8-Bit EPROM Microcomputer Programming Module* (AN-942).

INSTRUCTION SET

The MCU has a set of 42 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type.

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is the accumulator; the other is obtained from memory using one of the addressing modes. Refer to the following list of instructions.

Function	Mnemonic
Load A from Memory	LDA
Load XP from Memory	LDX
Load YP from Memory	LDY
Store A in Memory	STA
Add to A	ADD
Subtract from A	SUB
AND Memory to A	AND
Transfer A to XP	TAX
Transfer A to YP	TAY
Transfer YP to A	TYA
Clear A	CLRA
Clear XP	CLRX
Clear YP	CLRY
Arithmetic Compare with Memory	CMP
Move Immediate Value to Memory	MVI
Arithmetic Left Shift of A	ASLA
Complement A	COMA
Rotate A Left and Carry	ROLA
Transfer XP to A	TPA

READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. All INC and DEC forms along with all bit manipulation instructions use this method. Refer to the following list of instructions.

Function	Mnemonic
Increment Memory Location	INC
Increment A	INCA
Increment XP	INCX
Increment YP	INCY
Decrement Memory Location	DEC
Decrement A	DECA
Decrement XP	DECX
Decrement YP	DECY

BRANCH INSTRUCTIONS

This set of instructions branches if a particular condition is met; otherwise, no operation is performed. Branch instructions are two byte instructions. Refer to the following list of instructions.

Function	Mnemonic
Branch if Carry Clear	BCC
Branch if Higher or Same	(BHS)
Branch if Carry Set	BCS
Branch if Lower	(BLO)
Branch if Not Equal	BNE
Branch if Equal	BEQ

BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit which resides in the 256 bytes of data space, where all port registers, port DDRs, timer, timer control, and on-chip

RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear, and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to the following list of instructions.

Function	Mnemonic
Branch If Bit n is Set	BRSET n(n=0 . . . 7)
Branch If Bit n is Clear	BRCLR n(n=0 . . . 7)
Set Bit n	BSET n(n=0 . . . 7)
Clear Bit n	BCLR n(n=0 . . . 7)

CONTROL INSTRUCTIONS

These instructions are used to control processor operation during program execution. The jump conditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to the following list of instructions.

Function	Mnemonic
Return from Subroutine	RTS
Return from Interrupt	RTI
No Operation	NOP
Jump to Subroutine	JSR
Jump Unconditional	JMP

IMPLIED INSTRUCTIONS

Since the accumulator and all other registers are located in RAM, many implied instructions exist. Some of the instructions recognized and translated by the assembler are shown below:

Mnemonic	Becomes	Mnemonic	Becomes
ASLA	ADD $FF	INCX	INC $80
BHS	BCC	INCY	INC $81
BLO	BCS	LDXI	MVI $80 DATA
CLRA	SUB $FF	LDYI	MVI $81 DATA
CLRX	MVI $80 #0	NOP	BEQ (PC) +1
CLRY	MVI $81 #0	TAX	STA $80
DECA	DEC $FF	TAY	STA $81
DECX	DEC $80	TXA	LDA $80
DECY	DEC $81	TYA	LDA $81
INCA	INC $FF		

Some examples of valuable instructions not specifically recognized by the assembler are shown below:

Mnemonic	Meaning
BCLR 7,$FF	Ensures A is plus
BSET 7, $FF	Ensures A is minus
BRCLR 7, $FF	Branch if A is plus
BRSET 7, $FF	Branch if A is minus
BRCLR 7, $80	Branch if X is plus (BXPL)
BRSET 7, $80	Branch if X is minus (BXMI)
BRCLR 7, $81	Branch if Y is plus (BYPL)
BRSET 7, $81	Branch if Y is minus (BYMI)

OPCODE MAP

Table 1 is a listing of all the instruction set opcodes applicable to the MC6804P2 MCU.

ADDRESSING MODES

The MCU has nine different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. It deals with objects in three different address spaces: program space, data space, and stack space. The term "effective address" (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE

In the immediate addressing mode, the operand is located in program ROM. It is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution, such as a constant used to initialize a loop counter.

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the 256 bytes of data space with a single two-byte instruction.

SHORT DIRECT

In the short direct addressing mode, the MCU has four locations in data space RAM it can use, ($80, $81, $82, and $83). The opcode determines the data space RAM location, and the instruction is only one byte. Short direct addressing is a subset of the direct addressing mode. The X and Y registers are at locations $80 and $81, respectively.

EXTENDED

In the extended addressing mode, the effective address of the argument is obtained by concatenating the four least-significant bits of the opcode with the byte following the opcode to form a 12-bit address. Instructions using the extended addressing mode, such as JMP or JSR, are capable of branching anywhere in program space. An extended addressing mode instruction is two bytes long.

Table 1. Opcode Map

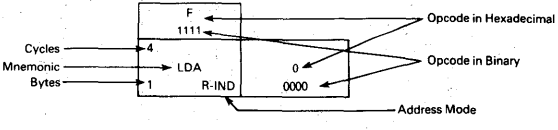
Hi / Low	Branch Instructions								Register/Memory, Control, and Read/Modify/Write Instructions				Bit Manipulation Instructions		Register/Memory and Read/Modify/Write		Hi / Low
	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	
0 0000	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	4 3 MVI IMM	5 3 BRCLR0 B-T-B	4 2 BCLR0 BSC	4 1 LDA R-IND	4 1 LDA R-IND	0 0000
1 0001	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	*	5 3 BRCLR1 B-T-B	4 2 BCLR1 BSC	4 1 STA R-IND	4 1 STA R-IND	1 0001
2 0010	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	2 1 RTI INH	5 3 BRCLR2 B-T-B	4 2 BCLR2 BSC	4 1 ADD R-IND	4 1 ADD R-IND	2 0010
3 0011	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	2 1 RTS INH	5 3 BRCLR3 B-T-B	4 2 BCLR3 BSC	4 1 SUB R-IND	4 1 SUB R-IND	3 0011
4 0100	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	4 1 COMA INH	5 3 BRCLR4 B-T-B	4 2 BCLR4 BSC	4 1 CMP R-IND	4 1 CMP R-IND	4 0100
5 0101	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	4 1 ROLA INH	5 3 BRCLR5 B-T-B	4 2 BCLR5 BSC	4 1 AND R-IND	4 1 AND R-IND	5 0101
6 0110	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	*	5 3 BRCLR6 B-T-B	4 2 BCLR6 BSC	4 1 INC R-IND	4 1 INC R-IND	6 0110
7 0111	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	*	*	5 3 BRCLR7 B-T-B	4 2 BCLR7 BSC	4 1 DEC R-IND	4 1 DEC R-IND	7 0111
8 1000	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 INC S-D	4 1 DEC S-D	5 3 BRSET0 B-T-B	4 2 BSET0 BSC	4 2 LDA IMM	4 2 LDA DIR	8 1000
9 1001	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 INC S-D	4 1 DEC S-D	5 3 BRSET1 B-T-B	4 2 BSET1 BSC	#	4 2 STA DIR	9 1001
A 1010	2 1 BNE REL	2 2 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 INC S-D	4 1 DEC S-D	5 3 BRSET2 B-T-B	4 2 BSET2 BSC	4 2 ADD IMM	4 2 ADD DIR	A 1010
B 1011	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 INC S-D	4 1 DEC S-D	5 3 BRSET3 B-T-B	4 2 BSET3 BSC	SUB IMM	4 2 SUB DIR	B 1011
C 1100	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 LDA S-D	4 1 STA S-D	5 3 BRSET4 B-T-B	4 2 BSET4 BSC	4 2 CMP IMM	CMP DIR	C 1100
D 1101	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 LDA S-D	4 1 STA S-D	5 3 BRSET5 B-T-B	4 2 BSET5 BSC	4 2 AND IMM	4 2 AND DIR	D 1101
E 1110	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JRSn EXT	4 2 JMPn EXT	4 1 LDA S-D	4 1 STA S-D	5 3 BRSET6 B-T-B	4 2 BSET6 BSC	#	4 2 INC DIR	E 1110
F 1111	2 1 BNE REL	2 1 BNE REL	2 1 BEQ REL	2 1 BEQ REL	2 1 BCC REL	2 1 BCC REL	2 1 BCS REL	2 1 BCS REL	4 2 JSRn EXT	4 2 JMPn EXT	4 1 LDA S-D	4 1 STA S-D	5 3 BRSET7 B-T-B	4 2 BSET7 BSC	#	4 2 DEC DIR	F 1111

Abbreviations for Address Modes

INH	Inherent
S-D	Short Direct
B-T-B	Bit Test and Branch
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
R-IND	Register Indirect

*	Indicates Instruction Reserved for Future Use
#	Indicates Illegal Instruction

LEGEND



RELATIVE

The relative addressing mode is only used in conditional branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from −15 to +16 from the opcode address. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

BIT SET/CLEAR

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the direct addressing of the byte in which the specified bit is to be set or cleared. Thus, any bit in the 256 locations of data space memory that can be written to can be set or cleared with a single 2-byte instruction.

CAUTION

The corresponding DDRs for ports A, B, and C are write only registers (registers at $04, $05, and $06). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write functions, they cannot be used to set or clear a DDR bit; all "unaffected" bits would be set. Write all DDR bits in a port using a single-store instruction.

BIT TEST AND BRANCH

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit that is to be tested and its condition (set or clear) is included in the opcode. The data space address of the byte to be tested is in the single byte immediately following the opcode byte. The third byte is sign extended to twelve bits and becomes the offset added to the PC if the condition is true. This single 3-byte instruction allows the program to branch based on the condition of any readable bit in the 256 locations of data space. The span of branching is from −125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry flag.

REGISTER-INDIRECT

In the register-indirect addressing mode, the operand is at the address in data space pointed to by the contents of one of the indirect registers, X or Y. The particular indirect register is selected by bit 4 of the opcode. Bit 4 decodes into an address that represents the register, $80 or $81. A register-indirect instruction is one byte long.

INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range (Comm.)	T_A	0 to 70	°C
Operating Temperature Range (Ind.)	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature (Cerdip)	T_J	175	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Cerdip	θ_{JA}	60	°C/W

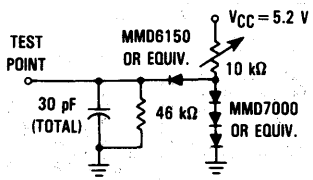


Figure 10. LSTTL Equivalent Test Load (Ports A, C, and TIMER)

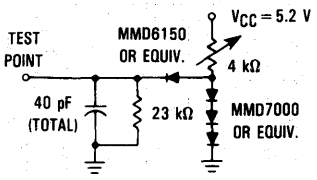


Figure 11. LSTTL Equivalent Test Load (Port B)

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{PORT}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} < P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

PROGRAMMING OPERATION ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 20°C to 30°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage	V_{PP}	20	21	22	V
V_{PP} Supply Current (V_{PP} = 22.0 V)	I_{PP}	—	10	20	mA
Programming Oscillator Frequency	f_{oscp}	—	10	11	MHz
Programming Time (Per Byte)	t_{PRG}	—	5	50	ms

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0°C to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Power Dissipation — No Port Loading	P_{INT}	—	165	275	mW
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input Capacitance	C_{in}	—	10	—	pF
Input Current ($\overline{IRQ}$, $\overline{RESET}$)	I_{in}	—	2	20	μA

SWITCHING CHARACTERISTICS

(V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0°C to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	4.0	—	11.0	MHz
Bit Time	t_{bit}	0.364	—	1.0	μs
Byte Cycle Time	t_{byte}	4.36	—	12.0	μs
$\overline{IRQ}$ and TIMER Pulse Width	t_{WL}, t_{WH}	$2 \times t_{byte}$	—	—	—
$\overline{RESET}$ Pulse Width	t_{RWL}	$2 \times t_{byte}$	—	—	—
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 μF)	t_{RHL}	100	—	—	ms

PORT DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0°C to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Ports A and C (Open Drain)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	—	—	0.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	4	40	μA
Open Drain Leakage (V_{out} = V_{CC})	I_{LOD}	—	4	40	μA
Port B (Open Drain)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	—	—	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	—	—	1.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	8	80	μA
Open Drain Leakage (V_{out} = V_{CC})	I_{LOD}	—	8	80	μA
Ports A, C, and Timer (Push-Pull)					
Output Low Voltage, I_{Load} = 0.4 mA	V_{OL}	—	—	0.5	V
Output High Voltage, I_{Load} = −50 μA	V_{OH}	2.3	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	4	40	μA
Port B (Push-Pull)					
Output Low Voltage, I_{Load} = 1.0 mA	V_{OL}	—	—	0.5	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	—	—	1.5	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.3	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	8	80	μA

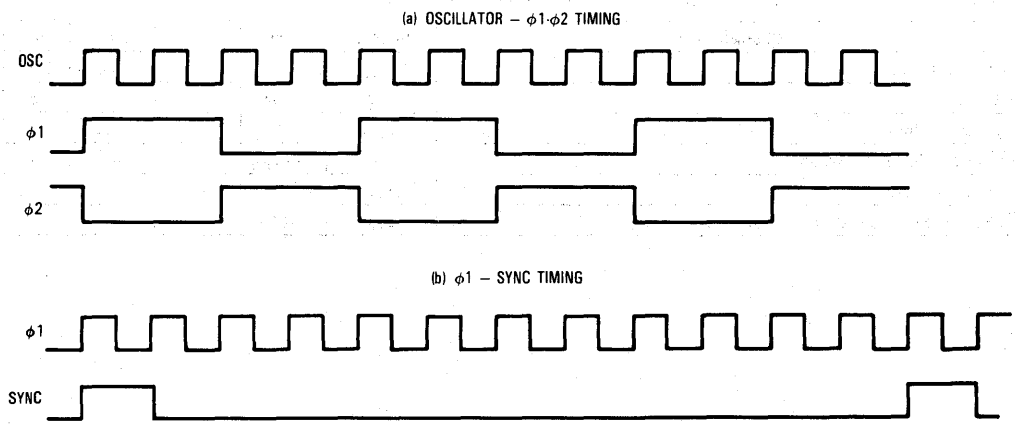


Figure 12. Clock Generator Timing Diagrams

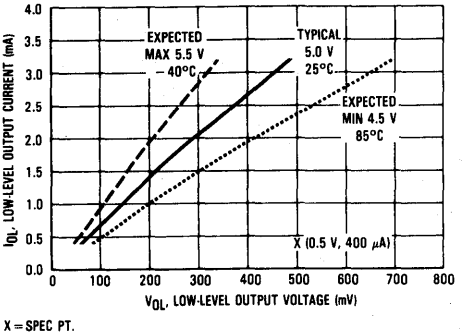


Figure 13. Typical V_{OL} vs I_{OL} for Ports A, C, and Timer

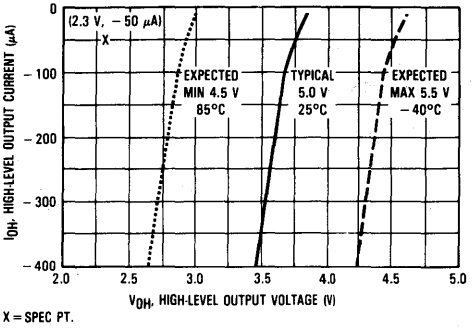


Figure 14. Typical V_{OH} vs I_{OH} for Ports A, C, and TIMER

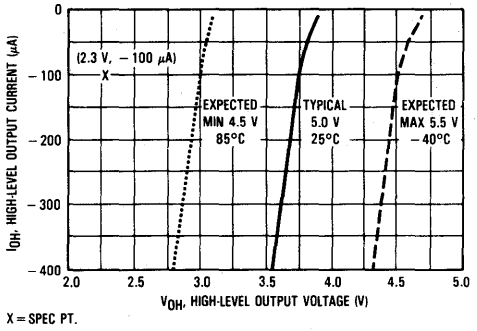


Figure 15. Typical V_{OH} vs I_{OH} for Port B

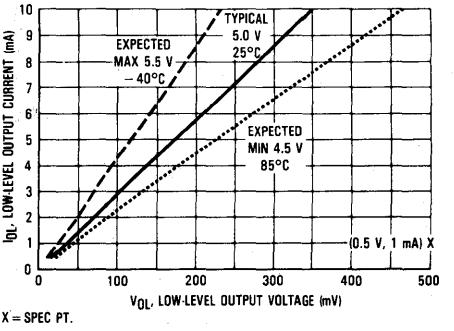


Figure 16. Typical V_{OL} vs I_{OL} for Port B

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ORDERING INFORMATION

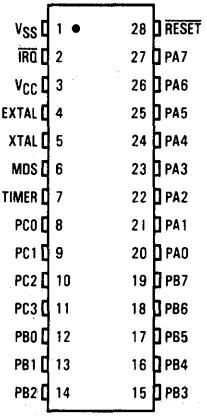
The MC68704P2 EPROM MCU device is only available in the 28-pin ceramic dual-in-line (CERDIP) package. The following table provides information pertaining to the temperature and MC order numbers of the MC68704P2.

Table 2. Generic Information

Package Type	Temperature	Order Number
Cerdip (S Suffix)	0°C to 70°C – 40°C to + 85°C	MC68704P2S MC68704P2CS

MECHANICAL DATA

PIN ASSIGNMENTS



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