

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μ A at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

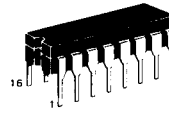
The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

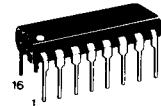
MC8T26A (MC6880A)

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

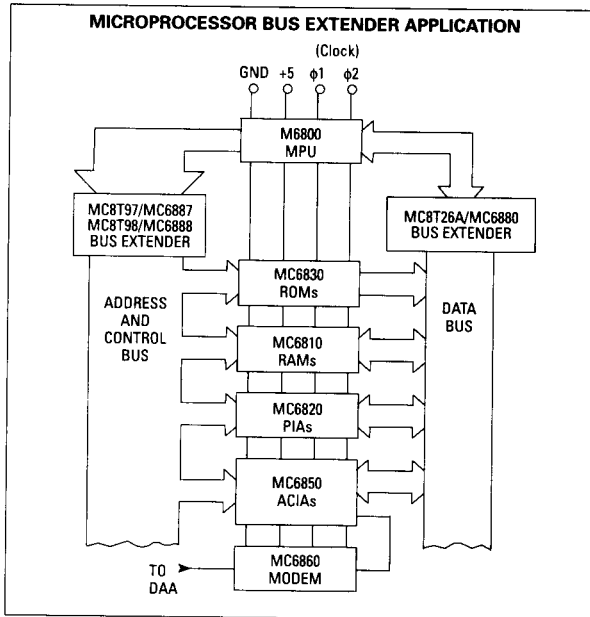


L SUFFIX CERAMIC PACKAGE CASE 620

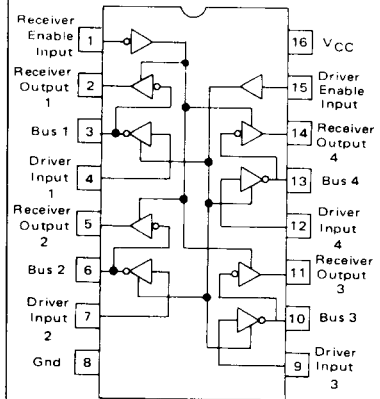


P SUFFIX PLASTIC PACKAGE CASE 648

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PIN CONNECTIONS — MC8T26A (MC6880A)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to +75°C	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

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MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature	T_J		$^\circ\text{C}$
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T_A	0 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ and $0^\circ\text{C} \leq T_A \leq 75^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (Receiver Enable Input, $V_{IL}(\overline{RE}) = 0.4\text{ V}$) (Driver Enable Input, $V_{IL}(\overline{DE}) = 0.4\text{ V}$) (Driver Input, $V_{IL}(D) = 0.4\text{ V}$) (Bus (Receiver) Input, $V_{IL}(B) = 0.4\text{ V}$)	$I_{IL}(\overline{RE})$ $I_{IL}(\overline{DE})$ $I_{IL}(D)$ $I_{IL}(B)$	—	—	-200	μA
Input Disabled Current — Low Logic State (Driver Input, $V_{IL}(D) = 0.4\text{ V}$)	$I_{IL}(D)\text{ DIS}$	—	—	-25	μA
Input Current—High Logic State (Receiver Enable Input, $V_{IH}(\overline{RE}) = 5.25\text{ V}$) (Driver Enable Input, $V_{IH}(\overline{DE}) = 5.25\text{ V}$) (Driver Input, $V_{IH}(D) = 5.25\text{ V}$) (Receiver Input, $V_{IH}(B) = 5.25\text{ V}$)	$I_{IH}(\overline{RE})$ $I_{IH}(\overline{DE})$ $I_{IH}(D)$ $I_{IH}(B)$	—	—	25	μA
Input Voltage — Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	$V_{IL}(\overline{RE})$ $V_{IL}(\overline{DE})$ $V_{IL}(D)$ $V_{IL}(B)$	—	—	0.85	V
Input Voltage — High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	$V_{IH}(\overline{RE})$ $V_{IH}(\overline{DE})$ $V_{IH}(D)$ $V_{IH}(B)$	2.0	—	—	V
Output Voltage — Low Logic State (Bus (Driver) Output, $I_{OL}(B) = 48\text{ mA}$) (Receiver Output, $I_{OL}(R) = 20\text{ mA}$)	$V_{OL}(B)$ $V_{OL}(R)$	—	—	0.5	V
Output Voltage — High Logic State (Bus (Driver) Output, $I_{OH}(B) = -10\text{ mA}$) (Receiver Output, $I_{OH}(R) = -2.0\text{ mA}$) (Receiver Output, $I_{OH}(R) = -100\text{ }\mu\text{A}$, $V_{CC} = 5.0\text{ V}$)	$V_{OH}(B)$ $V_{OH}(R)$	2.4	3.1	—	V
Output Disabled Leakage Current — High Logic State (Bus (Driver) Output, $V_{OH}(B) = 2.4\text{ V}$) (Receiver Output, $V_{OH}(R) = 2.4\text{ V}$)	$I_{OHL}(B)$ $I_{OHL}(R)$	—	—	100	μA
Output Disabled Leakage Current — Low Logic State (Bus Output, $V_{OL}(B) = 0.5\text{ V}$) (Receiver Output, $V_{OL}(R) = 0.5\text{ V}$)	$I_{OLL}(B)$ $I_{OLL}(R)$	—	—	-100	μA
Input Clamp Voltage (Driver Enable Input $I_{ID}(\overline{DE}) = -12\text{ mA}$) (Receiver Enable Input $I_{IC}(\overline{RE}) = +12\text{ mA}$) (Driver Input $I_{IC}(D) = -12\text{ mA}$)	$V_{IC}(\overline{DE})$ $V_{IC}(\overline{RE})$ $V_{IC}(D)$	—	—	-1.0	V
Output Short Circuit Current, $V_{CC} = 5.25\text{ V}$, Note 1 (Bus (Driver) Output) (Receiver Output)	$I_{OS}(B)$ $I_{OS}(R)$	-50	—	-150	mA
Power Supply Current ($V_{CC} = 5.25\text{ V}$)	I_{CC}	—	—	87	mA

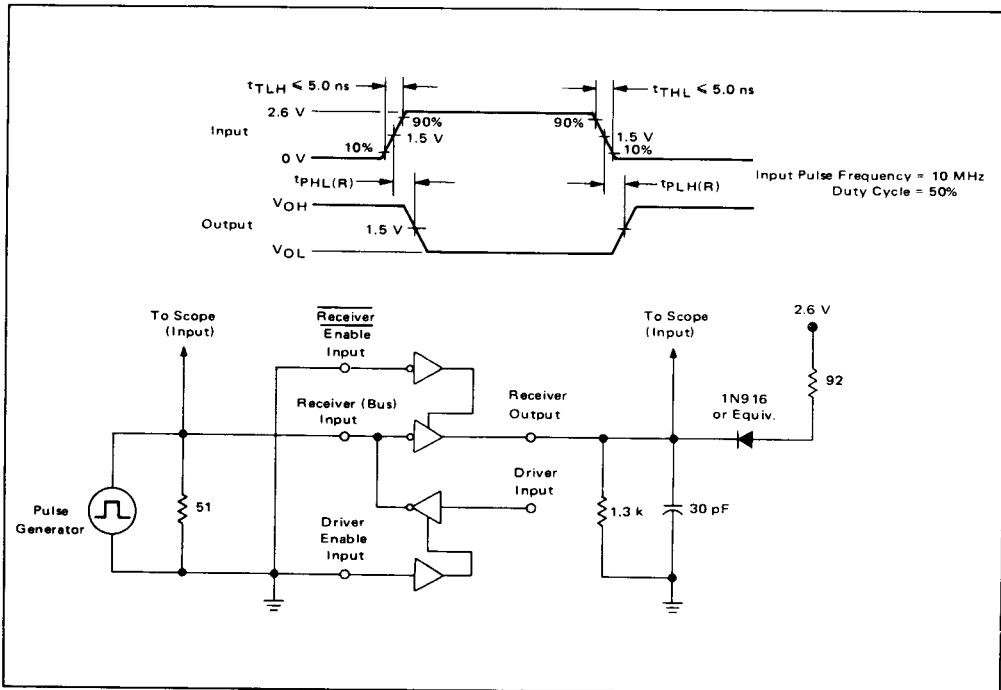
Note 1. Only one output may be short-circuited at a time.

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SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$)

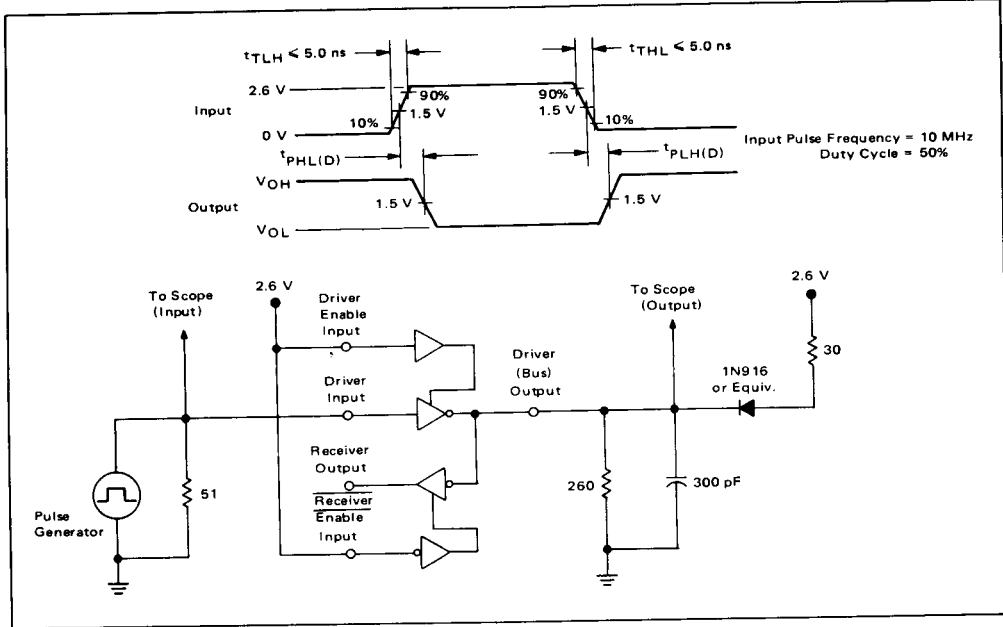
Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	—	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	—	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	—	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	—	14	ns
Propagation Delay Time from Receiver Enable Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	—	15	ns
Propagation Delay Time from Receiver Enable Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	—	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	—	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	—	25	ns

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$



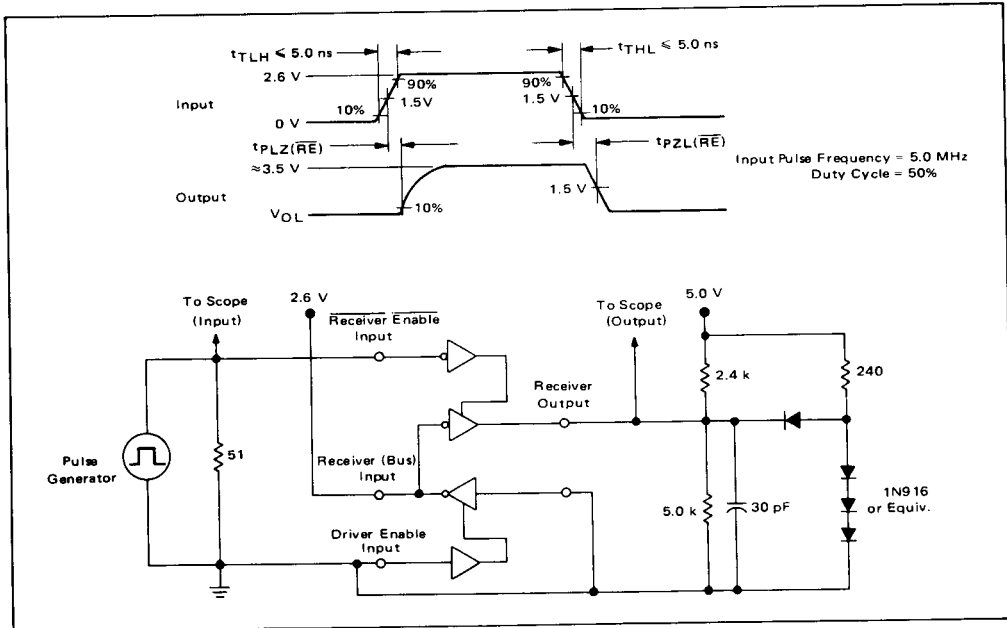
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FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PLH(D)}$



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FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{pZL(RE)}$



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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PLZ(IE)}$

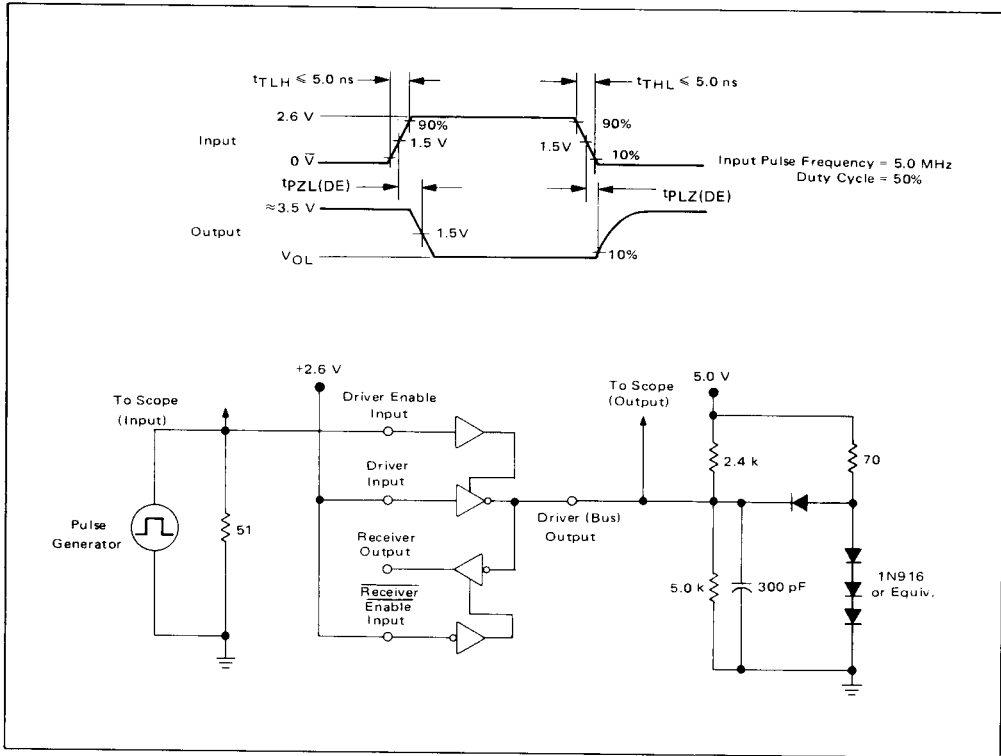


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS

