Technical Summary

Token-Passing Bus Controller (TBC)

The Motorola MC68824 Token Bus Controller (TBC) is a silicon integrated circuit which implements the Media Access Control (MAC) function for an IEEE 802.4 LAN station and the receiver portion for IEEE 802.2 Logical Link Control (LLC) type 3 as well as providing support for LLC type 1 and type 2 (see Figure 1). IEEE 802.4 defines the physical and MAC portion of the data link layer of the Manufacturing Automation Protocol (MAP) specification. The LLC functions implemented on chip are those associated with real time applications, namely "Acknowledged Connectionless Service" (type 3) as required in the Enhanced Performance Architecture (EPA) specified in Manufacturing Automation Protocol (MAP) 3.0.

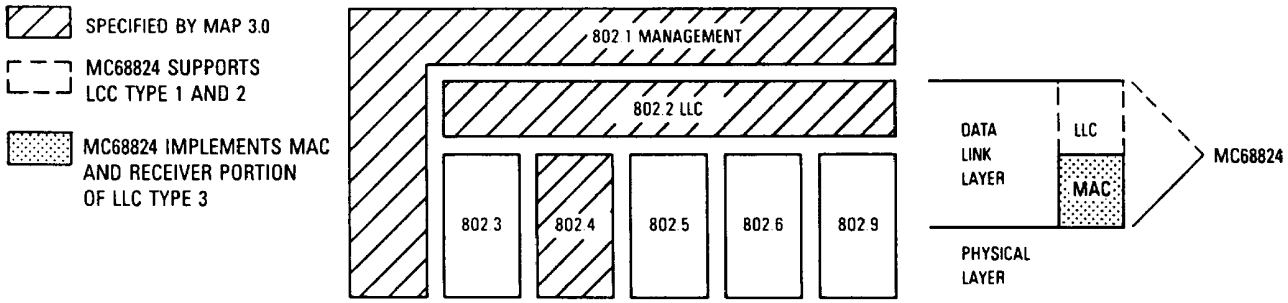

Figure 1. IEEE Standard Model

The major features of the MC68824 are:

- Implementation of the MAC Portion of the IEEE 802.4 Standard
- Implementation of the Receiver Portion of IEEE 802.2 LLC Acknowledged Connectionless Service (type 3)
- Support of IEEE 802.2 LLC Type 1 and Type 2
- Support of ANSI/ISA-72.01 PROWAY PLC Send Data with Acknowledge (SDA) and Request Data with Reply (RDR)
- MAC Options Suitable for Real Time Environments
  - — Four Receive and Four Transmit Queues Supporting Four Priority Levels
  - — Immediate Response Mechanism
- On-Chip Network Monitoring and Diagnostics
- Simple Interface to Higher Level Software by means of Powerful, Fully Linked Data Structure
- Options for Bridging Include: Hierarchical and IBM Defined Source Routing as well as Support for Flat Bridges
- Powerful Addressing; Group Address Recognition and Multidrop Capability
- Contains Several Modes to Increase Reliability and Flexibility Including:
  - — Reduced Data Structure Mode for Increased Performance
  - — Control Frame Preference for Increased Reliability
  - — Address Comparison Options for Increased Performance
  - — Bus Analyzer Mode to Enable Running the TBC as a Powerful Protocol Analyzer

— Continued —

Features (Continued)

- System Clock Rate up to 16.67 MHz
- Serial Data Rates from 10 Kbits/Second to 12.5 Mbits/Second
- IEEE 802.4 Recommended Serial Interface Supporting Various Physical Layers
- Highly Integrated M68000 Family Bus Master/Slave Interface
  - — Four Channel DMA for Transfer of Data Frames to and from Memory
    - – 40-Byte FIFO to Efficiently Support High Data Rate
    - – 32-Bit Address Bus with Virtual Address Capabilities
- Simplified Interface to Other Processor Environments
  - — Byte Swapping Capability for Alternate Memory Structures
  - — 8- or 16-Bit Data Bus
- Low Power Consumption through 1.5 Micron HCMOS Fabrication

GENERAL DESCRIPTION

The TBC functions as an intelligent peripheral device to a microprocessor. An on-chip DMA transfers data frames to and from a buffer memory with minimal microprocessor interference required. A microcoded fully linked buffer management scheme queues frames during transmission and reception, and optimizes memory use. The TBC simplifies interfacing a microcomputer to a token bus network by providing the link layer services including: managing ordered access to the token bus medium, providing a means for admission and deletion of stations, and handling fault recovery. This allows the host to operate almost totally isolated from the task of ensuring error free transmission and reception of data.

The TBC can be used in a variety of machines in the factory from programmable controllers to large computers. Although token bus is especially well suited to the factory because of its deterministic characteristics, the TBC can be used in other networking applications such as office automation. The TBC provides the capability to swap the byte ordering of data to support alternate memory organizations. Additionally, the TBC is a full M68000 bus master, providing on-chip DMA capability for management of memory tables and frame buffers. Since the TBC bus interface is configurable, the TBC can handle both 8-bit and 16-bit data transfers. Figure 2 shows the TBC in a typical intelligent I/O processor system environment.

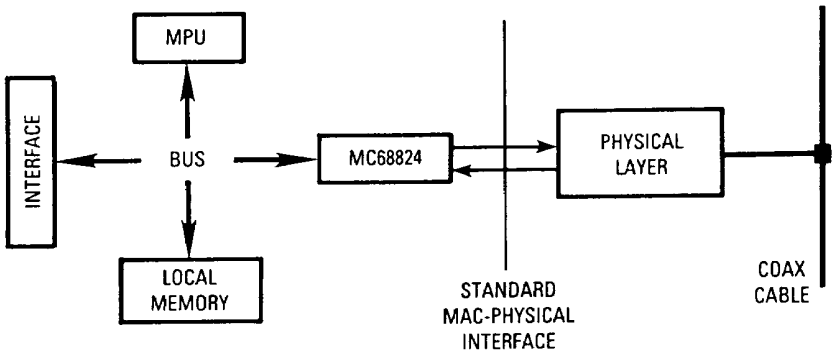

Figure 2. Token Bus LAN Node

Section 8 – Signal Processing