MOTOROLA
SEMICONDUCTOR
PRODUCT INFORMATION

Order this document
by M68IFDDI/D

MC68840/MC68836

Product Brief

FDDI Chip Set

Fiber distributed data interface (FDDI) is a 100-Mbps, fiber-optic-based, token-ring local area network (LAN) standard developed to accommodate rings of up to 1000 stations and a total ring length of 200 km. FDDI is an American National Standards Institute (ANSI) standard. This standard specifies the media access control (MAC) layer, the physical (PHY) layer, the physical medium dependent (PDM) function, and the station management (SMT) function.

Motorola's FDDI chip set supports both fiber-optic and twisted-pair wiring. It includes the MC68836 FDDI clock generator (FCG) and the MC68840 integrated FDDI (IFDDI). Figure 1 shows the relationship of the circuits in this chip set. Additionally, the MC68834 Cipher chip can be used to provide designers with an easy-to-implement solution for twisted-pair wiring.

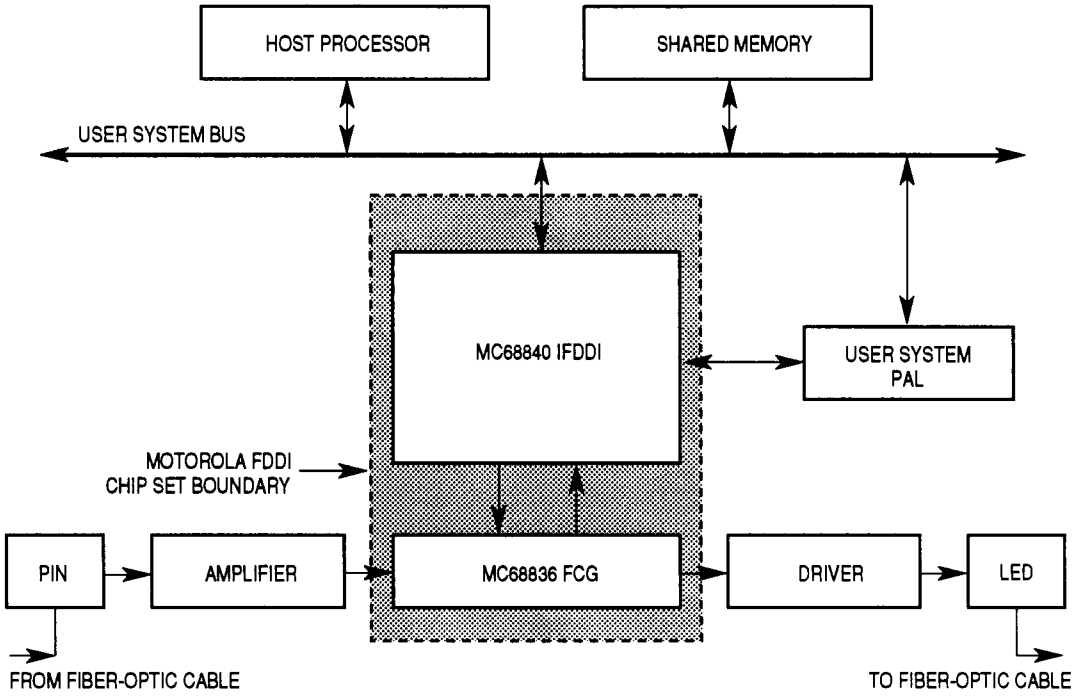

Figure 1. FDDI Chip Set

FDDI CLOCK GENERATOR (FCG)

The MC68836 FCG implements the lower portion of the physical layer (PHY) functions of the FDDI standard, including clock recovery, data recovery, and NRZI conversions. The FCG also performs a 5-bit parallel-to-serial conversion during transmission and a 5-bit serial-to-parallel conversion during reception. The FCG uses the 5-bit parallel interface to communicate with the MC68840 IFDDI device. The FCG connects directly to fiber-optic modules through differential drivers/receivers.

FCG FEATURES

The FCG's features are as follows:

- Full-Duplex Operation
- Recovers 125-MHz Clock from Incoming Serial NRZI Data Stream
- Re-clocks Incoming Serial NRZI Data Stream Using Recovered Clock
- Converts NRZI Data to NRZ
- Converts Received Serial Bit Stream to 5-Bit Parallel Form and 5-Bit Parallel Transmit Data to 1-Bit Serial Data
- Generates 25-MHz Receive Clock
- Generates 125-MHz Transmit Clock from either External 25-MHz Transmit Clock or On-Chip 25-MHz Crystal Oscillator
- Converts Transmit NRZ Data to NRZI Data
- Loopback and Transmitter-Off Modes
- TTL Outputs Three-State to Allow Board Testing

INTEGRATED FDDI (IFDDI)

The MC68840 IFDDI connects the FDDI media into the user's system. The IFDDI implements a system interface (FSI), CAMEL (MAC and ELM) functionality, and a 64-entry CAM on chip. It is designed so that external FDDI-specific memory is not required. On-chip memory is 8 Kbytes, which allows system bus latencies of more than 80 μs to be supported with all receive and all transmit FIFOs active. Approximately 250 μs may be supported with a single transmit and single receive FIFO active. The IFDDI provides functionality for local memory use, supports several bridging facilities, and has a hardware assist for critical SMT parameter processing. An additional feature is the ability to separate the clocks used in the system interface section from the clocks used by the FDDI media interface. A block diagram of the IFDDI is shown in Figure 2.

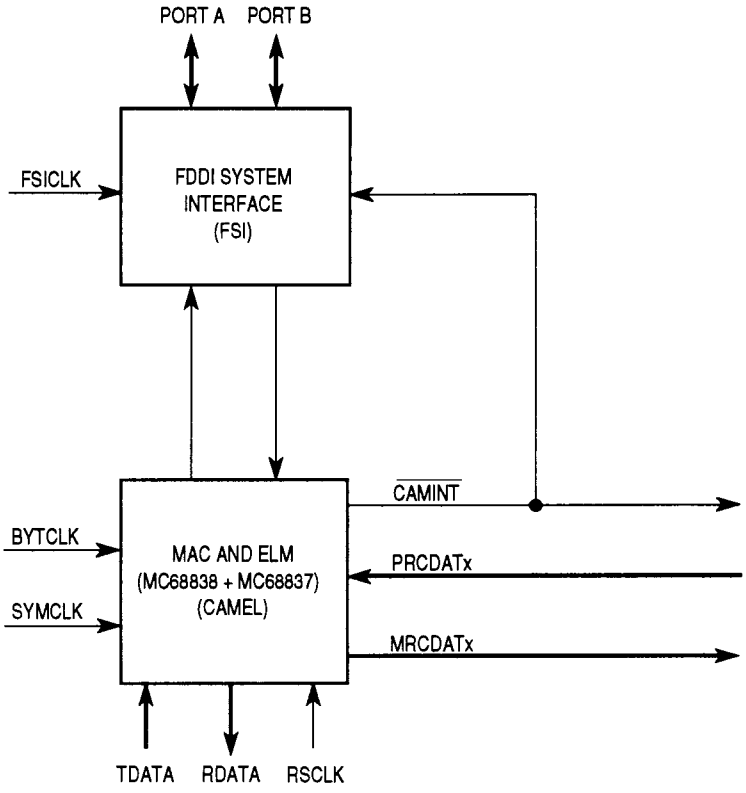

Figure 2. IFDDI Block Diagram

IFDDI FEATURES

The IFDDI consists of the FSI, CAMEL (MAC and ELM) blocks, and a 64-entry CAM.

The FDDI system interface (FSI) block provides the following features:

- Supports up to a 50-MHz Two-Clock Processor Access Cycle Time or 25-MHz System Bus Access Cycle Time (40-ns Cycle Time) in Normal Mode, with Higher Performance in Additional Modes
- Easily Connects to Any Bus Including Burst, High-Speed Processors, Little- and Big-Endian Buses, and Multiplexed/Nonmultiplexed Address/Data Buses
- Programmable Partitioned 8-Kbyte Internal RAM for Temporary Data Storage
- Four Fixed-Priority Transmit Rings and Two Receive Rings Support Synchronous/Asynchronous Frames
- Receive Filtering by Frame Control Field
- Ring Memory Structure with Multiple Buffers per Frame
- Data Path Parity Generation and Checking
- Two Identical 32-Bit Ports Allowing Multiple Configurations Including 64-Bit Operations
- Port to Port DMA Capability
- On-Chip SMT Timer
- JTAG Functionality

The CAMEL core provides the following features:

- Completely Implements ANSI FDDI PHY and MAC Standards
- 4B/5B Encoding and Decoding, Elasticity Buffer, and Smoother Functions
- Hardware Assist for PCM State Machine Reduces Load on SMT Processing
- Line State Detector and Repeat Filter
- On-Chip LEM Detection and Counting
- Full-Duplex Operation
- Independent Receive and Transmit Data Paths and State Machines Can Simultaneously Generate and Check CRC
- Supports Several Bridging Facilities:
  — Can Reverse Bit Ordering on DA and SA
  — Supports Frame-Stripping Algorithm Based on Frame Counting and Void Frames
  — Allows Generating Frame CRC on a per-Frame Basis
  — Supports A and C Bit Handling for Transparent Bridging Mode
  — Supports Extended Address Recognition Timing for Address Recognition
- Supports Optional FDDI Standard Capabilities Such As:
  — Transmission and Reception of Additional Frame Status Indicators
  — Restricted Tokens
  — Synchronous Frames
- Built-In Self-Test

IFDDI SIGNALS

The IFDDI signals are shown in Figure 3.

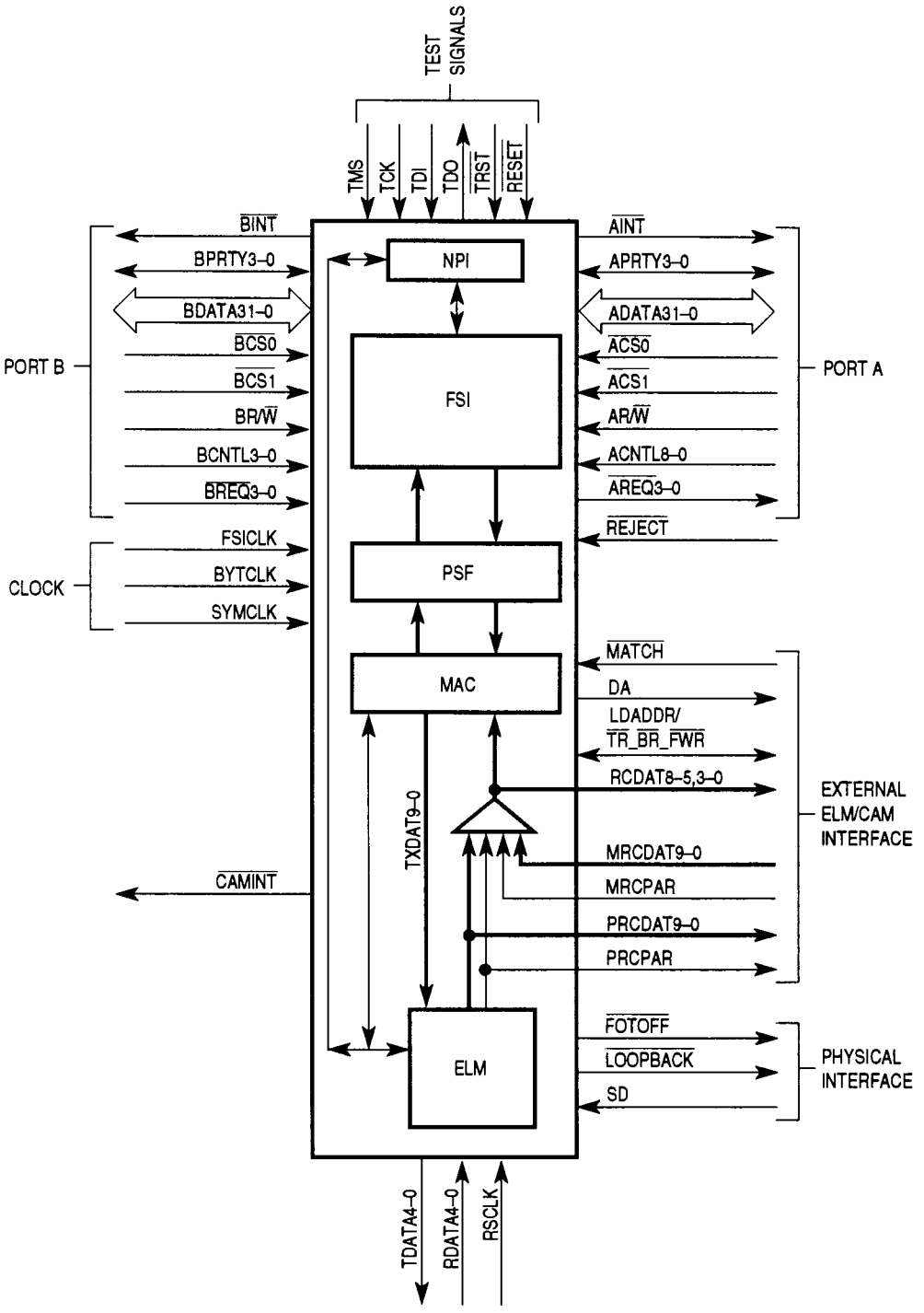

Figure 3. IFDDI Signals

The following table identifies the packages and operating frequencies available for the MC68840.

MC68840 Package/Frequency Availability

Package	Frequency, 25 MHz
Pin Grid Array (RC)	✓
Ceramic Surface Mount (FE)	✓

The documents listed in the following table contain detailed information on the MC68840. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Title	Order Number	Contents
MC68840 User's Manual	MC68840UM/AD	Detailed Information for Design
MC68836 User's Manual	MC68836UM/AD	Detailed Information for Design

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MOTOROLA
1ATX31357-0 PRINTED IN USA 5/93 IMPERIAL LITHO 91820 18,000 MPU YGABBA
M68IFDDI/D