SECTION 11
ELECTRICAL AND THERMAL CHARACTERISTICS

11.1 JTAG ELECTRICAL CHARACTERISTICS

The following paragraphs provide information on JTAG electrical and timing specifications. This section is subject to change. For the most recent specifications, contact a Motorola sales office or complete the registration card at the beginning of this manual.

JTAG DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot	—	—	0.8	V
TCK Input Leakage Current @ 0.5–2.4 V	I_{in}	20	20	µA
TDO Hi-Z (Off-State) Leakage Current @ 0.5–2.4 V	I_{TST}	20	20	µA
Signal Low Input Current, V_{IL} = 0.8 V TMS, TDI, $\overline{TRST}$	I_L	–1.1	–0.18	mA
Signal High Input Current, V_{IH} = 2.0 V TMS, TDI, TRST	I_H	–0.94	–0.16	mA
TDO Output High Voltage	V_{OH}	2.4	—	V
TDO Output Low Voltage	V_{OL}	—	0.5	V
Capacitance*, V_{in} = 0 V, f = 1 MHz	C_{in}	—	25	pF

*Capacitance is periodically sampled rather than 100% tested.

JTAG Timing Specifications (All Operating Frequencies)

Num	Characteristic	Min	Max	Unit
	TCK Frequency of Operation	0	10	MHz
1	TCK Cycle Time	100	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	40	—	ns
3	TCK Rise and Fall Times	0	10	ns
4	$\overline{\text{TRST}}$ Setup Time to TCK Falling Edge	40	—	ns
5	$\overline{\text{TRST}}$ Assert Time	100	—	ns
6	Boundary Scan Input Data Setup Time	50	—	ns
7	Boundary Scan Input Data Hold Time	50	—	ns
8	TCK to Output Data Valid	0	50	ns
9	TCK to Output High Impedance	0	50	ns
10	TMS, TDI Data Setup Time	20	—	ns
11	TMS, TDI Data Hold Time	5	—	ns
12	TCK to TDO Data Valid	0	20	ns
13	TCK to TDO High Impedance	0	20	ns

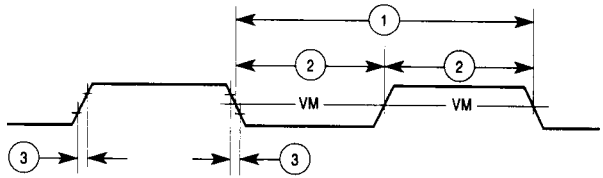


Figure 11-1. Clock Input Timing Diagram

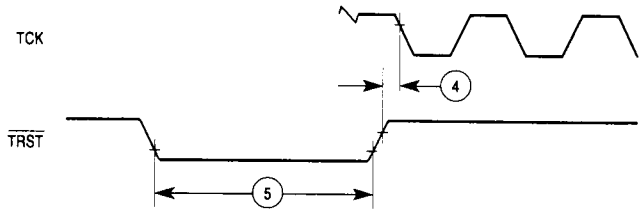


Figure 11-2. $\overline{\text{TRST}}$ Timing Diagram

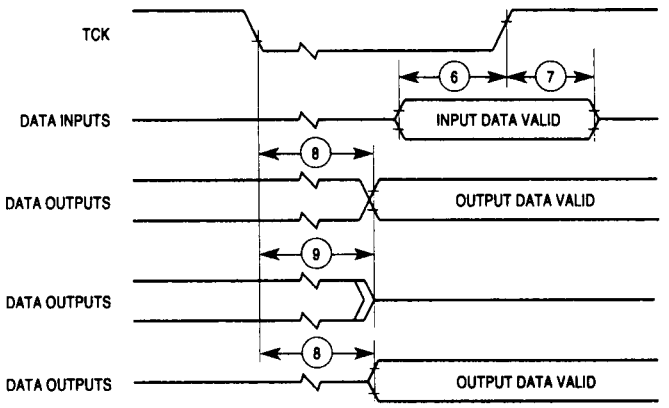


Figure 11-3. Boundary Scan Timing Diagram

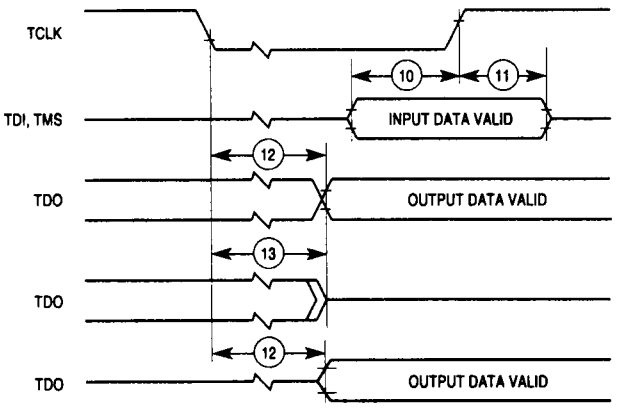


Figure 11-4. Test Access Port Timing Diagram

11.2 MC68040 ELECTRICAL CHARACTERISTICS

The following paragraphs provide information on the maximum rating and thermal characteristics for the MC68040. This section is subject to change. For the most recent specifications, contact a Motorola sales office or complete the registration card at the beginning of this manual.

MC68040 Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
Input Voltage	V_{in}	–0.5 to +7.0	V
Maximum Operating Junction Temperature	T_J	110	°C
Minimum Operating Ambient Temperature	T_A	0	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

MC68040 Thermal Characteristics—PGA Package

Characteristic	Symbol	Value	Rating
Thermal Resistance, Junction to Case	θ_{JC}	3	°C/W

MC68040 DC Electrical Specifications (V_{CC} = 5.0 Vdc ±5 %)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot	—	—	0.8	V
Input Leakage Current @ 0.5/2.4 V $\overline{AVEC}$, BCLK, $\overline{BG}$, $\overline{CDIS}$, $\overline{MDIS}$, $\overline{IPLx}$, PCLK, $\overline{RSTI}$, SCx, $\overline{TBI}$, TLNx, $\overline{TCI}$, TCK, $\overline{TEA}$	I_{in}	20	20	µA
Hi-Z (Off-State) Leakage Current @ 0.5/2.4 V An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, $\overline{TA}$, TDO, $\overline{TIP}$, TMx, TLNx, $\overline{TS}$, TTx, UPAx	I_{TSI}	20	20	µA
Signal Low Input Current, V_{IL} = 0.8 V TMS, TDI, $\overline{TRST}$	I_{IL}	–1.1	–0.18	mA
Signal High Input Current, V_{IH} = 2.0 V TMS, TDI, $\overline{TRST}$	I_{IH}	–0.94	–0.16	mA
Output High Voltage, I_{OH} = 5 mA (Small Buffer Mode)	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 5 mA (Small Buffer Mode)	V_{OL}	—	0.5	V
Output High Voltage, I_{OH} = 55 mA (Large Buffer Mode)	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 55 mA (Large Buffer Mode)	V_{OL}	—	0.5	V
Capacitance*, V_{in} = 0 V, f = 1 MHz	C_{in}	—	25	pF

*Capacitance is periodically sampled rather than 100% tested.

MC68040 Power Dissipation

Buffer Mode	25 MHz	33 MHz	40 MHz (Preliminary)
Worst Case (V_{CC} = 5.25 V , T_A = 0°C)			
Small Unterminated, I_{OL} = I_{OH} = 5 mA	6.3 W	7.7 W	8.4 W
Large Unterminated, I_{OL} = I_{OH} = 5 mA	6.6 W	8.0 W	8.7 W
Large Terminated, 50 Ω, 2.5 V, I_{OL} = I_{OH} = 55 mA	8.0 W	9.5 W	10.2 W
Typical Values (V_{CC} = 5 V, T_J = 90°C)*			
Small	4.3 W	5.4 W	5.9 W
Large Unterminated	4.6 W	5.7 W	6.2 W
Large Terminated, 50 Ω, 2.5 V	5.8 W	6.9 W	7.4 W

*This information is for system reliability purposes.

MC68040 Clock AC Timing Specifications (see Figure 11-5)

These specifications are for 25, 33, and 40 MHz; the 40 MHz specifications are preliminary.

Num	Characteristic	25 MHz		33 MHz		40 MHz (Preliminary)		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation	16.67	25	16.67	33	20	40	MHz
1	PCLK Cycle Time	20	30	15	30	12.5	25	ns
2	PCLK Rise Time	—	1.7	—	1.7	—	1.5	ns
3	PCLK Fall Time	—	1.6	—	1.6	—	1.5	ns
4	PCLK Duty Cycle Measured at 1.5 V	47.50	52.50	46.67	53.33	46.00	54.00	%
4a*	PCLK Pulse Width High Measured at 1.5 V	9.50	10.50	7	8	5.75	6.75	ns
4b*	PCLK Pulse Width Low Measured at 1.5 V	9.50	10.50	7	8	5.75	6.75	ns
5	BCLK Cycle Time	40	60	30	60	25	50	ns
6,7	BCLK Rise and Fall Time	—	4	—	3	—	3	ns
8	BCLK Duty Cycle Measured at 1.5 V	40	60	40	60	40	60	%
8a*	BCLK Pulse Width High Measured at 1.5 V	16	24	12	18	10	15	ns
8b*	BCLK Pulse Width Low Measured at 1.5 V	16	24	12	18	10	15	ns
9	PCLK, BCLK Frequency Stability	—	1000	—	1000	—	1000	ppm
10	PCLK to BCLK Skew	—	9	—	n/a	—	n/a	ns

*Specification value at maximum frequency of operation.

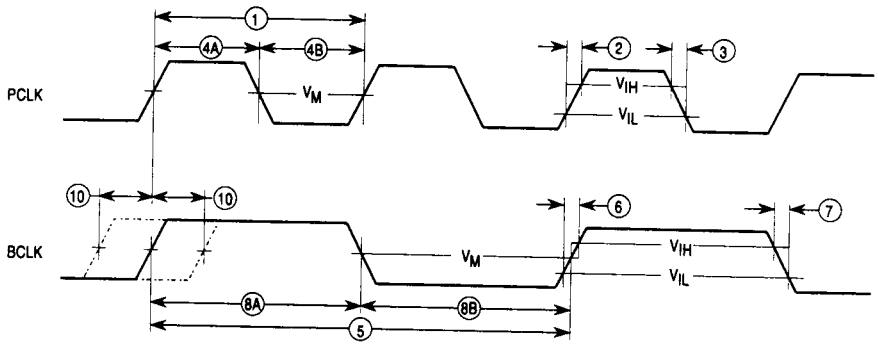


Figure 11-5. Clock Input Timing Diagram

MC68040 Output AC Timing Specifications (See Figures 11-6–11-11)

These specifications are for 25, 33, and 40 MHz; the 40 MHz specifications are preliminary.

Num	Characteristic	25 MHz				33 MHz				40 Mhz (Preliminary)				Unit
		Large[1]		Small[2]		Large[1]		Small[2]		Large[1]		Small[2]		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
11[3]	BCLK to Address CIOUT, LOCK, LOCKE, R/W, SIZx, TLN, TMx, TTx, UPAx Valid	9	21	9	30	6.50	18	6.50	25	5.25	16	5.25	24	ns
12	BCLK to Output Invalid (Output Hold)	9	—	9	—	6.50	—	6.50	—	5.25	—	5.25	—	ns
13	BCLK to TS Valid	9	21	9	30	6.50	18	6.50	25	5.25	16	5.25	24	ns
14	BCLK to TIP Valid	9	21	9	30	6.50	18	6.50	25	5.25	17	5.25	24	ns
18[4]	BCLK to Data Out Valid	9	23	9	32	6.50	20	6.50	27	5.25	18	5.25	26	ns
19[4]	BCLK to Data Out Invalid (Output Hold)	9	—	9	—	6.50	—	6.50	—	5.25	—	5.25	—	ns
20[3,4]	BCLK to Output Low Impedance	9	—	9	—	6.50	—	6.50	—	5.25	—	5.25	—	ns
21[5]	BCLK to Data-Out High Impedance	9	20	9	20	6.50	17	6.50	17	5.25	16	5.25	16	ns
26[3]	BCLK to Multiplexed Address Valid	19	31	19	40	14	26	14	33	13	25	13	32	ns
27[3,5]	BCLK to Multiplexed Address Driven	19	—	19	—	14	—	14	—	13	—	13	—	ns
28[3,4,5]	BCLK to Multiplexed Address High Impedance	9	18	9	18	6.50	15	6.50	15	5.25	14	5.25	14	ns
29[4,5]	BCLK to Multiplexed Data Driven	19	—	19	—	14	20	14	20	13	19	13	19	ns
30[4]	BCLK to Multiplexed Data Valid	19	33	19	42	14	28	14	35	13	27	13	34	ns
38[3]	BCLK to Address, CIOUT, LOCK, LOCKE, R/W, SIZx, TS, TLNx, TMx, TTx, UPAx High Impedance	9	18	9	18	6.50	15	6.50	15	5.25	14	5.25	14	ns
39	BCLK to BB, TA, TIP High Impedance	19	28	19	28	14	23	14	23	11.5	22	11.5	22	ns
40	BCLK to BR, BB Valid	9	21	9	30	6.50	18	6.50	25	5.25	16	5.25	24	ns
43	BCLK to MI Valid	9	21	9	30	6.50	18	6.50	25	5.25	17	5.25	24	ns
48	BCLK to TA Valid	9	21	9	30	6.50	18	6.50	25	5.25	17	5.25	24	ns
50	BCLK to IPEND, PSTx, RSTO Valid	9	21	9	30	6.50	18	6.50	25	5.25	17	5.25	24	ns

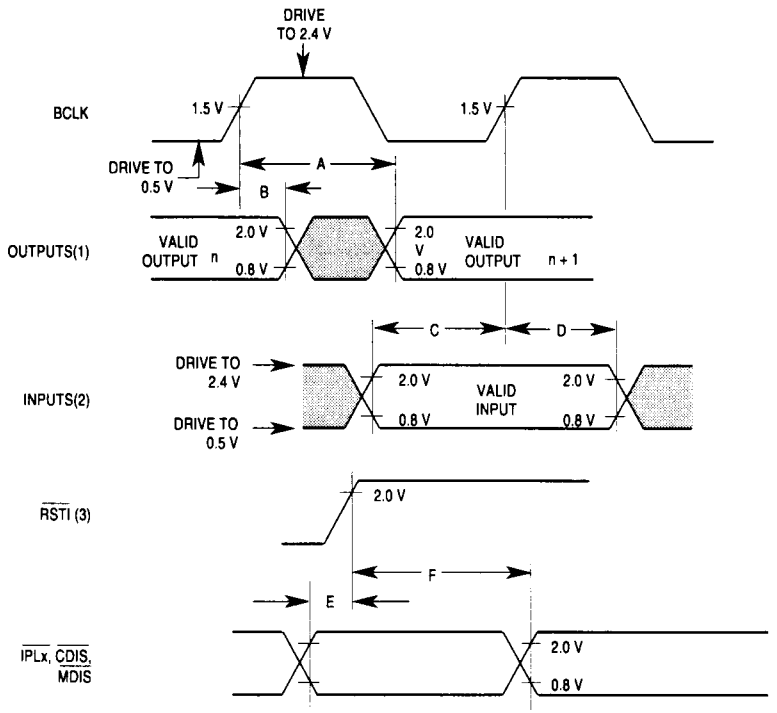
NOTES:

1. Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50 Ω transmission line with a length characterized by a 2.5-ns one-way propagation delay, terminated through 50 Ω to 2.5 V. Large buffer output impedance is 4–12 Ω, resulting in incident wave switching for this environment. All large buffer outputs must be terminated to guarantee operation.
2. Small buffer timing is specified driving an unterminated 30 Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30 Ω; the small buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
3. Timing specifications 11, 20, and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27, and 28 should be used when the multiplexed bus mode of operation is enabled.
4. Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.
5. Timing specifications 21, 27, 28, and 29 are measured from BCLK edges. By design, the MC68040 cannot drive address and data simultaneously during multiplexed operations.

MC68040 Input AC Timing Specifications (see Figures 11-8–11-11)

These specifications are for 25, 33, and 40 MHz; the 40 MHz specifications are preliminary.

Num	Characteristic	25 MHz		33 MHz		40 MHz (Preliminary)		Unit
		Min	Max	Min	Max	Min.	Max.	
15	Data-In Valid to BCLK (Setup)	5	—	4	—	3	—	ns
16	BCLK to Data-In Invalid (Hold)	4	—	4	—	3	—	ns
17	BCLK to Data-In High Impedance (Read Followed by Write)	—	49	—	36.5	—	30.25	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	10	—	10	—	8	—	ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	10	—	10	—	9	—	ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	10	—	10	—	9	—	ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	11	—	10	—	9	—	ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2	—	2	—	2	—	ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	5	—	5	—	5	—	ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2	—	2	—	2	—	ns
31	DLE Width High	8	—	8	—	8	—	ns
32	Data-In Valid to DLE (Setup)	2	—	2	—	2	—	ns
33	DLE to Data-In Invalid (Hold)	8	—	8	—	8	—	ns
34	BCLK to DLE Hold	3	—	3	—	3	—	ns
35	DLE High to BCLK	16	—	12	—	12	—	ns
36	Data-In Valid to BCLK (DLE Mode Setup)	5	—	5	—	5	—	ns
37	BCLK to Data-In Invalid (DLE Mode Hold)	4	—	4	—	4	—	ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	7	—	7	—	7	—	ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	8	—	7	—	7	—	ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	10	—	8	—	8	—	ns
41d	$\overline{IPLx}$ Valid to BCLK (Setup)	4	—	3	—	3	—	ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLx}$, $\overline{MDIS}$ Invalid (Hold)	2	—	2	—	2	—	ns
44a	Address Valid to BCLK (Setup)	8	—	7	—	7	—	ns
44b	SIZx Valid to BCLK (Setup)	12	—	8	—	8	—	ns
44c	TTx Valid to BCLK (Setup)	6	—	8.5	—	8.5	—	ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	6	—	5	—	5	—	ns
44e	SCx Valid to BCLK (Setup)	10	—	11	—	8	—	ns
45	BCLK to Address,SIZx, TTx, R/$\overline{W}$, SCx Invalid (Hold)	2	—	2	—	2	—	ns
46	$\overline{TS}$ Valid to BCLK (Setup)	5	—	9	—	7	—	ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2	—	2	—	2	—	ns
49	BCLK to $\overline{BB}$ High Impedance (MC68040 Assumes Bus Mastership)	—	9	—	9	—	9	ns
51	$\overline{RSTI}$ Valid to BCLK	5	—	4	—	4	—	ns
52	BCLK to $\overline{RSTI}$ Invalid	2	—	2	—	2	—	ns
53	Mode Select Setup to $\overline{RSTI}$ Negated	20	—	20	—	20	—	ns
54	$\overline{RSTI}$ Negated to Mode Selects Invalid	2	—	2	—	2	—	ns



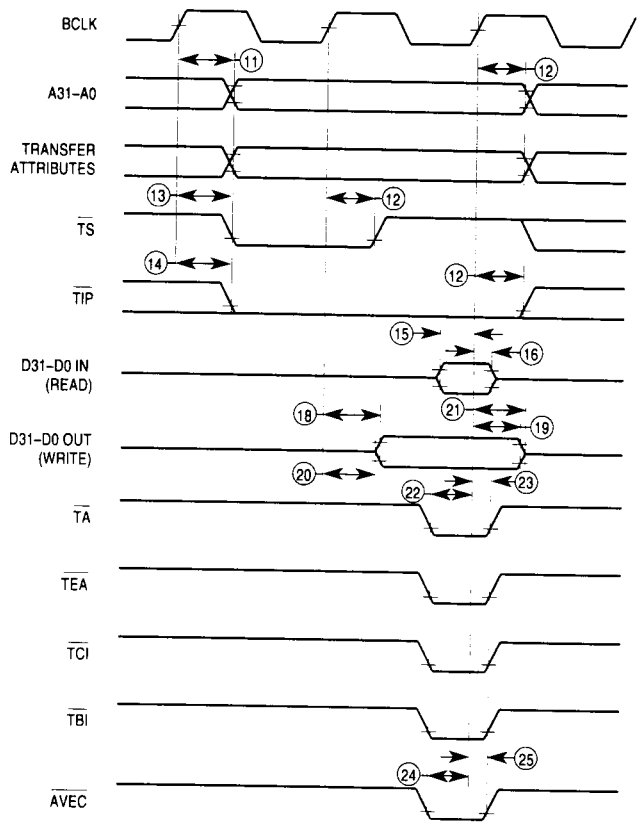
NOTES:

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
3. This timing is applicable to all parameters specified relative to the negation of the RSTI signal.

LEGEND:

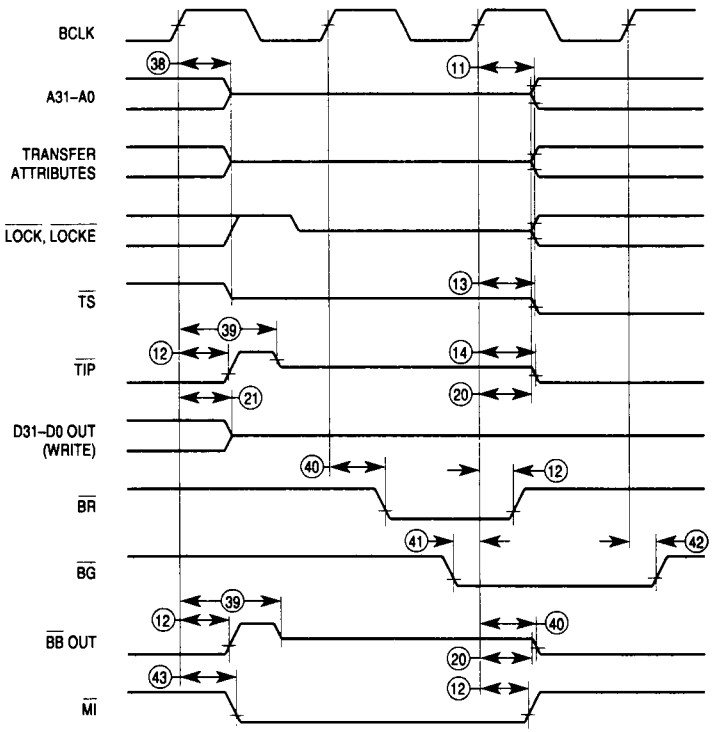
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Mode select setup time to RSTI negated.
F. Mode select hold time from RSTI negated.

Figure 11-6. Drive Levels and Test Points for AC Specifications



NOTE: Transfer Attribute Signals = UPAx, SIZx, TTx, TMx, TLNx, R/W, LOCK, LOCKE, CIOUT

Figure 11-7. Read/Write Timing



NOTE: Transfer Attribute Signals = UPAx, SIZx, TTx, TMx, TLNx, R/W, CIOUT

Figure 11-8. Bus Arbitration Timing

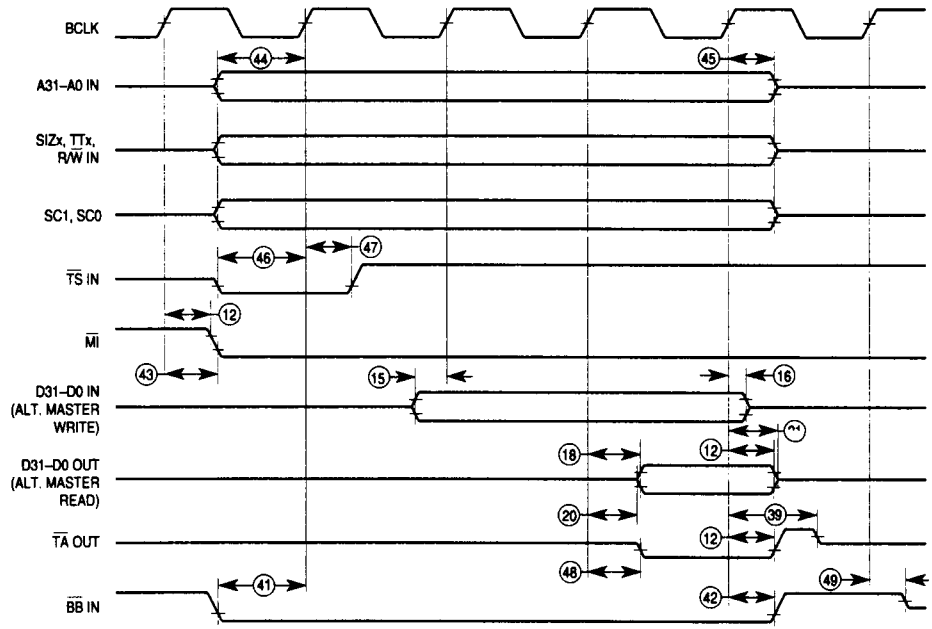


Figure 11-9. Snoop Hit Timing

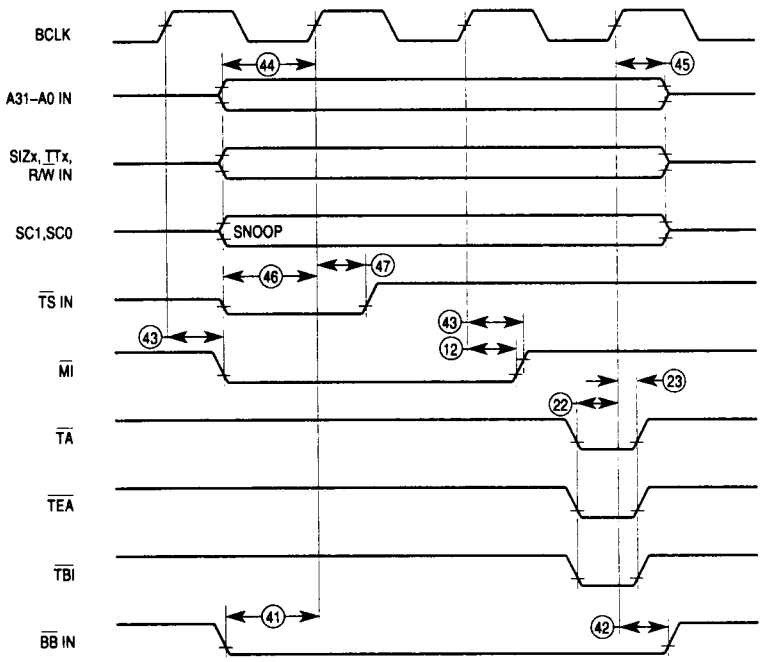


Figure 11-10. Snoop Miss Timing

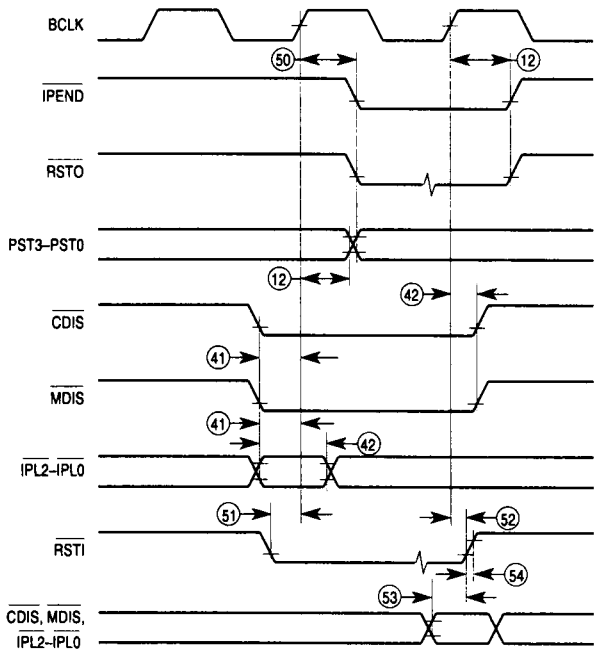


Figure 11-11. Other Signal Timing

11.3 MC68LC040 ELECTRICAL CHARACTERISTICS

The following paragraphs provide information on the maximum rating and thermal characteristics for the MC68LC040. This section is subject to change. For the most recent specifications, contact a Motorola sales office or complete the registration card at the beginning of this manual.

MC68LC040 Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
Input Voltage	V_{in}	–0.5 to +7.0	V
Maximum Operating Junction Temperature	T_J	110	°C
Minimum Operating Ambient Temperature	T_A	0	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

MC68LC040 Thermal Characteristics PGA Package

Characteristic	Symbol	Value	Rating
Thermal Resistance, Junction to Case	θ_{JC}	3	°C/W

MC68LC040 DC Electrical Specifications (V_{CC} = 5.0 Vdc ±5 %)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot	—	—	0.8	V
Input Leakage Current @ 0.5–2.4 V $\overline{AVEC}$, BCLK, $\overline{BG}$, $\overline{CDIS}$, $\overline{MDIS}$, $\overline{IPLx}$, PCLK, $\overline{RSTI}$, SCx, $\overline{TBI}$, TLNx, $\overline{TCI}$, TCK, $\overline{TEA}$	I_{in}	20	20	µA
Hi-Z (Off-State) Leakage Current @ 0.5–2.4 V An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, $\overline{TA}$, TDO, $\overline{TIP}$, TMx, TLNx, $\overline{TS}$, TTx, UPAx	I_{TSI}	20	20	µA
Signal Low Input Current, V_{IL} = 0.8 V TMS, TDI, $\overline{TRST}$	I_{IL}	–1.1	–0.18	mA
Signal High Input Current, V_{IH} = 2.0 V TMS, TDI, $\overline{TRST}$	I_{IH}	–0.94	–0.16	mA
Output High Voltage, I_{OH} = 5 mA	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 5 mA	V_{OL}	—	0.5	V
Capacitance*, V_{in} = 0 V, f = 1 MHz	C_{in}	—	25	pF

*Capacitance is periodically sampled rather than 100% tested.

MC68LC040 Power Dissipation

Frequency	Watts
Maximum Values (V_{CC} = 5.25 V, T_A = 0°C)	
20 MHz	4.0
25 MHz	5.0
33 MHz	6.3
Typical Values (V_{CC} = 5 V, T_A = 25°C)*	
20 MHz	3.0
25 MHz	3.8
33 MHz	4.8

*This information is for system reliability purposes.

MC68LC040 Clock AC Timing Specifications (see Figure 11-12)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation	16.67	20	16.67	25	16.67	33	MHz
1	PCLK Cycle Time	25	30	20	30	15	30	ns
2	PCLK Rise Time	—	1.7	—	1.7	—	1.7	ns
3	PCLK Fall Time	—	1.6	—	1.6	—	1.6	ns
4	PCLK Duty Cycle Measured at 1.5 V	48	52	47.5	52.5	46.67	53.33	%
4a*	PCLK Pulse Width High Measured at 1.5 V	12	13	9.5	10.5	7	8	ns
4b*	PCLK Pulse Width Low Measured at 1.5 V	12	13	9.5	10.5	7	8	ns
5	BCLK Cycle Time	50	60	40	60	30	60	ns
6,7	BCLK Rise and Fall Time	—	4	—	4	—	3	ns
8	BCLK Duty Cycle Measured at 1.5 V	40	60	40	60	40	60	%
8a*	BCLK Pulse Width High Measured at 1.5 V	20	30	16	24	12	18	ns
8b*	BCLK Pulse Width Low Measured at 1.5 V	20	30	16	24	12	18	ns
9	PCLK, BCLK Frequency Stability	—	1000	—	1000	—	1000	ppm
10	PCLK to BCLK Skew	—	9	—	9	—	n/a	ns

*Specification value at maximum frequency of operation.

MC680LC40 Output AC Timing Specifications (see Figures 11-13*–11-17)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
11	BCLK to Address, $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, PSTx, R/$\overline{W}$, SIZx, TLNx,TMx, TTx, UPAx Valid	11.5	35	9	30	6.5	25	ns
12	BCLK to Output Invalid (Output Hold)	11.5	—	9	—	6.5	—	ns
13	BCLK to $\overline{TS}$ Valid	11.5	35	9	30	6.5	25	ns
14	BCLK to $\overline{TIP}$ Valid	11.5	35	9	30	6.5	25	ns
18	BCLK to Data-Out Valid	11.5	37	9	32	6.5	27	ns
19	BCLK to Data-Out Invalid (Output Hold)	11.5	—	9	—	6.5	—	ns
20	BCLK to Output Low Impedance	11.5	—	9	—	6.5	—	ns
21	BCLK to Data-Out High Impedance	11.5	25	9	20	6.5	17	ns
38	BCLK to Address, $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, $\overline{TS}$, TLNx, TMx, TTx, UPAx High Impedance	11.5	23	9	18	6.5	15	ns
39	BCLK to $\overline{BB}$, $\overline{TA}$, $\overline{TIP}$ High Impedance	23	33	19	28	14	25	ns
40	BCLK to $\overline{BR}$, $\overline{BB}$ Valid	11.5	35	9	30	6.5	23	ns
43	BCLK to $\overline{MI}$ Valid	11.5	35	9	30	6.5	25	ns
48	BCLK to $\overline{TA}$ Valid	11.5	35	9	30	6.5	25	ns
50	BCLK to $\overline{IPEND}$, PSTx, $\overline{RSTO}$ Valid	11.5	35	9	30	6.5	25	ns

* Output timing is specified for a valid signal measured at the pin. Timing is specified driving an unterminated 30-Ω transmission line with a length characterized by a 2.5-ns one-way propagation delay. Buffer output impedance is typically 30 Ω; the buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.

MC680LC40 Input AC Timing Specifications (See Figures 11-14–11-17)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
15	Data-In Valid to BCLK (Setup)	6	—	5	—	4	—	ns
16	BCLK to Data-In Invalid (Hold)	5	—	4	—	4	—	ns
17	BCLK to Data-In High Impedance (Read Followed by Write)	—	61	—	49	—	36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	14	—	11	—	10	—	ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	6	—	5	—	5	—	ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	8	—	7	—	7	—	ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	10	—	8	—	7	—	ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	12.5	—	10	—	8	—	ns
41d	$\overline{IPLx}$ Valid to BCLK (Setup)	5	—	4	—	3	—	ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{MDIS}$, $\overline{IPLx}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
44a	Address Valid to BCLK (Setup)	10	—	8	—	7	—	ns
44b	SIZx Valid to BCLK (Setup)	15	—	12	—	8	—	ns
44c	TTx Valid to BCLK (Setup)	7.5	—	6	—	8.5	—	ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	7.7	—	6	—	5	—	ns
44e	SCx Valid to BCLK (Setup)	12.5	—	10	—	11	—	ns
45	BCLK to Address SIZx, TTx, R/$\overline{W}$, SCx Invalid (Hold)	2.5	—	2	—	2	—	ns
46	$\overline{TS}$ Valid to BCLK (Setup)	6	—	5	—	9	—	ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
49	BCLK to $\overline{BB}$ High Impedance (MC68LC040 Assumes Bus Mastership)	—	11	—	9	—	9	ns
51	$\overline{RSTI}$ Valid to BCLK	6	—	5	—	4	—	ns
52	BCLK to $\overline{RSTI}$ Invalid	2.5	—	2	—	2	—	ns

11.4 MC68EC040 ELECTRICAL CHARACTERISTICS

The following paragraphs provide information on the maximum rating and thermal characteristics for the MC68EC040. This section is subject to change. For the most recent specifications, contact a Motorola sales office or complete the registration card at the beginning of this manual.

MC68EC040 Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
Input Voltage	V_{in}	–0.8 to +7.0	V
Maximum Operating Junction Temperature	T_J	110	°C
Minimum Operating Ambient Temperature	T_A	0	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

MC68EC040 Thermal Characteristics PGA Package

Characteristic	Symbol	Value	Rating
Thermal Resistance, Junction to Case	θ_{JC}	3	°C/W

MC68EC040 DC Electrical Specifications (V_{CC} = 5.0 Vdc ±5 %)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot	—	—	0.8	V
Input Leakage Current @ 0.5–2.4 V $\overline{AVEC}$, BCLK, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLx}$, PCLK, $\overline{RSTI}$, SCx, $\overline{TBI}$, TLNx, $\overline{TCI}$, TCK, $\overline{TEA}$	I_{in}	20	20	mA
Hi-Z (Off-State) Leakage Current @ 0.5–2.4 V An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, $\overline{TA}$, TDO, $\overline{TIP}$, TMx, TLNx, $\overline{TS}$, TTx, UPAx	I_{TSI}	20	20	mA
Signal Low Input Current, V_{IL} = 0.8 V TMS, TDI, $\overline{TRST}$	I_{IL}	–1.1	–0.18	mA
Signal High Input Current, V_{IH} = 2.0 V TMS, TDI, $\overline{TRST}$	I_{IH}	–0.94	–0.16	mA
Output High Voltage, I_{OH} = 5 mA	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 5 mA	V_{OL}	—	0.5	V
Capacitance*, V_{in} = 0 V, f = 1 MHz	C_{in}	—	25	pF

*Capacitance is periodically sampled rather than 100% tested.

MC68EC040 Power Dissipation

Frequency	Watts
Maximum Values (V_{CC} = 5.25 V, T_A = 0°C)	
20 MHz	4.0
25 MHz	5.0
33 MHz	6.3
Typical Values (V_{CC} = 5 V, T_A = 25°C)*	
20 MHz	3.0
25 MHz	3.8
33 MHz	4.8

*This information is for system reliability purposes.

MC68EC040 Clock AC Timing Specifications (see Figure 11-12)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation	16.67	20	16.67	25	16.67	33.3	MHz
1	PCLK Cycle Time	25	30	20	30	15	30	ns
2	PCLK Rise Time	—	1.7	—	1.7	—	1.7	ns
3	PCLK Fall Time	—	1.6	—	1.6	—	1.6	ns
4	PCLK Duty Cycle Measured at 1.5 V	48	52	47.5	52.5	46.67	53.33	%
4a*	PCLK Pulse Width High Measured at 1.5 V	12	13	9.5	10.5	7	8	ns
4b*	PCLK Pulse Width Low Measured at 1.5 V	12	13	9.5	10.5	7	8	ns
5	BCLK Cycle Time	50	60	40	60	30	60	ns
6,7	BCLK Rise and Fall Time	—	4	—	4	—	3	ns
8	BCLK Duty Cycle Measured at 1.5 V	40	60	40	60	40	60	%
8a*	BCLK Pulse Width High Measured at 1.5 V	20	30	16	24	12	18	ns
8b*	BCLK Pulse Width Low Measured at 1.5 V	20	30	16	24	12	18	ns
9	PCLK, BCLK Frequency Stability	—	1000	—	1000	—	1000	ppm
10	PCLK to BCLK Skew	—	9	—	9	—	n/a	ns

*Specification value at maximum frequency of operation.

MC68EC040 Output AC Timing Specifications (see Figures 11-13*–11-17)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
11	BCLK to Address $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, TLNx,TMx, TTx, UPAx Valid	11.5	35	9	30	6.5	25	ns
12	BCLK to Output Invalid (Output Hold)	11.5	—	9	—	6.5	—	ns
13	BCLK to $\overline{TS}$ Valid	11.5	35	9	30	6.5	25	ns
14	BCLK to $\overline{TIP}$ Valid	11.5	35	9	30	6.5	25	ns
18	BCLK to Data-Out Valid	11.5	37	9	32	6.5	27	ns
19	BCLK to Data-Out Invalid (Output Hold)	11.5	—	9	—	6.5	—	ns
20	BCLK to Output Low Impedance	11.5	—	9	—	6.5	—	ns
21	BCLK to Data-Out High Impedance	11.5	25	9	20	6.5	17	ns
38	BCLK to Address, $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZx, $\overline{TS}$, TLNx, TMx, TTx, UPAx High Impedance	11.5	23	9	18	6.5	15	ns
39	BCLK to $\overline{BB}$, $\overline{TA}$, $\overline{TIP}$ High Impedance	23	33	19	28	14	25	ns
40	BCLK to $\overline{BR}$, $\overline{BB}$ Valid	11.5	35	9	30	6.5	23	ns
43	BCLK to $\overline{MI}$ Valid	11.5	35	9	30	6.5	25	ns
48	BCLK to $\overline{TA}$ Valid	11.5	35	9	30	6.5	25	ns
50	BCLK to $\overline{IPEND}$, PSTx, $\overline{RSTO}$ Valid	11.5	35	9	30	6.5	25	ns

*Output timing is specified for a valid signal measured at the pin. Timing is specified driving an unterminated 30-Ω transmission line with a length characterized by a 2.5-ns one-way propagation delay. Buffer output impedance is typically 30 Ω; the buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.

MC68EC040 Input AC Timing Specifications (see Figures 11-14–11-17)

Num	Characteristic	20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
15	Data-In Valid to BCLK (Setup)	6	—	5	—	4	—	ns
16	BCLK to Data-In Invalid (Hold)	5	—	4	—	4	—	ns
17	BCLK to Data-In High Impedance (Read Followed by Write)	—	61	—	49	—	36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	12.5	—	10	—	10	—	ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	14	—	11	—	10	—	ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	6	—	5	—	5	—	ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	8	—	7	—	7	—	ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	10	—	8	—	7	—	ns
41c	$\overline{CDIS}$ Valid to BCLK (Setup)	12.5	—	10	—	8	—	ns
41d	$\overline{IPLx}$ Valid to BCLK (Setup)	5	—	4	—	3	—	ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLx}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
44a	Address Valid to BCLK (Setup)	10	—	8	—	7	—	ns
44b	SIZx Valid to BCLK (Setup)	15	—	12	—	8	—	ns
44c	TTx Valid to BCLK (Setup)	7.5	—	6	—	8.5	—	ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	7.7	—	6	—	5	—	ns
44e	SCx Valid to BCLK (Setup)	12.5	—	10	—	11	—	ns
45	BCLK to Address SIZx, TTx, R/$\overline{W}$, SCx Invalid (Hold)	2.5	—	2	—	2	—	ns
46	$\overline{TS}$ Valid to BCLK (Setup)	6	—	5	—	9	—	ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2.5	—	2	—	2	—	ns
49	BCLK to $\overline{BB}$ High Impedance (MC68EC040 Assumes Bus Mastership)	—	11	—	9	—	9	ns
51	$\overline{RSTI}$ Valid to BCLK	6	—	5	—	4	—	ns
52	BCLK to $\overline{RSTI}$ Invalid	2.5	—	2	—	2	—	ns

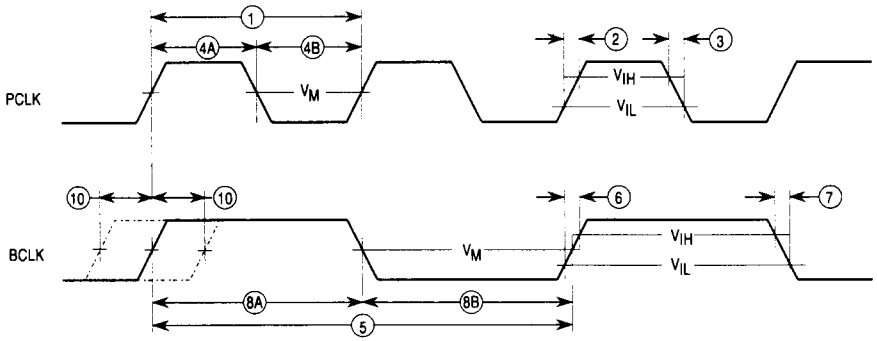
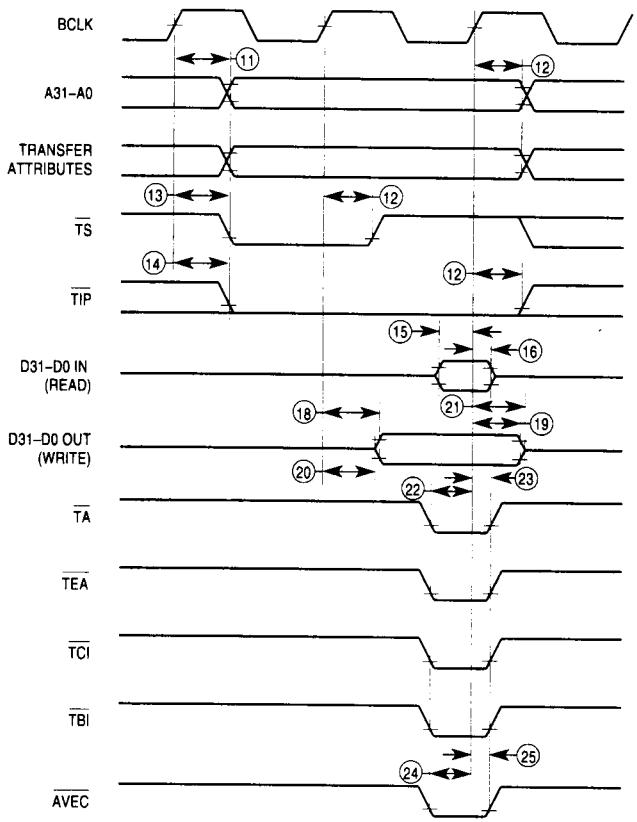
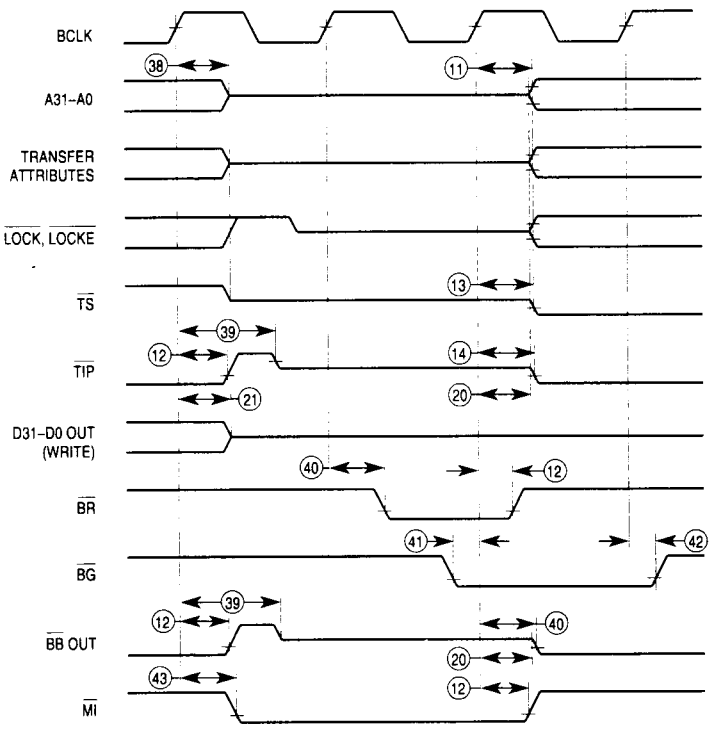


Figure 11-12. Clock Input Timing Diagram



NOTE: Transfer Attribute Signals = UPAx, SIZx, TTx, TMx, TLNx, R/W, LOCK, LOCKE, CIOUT

Figure 11-13. Read/Write Timing



NOTE: Transfer Attribute Signals = UPAx, SIZx, TTx, TMx, TLNx, R/W, CIOUT

Figure 11-14. Bus Arbitration Timing

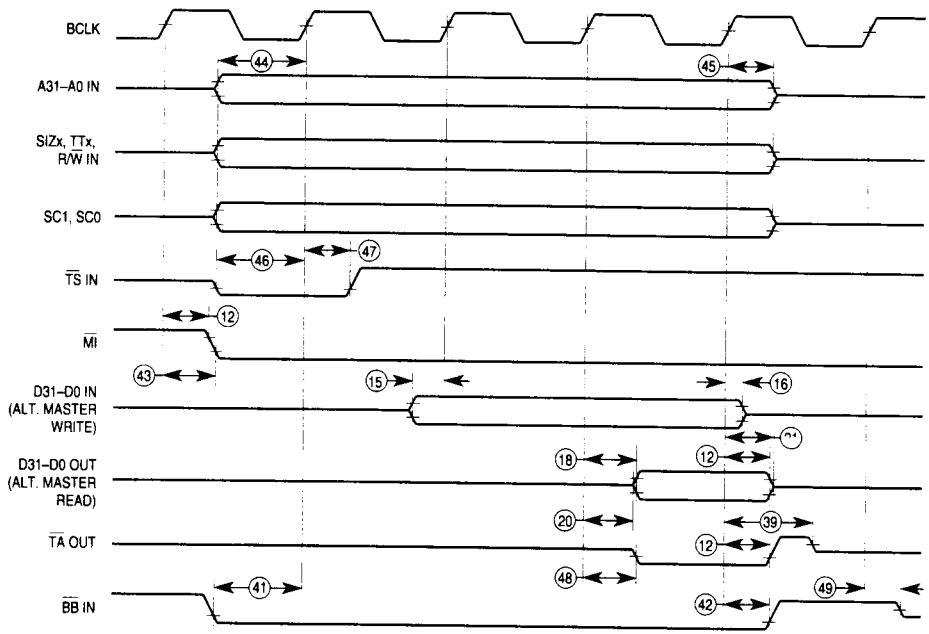


Figure 11-15. Snoop Hit Timing

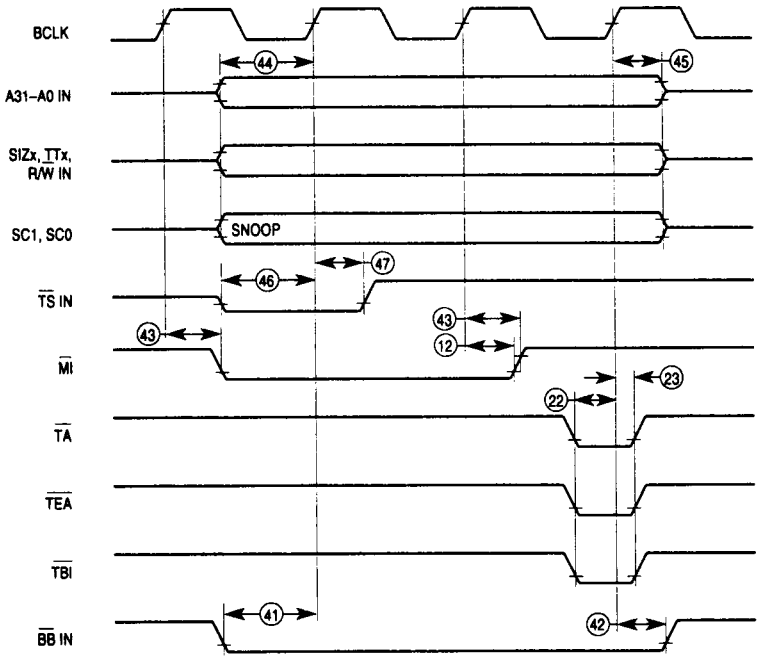


Figure 11-16. Snoop Miss Timing

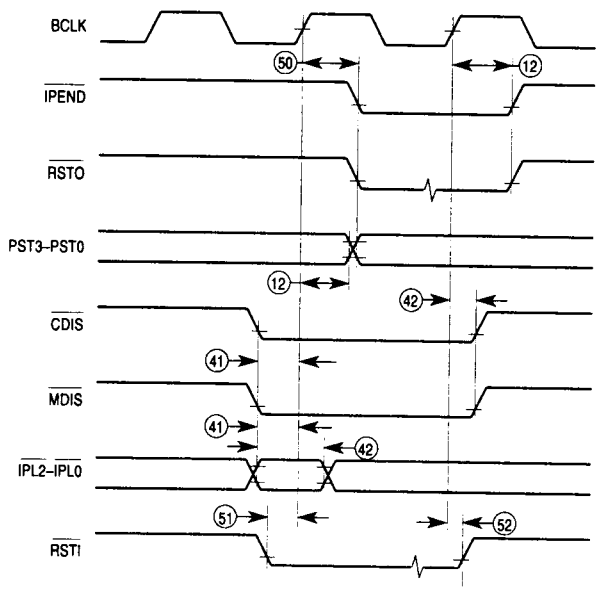


Figure 11-17. Other Signal Timing

11.5 MC68040 THERMAL DEVICE CHARACTERISTICS

The need to efficiently cool microprocessors is becoming more important as they become more complex and require more power. In the past, the M68000 family has been able to provide a 0–70°C ambient temperature part for speeds less than 40 MHz. However, the MC68040, MC68LC040, and MC68EC040 with a 50 MHz processor clock has a maximum power dissipation for a particular operating mode, a maximum junction temperature, and a thermal resistance from the die junction to the case. This provides a more accurate method of evaluating the environment, taking into consideration both the airflow and ambient temperature. This also gives the user information to design a cooling method that meets both thermal performance requirements and constraints of the board environment. This section discusses the device characteristics and several methods for thermal management as well as an example of one method for cooling the MC68040, MC68LC040, and MC68EC040. The MC68040, MC68LC040, and MC68EC040 contain inherent characteristics that should be considered when evaluating a method for cooling the device. The following paragraphs discuss these die/package and power considerations for each of these parts.

NOTE

All references to the MC68040 also include the MC68LC040 and MC68EC040. Note that the MC68LC040 and MC68EC040 only implement the small buffer mode.

11.5.1 MC68040 Die and Package

The MC68040 is in a cavity-down alumina-ceramic 179-pin PGA that has a worst case thermal resistance from junction to case of 3°C/W. The package differs from previous M68000 family PGA packages that are cavity-up. The cavity-down design allows the die to be attached to the top surface of the package, increasing the part's ability to dissipate heat through the package surface or an attached heat sink. The system designer needs to determine the specific dimensions and design of the particular heat sink, considering both thermal performance and size requirements.

11.5.2 MC68040 Power Considerations

The MC68040 has a maximum power rating, which varies depending on the combination of output buffer mode and operating frequency. Note that this section assumes large buffers terminated to 2.5 V. The large buffer output mode dissipates more power than the small, and higher frequencies of operation dissipate more power than the lower frequencies.

The MC68040 allows a combination of either large or small buffers on the outputs of the miscellaneous control signals, data bus, and address bus/transfer attribute pins. The large buffers offer quicker output times, allowing for an easier logic design. However, they do so by driving about 10 times as much current as the small buffers. The designer should consider whether the quicker timings present enough advantage to justify the additional consideration to the individual signal terminations, the die power consumption, and the required cooling for the device. Since the MC68040 can be powered up in one of many output buffer modes upon reset, the actual maximum power consumption for an MC68040

rated at a particular maximum operating frequency is dependent upon the power-up mode. Therefore, the MC68040 is rated at a maximum power dissipation for either the large or small buffers at a particular frequency. This allows for control of some of the thermal management upon reset. The following equation provides a rough method to calculate the maximum power consumption for a chosen output buffer mode:

$$P_D = P_{DSB} + (P_{DLB} - P_{DSB}) \times (PINS_{LB} + PINS_{CLB})$$

where:

P_D = Maximum Power Dissipation for Output Buffer Mode Selected
P_{DSB} = Maximum Power Dissipation for Small Buffer Mode (All Outputs)
P_{DLB} = Maximum Power Dissipation for Large Buffer Mode (All Outputs)
$PINS_{LB}$ = Number of Pins Large Buffer Mode
$PINS_{CLB}$ = Number of Pins Capable of the Large Buffer Mode

Table 11-1 lists the simplified relationship on the maximum power dissipation for eight possible configurations of output buffer modes.

Table 11-1. Maximum Power Dissipation for Output Buffer Mode Configurations

Output Configuration			Maximum Power Dissipation
Data Bus	Address Bus and Transfer Attributes	Control Signals	
Small*	Small	Small	P_{DSB}
Small	Small	Large	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 13\%$
Small	Large	Small	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 52\%$
Small	Large	Large	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 65\%$
Large	Small	Small	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 35\%$
Large	Small	Large	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 48\%$
Large	Large	Small	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 87\%$
Large	Large	Large	$P_{DSB} + (P_{DLB} - P_{DSB}) \times 100\%$

*The MC68LC040 and MC68EC040 only utilize this row of information.

To calculate the specific power dissipation of a design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large rather than the small buffer mode. Since the maximum operating junction temperature is specified as 110°C, the maximum case temperature (T_C) in °C can be obtained from the following equation:

$$T_C = T_J - P_D \times \theta_{JC}$$

where:

T_C = Maximum Case Temperature
T_J = Maximum Junction Temperature
P_D = Maximum Power Dissipation of the Device
θ_{JC} = Thermal Resistance between the Junction of the Die and the Case

In general, the ambient temperature (T_A) in °C is a function of the following equation:

$$T_A = T_J - P_D \times \theta_{JC} - P_D \times \theta_{CA}$$

The thermal resistance from case to outside ambient (θ_{CA}) is the only user-dependent parameter once a buffer output configuration has been determined. Reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing methods such as heat sinks and ambient air cooling to minimize θ_{CA}, a higher ambient operating temperature and/or a lower junction temperature can be achieved. However, an easier approach to thermal evaluation uses the following equations:

$$T_A = T_J - P_D \times \theta_{JA} \quad \text{or} \quad T_J = T_A + P_D \times \theta_{JA}$$

where:

θ_{JA} = Thermal Resistance from the Junction to the Ambient ($\theta_{JC} + \theta_{CA}$)

The total thermal resistance for a package (θ_{JA}) is a combination of its two components, θ_{JC} and θ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package case surface (θ_{JC}) and θ_{CA}. Although θ_{JC} is package related and the user cannot influence it, θ_{CA} is user dependent. Good thermal management by the user, such as heat sink and airflow, can significantly reduce θ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

11.6 THERMAL MANAGEMENT TECHNIQUES

To attain a reasonable maximum ambient operating temperature, the user must reduce the barrier to heat flow from θ_{JA}. The only way to accomplish this is to significantly reduce θ_{CA} by applying thermal management techniques such as heat sinks and forced air cooling. The following paragraphs discuss thermal study results for the MC68040 that did not use thermal management techniques, airflow cooling, heat sink, and heat sink combined with airflow cooling.

The MC68040 power dissipation values given in this section represent the sum of the power dissipated by the internal circuitry and the output buffers of the MC68040. The termination network chosen by the system designer strongly influences this last component of power. Values listed in this section for large buffer terminated entries reflect a termination network as illustrated in Figure 11-18 and are consistent with specifications for the MC68040. For additional termination schemes, refer to AN1051, *Transmission Line Effects in PCB Applications*, or AN1061, *Reflecting on Transmission Line Effects*.

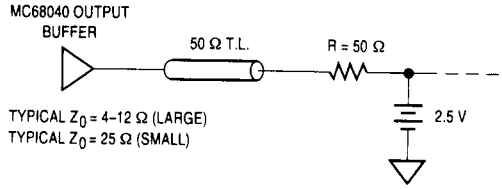


Figure 11-18. MC68040 Termination Network

If a designer uses alternative standard termination methods, such as RC termination network (see Figure 11-19), Thévenin termination network (not illustrated), or no termination method at all, which is not recommended, then the power dissipation of the MC68040 will be significantly less than the large buffer terminated values. For termination networks other than that illustrated in Figure 11-19, the designer must calculate the component of power dissipated in the output buffer and add this value to the small buffer unterminated value.

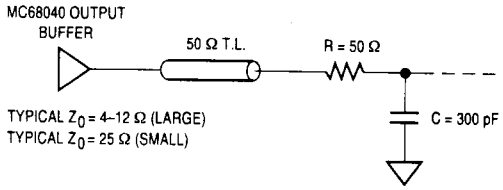


Figure 11-19 Typical Configuration for RC Termination Network

The following paragraphs describe how the large buffer terminated values were calculated. The MC68040 termination network causes current flow through the output buffer of the MC68040, regardless of whether the MC68040 is driving a logic one or a logic zero. The following equation gives the large buffer termination network power dissipation for a given pin:

$$I = (V \div (R + Z_o)) + 5\ mA$$

$$P = I^2 R_{eff}$$

R_{eff} is the effective average output resistance, including typical pullup resistance, typical pulldown resistance, and a duty cycle average of how often the pin is high, low, or three-stated. Typical values for Z_o are 6 Ω for large buffer low output, 12 Ω for large buffer high output, and 25 Ω for small buffer output. Using these values and duty cycle assumptions based on sequential burst write cycles, R_{eff} calculates to 7.7 Ω for the MC68040 large buffer mode and 25 Ω for the small buffer mode.

Maximum termination current in the large buffer mode occurs for output:

Low: $I_{tl} = (2.5\ V \div (50 + 6\ \Omega)) + 5\ mA = 49.6\ mA$

High: $I_{th} = (2.75\ V \div (50 + 12\ \Omega)) + 5\ mA = 50.8\ mA$

Maximum power dissipation in the large buffer mode occurs for output:

Low: $P_{llb} = I^2R = (49.6\ mA)^2 \times 6\ \Omega = 14.8\ mW$

High: $P_{hlb} = I^2R = (50.8\ mA)^2 \times 12\ \Omega = 30.1\ mW$

Similar calculations for unterminated small buffers yield:

$$I = 5\ mA\ (by\ spec)$$

and

$$P = I^2R = (5\ mA)^2 \times 25\ \Omega$$

so

$$P_{hsb} = 0.625\ mW$$
$$P_{lsb} = 0.625\ mW$$

Assuming that the duty cycle of output j is driving a valid logic value instead of being three-stated as given by DC_j, then the following equation approximates total average power dissipation in the output buffers:

$$I_{Total} = \sum_{j=1}^{\text{Number of Outputs Used}} (I_j \times DC_j)^2 \times R_{effj}$$

I_j and Z_{oj} are calculated for every pin as illustrated above. In practice the above summation is carried out by groups of pins instead of individual pins.

Motorola has calculated the values for DC_j for typical situations. On an average clock there will be 37.8 pins high, 41.5 pins low, and 11.7 pins three-stated. The following examples demonstrate how to calculate the power dissipation that is added to small buffer power dissipation numbers, assuming a termination as illustrated in Figure 11-18.

a. For the numbers listed in this section in a large buffer design with no caching.

   P = (Number of Pins High) × (P_{hlb}) + (Number of Pins Low) × (P_{llb})

   = 37.8 Pins × 30.1 mW per Pin + 41.5 Pins × 14.8 mW per Pin

   = 1.75 W

b. For a single bus master system in a large buffer design with no caching or snooping and only standard features (i.e., TLN, UPA, $\overline{BR}$, $\overline{BB}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{CIOUT}$, $\overline{TIP}$, $\overline{MI}$, TDO, $\overline{IPEND}$, PST not used):

   P = (Number of Pins High) × (P_{hlb}) + (Number of Pins Low) × (P_{llb})

   = 29.8 Pins × 30.1 mW per Pin + 34.5 Pins × 14.8 mW per Pin

   = 1.41 W

c. For the example b system with copyback caching, assuming 85% cache hit rate:

   P = (29.8 Pins × 30.1 mW per Pin + 34.5 Pins × 14.8 mW per Pin) × (1 – 0.85)

   = 0.21 W

d. For the example c system running the data bus in small buffer mode with other outputs in large buffer mode terminated:

P = (Number of Pins Large Buffer High) × (P_{hlb}) + (Number of Pins Large Buffer Low) × (P_{llb}) + (Number of Pins Small Buffer High) × (P_{hsb}) + (Number of Pins Small Buffer Low) × (P_{lsb})

= 19.1 Pins × 30.1 mW per Pin + 23.8 Pins × 14.8 mW per Pin + 10.7 Pins × 0.625 mW per Pin + 10.7 Pins × 0.625 mW per Pin

= 0.94 W × (1 – 0.85)

= 0.14 W

11.6.1 MC68040 Thermal Characteristics in Still Air

In this study, a small sample of MC68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average θ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with approximately 6 W of power being dissipated from within the package. The test determined that θ_{JA} decreases slightly for the increasing power dissipation range possible. Therefore, since the variance in θ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that θ_{JA} is valid at all power levels. Using the previous equations, Table 11-2 lists the results of a maximum power dissipation at maximum θ_{JC} with no heat sink or airflow (see Table 11-1 to calculate other power dissipation values). The ambient temperature results illustrate the need to implement some type of thermal management to obtain a reasonable maximum ambient temperature.

Table 11-2. Thermal Parameters with No Heat Sink or Airflow

MHz	Defined Parameters			Measured	Calculated		
	P_D	T_J	θ_{JC}	θ_{JA}	θ_{CA} ($\theta_{JA} - \theta_{JC}$)	T_C ($T_J - P_D \times \theta_{JC}$)	T_A ($T_J - P_D \times \theta_{JA}$)
MC68040							
25	6.3	110 °C	3	22.8	19.8	91.1	–33.64
25	6.6	110 °C	3	22.8	19.8	90.2	–40.48
25	8.6	110 °C	3	22.8	19.8	84.2	–86.08
33	7.7	110 °C	3	22.8	19.8	86.9	–65.56
33	8.0	110 °C	3	22.8	19.8	86.0	–72.40
33	10.0	110 °C	3	22.8	19.8	80.0	–118.00
MC68LC040 and MC68EC040							
20	4	110 °C	3	22.8	19.8	98	18.8
25	5	110 °C	3	22.8	19.8	95	–4
33	6.3	110 °C	3	22.8	19.8	91.1	–33.64

11.6.2 MC68040 Thermal Characteristics in Forced Air

In this study, a small sample of MC68040 packages was tested in forced-air cooling in a wind tunnel with no heat sink. The test was performed with approximately 6 W of power being dissipated from within the package. As previously mentioned, since the variance in θ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that θ_{JA} is constant at all power levels. Using the previous equations, Table 11-3 lists the results of the maximum power dissipation at maximum θ_{JC} with airflow and no heat sink for the MC68040, and Table 11-4 lists the results for the MC68LC040 and MC68EC040. Refer to Table 11-1 for calculating other power dissipation values.

Table 11-3. Thermal Parameters with Forced Airflow and No Heat Sink for the MC68040

	Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
MHz	Airflow Velocity	P_D	T_J	θ_{JC}	θ_{JA}	θ_{CA}	T_C	T_A
25	100 LFM	6.3 W	110 °C	3 °C/W	12.7 °C/W	9.7 °C/W	91.1 °C	29.90 °C
25		6.6 W					90.2 °C	26.18 °C
25		8.6 W					84.9 °C	00.76 °C
33		7.7 W					86.9 °C	12.21 °C
33		8.0 W					86.0 °C	08.40 °C
33		10.0 W					80.0 °C	00.00°C
25	250 LFM	6.3 W	110 °C	3 °C/W	11.0 °C/W	8.0 °C/W	91.1 °C	40.70 °C
25		6.6 W					90.2 °C	37.40 °C
25		8.6 W					84.2 °C	15.40 °C
33		7.7 W					86.9 °C	25.30 °C
33		8.0 W					86.0 °C	22.00 °C
33		10.0 W					80.0 °C	00.00 °C
25	500 LFM	6.3 W	110 °C	3 °C/W	9.9 °C/W	6.9 °C/W	91.1 °C	47.63 °C
25		6.6 W					90.2 °C	44.66 °C
25		8.6 W					84.2 °C	24.86 °C
33		7.7 W					86.9 °C	33.77 °C
33		8.0 W					86.0 °C	30.80 °C
33		10.0 W					80.0 °C	11.00 °C
25	750 LFM	6.3 W	110 °C	3 °C/W	9.5 °C/W	6.5 °C/W	91.1 °C	50.15 °C
25		6.6 W					90.2 °C	47.30 °C
25		8.6 W					84.2 °C	28.30 °C
33		7.7 W					86.9 °C	36.85 °C
33		8.0 W					86.0 °C	34.00 °C
33		10.0 W					80.0 °C	15.00 °C
25	1000 LFM	6.3 W	110 °C	3 °C/W	9.3 °C/W	6.3 °C/W	91.1 °C	51.41 °C
25		6.6 W					90.2 °C	48.62 °C
25		8.6 W					84.2 °C	30.02 °C
33		7.7 W					86.9 °C	38.39 °C
33		8.0 W					80.0 °C	17.00 °C
33		10.0 W					81.8 °C	22.58 °C

Table 11-4. Thermal Parameters with Forced Airflow and No Heat Sink for the MC68LC040 and MC68EC040

	Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
MHz	Airflow Velocity	P_D	T_J	θ_{JC}	θ_{JA}	θ_{CA}	T_C	T_A
20 25 33	100 LFM	4 W 5 W 6.3W	110 °C	3 °C/W	12.7 °C/W	9.7 °C/W	98 °C 95 °C 91.1 °C	59.2 °C 46.5 °C 29.9 °C
20 25 33	250 LFM	4 W 5 W 6.3W	110 °C	3 °C/W	11 °C/W	8 °C/W	98 °C 95 °C 91.1 °C	66 °C 55 °C 40.70 °C
20 25 33	500 LFM	4 W 5 W 6.3W	110 °C	3 °C/W	9.9 °C/W	6.9 °C/W	98 °C 95 °C 91.1 °C	70.4 °C 60.5 °C 47.63 °C
20 25 33	750 LFM	4 W 5 W 6.3W	110 °C	3 °C/W	9.5 °C/W	6.5 °C/W	98 °C 95 °C 91.1 °C	72 °C 62.5 °C 50.15 °C
20 25 33	1000 LFM	4 W 5 W 6.3W	110 °C	3 °C/W	9.3 °C/W	6.3 °C/W	98 °C 95 °C 91.1 °C	72.8 °C 63.5 °C 51.41 °C

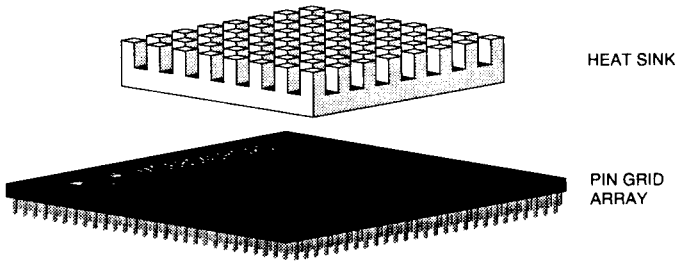
Reviewing the maximum ambient operating temperatures illustrates that using an all small buffer configuration of the MC68040 with a relatively small amount of airflow (100 LFM) achieves a 0–70 °C ambient operating temperature. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

11.6.3 MC68040 Thermal Characteristics with a Heat Sink

The designer must consider many factors in choosing a heat sink: heat-sink size and composition, method of attachment, and choice of a dry or wet (i.e., thermal grease) connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat-sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink provides better cooling. Under forced-air conditions as low as 100 LFM, the difference between the θ_{CA} is very small (0.4 °C/W or less). This difference continues to decrease as the forced airflow increases.

The area of this example heat-sink base perimeter is 1.8" × 1.8", with a height of 0.65". The heat-sink used a pin-fin (i.e., bed-of-nails) design composed of aluminum alloy. Figure 11-20 illustrates the heat sink, which can be obtained through Thermalloy, Inc.



NOTE: Do not cover up microprocessor markings with an adhesive mounted heat sink.

Figure 11-20. Heat Sink with Adhesive

All pin-fin heat sinks tested were made from extrusion aluminum products. The planar face of the heat-sink matting to the package should have a good degree of planarity; if it has any curvature, the curvature should be convex at the central region of the heat-sink surface to provide intimate physical contact to the PGA surface. This heat sinks meet this criteria. Nonplanar, concave curvature in the central regions of the heat sink results in poor thermal contact to the package.

Although there are several ways to attach a heat sink to the package, it is easiest to use a demountable heat-sink attachment called "E-Z attach for PGA packages" (see Figure 11-21). A steel spring clamps the heat sink and the package to a plastic frame. Besides the height of the heat sink and plastic frame, no additional height is added to the package. The interface between the ceramic package and the aluminum heat sink was evaluated for both dry and wet interfaces in still air. The thermal grease reduced the θ_{CA} quite significantly (about 2.5 °C/W) in still air. An attachment with thermal grease provided about the same thermal performance as if a thermal epoxy had been used.

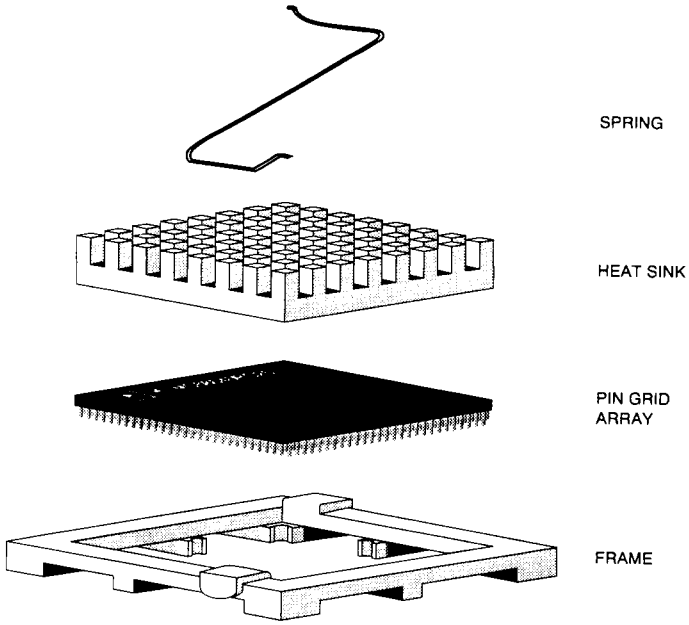


Figure 11-21. Heat Sink with Attachment

In the specification provided by Thermalloy, Inc., a chart illustrates the heat-sink temperature rise above ambient versus heat dissipated. This chart applies if no airflow is used with the heat-sink. Table 11-5 lists the calculations based on this chart.

Table 11-5. Thermal Parameters with Heat Sink and No Airflow

MHz	Thermal Mgmt. Technique / Airflow Velocity	Defined Parameters P_D	T_J	θ_{JC}	Heat-Sink Spec. T_C-T_A	Calculated T_C	T_A
MC68040							
25	0	6.3 W	110 °C	3 °C/W	64.4 °C	91.1 °C	26.7 °C
25	0	6.6 W	110 °C	3 °C/W	66.8 °C	90.2 °C	23.4 °C
25	0	8.6 W	110 °C	3 °C/W	82.8 °C	84.2 °C	1.4 °C
33	0	7.7 W	110 °C	3 °C/W	75.6 °C	86.9 °C	11.3 °C
33	0	8.0 W	110 °C	3 °C/W	78.0 °C	86.0 °C	8.0 °C
33	0	10.0 W	110 °C	3 °C/W	94.0 °C	80.0 °C	−14.0 °C
MC68LC040 and MC68EC040							
20	0	4.0 W	110 °C	3 °C/W	45.0 °C	98.0 °C	53.0 °C
25	0	5.0 W	110 °C	3 °C/W	54.0 °C	95.0 °C	41.0 °C
33	0	6.3 W	110 °C	3 °C/W	64.4 °C	91.1 °C	26.7 °C

11.6.4 MC68040 Thermal Characteristics with Heat Sink and Forced Air

In the specification provided by Thermalloy, Inc., a chart illustrates the air velocity versus thermal resistance. This chart applies if airflow is used with the heat sink. Table 11-6 lists the calculations based on this chart.

Table 11-6. Thermal Parameters with Heat Sink and Airflow

	Thermal Mgmt. Technique	Defined Parameters			Heat-Sink Spec.	Calculated		
MHz	Airflow Velocity	P_D	T_J	θ_{JC} Max.	θ_{CA}	θ_{JA}	T_C	T_A
MC68040								
25	200 LFM	6.3 W	110 °C	3 °C/W	4.25 °C/W	7.25 °C/W	91.1 °C	64.3 °C
25		6.6 W					90.2 °C	62.2 °C
25		8.6 W					84.2 °C	47.7 °C
33		7.7 W					86.9 °C	54.2 °C
33		8.0 W					86.0 °C	52.0 °C
33		10.0W					80.0 °C	37.5 °C
25	400 LFM	6.3 W	110 °C	3 °C/W	2.30 °C/W	5.25 °C/W	91.1 °C	76.9 °C
25		6.6 W					90.2 °C	75.4 °C
25		8.6 W					84.2 °C	64.9 °C
33		7.7 W					86.9 °C	69.6 °C
33		8.0 W					86.0 °C	68.0 °C
33		10.0W					80.0 °C	57.5 °C
25	600 LFM	6.3 W	110 °C	3 °C/W	1.50 °C/W	4.50 °C/W	91.1 °C	81.7 °C
25		6.6 W					90.2 °C	80.3 °C
25		8.6 W					84.2 °C	71.3 °C
33		7.7 W					86.9 °C	75.4 °C
33		8.0 W					86.0 °C	74.0 °C
33		10.0W					80.0 °C	65.0 °C
25	800 LFM	6.3 W	110 °C	3 °C/W	1.25 °C/W	4.25 °C/W	91.1 °C	83.2 °C
25		6.6 W					90.2 °C	82.0 °C
25		8.6 W					84.2 °C	73.5 °C
33		7.7 W					86.9 °C	77.3 °C
33		8.0 W					86.0 °C	76.0 °C
33		10.0W					80.0 °C	67.5 °C
MC68LC040 and MC68EC040								
20	200 LFM	4.0 W	110 °C	3 °C/W	4.25 °C/W	7.25 °C/W	98.0 °C	81.0 °C
25		5.0 W					95.0 °C	73.8 °C
33		6.3 W					91.1 °C	64.3 °C
20	400 LFM	4.0 W	110 °C	3 °C/W	2.30 °C/W	5.25 °C/W	98.0 °C	89.0 °C
25		5.0 W					95.0 °C	83.8 °C
33		6.3 W					91.1 °C	76.9 °C
20	600 LFM	4.0 W	110 °C	3 °C/W	1.50 °C/W	4.50 °C/W	98.0 °C	92.0°C
25		5.0 W					95.0 °C	87.5 °C
33		6.3 W					91.1 °C	81.7 °C
20	800 LFM	4.0 W	110 °C	3 °C/W	1.25 °C/W	4.25 °C/W	98.0 °C	93.0°C
25		5.0 W					95.0 °C	88.8 °C
33		6.3 W					91.1 °C	83.2 °C