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MC68HC11F1
MC68HC11FC0

Technical Summary
8-Bit Microcontroller

1 Introduction

The MC68HC11F1 is a high-performance member of the M68HC11 family of microcontroller units (MCUs). High-speed expanded systems required the development of this chip with its extra input/output (I/O) ports, an increase in static RAM (one Kbyte), internal chip-select functions, and a non-multiplexed bus which reduces the need for external interface logic. The timer, serial I/O, and analog-to-digital (A/D) converter enable functions similar to those found in the MC68HC11E9.

The MC68HC11FC0 is a low cost, high-speed derivative of the MC68HC11F1. It does not have EEPROM or an analog-to-digital converter. The MC68HC11FC0 can operate at bus speeds as high as six MHz.

This document provides a brief overview of the structure, features, control registers, packaging information and availability of the MC68HC11F1 and MC68HC11FC0. For detailed information on M68HC11 subsystems, programming and the instruction set, refer to the *M68HC11 Reference Manual* (M68HC11RM/AD).

1.1 Features

- MC68HC11 CPU
- 512 Bytes of On-Chip Electrically Erasable Programmable ROM (EEPROM) with Block Protect (MC68HC11F1 only)
- 1024 Bytes of On-Chip RAM (All Saved During Standby)
- Enhanced 16-Bit Timer System
  - — 3 Input Capture (IC) Functions
  - — 4 Output Compare (OC) Functions
  - — 4th IC or 5th OC (Software Selectable)
- On-Board Chip-Selects with Clock Stretching
- Real-Time Interrupt Circuit
- 8-Bit Pulse Accumulator
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communication Interface (SCI)
- Power saving STOP and WAIT Modes
- Eight-Channel 8-Bit A/D Converter (MC68HC11F1 only)
- Computer Operating Properly (COP) Watchdog System and Clock Monitor
- Bus Speeds of up to 6 MHz for the MC68HC11FC0 and up to 5 MHz for the MC68HC11F1
- 68-Pin PLCC (MC68HC11F1 only), 64-Pin QFP (MC68HC11FC0 only), and 80-pin TQFP package options

1.2 Ordering Information

The following devices all have 1024 bytes of RAM. In addition, the MC68HC11F1 devices have 512 bytes of EEPROM. None of the devices contain on-chip ROM.

Table 1 MC68HC11F1 Standard Device Ordering Information

Package	Temperature	Frequency	MC Order Number
80-Pin Thin Quad Flat Pack (TQFP) (14 mm X 14 mm, 1.4 mm thick)	0° to +70°	5 MHz	MC68HC11F1PU5
	-40° to +85°C	2 MHz	MC68HC11F1CPU2
		3 MHz	MC68HC11F1CPU3
		4 MHz	MC68HC11F1CPU4
		5 MHz	MC68HC11F1CPU5
	– 40° to + 105° C	2 MHz	MC68HC11F1VPU2
		3 MHz	MC68HC11F1VPU3
		4 MHz	MC68HC11F1VPU4
	– 40° to + 125° C	2 MHz	MC68HC11F1MPU2
		3 MHz	MC68HC11F1MPU3
		4 MHz	MC68HC11F1MPU4
68-Pin PLCC	0° to +70°	5 MHz	MC68HC11F1FN5
	– 40° to + 85° C	2 MHz	MC68HC11F1CFN2
		3 MHz	MC68HC11F1CFN3
		4 MHz	MC68HC11F1CFN4
		5 MHz	MC68HC11F1CFN5
	– 40° to + 105° C	2 MHz	MC68HC11F1VFN2
		3 MHz	MC68HC11F1VFN3
		4 MHz	MC68HC11F1VFN4
	– 40° to + 125° C	2 MHz	MC68HC11F1MFN2
		3 MHz	MC68HC11F1MFN3
		4 MHz	MC68HC11F1MFN4

Table 2 MC68HC11F1 Extended Voltage (3.0 to 5.5 V) Device Ordering Information

Package	Temperature	Frequency	MC Order Number
68-Pin Plastic Leaded Chip Carrier (PLCC)	0° to +70°C	3 MHz	MC68L11F1FN3
	–40° to +85°C	3 MHz	MC68L11F1CFN3
80-Pin Thin Quad Flat Pack (TQFP)	0° to +70°C	3 MHz	MC68L11F1PU3
	–40° to +85°C	3 MHz	MC68L11F1CPU3

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1.3 Block Diagrams

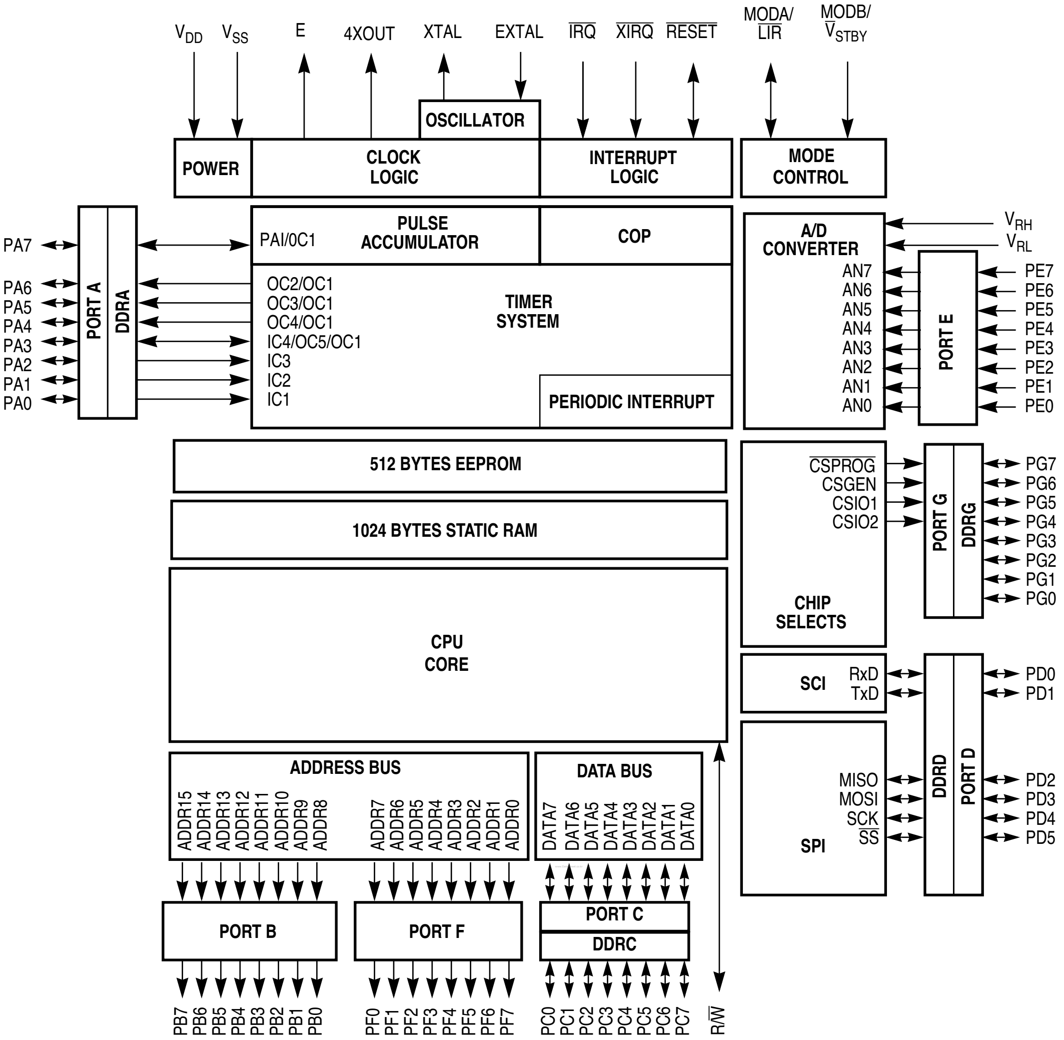


Figure 1 MC68HC11F1 Block Diagram

2 Pin Assignments and Signal Descriptions

2.1 MC68HC11F1 Pin Assignments

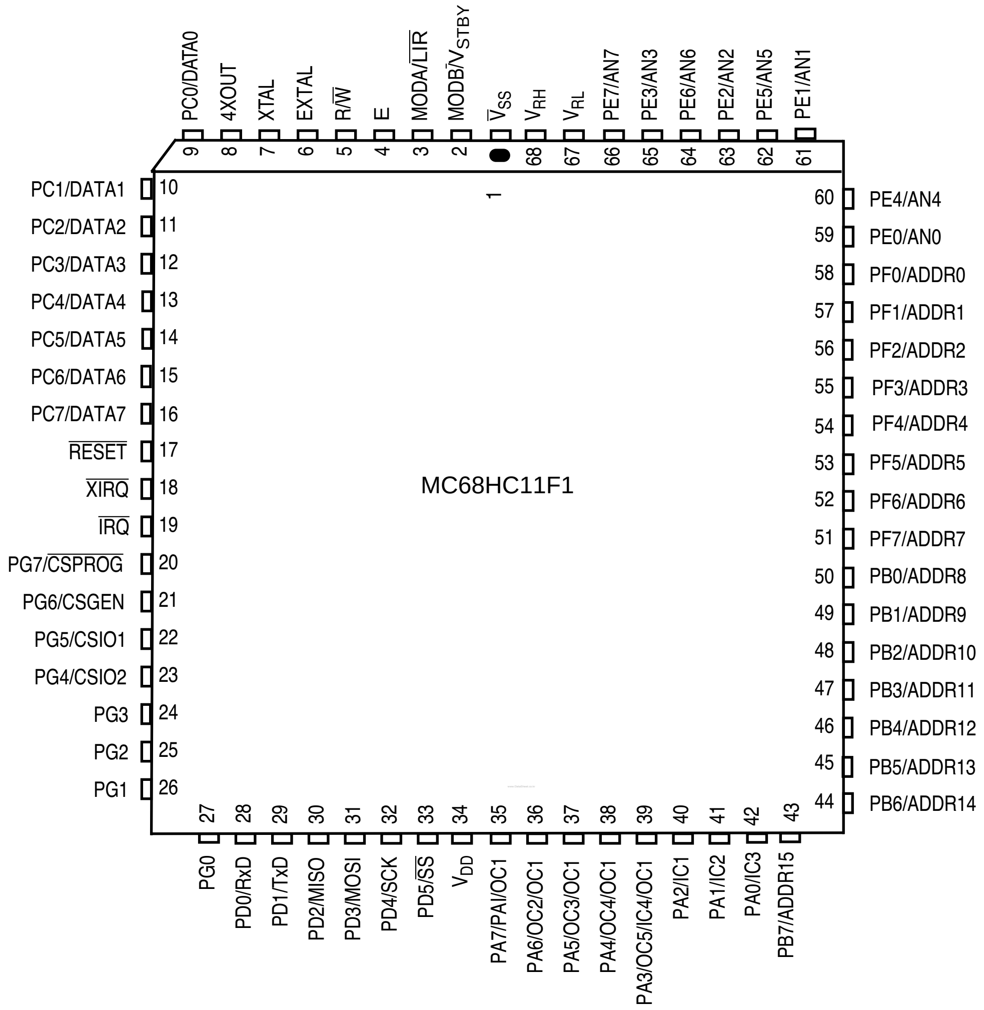


Figure 3 MC68HC11F1 68-Pin PLCC Pin Assignments

2.2 MC68HC11FC0 Pin Assignments

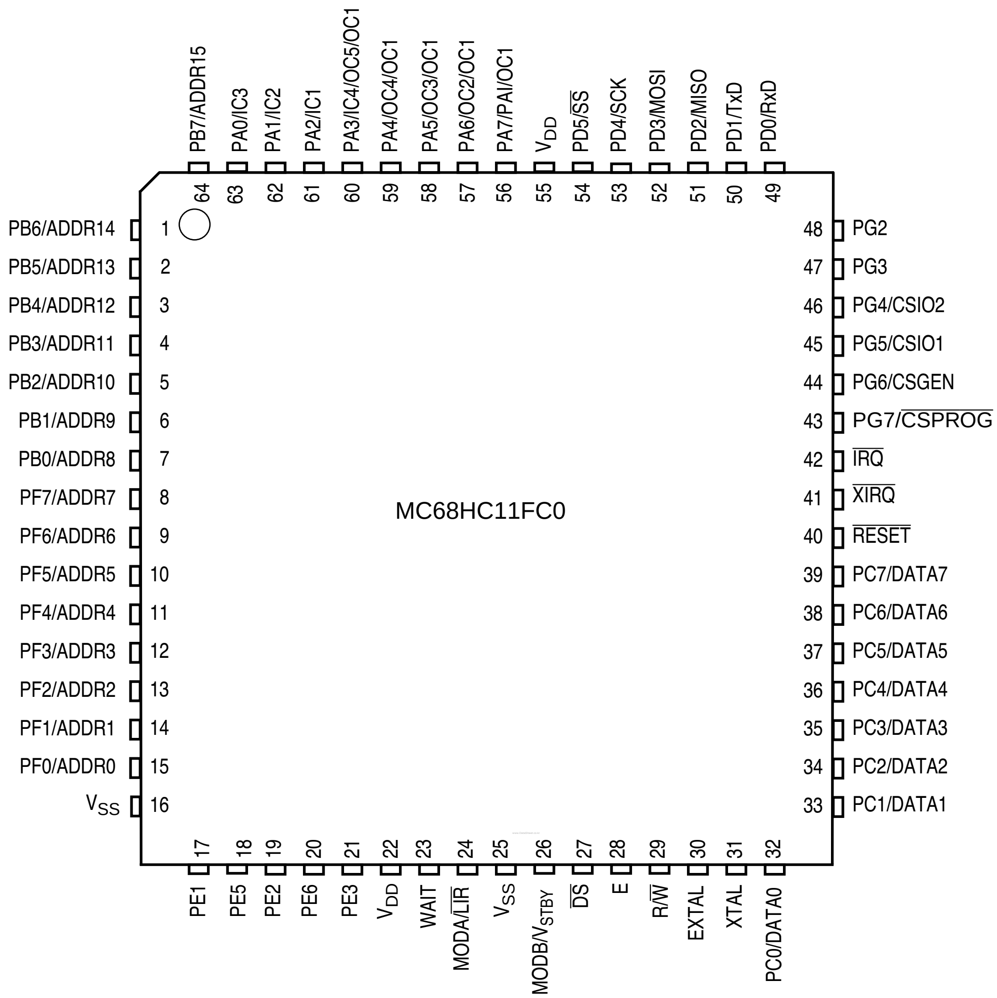


Figure 5 MC68HC11FC0 64-Pin QFP Pin Assignments

2.3 Pin Descriptions

V_{DD} and V_{SS}

V_{DD} is the positive power input to the MCU, and V_{SS} is ground.

$\overline{\text{RESET}}$

This active-low input initializes the MCU to a known startup state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the COP watchdog circuits.

XTAL and EXTAL

These two pins provide the interface for either a crystal or a CMOS-compatible clock to drive the internal clock circuitry. The frequency applied to these pins is four times the desired bus frequency (E clock).

E

This pin provides an output for the E clock, the basic timing reference signal for the bus circuitry. The address bus is active when E is low, and the data bus is active when E is high.

$\overline{\text{DS}}$

The data strobe output is the inverted E clock. **$\overline{\text{DS}}$ is present on the MC68HC11FC0 only.**

WAIT

This input is used to stretch the bus cycle to accomodate slower devices. The MCU samples the logic level at this pin on the rising edge of E clock. If it is high, the MCU holds the E clock high for the next four EXTAL clock cycles. If it is low, the E clock responds normally, going low two EXTAL cycles later. **The WAIT pin is present on the MC68HC11FC0 only**.

4XOUT

This pin provides a buffered oscillator signal to drive another M68HC11 MCU. **The 4XOUT pin is not present on the 64-pin QFP MC68HC11FC0 package**.

$\overline{\text{IRQ}}$

This active-low input provides a means of generating asynchronous, maskable interrupt requests for the CPU.

$\overline{\text{XIRQ}}$

This interrupt request input can be made non-maskable by clearing the X bit in the MCU's condition code register.

MODA/$\overline{\text{LIR}}$ and MODB/VSTBY

The logic level applied to the MODA and MODB pins at reset determines the MCU's opreating mode (see **Table 7** in **4 Operating Modes and System Initialization**). After reset, MODA functions as $\overline{\text{LIR}}$, an open-drain output that indicates the start of an instruction cycle. MODB functions as V_{STBY}, providing a backup battery to maintain the contents of RAM when V_{DD} falls.

R/$\overline{\text{W}}$

In expanded and test modes, R/$\overline{\text{W}}$ indicates the direction of transfers on the external data bus.

V_{RH} and V_{RL}

These pins provide the reference voltage for the analog-to-digital converter. Use bypass capacitors to minimize noise on these signals. Any noise on V_{RH} and V_{RL} will directly affect A/D accuracy. These pins are not present on the MC68HC11FC0.

3 Control Registers

The MC68HC11F1 and MC68HC11FC0 control registers determine most of the system's operating characteristics. They occupy a 96-byte relocatable memory block. Their names and bit mnemonics are summarized in the following table. Addresses shown are the default locations out of reset.

3.1 MC68HC11F1 Control Registers

Table 5 MC68HC11F1 Register and Control Bit Assignments

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$1002	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$1003	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$1006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2

3.2 MC68HC11FC0 Control Registers

Table 6 MC68HC11FC0 Register and Control Bit Assignments

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$1002	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$1003	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$1006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2

4 Operating Modes and System Initialization

The 16-bit address bus can access 64 Kbytes of memory. Because the MC68HC11F1 and MC68HC11FC0 are intended to operate principally in expanded mode, there is no internal ROM and the address bus is non-multiplexed. Both devices include 1 Kbyte of static RAM, a 96-byte control register block, and 256 bytes of bootstrap ROM. The MC68HC11F1 also includes 512 bytes of EEPROM.

RAM and registers can be remapped on both the MC68HC11F1 and the MC68HC11FC0. On both the MC68HC11F1 and the MC68HC11FC0, out of reset RAM resides at $0000 to $03FF and registers reside at $1000 to $105F. On the MC68HC11F1, RAM and registers can both be remapped to any 4-Kbyte boundary. On the MC68HC11FC0, RAM can be remapped to any 1-Kbyte boundary, and registers can be remapped to any 4-Kbyte boundary in the first 16 Kbytes of address space.

RAM and control register locations are defined by the INIT register, which can be written only once within the first 64 E-clock cycles after a reset in normal modes. It becomes a read-only register thereafter. If RAM and the control register block are mapped to the same boundary, the register block has priority of the first 96 bytes.

In expanded and special test modes in the MC68HC11F1, EEPROM is located from $*x*E00 to $*x*FFF, where *x* represents the value of the four high-order bits of the CONFIG register. EEPROM is enabled by the EEON bit of the CONFIG register. In single-chip and bootstrap modes, the EEPROM is located from $FE00 to $FFFF.

4.1 Operating Modes

Bootstrap ROM resides at addresses $BF00–$BFFF, and is only available when the MCU operates in special bootstrap operating mode. Operating modes are determined by the logic levels applied to the MODB and MODA pins at reset.

In single-chip mode, the MCU functions as a self-contained microcontroller and has no external address or data bus. Ports B, C and F are available for general-purpose I/O (GPIO). Ports B and F are outputs only; each of the port C pins can be configured as input or output.

CAUTION

The MC68HC11FC0 must not be configured to boot in single-chip mode because it has no internal ROM or EEPROM. Operation of the device in single-chip mode will result in erratic behavior.

In expanded mode, the MCU can access external memory. Ports B and F provide the address bus, and port C is the data bus.

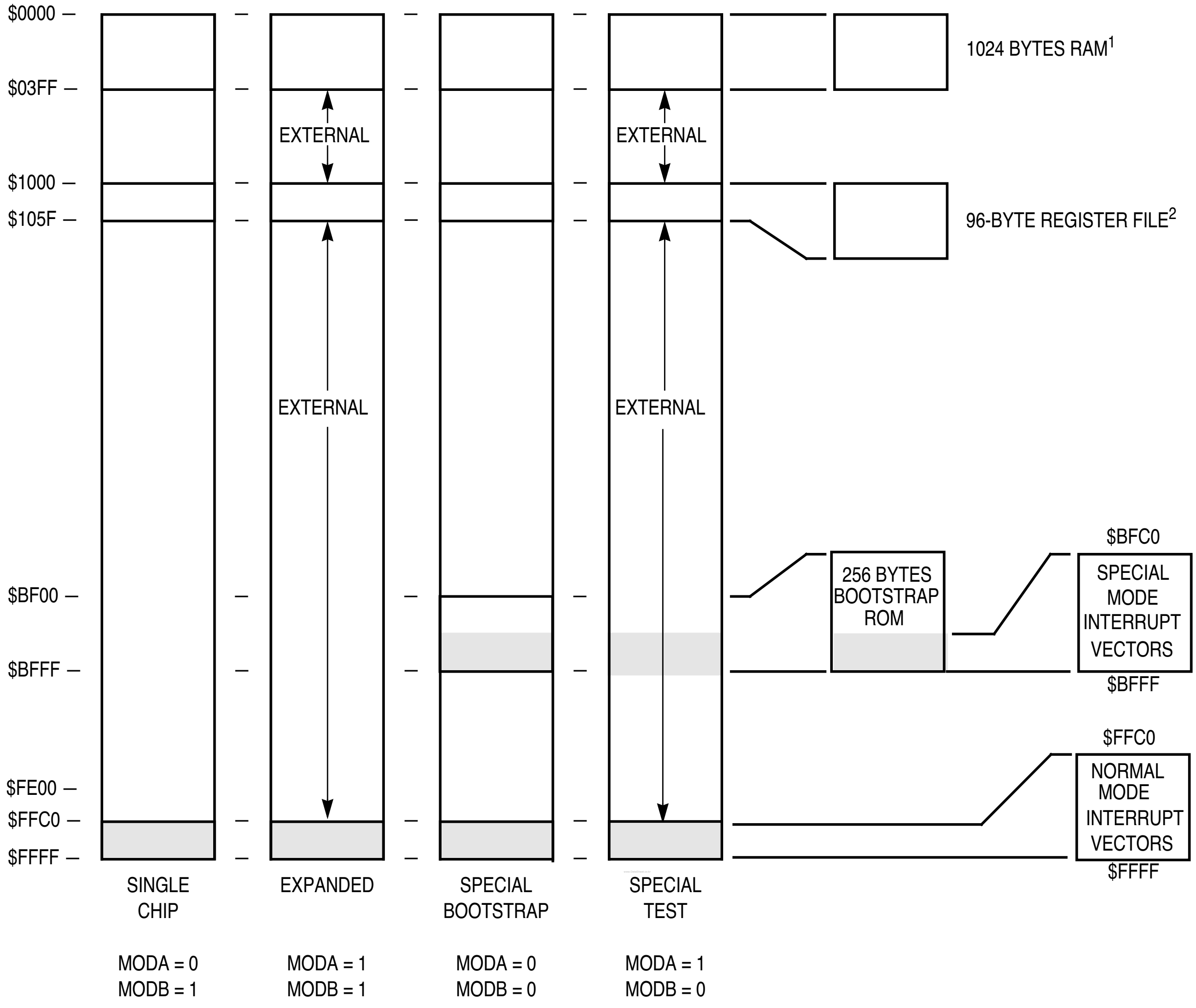
Special bootstrap mode is a variation of single chip mode that provides access to the internal bootstrap ROM. In this mode, the user can download a program into on-chip RAM through the serial communication interface (SCI).

Special test mode, a variation of expanded mode, is primarily used during Motorola’s internal production testing, but can support emulation and debugging during program development.

Table 7 shows a summary of operating modes, mode select pins, and control bits in the HPRIO register.

Table 7 Hardware Mode Select Summary

Input Pins		Mode Description	Control Bits in HPRIO (Latched at Reset)		
MODB	MODA		RBOOT	SMOD	MDA
1	0	Single Chip	0	0	0
1	1	Expanded	0	0	1
0	0	Special Bootstrap	1	1	0
0	1	Special Test	0	1	1



NOTES:
1. RAM can be remapped to any 1-Kbyte boundary, depending on the value contained in the RAM field in the INIT register.
2. The register block can be remapped to $0000, $2000, or $3000, depending on the value contained in REG[1:0] in the INIT register.

Figure 8 MC68HC11FC0 Memory Map

4.3 System Initialization Registers

HPRIO — Highest Priority Interrupt and Miscellaneous **$x03C**

	Bit 7	6	5	4	3	2	1	Bit 0	
	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	
RESET:	0	0	0	0	0	1	0	1	Single-Chip
	0	0	1	0	0	1	0	1	Expanded
	1	1	0	1	0	1	0	1	Bootstrap
	0	1	1	1	0	1	0	1	Special Test

INIT — RAM and I/O Mapping (**MC68HC11F1 only**) **$x03D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG4	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

The INIT register can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

NOTE

The register diagram above applies to the MC68HC11F1 only. A diagram and bit descriptions of the INIT register in the MC68HC11FC0 are provided elsewhere in this section.

RAM[3:0] — Internal RAM Map Position

These bits determine the upper four bits of the RAM address and allow mapping of the RAM to any four-Kbyte boundary. Refer to **Table 10**.

REG[3:0] — 96-Byte Register Block Map Position

These bits determine bits the upper 4 bits of the register block and allow mapping of the register block to any four-Kbyte boundary. Refer to **Table 10**.

Table 10 RAM and Register Mapping

RAM[3:0]	Location
0000	$0000-$03FF
0001	$1000-$13FF
0010	$2000-$23FF
0011	$3000-$33FF
0100	$4000-$43FF
0101	$5000-$53FF
0110	$6000-$63FF
0111	$7000-$73FF
1000	$8000-$83FF
1001	$9000-$93FF
1010	$A000-$A3FF
1011	$B000-$B3FF
1100	$C000-$C3FF
1101	$D000-$D3FF
1110	$E000-$E3FF
1111	$F000-$F3FF

REG[3:0]	Location
0000	$0000-$005F
0001	$1000-$105F
0010	$2000-$205F
0011	$3000-$305F
0100	$4000-$405F
0101	$5000-$505F
0110	$6000-$605F
0111	$7000-$705F
1000	$8000-$805F
1001	$9000-$905F
1010	$A000-$A05F
1011	$B000-$B05F
1100	$C000-$C05F
1101	$D000-$D05F
1110	$E000-$E05F
1111	$F000-$F05F

OPT2 — System Configuration Option Register 2 **$x038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	CLK4X	LIRDV	—	SPRBYP	—	—
RESET	0	0	1	0	0	0	0	0

GWOM — Port G Wired-OR Mode Option

Refer to **7.8 Parallel I/O Registers**, page 36.

CONFIG — EEPROM Mapping, COP, EEPROM Enables **$x03F**

	Bit 7	6	5	4	3	2	1	Bit 0
	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
RESET	U	U	U	U	1	U	1	U

U = Unaffected by reset

Bits 7:3 — See **6.2 EEPROM Registers**, page 30. (These bits are implemented on the MC68HC11F1 only.)

NOCOP — COP System Disable
0 = COP enabled (forces reset on time-out)
1 = COP disabled (does not force reset on time-out)

TEST1 — Factory Test **$x03E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	0
RESET:	0	0	0	0	—	0	0	0

These bits can only be written in test and bootstrap modes.

TILOP — Test Illegal Opcode
This test mode allows serial testing of all illegal opcodes without servicing an interrupt after each illegal opcode is fetched.
0 = Normal operation (trap on illegal opcodes)
1 = Inhibit $\overline{\text{LIR}}$ when an illegal opcode is found

Bit 6 — Not implemented. Reads always return zero and writes have no effect.

OCCR — Output Condition Code Register to Timer Port
0 = Normal operation
1 = Condition code bits H, N, Z, V and C are driven on PA[7:3] to allow a test system to monitor CPU operation

CBYP — Timer Divider Chain Bypass
0 = Normal operation
1 = The 16-bit free-running timer is divided into two 8-bit halves and the prescaler is bypassed. The system E clock drives both halves directly.

DISR — Disable Resets from COP and Clock Monitor
In test and bootstrap modes, this bit is reset to one to inhibit clock monitor and COP resets. In normal modes, DISR is reset to zero.
0 = Normal operation
1 = COP and Clock Monitor failure do not generate a system reset

FCM — Force Clock Monitor Failure
0 = Normal operation
1 = Generate an immediate clock monitor failure reset. Note that the CME bit in the OPTION register must also be set in order to force the reset.

FCOP — Force COP Watchdog Failure
0 = Normal operation
1 = Generate an immediate COP failure reset. Note that the NOCOP bit in the CONFIG register must be cleared (COP enabled) in order to force the reset.

Bit 0 — Not implemented. Reads always return zero and writes have no effect.

Table 11 Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask	Local Mask	Flag Bit
FFC0, C1 to FFD4, D5	Reserved	—	—	—
FFD6, D7	SCI Serial System	I Bit		
	SCI Transmit Complete		TCIE	TC
	SCI Transmit Data Register Empty		TIE	TDRE
	SCI Idle Line Detect		ILIE	IDLE
	SCI Receiver Overrun		RIE	OR
	SCI Receive Data Register Full		RIE	RDRF
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE	SPIF
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII	PAIF
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI	PAOVF
FFDE, DF	Timer Overflow	I Bit	TOI	TOF
FFE0, E1	Timer Input Capture 4/Output Compare 5	I Bit	I4/O5I	I4/O5F
FFE2, E3	Timer Output Compare 4	I Bit	OC4I	OC4F
FFE4, E5	Timer Output Compare 3	I Bit	OC3I	OC3F
FFE6, E7	Timer Output Compare 2	I Bit	OC2I	OC2F
FFE8, E9	Timer Output Compare 1	I Bit	OC1I	OC1F
FFEA, EB	Timer Input Capture 3	I Bit	IC3I	IC3F
FFEC, ED	Timer Input Capture 2	I Bit	IC2I	IC2F
FFEE, EF	Timer Input Capture 1	I Bit	IC1I	IC1F
FFF0, F1	Real-Time Interrupt	I Bit	RTII	RTIF
FFF2, F3	$\overline{\text{IRQ}}$	I Bit	None	None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	X Bit	None	None
FFF6, F7	Software Interrupt	None	None	None
FFF8, F9	Illegal Opcode Trap	None	None	None
FFFA, FB	COP Failure	None	NOCOP	None
FFFC, FD	Clock Monitor Fail	None	CME	None
FFFE, FF	RESET	None	None	None

5.2 Reset and Interrupt Registers

OPTION — System Configuration Options **$x039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

Bits [7:6], [4:2]
Refer to **4.3 System Initialization Registers**, page 23, and **11.3 A/D Registers**, page 56.

IRQE — $\overline{\text{IRQ}}$ Select Edge Sensitive Only
0 = Low level recognition
1 = Falling edge recognition

Table 13 Highest Priority Interrupt Selection (Continued)

PSEL[3:0]	Interrupt Source Promoted
1011	Timer Output Compare 1
1100	Timer Output Compare 2
1101	Timer Output Compare 3
1110	Timer Output Compare 4
1111	Timer Output Compare 5/Input Capture 4

CONFIG — EEPROM Mapping, COP, EEPROM Enables **$x03F**

	Bit 7	6	5	4	3	2	1	Bit 0
	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
RESET	U	U	U	U	1	U	1	U

Bits 7:3, 1:0 — See **6.2 EEPROM Registers**, page 30.

NOCOP — COP System Disable
0 = COP enabled (forces reset on time-out)
1 = COP disabled (does not force reset on time-out)

PPROG — EEPROM Programming Control $x**03B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET	0	0	0	0	0	0	0	0

ODD — Program Odd Rows (TEST)

EVEN — Program Even Rows (TEST)

ROW and BYTE — Row Erase Select Bit and Byte Erase Select

The value of these bits determines the manner in which EEPROM is erased. Bit encodings are shown in **6.2 EEPROM Registers**, page 30.

Table 15 ROW and BYTE Encodings

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
0 = Normal read or program mode
1 = Erase mode

EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

EEPGM — EEPROM Program Command
0 = Program or erase voltage to EEPROM array switched off
1 = Program or erase voltage to EEPROM array switched on

CONFIG — EEPROM Mapping, COP, EEPROM Enables **$x03F**

	Bit 7	6	5	4	3	2	1	Bit 0
	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
RESET	U	U	U	U	1	U	1	U

U = Unaffected by reset.

The CONFIG register is used to assign EEPROM a location in the memory map and to enable or disable EEPROM operation. Bits in this register are user-programmed except when forced to certain values, as noted in the following bit descriptions.

EE[3:0] — EEPROM Map Position

EEPROM is located at $xE00 – $xFFF, where x is the value represented by these four bits. In single-chip and bootstrap modes, EEPROM is forced to $FE00 – $FFFF, regardless of the state of these bits. On factory-fresh devices, EE[3:0] = $0.

Bit 3 — Not implemented. Reads always return one and writes have no effect.

NOCOP — COP System Disable
0 = COP enabled (forces reset on time-out)
1 = COP disabled (does not force reset on time-out)

```
          STAB      $FE00        Store any data to any EEPROM address
          LDAB      #$07         EELAT=1, EEPGM=1
          STAB      $103B        Turn on programming voltage
          JSR       DLY10        Delay 10 ms
          CLR       $103B        Turn off high voltage and set to READ mode
```

6.3.3 Row Erase

The following example shows how to perform a fast erase of large sections of EEPROM. This example assumes that index register X contains the address of a location in the desired row.

```
ROWE      LDAB      #$0E         ROW=1, ERASE=1, EELAT=1, EEPGM=0
          STAB      $103B        Set to ROW erase mode
          STAB      $xxxx        Store any data to any address in ROW
          LDAB      #$0F         ROW=1, ERASE=1, EELAT=1, EEPGM=1
          STAB      $103B        Turn on high voltage
          JSR       DLY10        Delay 10 ms
          CLR       $103B        Turn off high voltage and set to READ mode
```

6.3.4 Byte Erase

The following is an example of how to erase a single byte of EEPROM. This example assumes that index register X contains the address of the byte to be erased.

```
BYTEE     LDAB      #$16         BYTE=1, ROW=0, ERASE=1, EELAT=1, EEPGM=0
          STAB      $103B        Set to BYTE erase mode
          STAB      $0,X         Store any data to address to be erased
          LDAB      #$17         BYTE=1, ROW=0, ERASE=1, EELAT=1, EEPGM=1
          STAB      $103B        Turn on high voltage
          JSR       DLY10        Delay 10 ms
          CLR       $103B        Turn off high voltage and set to READ mode
```

6.4 CONFIG Register Programming

Because the CONFIG register is implemented with EEPROM cells, use EEPROM procedures to erase and program this register. The procedure for programming is the same as for programming a byte in the EEPROM array, except that the CONFIG register address is used. CONFIG can be programmed or erased (including byte erase) while the MCU is operating in any mode, provided that PTCON in BPROT is clear. To change the value in the CONFIG register, complete the following procedure. Do not initiate a reset until the procedure is complete. The new value will not take effect until after the next reset sequence.

1. Erase the CONFIG register.
2. Program the new value to the CONFIG address.
3. Initiate reset.

7.7 Port G

Port G is an eight-bit general-purpose I/O port with a data register (PORTG) and a data direction register (DDRG). When enabled, the upper four lines (PG[7:4] can be used as chip-select outputs in expanded modes. When any of these pins are not being used for chip selects, they can be used for general-purpose I/O. Port G can be configured for wired-OR operation by setting the GWOM bit in the OPT2 register.

NOTE

PG[1:0] are not available on the 64-pin MC68HC11FC0.

7.8 Parallel I/O Registers

Port pin function is mode dependent. Do not confuse pin function with the electrical state of the pin at reset. Port pins are either driven to a specified logic level or are configured as high impedance inputs. I/O pins configured as high-impedance inputs have port data that is indeterminate. The contents of the corresponding latches are dependent upon the electrical state of the pins during reset. In port descriptions, an “I” indicates this condition. Port pins that are driven to a known logic level during reset are shown with a value of either one or zero. Some control bits are unaffected by reset. Reset states for these bits are indicated with a “U”.

PORTA — Port A Data Register **$x000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	I	I	I	I	I	I	I	I
Alternate Function:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

I = Indeterminate value

DDRA — Port A Data Direction Register **$x001**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

PORTG — Port G Data Register **$x002**

	Bit 7	6	5	4	3	2	1	Bit 0
	PG7	PG6	PG5	PG4	PG3	PG2	PG1*	PG0*
RESET:	I	I	I	I	I	I	I	I
Alternate Function:	$\overline{\text{CSPROG}}$	CSGEN	CSIO1	CSIO2				

*These bits are not present on the 64-pin QFP version of the MC68HC11FC0.
I = Indeterminate value

PORTD — Port D Data Register **$x008**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	I	I	I	I	I	I
Alternate Function:	—	—	$\overline{\text{SS}}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Port D Data Direction Register **$x009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

NOTE

When the SPI system is in slave mode, DDD5 has no meaning or effect. When the SPI system is in master mode, DDD5 determines whether bit 5 of PORTD is an error detect input (DDD5 = 0) or a general-purpose output (DDD5 = 1). If the SPI system is enabled and expects one or more of bits [4:2] to be inputs, those bits will be inputs regardless of the state of the associated DDR bits. If one or more of bits [4:2] are expected to be outputs, those bits will be outputs only if the associated DDR bits are set.

PORTE — Port E Data **$x00A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7[1]	PE6	PE5	PE4[2]	PE3	PE2	PE1	PE0[1]
RESET:	U	U	U	U	U	U	U	U
Alternate Function	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

NOTES:

1. These bits are not present on the MC68HC11FC0 and will always read zero.
2. This bit is not present on the 64-pin QFP version of the MC68HC11FC0 and will always read zero.

U = Unaffected by rest.

PORTE is an input-only register. Reads return the digital state of the I/O pins, and writes have no effect. On the MC68HC11F1, port E is shared with the analog-to-digital converter. (The A/D converter is not present on the MC68HC11FC0.)

OPT2 — System Configuration Option Register 2 **$x038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	CLK4X	LIRDV	—	SPRBYP	—	—
RESET	0	0	1	0	0	0	0	0

GWOM — Port G Wired-OR Mode Option

This bit affects all port G pins together.

0 = Port G outputs are normal CMOS outputs
1 = Port G outputs act as open-drain outputs

8 Chip-Selects

Chip selects eliminate the need for additional external components to interface with peripherals in expanded non-multiplexed modes. Chip-select registers control polarity, address block size, base address, and clock stretching.

8.1 Chip-Select Operation

There are four programmable chip selects on the MC68HC11F1 and MC68HC11FC0: two for external I/O (CSIO1 and CSIO2), one for external program space ($\overline{\text{CSPROG}}$), and one general-purpose chip select (CSGEN).

$\overline{\text{CSPROG}}$ is active low and becomes active at address valid time. $\overline{\text{CSPROG}}$ is enabled by the PCSEN bit of the chip-select control register (CSCTL). Its address block size is selected by the PSIZA and PSIZB bits of CSCTL.

Use the I/O chip selects (CSIO1 and CSIO2) for external I/O devices. These chip-select addresses are found in the memory map block that contains the status and control registers. CSIO1 is mapped from \$x060 to \$x7FF, and CSIO2 is mapped from \$x800 to \$xFFF, where x represents the REG[3:0] bits of the INIT register on the MC68HC11F1 or the REG[1:0] bits of the INIT register on the MC68HC11FC0. Polarity and enable-disable selections are controlled by CSCTL register bits IO1EN, IO1PL, IO2EN, and IO2PL. The IO1AV and IO2AV bits of the CSGSIZ register determine whether the chip selects are valid during address or E-clock valid times.

The general-purpose chip select is the most flexible of the four chip selects. Polarity, valid assertion time, and block size are determined by the GNPOL, GAVLD, GSIZA, GSIZB, and GSIZC bits of the CSGSIZ register. The starting address is selected with the CSGADR register.

Each of the four chip selects has two associated bits in the chip-select clock stretch register (CSSTRH). These bits allow clock stretching from zero to three cycles (full E-clock periods) to accommodate slow device interfaces. Any of the chip selects can be programmed to cause a clock stretch to occur only during access to addresses that fall within that particular chip select’s address range.

During the stretch period, the E-clock is held high and the bus remains in the state that it is normally in at the end of E high time. Internally, the clocks continue to run, which maintains the integrity of the timers and baud-rate generators.

Priority levels are assigned to prevent the four chip selects from conflicting with each other or with internal memory and registers. There are two sets of priorities controlled by the value of the general-purpose chip-select priority bit (GCSPR) of the CSCTL register. Refer to **Table 17**.

8.2 Chip-Select Registers

CSSTRH — Clock Stretching **\$x05C**

	Bit 7	6	5	4	3	2	1	Bit 0
	IO1SA	IO1SB	IO2SA	IO2SB	GSTHA	GSTHB	PSTHA	PSTHB
RESET:	0	0	0	0	0	0	0	0

IO1SA, IOS1B — I/O Chip-Select 1 Clock Stretch

IO2SA, IO2SB — I/O Chip-Select 2 Clock Stretch

GSTHA, GSTHB — General-Purpose Chip-Select Clock Stretch

PSTHA, PSSTHB — Program Chip-Select Clock Stretch

Each pair of bits selects the number of clock cycles of stretch for the corresponding chip select.

PCSEN — Program Chip-Select Enable

Reset clears PCSEN in single-chip modes and sets PCSEN in expanded modes.

0 = CSPROG disabled
1 = CSPROG enabled

PSIZA, PSIZB — Select Size of Program Chip-Select

Table 18 Program Chip Select Size Control

PSIZA	PSIZB	Size	Address Range
0	0	64 Kbytes	$0000–$FFFF
0	1	32 Kbytes	$8000–$FFFF
1	0	16 Kbytes	$C000–$FFFF
1	1	8 Kbytes	$E000–$FFFF

CSGADR — General-Purpose Chip-Select Address Register **$x05E**

	Bit 7	6	5	4	3	2	1	Bit 0
	GA15	GA14	GA13	GA12	GA11	GA10	—	—
RESET:	0	0	0	0	0	0	0	0

GA[15:10] — General-Purpose Chip-Select Starting Address

These bits determine the starting address of the CSGEN valid address space and correspond to the high-order address bits ADDR[15:10]. **Table 19** illustrates how the block size selected determines which of this register's bits are valid.

Table 19 General Purpose Chip Select Starting Address

CSGEN Block Size	CSGADR Bits Valid
0 Kbytes	None
1 Kbyte	GA15 – GA10
2 Kbytes	GA15 – GA11
4 Kbytes	GA15 – GA12
8 Kbytes	GA15 – GA13
16 Kbytes	GA15 – GA14
32 Kbytes	GA15
64 Kbytes	None

Bits [1:0] — Not implemented. Reads always return zero and writes have no effect.

CSGSIZ — General-Purpose Chip-Select Size Register **$x05F**

	Bit 7	6	5	4	3	2	1	Bit 0
	IO1AV	IO2AV	—	GNPOL	GAVLD	GSIZA	GSIZB	GSIZC
RESET:	0	0	0	0	0	1	1	1

IO1AV — I/O Chip-Select 1 Address Valid

0 = CSIO1 is valid during E-clock valid time (E-clock high)
1 = CSIO1 is valid during address valid time

IO2AV — I/O Chip-Select 2 Address Valid

0 = CSIO2 is valid during E-clock valid time (E-clock high)
1 = CSIO2 is valid during address valid time

9 Serial Communications Interface (SCI)

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is one of two independent serial I/O subsystems in the MC68HC11F1 and MC68HC11FC0. The SCI has a standard non-return to zero (NRZ) format (one start bit, eight or nine data bits, and one stop bit) and several selectable baud rates. The transmitter and receiver are independent but use the same data format and bit rate.

9.1 SCI Block Diagrams

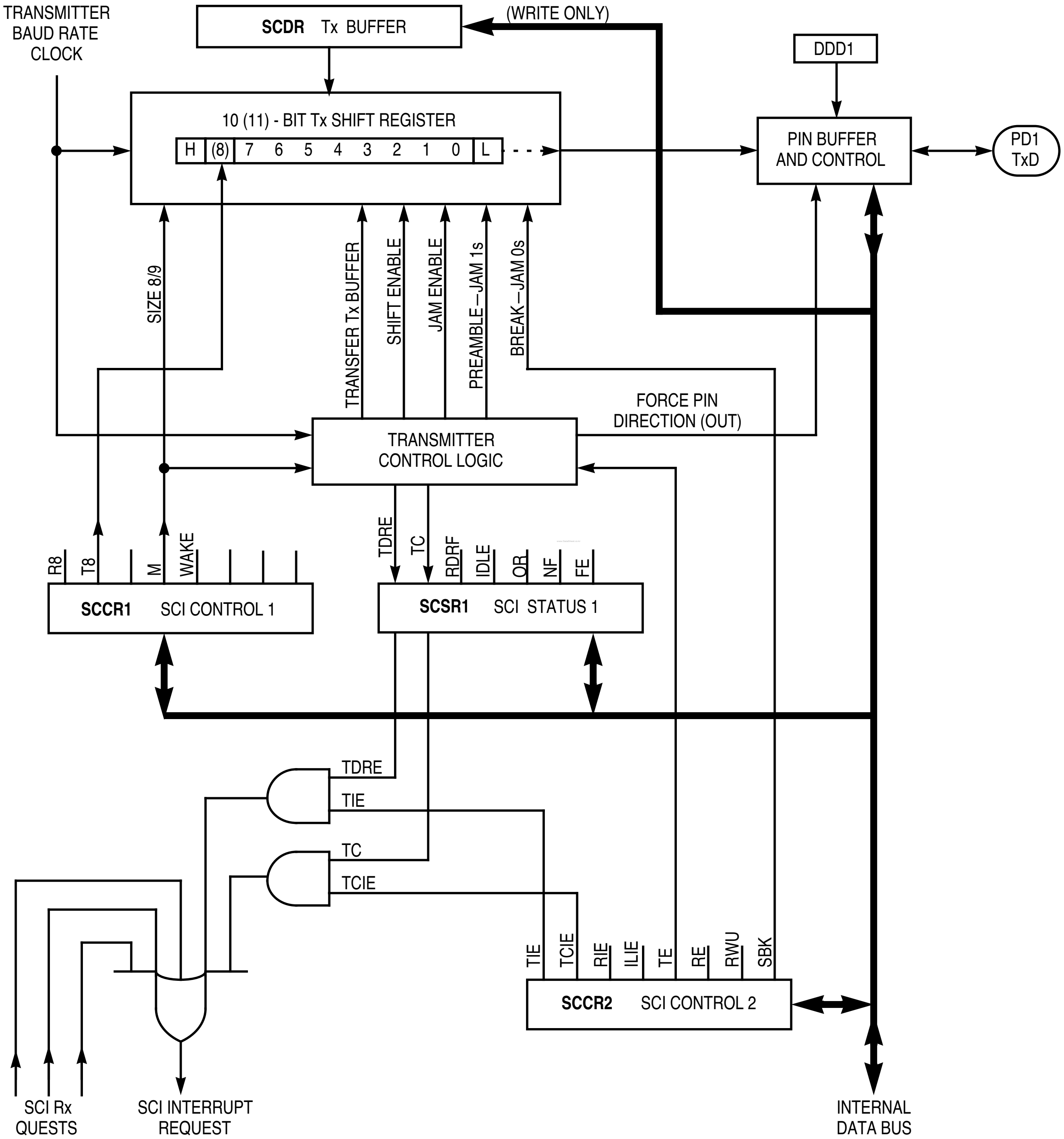


Figure 9 SCI Transmitter Block Diagram

Home Page:
www.freescale.com
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support@freescale.com
Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com
Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com
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