MC68HC33

Technical Summary

Port-Replacement Unit

1 Introduction

The MC68HC33 single-chip integration module (SCIM) port-replacement unit (PRU) replaces the SCIM general-purpose I/O ports that are lost when the microcontroller unit (MCU) is placed in expanded mode. The MC68HC33 is suitable for emulator applications as a port replacement unit or for parallel I/O in expanded systems. The MC68HC33 can be used with any 16- or 32-bit modular microcontroller that contains the SCIM. It can also be used for port expansion with any 16- or 32-bit MCU that contains the system integration module (SIM).

1.1 Features

- Suitable for emulator applications or as a parallel I/O expansion unit
- Compatible with all 16- and 32-bit modular microcontrollers
- Software compatible with single-chip operation of all 16- and 32-bit modular microcontrollers that use a SCIM
- Uses MDA15 standard cell methodology and 1.5-micron CMOS, 2-layer metal technology

Ordering Information

Package Type	Frequency	Temperature	Order Number
100-pin QFP	16.78 MHz	0° to 70°C –40 to 85°C –40 to 125°C	MC68HC33FG MC68HC33CFG MC68HC33MFG

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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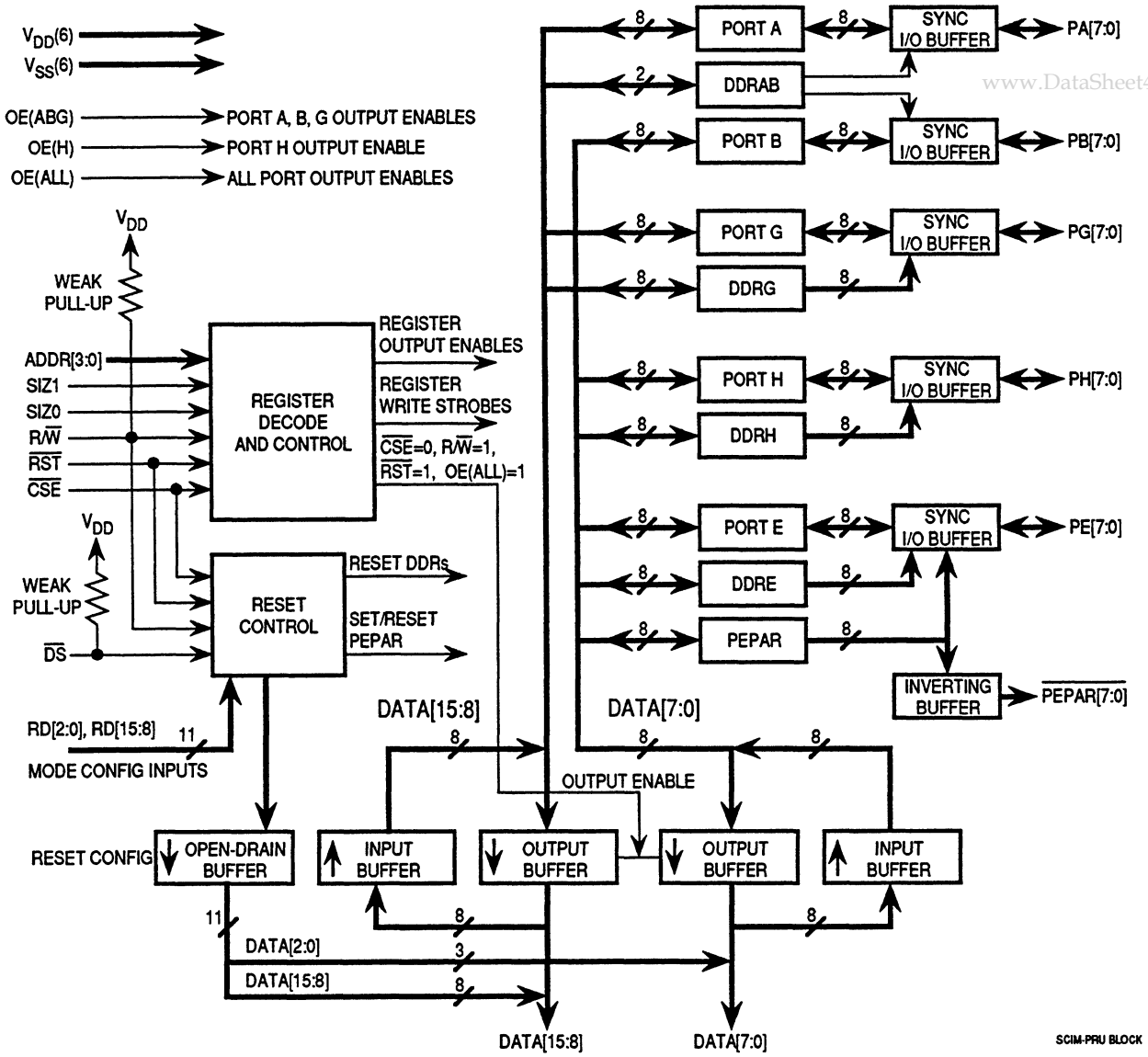
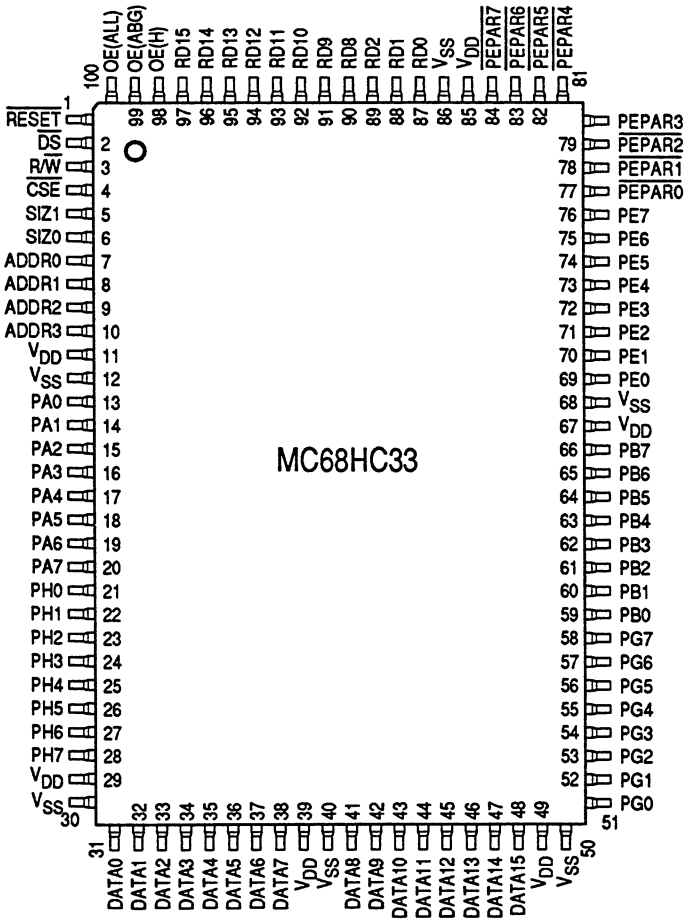
1.2 Block Diagram

A block diagram of the MC68HC33 is shown below.



MC68HC33 Block Diagram

1.3 Pin Assignments

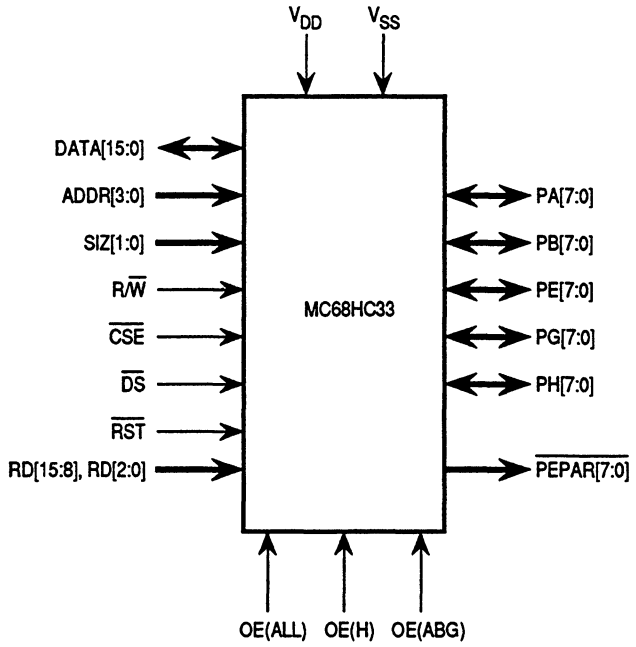


SCIM-PRU 100-PIN QFP

MC68HC33 Pinout

2 Pin Descriptions

The MC68HC33 makes use of all 100 available pins. The following diagram provides an overview of MC68HC33 pins.



MC68HC33 Pin Overview

2.1 Pin Characteristics

Pin Name	Function	Direction	Hysteresis	Quantity
ADDR[3:0]	Address bus	In	N	4
$\overline{CSE}$	Chip select	In	N	1
DATA[15:0]	Data bus	I/O	Y	16
$\overline{DS}$	Data strobe	In	Y	1
OE(ABG)	Port output enable	In	Y	1
OE(ALL)	Port output enable	In	Y	1
OE(H)	Port output enable	In	Y	1
PA[7:0]	Port A	I/O	Y	8
PB[7:0]	Port B	I/O	Y	8
PE[7:0]	Port E	I/O	Y	8
PG[7:0]	Port G	I/O	Y	8
PH[7:0]	Port H	I/O	Y	8
$\overline{PEPAR[7:0]}$	Port E pin-assignment register output	Out	—	8
RD[15:8], RD[2:0]	Reset data control	In	Y	11
$\overline{RST}$	Reset	In	Y	1
R/$\overline{W}$	Read/$\overline{Write}$ select	In	N	1
SIZ[1:0]	Size control	In	N	2
V_{DD}	5-Volt supply	Power	—	6
V_{SS}	Ground	Power	—	6

2.2 System Power and Ground (V_{DD}, V_{SS})

The six V_{DD} pins supply the positive voltage source to the MC68HC33. The actual operating range of the power supply is specified in **6 Electrical Characteristics**. All V_{DD} pins must be connected to the positive voltage source for proper operation.

The six V_{SS} pins provide a current return path for the MC68HC33 power supply. All signal levels are referenced to V_{SS}. For proper operation, all V_{SS} pins must be connected to the power supply return.

2.3 Reset ($\overline{RST}$)

Connect this active-low input to the $\overline{RST}$ line on the MCU. Refer to **3 Reset Operation** for more information on this signal.

2.4 Address Bus (ADDR[3:0])

Connect these inputs to ADDR[3:0] of the MCU. These lines are used in conjunction with the SIZE and R/$\overline{W}$ lines to generate the MC68HC33 internal register-select and write-strobe signals. The MC68HC33 registers are memory-mapped in exactly the same way as the associated registers in the SCIM. The MC68HC33 ignores the state of the address lines unless $\overline{CSE}$ is asserted. Refer to **4 Bus Operation** for more information.

2.5 Data Bus (DATA[15:0])

Connect these 16 bidirectional MC68HC33 pins to the 16 most significant data lines on the controlling MCU. Their purpose is to transfer data between the MCU and the MC68HC33. In order to function properly, the MC68HC33 must be connected to a 16-bit data bus. Refer to **4 Bus Operation** for more information on these pins.

2.6 Reset Data Control (RD[15:8], RD[2:0])

Tie these eleven input pins high or low depending on the state desired on the data bus when $\overline{RST}$ is asserted. Refer to **3 Reset Operation** for more information on these pins.

2.7 Bus Control Signals

These signals control bus transfer operations between the MCU and the MC68HC33.

2.7.1 Size (SIZ[1:0])

Connect these two input pins to the SIZ[1:0] output pins of the MCU. These signals, in conjunction with ADDR0, permit correct operation of byte and word bus cycles. They are also necessary to fully support misaligned accesses. For a detailed discussion of the SIZ[1:0] pins, refer to the appropriate MCU user's manual.

2.7.2 Read/$\overline{\text{Write}}$ (R/$\overline{W}$)

Connect this input pin to the R/$\overline{W}$ output pin of the MCU. When $\overline{CSE}$ is asserted and R/$\overline{W}$ is high, denoting a read cycle, the MC68HC33 drives the data onto the data bus. When $\overline{CSE}$ is asserted, R/$\overline{W}$ is low (denoting a write cycle), and a valid MC68HC33 address is selected, the MCU writes data into the appropriate MC68HC33 register.

Since the SCIM places the R/$\overline{W}$ pin of the PRU in a high-impedance state when reset is recognized, an internal weak pull-up is present on the R/$\overline{W}$ input. This is necessary to qualify $\overline{RST}$ to the MC68HC33. Refer to **3 Reset Operation** for additional information on qualifying the $\overline{RST}$ signal.

2.7.3 Data Strobe ($\overline{DS}$)

Connect this input pin to the MCU $\overline{DS}$ output pin. This signal determines whether or not valid data is present on the data bus. The MC68HC33 uses this signal to qualify the $\overline{RST}$ input. This prevents data bus contention between the reset configuration drivers on the MC68HC33 and an external bus cycle when an asynchronous reset is asserted.

Since the SCIM places the $\overline{DS}$ pin of the MC68HC33 in a high-impedance state during reset, an internal weak pull-up is present on the $\overline{DS}$ input. This is necessary to qualify $\overline{RST}$ to the MC68HC33. For additional information on $\overline{RST}$ qualification, refer to **3 Reset Operation**.

2.8 Chip Select ($\overline{CSE}$)

When using the MC68HC33 for emulation, tie this active-low input to the $\overline{CSE}$ output of the MCU. This signal selects the MC68HC33 as the target of the current bus cycle. Whenever the SCIM is operating in fully-expanded mode, the port control registers which become unusable are mapped into external space. When a read or write to one of these addresses occurs while the SCIM is in emulator mode, the SCIM $\overline{CSE}$ signal is asserted. This allows the MC68HC33 to perform the

functions of those registers, regardless of the base address into which they are mapped. The rising edge of $\overline{CSE}$ marks the termination of the bus cycle.

If the MC68HC33 is being used as a general-purpose I/O expansion chip (not for emulating the ports lost due to bus expansion), then any general-purpose chip select can be used to drive the $\overline{CSE}$ pin.

2.9 Output Enables

These signals enable MC68HC33 ports for output.

2.9.1 Port H Enable (OE(H))

This active-high input enables the output drivers on port H. This allows the MC68HC33 to faithfully emulate the SCIM's partially-expanded mode (8-bit data bus). If a port H pin is configured for output (the corresponding DDRH signal is high) and both OE(H) and OE(ALL) are asserted, the pin is enabled for output. If the pin is configured for input (the DDRH signal is low), the OE(H) and OE(ALL) pins have no effect. A sample configuration is provided in **7 Applications** that illustrates the use of this pin.

2.9.2 Ports A-B-G Output Enable (OE(ABG))

This active-high input enables the output drivers on ports A, B, and G. OE(ABG), in conjunction with OE(H), allows the MC68HC33 to faithfully emulate the SCIM's fully-expanded mode. When both OE(ABG) and OE(H) are low, these four ports are placed in a high-impedance state, allowing the MCU's expanded-mode SCIM pins to drive these nodes. This is necessary for cost-effective emulator construction.

If a port A, B, or G pin is configured for output (the corresponding DDR signal is high) and both OE(ABG) and OE(ALL) are asserted, the pin is enabled for output. If the pin is configured for input (the DDR signal is low), the OE(ABG) and OE(ALL) pins have no effect. A sample configuration is provided in **7 Applications** that illustrates the use of this pin.

2.9.3 All Ports Output Enable (OE(ALL))

This active-high input enables the output drivers on all output and I/O pins. If OE(ALL) is low, all MC68HC33 outputs are disabled, regardless of the state of any other pin. If OE(ALL) is high, all I/O pins are controlled by their respective data direction registers (DDRs) or control pins (or DDRE and PEPAR in the case of port E), and dedicated output pins become enabled. Note that OE(ABH) and OE(G) may also disable their respective ports.

The main purpose of this signal is to ease board-level testing. For normal MC68HC33 operation, tie OE(ALL) high.

2.10 Ports

40 pins on the MC68HC33 serve as ports A, B, E, G, and H. All port I/O pins latch the input state on the falling edge of $\overline{CSE}$. Refer to **5 Registers** for descriptions of the data, data direction, and pin-assignment registers associated with MC68HC33 ports. Refer to **6 Electrical Characteristics** for timing specifications.

2.10.1 Port A (PA[7:0])

These eight bidirectional pins replace the port A function lost when the controlling MCU is operated in fully-expanded mode. The pins behave as though they are the port A pins on the controlling MCU.

2.10.2 Port B (PB[7:0])

These eight bidirectional pins replace the port B function lost when the controlling MCU is operated in fully-expanded mode. The pins behave as though they are the port B pins on the controlling MCU.

2.10.3 Port E (PE[7:0])

These eight bidirectional pins replace the port E function lost when the controlling MCU is operated in fully-expanded mode. The pins behave as though they are the port E pins on the controlling MCU.

2.10.4 Port G (PG[7:0])

These eight bidirectional pins replace the port G function lost when the controlling MCU is operated in fully-expanded mode. The pins behave as though they are the port G pins on the controlling MCU.

2.10.5 Port H (PH[7:0])

These eight bidirectional pins replace the port H function lost when the controlling MCU is operated in fully-expanded mode. The pins behave as though they are the port H pins on the controlling MCU.

2.11 Port E Pin Assignment Register Outputs ($\overline{\text{PEPAR[7:0]}}$)

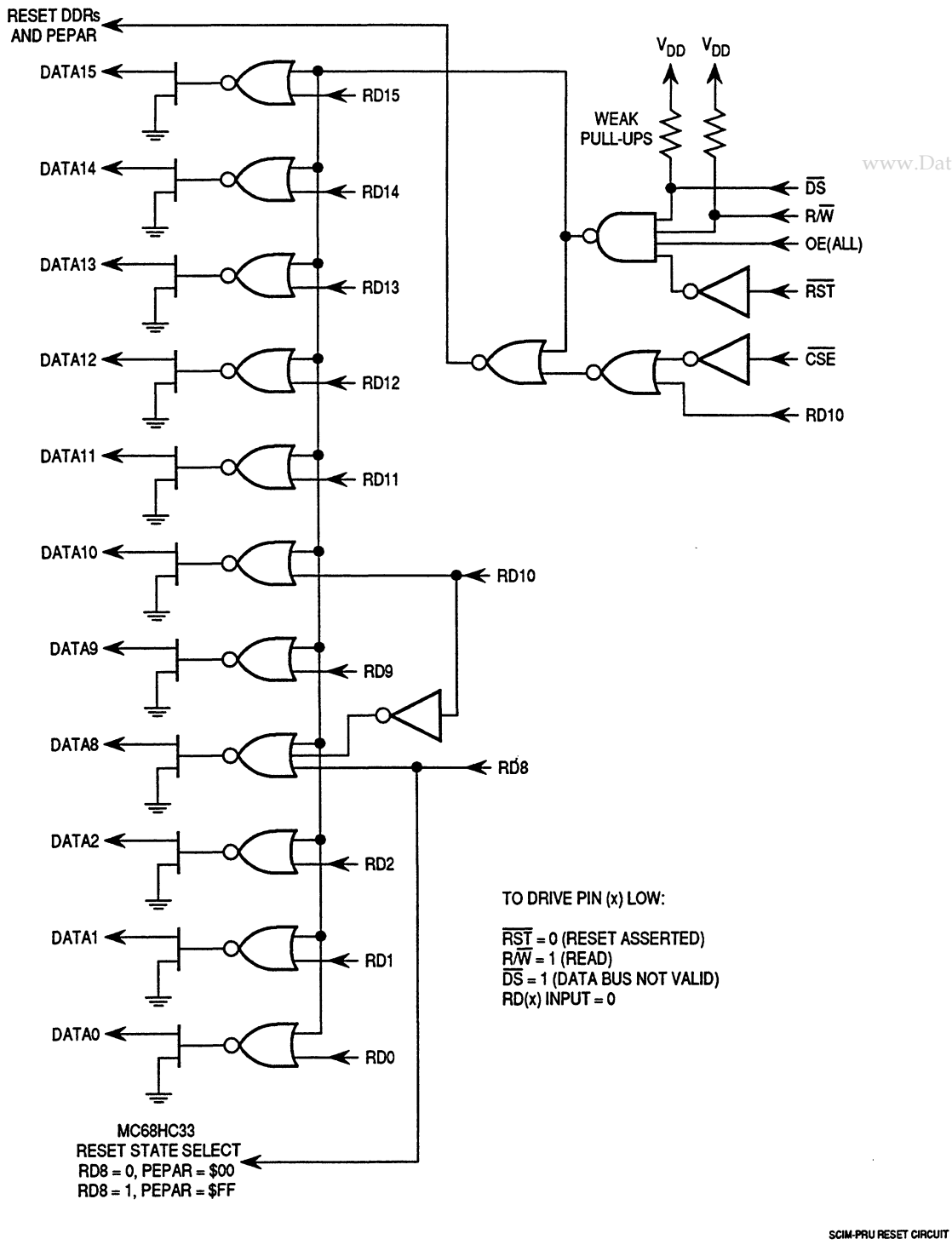
These eight active-low output pins reflect the complement of the PEPAR register contents. These outputs are necessary in some emulation systems. They allow dynamic control of external transmission gates connected to the MCU in order to select port E function or bus control function on a pin-by-pin basis. The output pins are active-low (the complement of PEPAR value) because most transmission gates are on when their gate input is low. This condition selects the bus control function for the target system and places the appropriate port E I/O pin of the MC68HC33 in a high-impedance state. A sample emulation system is provided in **7 Applications** that illustrates the use of these pins.

The state of the $\overline{\text{PEPAR[7:0]}}$ pins during and after reset is controlled by the RD8 pin. If RD8 is low during reset, the $\overline{\text{PEPAR[7:0]}}$ output pins are high. (The actual PEPAR register contents are 0x00.) If RD8 is high during reset, the $\overline{\text{PEPAR[7:0]}}$ output pins are low. (The PEPAR register contents are 0xFF.)

Note that the $\overline{\text{PEPAR[7:0]}}$ pins are placed in a high-impedance state unless OE(ALL) is high.

3 Reset Operation

The MC68HC33 reset circuit is shown below. Notice that the requirements for recognition of the reset ($\overline{\text{RST}}$) signal are different for the data direction registers (DDRs) than for the data bus pins. In addition, a special set of conditions governs the DATA8 pin, in order to provide access to the SCIM bus control signals.



MC68HC33 Reset Circuit

3.1 DDR Reset

When the $\overline{RST}$ signal is recognized as asserted, all the MC68HC33 data direction registers are cleared, causing all port I/O lines to be configured as inputs.

For $\overline{RST}$ to be recognized, R/$\overline{W}$ must be high, indicating a read cycle, and $\overline{DS}$ must be high, indicating that no valid data is present on the data bus. This ensures that SCIM write bus cycles (to external devices) are not abnormally terminated. Since the SCIM places R/$\overline{W}$ and $\overline{DS}$ in a high-impedance state during reset, weak pull-ups are provided on these inputs.

A further requirement for recognition of $\overline{RST}$ is that either $\overline{CSE}$ must be asserted (low) or RD10 must be high. When in emulation mode, the SCIM will drive $\overline{CSE}$ whenever the MC68HC33 registers are to be reset. This allows the MC68HC33 to ignore the peripheral reset issued by the CPU RESET instruction. When RD10 is high, the MC68HC33 is not being used for port emulation, so $\overline{RST}$ is recognized regardless of whether $\overline{CSE}$ is asserted. In this case, the MC68HC33 behaves as a normal external peripheral.

3.2 DATA Pins Reset

When the mode configuration circuitry recognizes $\overline{RST}$, any SCIM reset mode-configuration pins (DATA[15:8] and DATA[2:0]) are driven low if their associated control inputs (RD[15:8] and RD[2:0]) are tied low. If a reset data control pin is high, the corresponding data bus pin is not driven by the MC68HC33 when $\overline{RST}$ is asserted. Since the data bus pin is allowed to float, the SCIM may pull the pin up, or an external device may pull the pin low. The behavior of the DATA8 pin is an exception to this scheme. Refer to **3.3 SCIM PEPAR Reset** for more information.

When DATA10 is pulled low during reset, the SCIM is configured for emulator mode. This causes the SCIM to select the $\overline{CSE}$ output function for the $\overline{BGACK}$/$\overline{CSE}$ pin and maps SCIM port register accesses (ports A, B, E, G, and H) to the external data bus. In addition, the SCIM selects the $\overline{CSM}$ output function for the $\overline{BG}$/$\overline{CSM}$ pin. This allows external emulation of internal ROM.

For the mode configuration circuitry to recognize $\overline{RST}$, R/$\overline{W}$ and $\overline{DS}$ must be high. This prevents write-cycle corruption but allows SCIM configuration. To allow SCIM configuration, $\overline{RST}$ cannot be qualified with $\overline{CSE}$ and RD10 (as is $\overline{RST}$ recognition for the DDRs, discussed in the preceding paragraphs).

Refer to the SCIM reference manual or the appropriate MCU user's manual for a complete discussion of data bus pins and system configuration.

3.3 SCIM PEPAR Reset

Since a user might require ROM emulation in an expanded system, the configuration of the SCIM PEPAR must be user-selectable. The application might require all port E pins for discrete I/O. However, whenever the MC68HC33 is used in a design, it requires the SIZ[1:0] signals to operate properly.

To ensure proper operation, if RD10 is tied low, enabling emulator mode, data bus pin DATA10 is driven low, and DATA8 is not driven during reset; it is allowed to be pulled high by the SCIM. This causes the SCIM port E pin assignment register (PEPAR) to be set, making the bus control signals (SIZ[1:0], $\overline{DS}$) available. The SIZ signals cannot be turned off in emulation mode because SCIM PEPAR accesses become external bus cycles.

Notice that the reset state of the PEPAR in the MC68HC33 is still determined by the state of RD8. It is set to 0x00 if RD8 is tied low, or 0xFF if RD8 is tied high. Since PEPAR controls whether or not the port E outputs are enabled, this determines if the port E I/O pins become outputs when the DDRE bits are set.

4 Bus Operation

ADDR[3:0] are used in conjunction with the SIZ[1:0] and R/$\overline{W}$ lines to generate the MC68HC33 internal register-select and write-strobe signals. The MC68HC33 registers are memory-mapped in exactly the same way as the associated registers in the SCIM. The MC68HC33 register addresses correspond to the four LSBs of the equivalent SCIM registers. The MC68HC33 ignores the state of the address lines unless $\overline{CSE}$ is asserted.

The SIZ[1:0] signals, in conjunction with ADDR0, permit correct operation of byte, word, and long-word bus cycles. They are also necessary to fully support misaligned accesses. For a detailed discussion of the SIZ[1:0] pins, refer to the appropriate MCU user's manual.

For read cycles when the MC68HC33 is selected (R/$\overline{W}$ = 1, $\overline{CSE}$ = 0), the MC68HC33 outputs the contents of the selected registers onto the data bus. All 16 bits of the data bus are driven during a MC68HC33 read cycle, regardless of the state of the SIZ1 and SIZ0 inputs. The MCU ignores the irrelevant byte during byte reads.

For write cycles (R/$\overline{W}$ = 0, $\overline{CSE}$ = 0), the MCU writes data into the appropriate PRU register. The MC68HC33 expects valid data to be terminated by the rising edge of either R/$\overline{W}$ or $\overline{CSE}$.

Note that the data present on all port input and output pins is stored (frozen) in an internal read latch whenever $\overline{CSE}$ is asserted (low). This ensures that the data bus is stable throughout the read cycle. The SCIM, in contrast, synchronizes port read data via an edge-triggered latch (D-type flip flop).

Refer to **6 Electrical Characteristics** for detailed bus cycle timing information.

5 Registers

The MC68HC33 registers are functional duplicates of their SCIM counterparts. All registers may be accessed as bytes, words, or long words. Misalignment is fully supported. Reads of reserved memory locations return zeros and writes have no meaning or effect.

Access to all registers requires three MCU clock cycles. Port registers are byte-addressable and are grouped to allow coherent word access to port data register pairs A-B and G-H, as well as word-aligned long word coherency of A-B-G-H port data registers.

Data direction for all port data registers is controlled by a data direction register (DDR). DDRE, DDRG, and DDRH designate individual pins in the associated port as input or output. DDRAB contains only two control bits, one for port A and one for port B. Each bit designates the associated port as an input or output port. In addition, port E has a pin assignment register that allows each pin to be selected for I/O or placed in a high-impedance state.

If a data port (or pin) is configured for input, when the software reads the port, the MC68HC33 drives the data bus with the synchronized digital levels (latched on the falling edge of $\overline{CSE}$) that appear on the port input(s). Pins with levels not meeting V_{IL} or V_{IH} specifications have an indeterminate value.

If a port is programmed for output, the value read reflects the contents of the port output latch regardless of the actual state of the pins' input synchronizers. Writes to the data register are stored in the port output latch and will affect the pins only if they are defined as outputs.

5.1 Register Map

The base address of the MC68HC33 is determined by the $\overline{CSE}$ input. The register decode map is fixed. As shown below, the MC68HC33 register addresses correspond to the four LSBs of the equivalent SCIM registers. The areas designated as reserved always return zeros when read, and writes to these locations have no meaning or effect.

MC68HC33 Register Map

$A	PORT A DATA (PORTA)	PORT B DATA (PORT B)	$B
$C	PORT G DATA (PORTG)	PORT H DATA (PORTH)	$D
$E	PORT G DATA DIRECTION (DDRG)	PORT H DATA DIRECTION (DDRH)	$F
$0	RESERVED	PORT E DATA (PORTE)	$1
$2	RESERVED	PORT E DATA (PORTE)	$3
$4	PORT A/B DATA DIRECTION (DDRAB)	PORT E DATA DIRECTION (DDRE)	$5
$6	RESERVED	PORT E PIN ASSIGNMENT (PEPAR)	$7
$8	RESERVED	RESERVED	$9

5.2 Ports A and B

Ports A and B on the MC68HC33 replace ports A and B on the MCU when those pins are used as ADDR[18:11] and ADDR[10:3], respectively. One two-bit data direction register controls data direction for both ports. DDA and DDB, when high, configure ports A and B, respectively, for output. For the outputs to be enabled, both OE(ALL) and OE(ABG) must be asserted.

PORTA — Port A Data Register **$XXXXXA**

7	6	5	4	3	2	1	0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:							
U	U	U	U	U	U	U	U

PORTB — Port B Data Register **$XXXXXB**

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:							
U	U	U	U	U	U	U	U

DDRAB — Port A/B Data Direction Register **$XXXXX4**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DDA	DDB
RESET:							
0	0	0	0	0	0	0	0

DDA and DDB control the direction of the pin drivers for Ports A and B, respectively, when the pins are configured for I/O. Setting DDA or DDB configures all pins in the corresponding port as outputs. For the outputs to be enabled, both OE(ABG) and OE(ALL) must be asserted. Clearing DDA or DDB configures all pins in the corresponding port as inputs.

5.3 Port E

Port E is a single port that appears in the memory map in two locations. This port can be used for general-purpose digital input or output on a pin-by-pin basis. Bits DDE[7:0] in the DDRE configure individual pins for input or output. Bits PEPA[7:0] in the PEPAR configure each port E pin for general-purpose I/O or bus control. If a given pin is defined as an input by DDRE, but the associated PEPAR bit is high (assigning the pin to its control function), reads return the state of the output latch.

Port E pin behavior and results of reads are summarized in the following table.

Port E Read Characteristics and Pin Behavior

DDE(x)	PEPA(x)	Read Data	Pin Behavior
0	0	Synchronized pin level	Discrete input
0	1	Output latch	High impedance
1	0	Output latch	Discrete output
1	1	Output latch	High impedance

Each bit in the DDRE, when high, configures the associated port E I/O pin to be an output. For the output to be enabled, OE(ALL) must be asserted (high) and the associated PEPAR bit must be low. When a bit in the DDRE is low, the associated port E I/O pin is configured as an input.

PORTE — Port E Data Register **$XXXXX1, $XXXXX3**

7	6	5	4	3	2	1	0
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:							
U	U	U	U	U	U	U	U

PORTE is a single register that can be accessed in two locations.

DDRE — Port E Data Direction Register **$XXXXX5**

7	6	5	4	3	2	1	0
DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0
RESET:							
0	0	0	0	0	0	0	0

The bits in this register control the direction of the pin drivers when the pins are configured as I/O. Any bit in this register set to one configures the corresponding pin as an output. Any bit in this register cleared to zero configures the corresponding pin as an input.

PEPAR — Port E Pin Assignment Register **$XXXXX7**

7	6	5	4	3	2	1	0
PEPA7	PEPA6	PEPA5	PEPA4	PEPA3	PEPA2	PEPA1	PEPA0
RESET:							
RD8	RD8	RD8	RD8	RD8	RD8	RD8	RD8

When the SCIM is operating in emulator mode, all reads and writes to PEPAR are directed to the PEPAR of the MC68HC33, rather than the SCIM PEPAR. When a PEPAR bit is low, the associated I/O pin functions as a discrete I/O line. When a PEPAR bit is high, the associated pin is placed in a high-impedance state, and reads of the associated port E data bit return the contents of the output latch.

In addition, the complement values of the PEPAR bits are available as output pins, allowing direct control of active-low transmission gates connected to the SCIM port E control signals. This allows proper functioning of the PEPAR in an emulation environment, while making all SCIM port E bus control signals available at all times. Refer to **7 Applications** for a sample emulation system that uses these signals.

5.4 Port G

Port G on the MC68HC33 replaces the port G function on the MCU when those pins are used as DATA[15:8]. Port G may be used for general-purpose digital input or output on a pin-by-pin basis as determined by its data direction register bits (DDG[7:0] in the DDRG). Each bit in the DDRG, when high, configures the associated port G I/O pin to be an output. For the output to be enabled, both OE(ALL) and OE(ABG) must be asserted (high). When a bit in the DDRG is low, the associated port G I/O pin is configured as an input.

PORTG — Port G Data Register **$XXXXXC**

7	6	5	4	3	2	1	0
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:							
U	U	U	U	U	U	U	U

DDRG — Port G Data Direction Register **$XXXXXE**

7	6	5	4	3	2	1	0
DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:							
0	0	0	0	0	0	0	0

5.5 Port H

Port H on the MC68HC33 replaces the port H function on the MCU when those pins are used as DATA[7:0]. Port H may be used for general-purpose digital input or output on a pin-by-pin basis as determined by its data direction register bits (DDH[7:0] in the DDRH). Each bit in the DDRH, when high, configures the associated port H I/O pin to be an output. For the output to be enabled, both OE(ALL) and OE(H) must be asserted (high). When a bit in the DDRH is low, the associated port H I/O pin is configured as an input.

PORTH — Port H Data Register **$XXXXXD**

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
RESET:							
U	U	U	U	U	U	U	U

DDRH — Port H Data Direction Register **$XXXXXF**

7	6	5	4	3	2	1	0
DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0
RESET:							
0	0	0	0	0	0	0	0

6 Electrical Characteristics

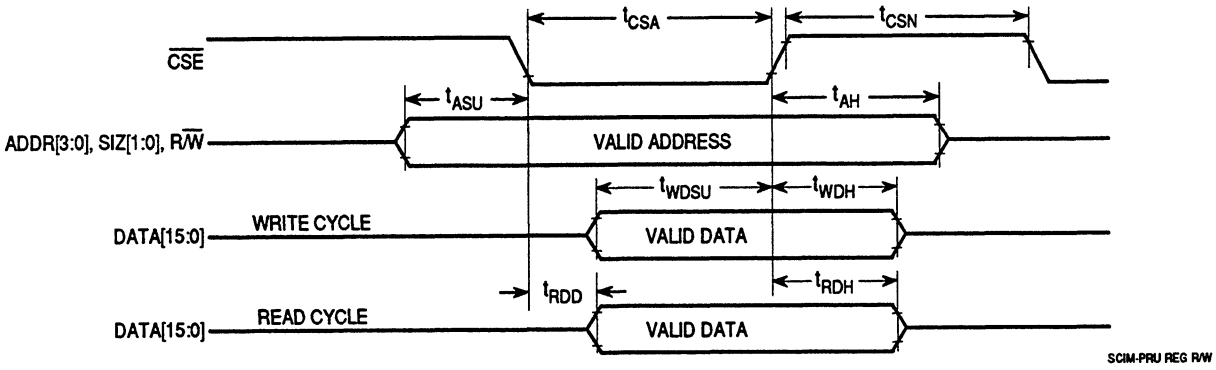
6.1 AC Characteristics

The AC characteristics of the MC68HC33 are summarized in the following table and figures.

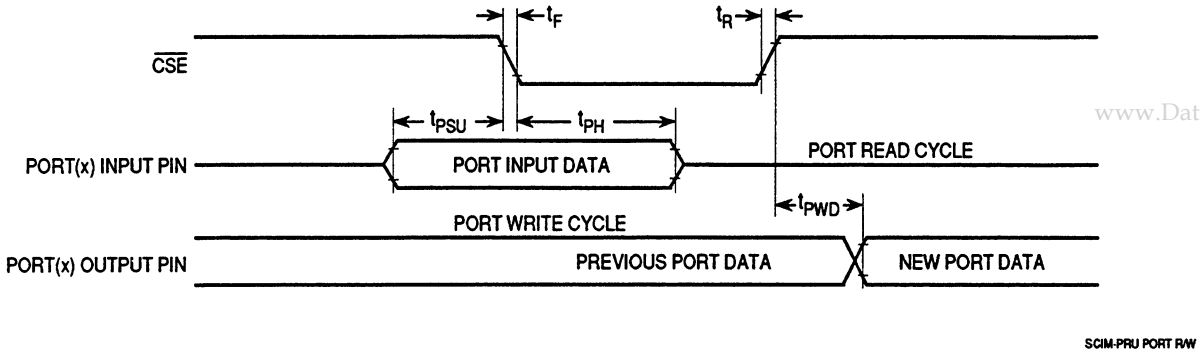
AC Characteristics[1]

Parameter	Symbol	Minimum	Maximum	Units
$\overline{CSE}$ pulse width asserted (low) $\overline{CSE}$ pulse width negated (high)	t_{CSA} t_{CSN}	60 20	— —	ns ns
Address/control setup time (to $\overline{CSE}$ falling) Address/control hold time (from $\overline{CSE}$ rising)	t_{ASU} t_{AH}	0 7	— —	ns ns
Write data setup time (to $\overline{CSE}$ rising) Write data hold time (from $\overline{CSE}$ rising)	t_{WDSU} t_{WDH}	30 7	— —	ns ns
Read data delay time (from $\overline{CSE}$ falling) Read data hold time (from $\overline{CSE}$ rising)	t_{RDD} t_{RDH}	— 0	40 30	ns ns
Port input setup time (to $\overline{CSE}$ falling) Port input hold time (from $\overline{CSE}$ falling)	t_{PSU} t_{PH}	20 10	— —	ns ns
Port write data delay (from $\overline{CSE}$ high)	t_{PWD}	—	50	ns
Rise and fall time (all inputs and outputs)[2]	t_R, t_F	—	30	ns
$\overline{RST}$ pulse width asserted (low)	t_{RA}	50	—	ns

1. All timing characteristics are for V_{DD} = 5.0 V ± 10%, T_A = –40°C to +125°C. All output timing parameters are guaranteed while driving a load of up to 110 pF.
2. Input rise and fall times are not tested.



Read or Write of MC68HC33 Register



Port Read and Write

6.2 DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
DC supply voltage	V_{DD}	–0.5 to +7.0	V
DC input voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V
DC output voltage	V_{OUT}	–0.5 to V_{DD} + 0.5	V
DC current (per pin)	I	±25	mA
DC Current (V_{DD} and V_{SS} pins)	I	±75	mA
Storage temperature	T_{STG}	–65 to +150	°C
Lead temperature	T_L	300	°C

Maximum ratings are those beyond which damage to the device may occur.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
DC supply voltage	V_{DD}	+3.0	+6.0	V
DC input voltage	V_{IN}	0.0	V_{DD}	V
DC output voltage	V_{OUT}	0.0	V_{DD}	V
Ambient operating temperature	T_A	–40	+125	°C

General DC Characteristics

(V_{DD} = 5.0 V_{DC} ± 10%, V_{SS} = 0 V_{DC}, T_A = - 40° to + 125°C

Parameter	Symbol	V_{DD} (V)	Minimum	Typical at 25° C	Maximum	Unit
Input high voltage[1]	V_{IH}	4.5 V	3.15	2.30	—	V
		5.5 V	3.85	2.80	—	V
Input low voltage[1]	V_{IL}	4.5 V	—	2.20	1.35	V
		5.5 V	—	2.70	1.65	V
Input leakage current						
Input-only pins[2]	I_{IN}	5.5 V	–1.0	±0.1	1.0	µA
Input pins with internal pull-ups[3]	I_{ILP}	5.0 V	–310	–140	–40	µA
Output high current[4]	I_{OH}					
$\overline{\text{PEPAR}}$[7:0]		4.5 V	–4	–15	—	mA
Ports		4.5 V	–8	–23	—	mA
DB[15:0]		4.5 V	–16	–60	—	mA
Output low current[4]	I_{OL}					
$\overline{\text{PEPAR}}$[7:0]		4.5 V	4	16	—	mA
Ports		4.5 V	8	25	—	mA
DB[15:0]		4.5 V	16	65	—	mA
High-impedance (off-state) output leakage current[5]	I_{OZ}	5.5 V	–5.0	±0.1	5.0	µA
Quiescent current[6]	I_{DD}	5.5 V	—	10.3	24.8	µA
Input capacitance[7]	C_{IN}	5.0 V	—	10.0	—	pF
Output capacitance[7]	C_{OUT}	5.0 V	—	12.5	—	pF
I/O pin capacitance[7]	$C_{I/O}$	5.0 V	—	15.0	—	pF

NOTES:

1. Applies to ADDR[3:0], SIZ[1:0], $\overline{\text{CSE}}$, and R/$\overline{\text{W}}$ only. All other input and I/O pins have hysteresis, and their input characteristics are described in the Hysteresis Input Characteristics table. V_{IH} and V_{IL} are measured with V_{OUT} = 0.1 V or V_{DD} –0.1 V, $|I_{OUT}|$ = 20 µA.
2. This applies to input-only pins not provided with internal pull-ups. These include RD[15:8], RD[2:0], ADDR[3:0], SIZ[1:0], $\overline{\text{CSE}}$, $\overline{\text{RST}}$, OE(ALL), OE(ABG), and OE(H). I_{IN} is measured with V_{IN} = V_{DD} or V_{SS}.
3. Only R/$\overline{\text{W}}$ and $\overline{\text{DS}}$ have internal pull-ups. I_{ILP} is measured with V_{IN} = V_{SS}.
4. Ports include PA[7:0], PB[7:0], PE[7:0], PG[7:0], and PH[7:0]. I_{OH} is measured with V_{OH} = 3.7 V. I_{OL} is measured with V_{OL} = 0.4 V. User is responsible for limiting output current to the maximum per pin specified in the Absolute Maximum Ratings table.
5. This applies only to I/O and output-only pins. These include DATA[15:0], PA[7:0], PB[7:0], PE[7:0], PG[7:0], PH[7:0], and $\overline{\text{PEPAR}}$[7:0]. I_{OZ} is measured with V_{OUT} = V_{DD} or V_{SS}, and outputs in high-impedance state.
6. V_{IN} = V_{DD} or V_{SS}, I_{OUT} = 0 µA.
7. Capacitance values are sampled periodically, not 100% tested. Capacitance is measured with outputs in high-impedance state and I/O pins configured as inputs.

Hysteresis Input Characteristics

Parameter	Symbol	V_{DD} (V)	Minimum	Typical	Maximum	Unit
Positive-going input threshold	V_{T+}	4.5 5.5	2.75 3.30	3.05 3.68	3.35 4.05	V V
Negative-going input threshold	V_{T-}	4.5 5.5	0.80 1.00	1.25 1.50	1.45 1.75	V V
Input high voltage	V_{IH}	4.5 5.5	3.35 4.05	3.05 3.68	— —	V V
Input low voltage	V_{IL}	4.5 5.5	— —	1.25 1.50	0.80 1.00	V V
Hysteresis voltage	V_H	4.5 5.5	1.30 1.55	1.80 2.18	— —	V V
Test Conditions: V_{OUT} = 0.1 V or V_{DD} - 0.1 V, $\|I_{OUT}\|$ = 20 μA						

This table applies to the following MC68HC33 pins only: PA[7:0], PB[7:0], PE[7:0], PG[7:0], PH[7:0], DATA[15:0], RD[15:8], RD[2:0], OE(ABG), OE(H), OE(ALL), RST, and DS. The properties described here are unique to pins with hysteresis input buffers. Any characteristic not explicitly described in this table is the same as for pins with non-hysteresis input buffers and is covered by the more general tables of this section.

7 Applications

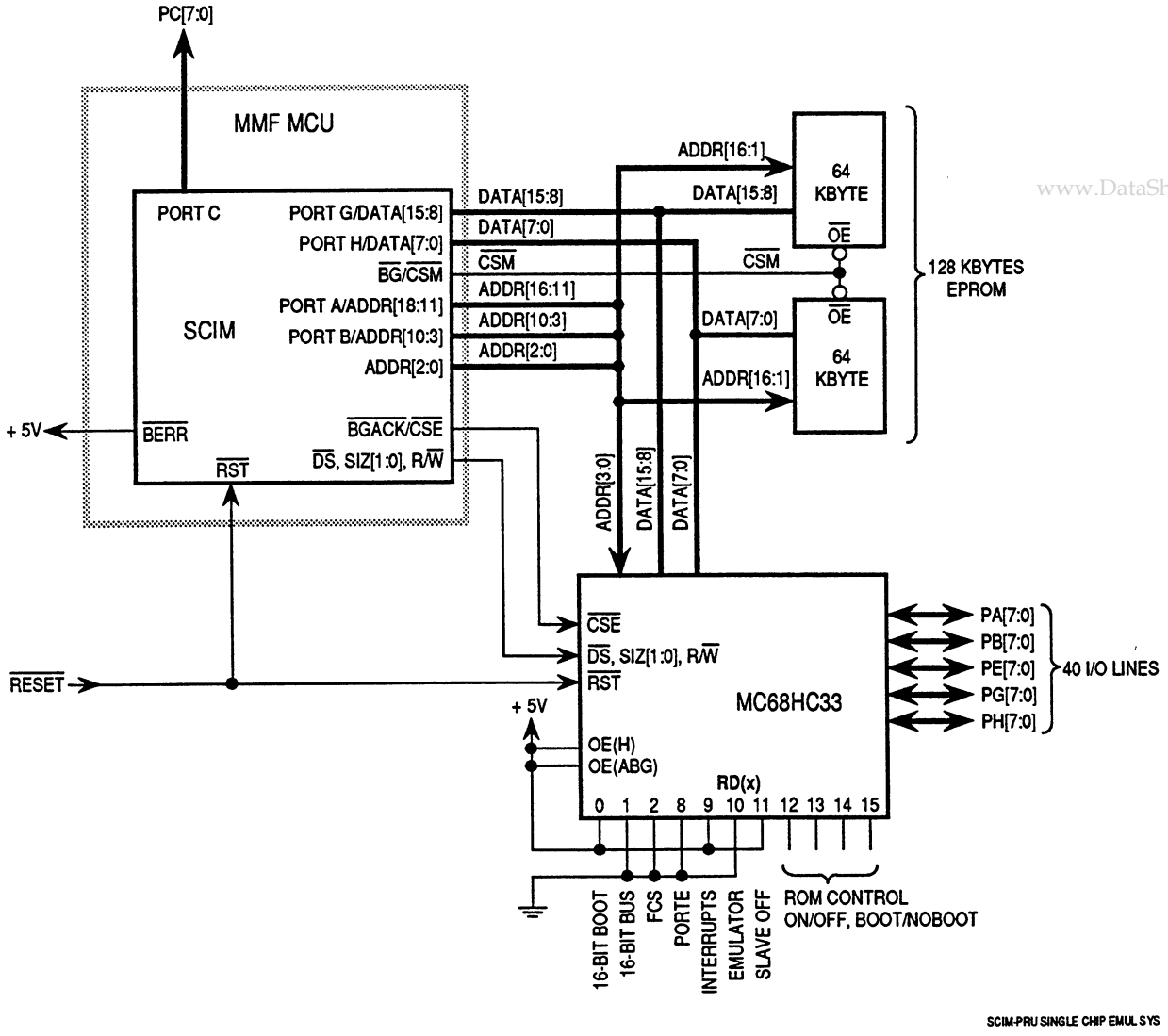
This section describes a basic single-chip emulation system using the MC68HC33, then a more complex system that allows emulation of all three operating modes (single chip, 8-bit expanded, and 16-bit expanded).

7.1 Single-Chip Emulation System

When most MCUs are operated in single-chip mode, critical address, data, and control signals become parallel ports and are unavailable to aid in debugging the application firmware. The MC68HC33 makes it easy to build a system that makes the parallel ports and the signals they normally replace available simultaneously. This allows the creation of a firmware debug environment that accurately emulates the operation of the final single-chip system.

Single-chip MCU systems normally use an MCU that contains on-chip non-volatile memory, usually ROM or EPROM. It is desirable to have an emulation system that can support the development of firmware to be incorporated into the internal ROM.

The basic development system pictured on the following page fulfills these requirements. The MC68HC33 is connected so that it replaces the lost ports when the MCU is operated in the expanded mode. A logic analyzer may be used to monitor address, data, and bus control signals. Firmware may be simulated using the 128 Kbytes of EPROM. The SCIM's $\overline{\text{CSM}}$ signal provides the EPROM chip select for on-chip ROM emulation. This ensures wait-state generation and address-space decoding characteristics that are identical to those of the on-chip ROM array.



Basic Emulation System

7.2 Universal Emulation System

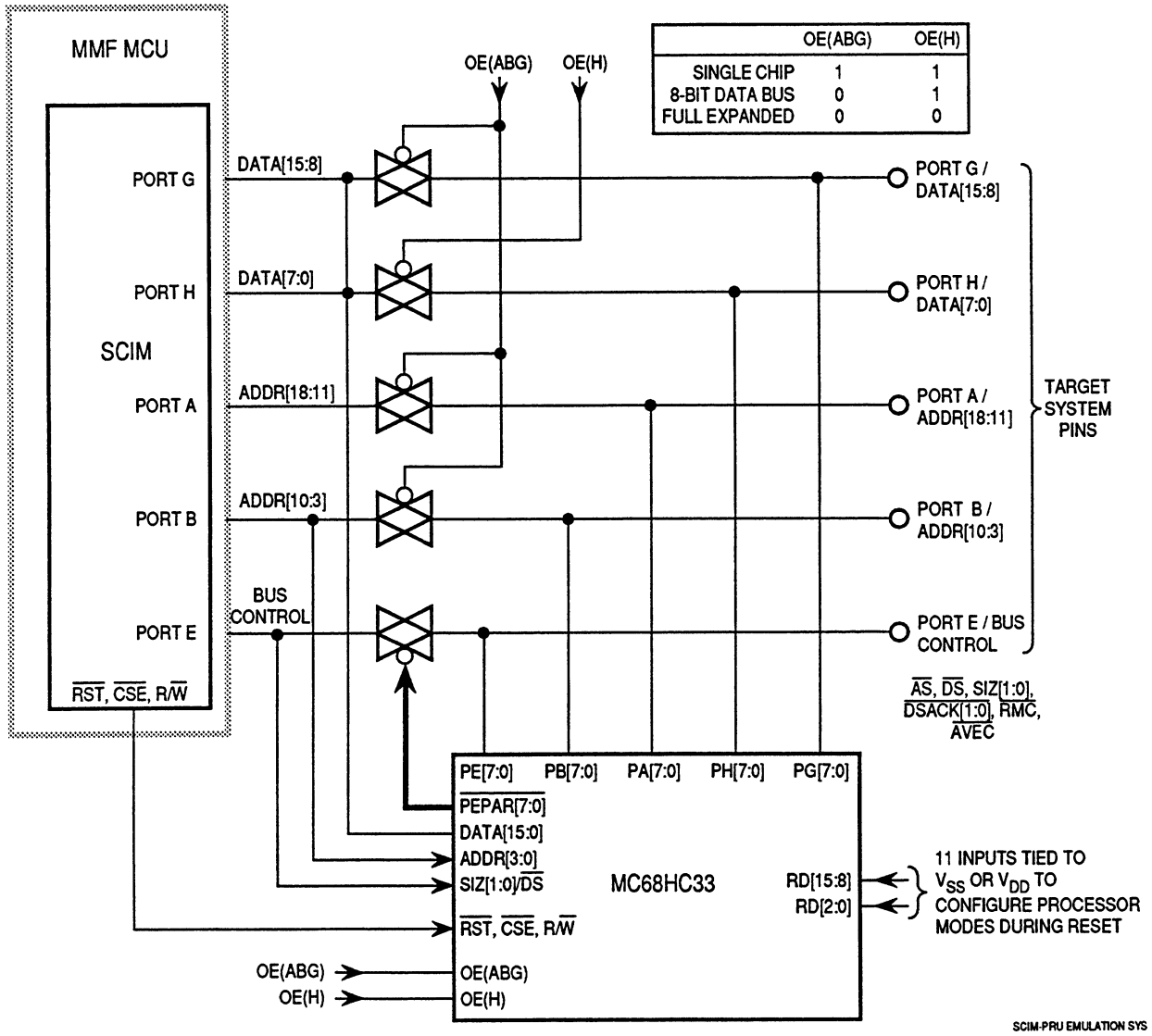
When an MCU emulator based on the SCIM is built, it may not be known whether the target system will require emulation of fully expanded mode (16-bit data bus), partially expanded mode (8-bit data bus), or single-chip mode. It is therefore necessary for the emulator to be able to mimic all three modes. Such a system is depicted in the accompanying diagram.

Regardless of the operating mode being emulated, the MCU is always operated in fully expanded mode. Different combinations of logic levels for OE(ABG) and OE(H) result in different emulation modes. In all cases, the PEPAR[7:0] outputs of the MC68HC33 select which MCU pins and which MC68HC33 pins will drive the port E pins of the target system. If a given bit in the PEPAR register is high, the corresponding PEPAR pin will be low and will select the MCU's bus control pin to drive the target system. The corresponding MC68HC33 port E output pin is automatically placed in a high-impedance state.

To emulate single-chip mode in this system, drive OE(H) and OE(ABG) high. This turns off the transmission gates connected to the address and data buses, isolating the MCU pins from the target system pins. At the same time, MC68HC33 ports A, B, G, and H are enabled and can drive the target system pins.

To emulate 8-bit expanded mode, drive OE(H) high and OE(ABG) low. This turns on the transmission gates connecting the target system pins to the MCU's address bus and the upper eight bits of the data bus. MC68HC33 ports A, B, and G are placed in a high-impedance state. The transmission gates connecting the target system to the lower eight bits of the MCU's data bus are turned off, and the MC68HC33 port H is enabled to drive the target system pins.

To emulate fully expanded mode, drive OE(H) and OE(ABG) low. This turns on the transmission gates connecting the target system pins to the address and data buses of the MCU. At the same time, MC68HC33 ports A, B, G, and H are placed in a high-impedance state.



Universal Emulation System

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MC68HC33/D