MOTOROLA

MC68HC68R1
MC68HC68R2

Advance Information

HCMOS
(HIGH-DENSITY CMOS SILICON-GATE)

8-BIT SERIAL STATIC RAMs

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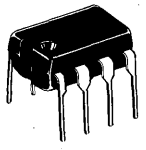
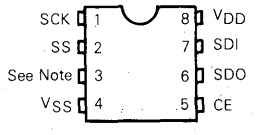
The MC68HC68R1 and MC68HC68R2 are serially organized 128-word (MC68HC68R1) or 256-word (MC68HC68R2) by 8-bit static random access memories (RAMs). These RAMs are intended for use in systems where minimum package and interconnect size, low power, and simplicity of use are desirable; for example, in systems utilizing synchronous serial 3-wire (clock, data in, data out) interfaces. Interface can be made with the MC68HC05D2 without additional components, provided the MC68HC05D2 SPI control register bits CPHA and CPOL are set.

- Fully Static Operation
- Operating Voltage Range: 3 V to 5.5 V
- Maximum Standby Current = 2 μA
- Directly Compatible with SPI Interface
- Separate Data Input and Data Output Pins
- Input Data and Clock Buffers Gated Off with Chip Enable
- Protocol for Fast Sequential Multiple Byte Accesses
- Minimum Data Retention Voltage: 2 V
- Small 8-Lead Plastic Package



P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN ASSIGNMENT



NOTE:
Pin 3 = N/C for MC68HC68R1
Pin 3 = A7 for MC68HC68R2

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SIGNAL DESCRIPTION

CHIP ENABLE AND SLAVE SELECT (CE AND SS)

A high level on the CE pin, coincident with a low level on the SS pin, is required for the RAM serial interface logic to become enabled. The device is held in the reset state if either CE is low or SS is high.

SERIAL CLOCK (SCK)

This clock input is used to synchronously latch data in and shift data out of the RAM chip.

SERIAL DATA IN (SDI)

Serial data, present at this port, is latched into the RAM chip by SCK if the chip is enabled and in a write cycle.

SERIAL DATA OUT (SDO)

Serial data is shifted out of this port by SCK if the RAM chip is enabled and in a read cycle.

V_{DD} AND V_{SS}

The V_{DD} pin is the +5 volt power supply and V_{SS} is the ground reference pin.

ADDRESS LINE (A7) — MC68HC68R2 ONLY

This address input is used in the 256-word RAM version to select either of two 128-word memory areas. (Address bits A0-A6, used to provide the address within the 128-word memory area in both the MC68HC68R1 and MC68HC68R2 versions, are the seven least significant bits of the first serial 8-bit byte received at the SDI port at the start of a read or write cycle. The most significant bit of this first byte is the read/write mode bit.)

DATA FORMAT, TRANSFER, AND TIMING

FORMAT

Two type of 8-bit bytes are used when storing or retrieving data in the RAM chip, as shown in Figure 1.

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FIGURE 1 — SERIAL DATA FORMAT

Address/Control Byte

Bit:	7	6	5	4	3	2	1	0
	R/W	A6	A5	A4	A3	A2	A1	A0

A0-A6: The seven least significant RAM address bits, sufficient to address 128 bytes.

R/W: Read or write data transfer control bit. R/W = 0 initiates one or more memory read cycles; R/W = 1 initiates one or more memory write cycles.

Data Byte

Bit:	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

D0-D7: 8 bits of data

TRANSFER

Data transfers, occurring only while CE is high and SS is low, are either single data byte or multiple data transfers. Only only address byte is required for each type of transfer. For multiple transfers, the RAM automatically increments the address as long as it remains enabled. However, anytime enabling signals CE and SS are removed, RAM is reset, and when re-enabled, interprets the first word received as an address word. Therefore, RAM must remain enabled throughout the entire transfer, whether single or multiple, as shown in Figure 2.

TIMING

Address, control, or data bits are latched into RAM by the rising edge of SCK during a write cycle. During a read cycle, the rising edge of SCK shifts out the data bits. Bit switching occurs during the trailing edge of SCK and ensures that the bit value is valid when the SCK rising edge occurs, as shown in Figure 3.

FIGURE 2 — SERIAL TRANSMISSION BYTE SEQUENCES

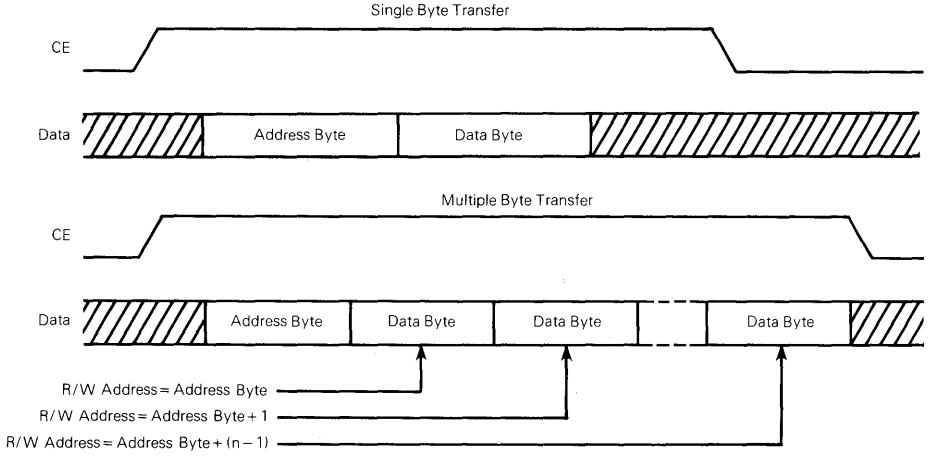

FIGURE 3 — RAM TIMING DIAGRAM