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Section 1. General Description

1.1 Contents

1.2 Introduction

The Motorola MC68HC68VBI is a low-cost HCMOS video peripheral capable of decoding user-definable vertical blanking interval (VBI) data formats from National Television System Committee (NTSC), phase alternating line system (PAL), or sequential color and memory system (SECAM) video signals. A fully duplexed serial peripheral interface (SPI) or Motorola 68HC(7)11 multiplexed expansion bus enables interface with the host processor. A functional block diagram of the MC68HC68VBI is shown in **Figure 1-1**.

1.3 Features

- Low Cost, HCMOS Technology
- 32-Pin Quad Flat Pack (QFP) Package
- Input Data Extraction
  - Closed Caption, Extended Data Service
  - Video Identification
  - Moji Tajuu, Japanese Closed Captioning in Kanji
  - Video Programming System (VPS)

- Program Delivery Control Mode (PDC)
  - Hamming Decoder
  - Packet 8/30 Format 1 and Format 2
- Serial Peripheral Interface (SPI)
- Motorola 68HC(7)11 Multiplexed Expansion Bus
- Internal Phase-Locked Loop (PLL) Frequency Generator
- Quasi-Horizontal Sync Detection

1.4 Functional Overview

The MC68HC68VBI contains three major functional blocks. They are:

1. SPI
2. VBI data extraction module
3. Multiplexed expansion bus

During communication with the host device, an input clock is needed. A single 5-volt ±10% power supply is required as well as a fixed-frequency resonator or input signal. All other timing and reference voltage signals are generated on chip.

1.4.1 VBI Data Extraction Module

The VBI data extraction module extracts data from the composite video signal according to the programming supplied by the host. Since critical parameters of the input signal to be extracted are programmable, extraction of most data formats is possible.

The VBI data extraction module is capable of extracting data of up to three modes from any line in the vertical blanking interval. A maximum of 84 8-bit bytes can be extracted and stored by this module in each field. This data is passed to the host MCU through the serial or expanded interface.

The data extraction module uses a PLL system with three programmable dividers for generation of suitable sampling clocks. Appropriate divide

ratios must be chosen and programmed by the user for generation of the sampling clocks. The clock switch may be used to switch between related clocks without re-stabilizing the PLL or for lower clock frequencies. External composite sync or internally separated sync pulses can be selected using the read sync select bit, RSS, in the MISC register.

The mode description memory is used to define the characteristics of the data formats to be extracted. These registers are organized into four groups of three registers.

Data to be extracted is described by:

- Clock delay, the number of output delay clocks from the horizontal sync leading edge until the first data
- PDC mode or not
- Number of bytes to be sampled per line
- PLL clock switch
- Data slice level
- Clock synchronization on rising or falling edge
- Digital LPF enable
- Resynchronization enable
- Output enable

The clock synchronization edge is used for initial clock synchronization and maintenance of clock synchronization. It is determined by MxRF. If this bit is clear, the clock will be resynchronized on the rising edge of the data contained in the video signal, and if it is set, on the falling edge.

The clock delay register is intended to allow the user to start data acquisition at the appropriate time. Prior to expiration of the count in the clock delay register, the data contained in the video signal will not be sampled. When the count in the clock delay register expires, the data acquisition module will synchronize the sampling clock to the first selected edge (depending on selection of MxRF) of the video signal.

For those data types with start bits, the clock delay register should expire after the last transition of the signal before the rising edge of the start bit. For those data types with a run-in clock but no start bit, the clock delay register should expire after the last transition of the signal before the rising edge of the run-in clock. In this way, proper clock synchronization of all data types can be achieved. The run-in clock can be used by software to verify proper synchronization.

Following expiration of the clock delay register, the sampling clock will re-establish synchronization at every selected edge of the input video signal. If several like data bits occur, the clock will detect these bits accurately until resynchronizing at the next edge.

When the number of bytes to be sampled has been entered into the internal memory, the data acquisition module will terminate data sampling. This allows the user to determine the beginning and end of each line's samples.

A specialized PDC mode has been included to allow selection of sampled data. When this mode is enabled, only those PDC lines with a magazine and row address group matching the 8/30 format code will be read into the internal data registers. If a PDC line with a different magazine and row address group is encountered, only the framing code is captured. If no data is detected, $00 is entered into the data registers.

Once the modes have been described, the user can read data of one of the three described modes using the line control registers. Data may be read from lines 7 through 28. The line control registers contain an enable bit and two bits to indicate the mode number desired for that line.

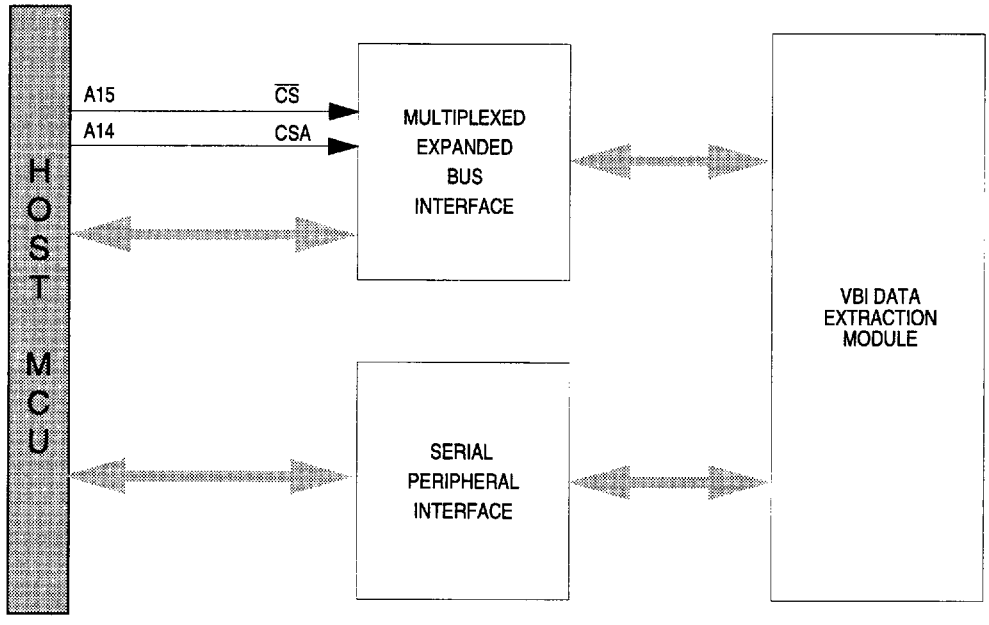


Figure 1-1. Example of Expanded or Serial Communication

1.4.2 Expanded Interface

The expanded interface provides high-speed access between Motorola 68HC(7)11 multiplex expansion MCUs and the control and data registers of the data extraction module. This is accomplished using the multiplex expansion mode of devices such as the 'HC11E9 or 'HC11A8.

The expanded interface is designed to require a minimum of interface hardware and to provide direct access to the control and data registers of the data extraction module. Using the configuration in **Figure 1-1**, VBI registers can be accessed by the software in exactly the same way as the 'HC11's internal memory locations. The VBI memory can be accessed using any high order addresses between $40XX and $7FXX. In its default state, the HC11E9 has no other memory in this range. Control signals are provided to coordinate communication with the HC11 MCU.

1.4.3 Serial Peripheral Interface (SPI)

A full-duplex serial peripheral interface (SPI) links the host device with the control and data registers of the data extraction module.

The SPI is designed to access the registers once between each vertical blanking interval. It is recommended that this be done some time during the display portion of the video output. Data can be read from and written to the registers simultaneously. Starting at address $80, all or part of the data can be read. Simultaneously, all or a single contiguous group of control registers may be written.

After chip select is asserted, the first two bytes clocked into the SPI are the write start and write ignore (stop) address. Thereafter, data is clocked into the registers starting from the start address. At the ignore address, data is no longer entered into the memory. Clocks must be applied for a full byte at the ignore address to enter the previous data into the register. Control signals are provided to coordinate communication with the host MCU.

Starting from the first clock used to clock in the start address, data is clocked out of the read-only registers from address $80. Even after the ignore address has been reached, data from the read-only registers will be clocked out. When the last byte is reached, $FF will be clocked out.

1.5 Pin Assignment

The MC68HC68VBI is available in a 32-pin QFP. The pin assignment for this package is shown in **Table 1-1**.

Table 1-1. MC68HC68VBI Pin Assignments

Pin No.	Name	Expanded Mode				Serial Mode			
		I/O	CMOS/TTL	Open Drain	Function	I/O	CMOS/TTL	Open Drain	Function
1	AD0/ SCLK	I/O	CMOS	No	AD0	O	CMOS	No	SCLK
2	AD1/ SDATA	I/O	CMOS	No	AD1	O	CMOS	No	SDATA
3	AD2/ SWIN	I/O	CMOS	No	AD2	O	CMOS	No	SWIN
4	AD3	I/O	CMOS	No	AD3	O	Note 4	—	—
5	AD4	I/O	CMOS	No	AD4	O	Note 4	—	—
6	AD5	I/O	CMOS	No	AD5	O	Note 4	—	—
7	AD6	I/O	CMOS	No	AD6	O	Note 4	—	—
8	AD7	Note 2	CMOS	No	AD7	O	Note 4	—	—
9	V_{DD3}	I	—	—	—	Note 2	—	—	—
10	SDI/AS	I	CMOS	No	AS	I	TTL	No	SDI
11	SDO/$\overline{RW}$	I	CMOS	Yes	$\overline{RW}$	O	CMOS	Yes	SDO
12	$\overline{SCK}$/E	I	CMOS	No	E	I	TTL	No	SCK
13	$\overline{CS}$	I	CMOS	No	CS	I	TTL	No	$\overline{CS}$
14	CSA	Note 2	CMOS	No	CSA	I	—	—	Note 5
15	V_{SS3}	Note 2	—	—	—	Note 2	—	—	—
16	V_{DD2}	I	—	—	—	Note 2	—	—	—
17	$\overline{SYNC}$	I	Note 1	No	$\overline{SYNC}$	I	Note 1	No	$\overline{SYNC}$
18	V_{Data}	Note 2	Note 1	No	V_{Data}	I	Note 1	No	V_{Data}
19	V_{SS2}	Note 2	—	—	—	Note 2	—	—	—
20	V_{SS1}	Note 3	—	—	—	Note2	—	—	—
21	XFC	Note 2	Note 1	No	XFC	Note 3	Note 1	No	XFC

Table 1-1. MC68HC68VBI Pin Assignments (Continued)

Pin No.	Name	Expanded Mode				Serial Mode			
		I/O	CMOS/TTL	Open Drain	Function	I/O	CMOS/TTL	Open Drain	Function
22	V_{DD1}	Note 2	—	—	—	Note 2	—	—	—
23	V_{DD3}	I/O	—	—	—	Note 2	—	—	—
24	PLLTA	I/O	—	No	Test	I/O	—	No	Test
25	$\overline{PLLTD}$	I	—	No	Test	I/O	—	No	Test
26	TEST	I	CMOS	No	Test	I	CMOS	No	Test
27	PAR/$\overline{SER}$	I	CMOS	No	Parallel	I	CMOS	No	Serial
28	$\overline{RESET}$	O	TTL	No	Reset	I	TTL	No	Reset
29	BUSY	Note 2	CMOS	Yes	Busy	O	CMOS	Yes	Busy
30	V_{SS3}	I	—	—	—	Note 2	—	—	—
31	OSC1	O	CMOS	No	OSC1	I	CMOS	No	OSC1
32	OSC2	I/O	CMOS	No	OSC2	O	CMOS	No	OSC2

NOTES:
1. Defined separately
2. Power supply or ground pin
3. Connection for external capacitor
4. Pulled down weakly; does not affect circuit operation in serial mode
5. No function

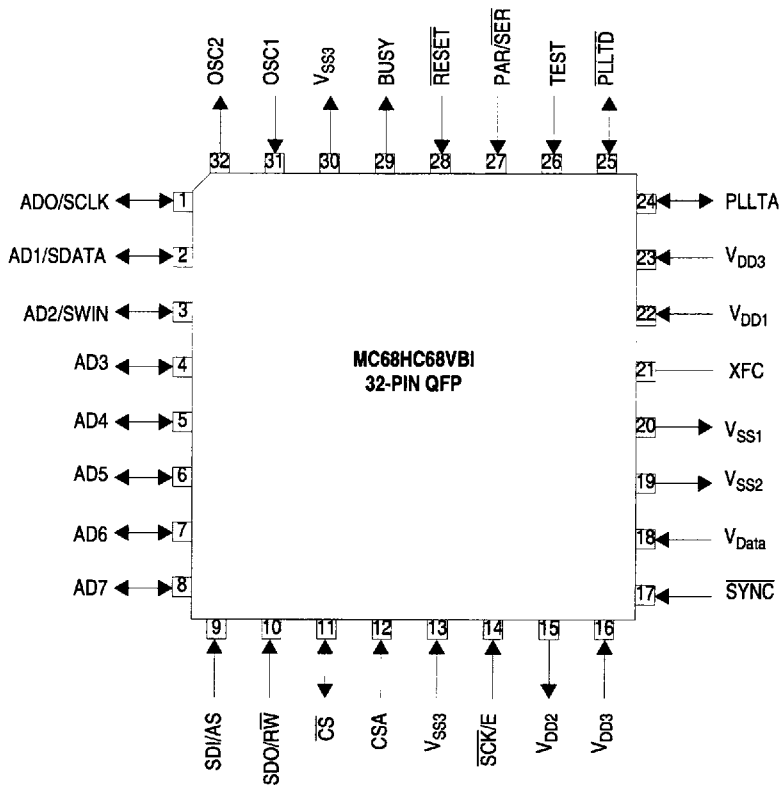


Figure 1-2. 32-Pin QFP Pinout

NOTE: *A line over a signal name indicates an active-low signal. Any reference to voltage, current, or frequency specified in the following sections will refer to the nominal values. The exact values and their tolerance or limits are specified in* ***Section 7. Electrical Specifications.***

1.6 Internal Structure

A block diagram of the MC68HC68VBI is shown in **Figure 1-3.**

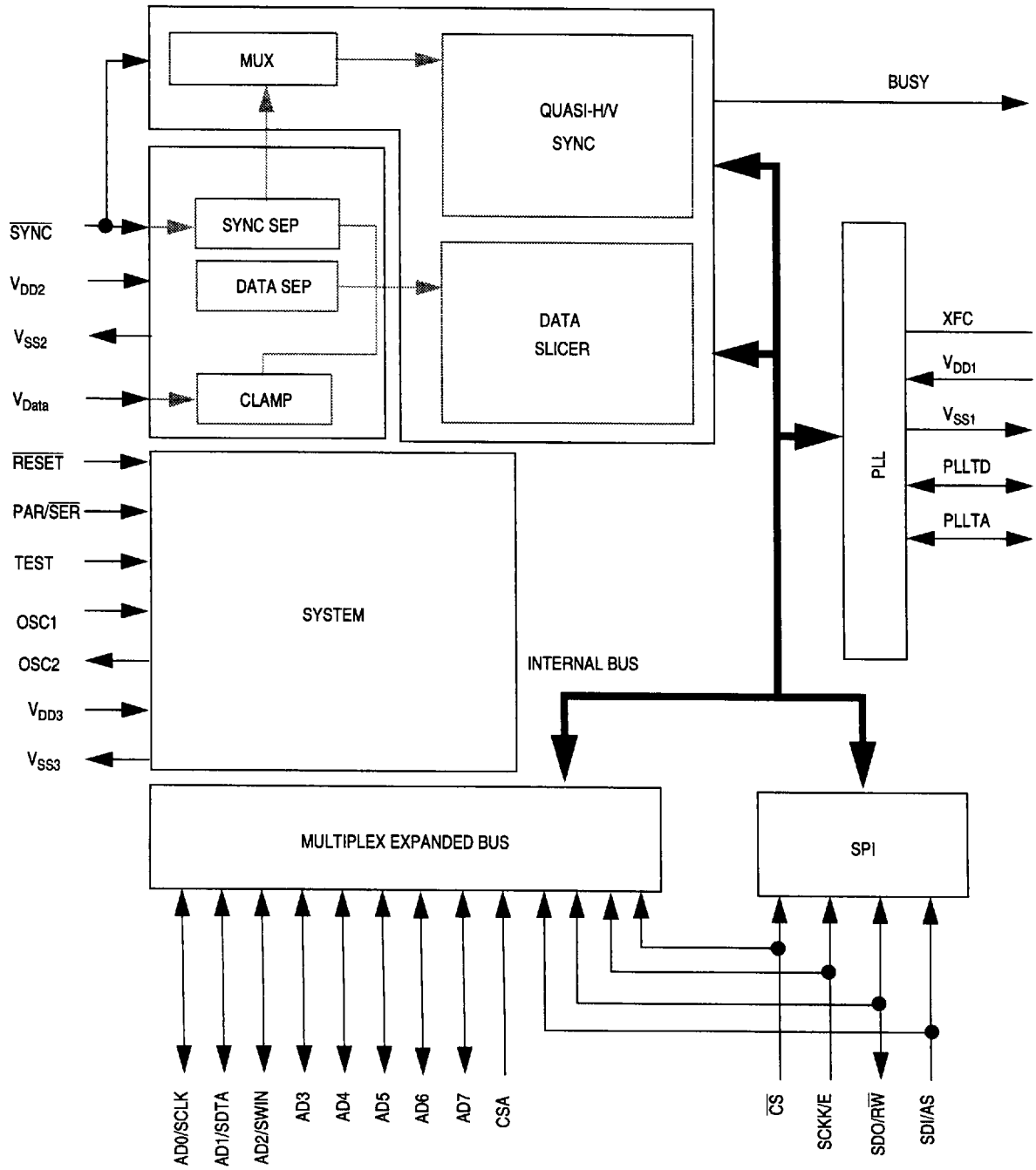


Figure 1-3. MC68HC68VBI Block Diagram

1.7 Functional Pin Description

1.7.1 PAR/$\overline{SER}$

This input-only pin activates either expanded or serial interface with the host controller. When this pin is at a low-voltage level, the serial communication interface is activated. When this pin is at a high-voltage level, the expanded interface is activated.

1.7.2 $\overline{CS}$

This input-only pin is the chip select for both the serial and expanded interfaces, depending on PAR/$\overline{SER}$. When serial is activated and this pin is at a high-voltage level, the serial interface is deselected. When it is at a low-voltage level, the serial interface is selected. The first SCK following the falling edge of $\overline{CS}$ clocks data.

When expanded is activated and this pin is a high-voltage level, the expanded interface is deselected. When it is a low-voltage level and CSA is a high-voltage level, the expanded interface is selected.

When the serial interface is activated, TTL input levels are used. When the expanded interface is activated, CMOS input levels are used.

1.7.3 CSA

This input-only pin is the alternate chip select for the expanded interface. When serial is activated, this pin has no affect. When expanded is activated and this pin is a high-voltage level and $\overline{CS}$ is a low-voltage level, the expanded interface is selected. To disable this pin, connect to low-voltage level.

1.7.4 AD0/SCLK

When the expanded mode is activated, this bidirectional pin is AD0 of the address/data bus of the expanded interface. When the serial mode is activated, this pin is the data slicer sampling clock output. When in

reset, this pin is high impedance. When the expanded interface is deactivated, this pin is weakly pulled down (about 100 kΩ).

1.7.5 AD1/SDATA

When the expanded mode is activated, this bidirectional pin is AD1 of the address/data bus of the expanded interface. When the serial mode is activated, this pin is the data slicer sampled data output. When in reset, this pin is high impedance. When the expanded interface is deactivated, this pin is weakly pulled down (about 100 kΩ).

1.7.6 AD2/SWIN

When the expanded mode is activated, this bidirectional pin is AD2 of the address/data bus of the expanded interface. When the serial mode is activated, this pin is the data slicer window output. When in reset, this pin is high impedance. When the expanded interface is deactivated, this pin is weakly pulled down (about 100 kΩ).

1.7.7 AD3:AD7

These bidirectional pins make up the remainder of the address/data bus of the expanded interface. While in reset, these pins are high impedance. When the expanded interface is deactivated, these pins are weakly pulled down (about 100 kΩ).

1.7.8 SDI/AS

When the expanded interface is enabled, this input-only, TTL-level (transistor-transistor logic) pin functions as the expanded interface address strobe. When the serial communication interface is enabled, this pin is the serial communication data input pin.

When the serial interface is activated, TTL input levels are used. When the expanded interface is activated, CMOS input levels are used.

1.7.9 SDO/$\overline{RW}$

When the expanded interface is enabled, this open drain, input/output pin determines read from memory or write to memory. When the serial communication interface is enabled, this pin is the serial communication data output pin and an external pullup resistor should be attached. While in reset, this pin is high impedance.

1.7.10 SCK/E

This input-only, TTL-level dual function pin is the clock input for both the expanded interface or the serial interface. When serial mode is selected, an external pullup resistor should be connected to this pin to control the pin state during idle periods.

When the serial interface is activated, TTL input levels are used. When the expanded interface is activated, CMOS input levels are used.

1.7.11 $\overline{SYNC}$

This input-only pin accepts synchronization signals from the video source. These signals may be a composite video signal or digital level composite sync. If composite video is input, a series capacitor should be used. If composite sync is input, direct coupling should be used and RSS should be set.

1.7.12 V_{Data}

This pin accepts the video input signal for determination of the pedestal level and data extraction. Synchronization signals are input at the $\overline{SYNC}$ pin.

1.7.13 XFC

This pin is used for connection to external passive components used to determine the characteristics of PLL. Typical passive component is 0.1 µF capacitor and might be sourced to $V_{SS}1$.

1.7.14 PLLTD

This input/output pin is the digital test pin for the extraction module PLL. It is reserved for factory use and should always be connected to V_{SS3}.

1.7.15 PLLTA

This input/output pin is the analog test pin for the extraction module PLL. It is reserved for factory use and should always be connected to V_{SS3}.

1.7.16 TEST

This input-only pin is for factory use only and should always be connected to V_{SS3}.

1.7.17 $\overline{\text{RESET}}$

This input-only TTL-level pin resets the peripheral to a known state.

1.7.18 BUSY

This open-drain output-only pin is high during lines 1 through 29. When this signal is low, it is safe to access the extraction data registers. When this signal is high, the registers may be busy. The signal on this pin is referenced to the sync selected by RSS. While in reset, this pin outputs a low level.

1.7.19 OSC1

This input-only pin is the input for the fixed-frequency oscillator.

1.7.20 OSC2

This output-only pin is the output for the fixed-frequency oscillator.

1.7.21 V_{DD1}

This is the analog power supply pin for PLL1.

1.7.22 V_{SS1}

This is the analog ground pin for PLL1.

1.7.23 V_{DD3}

This is the digital power supply pin for logic circuits.

1.7.24 V_{SS3}

This is the digital ground pin for logic circuits.

1.7.25 V_{DD2}

This is the digital power supply pin for noise-sensitive analog circuits.

1.7.26 V_{SS2}

This is the digital ground pin for noise-sensitive analog circuits.

1.8 Mode Selection

Modes are selected per the information in **Table 1-2.**

Table 1-2. Mode Selection Table

Mode	Test	PAR/$\overline{SER}$	$\overline{CS}$	CSA
Serial	0	0	Active Low	Inactive
Expanded	0	1	Active Low	Active High
Test	1	Factory Test Mode		

1.9 Fixed Frequency Oscillator

A fixed-frequency oscillator is included for generation of timing signals when a stable PLL frequency is not available.

The OSC1 and OSC2 pins are the connections for the 2-pin on-chip oscillator. The OSC1 and OSC2 pins can accept these two sets of components:

- A crystal or ceramic oscillator as shown in **Figure 1-4(a)**
- An external clock signal as shown in **Figure 1-4(b)**

1.9.1 Ceramic or Crystal Resonator

The circuit in **Figure 1-4** shows a typical 2-pin oscillator circuit for a ceramic or crystal resonator. The crystal manufacturer's recommendations should be followed, as the resonator's parameters determine the external component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for startup stabilization and to minimize output distortion.

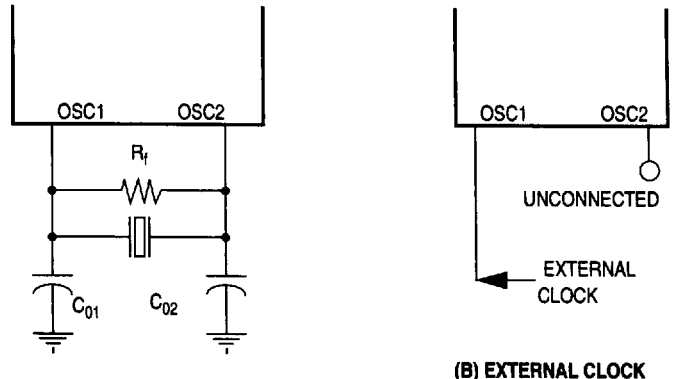


Figure 1-4. Oscillator Connections

1.9.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-4**. This configuration is possible regardless of oscillator connection or not.

1.9.3 Oscillator Frequency (f_{OSC})

When SYS = 0 (525-line system), a frequency of 3.57954 MHz (NTSC f_{OSC}) must be used. When SYS = 1 (625-line system), a frequency of 4.43362 MHz (PAL f_{OSC}) must be used. This oscillator must always be connected to ensure proper operation. Vertical sync signals detected using the fixed-frequency oscillator must be longer than 63 times the duration of one fixed-frequency clock period to be considered vertical sync signals.

Section 2. Memory

2.1 Contents

2.2 Introduction

Information concerning the MC68HC68VBI memory map and its control registers and status/data registers are found in this section.

2.3 MC68HC68VBI Memory Map

The MC68HC68VBI has 119 active bytes of registers as shown in **Figure 2-1.**

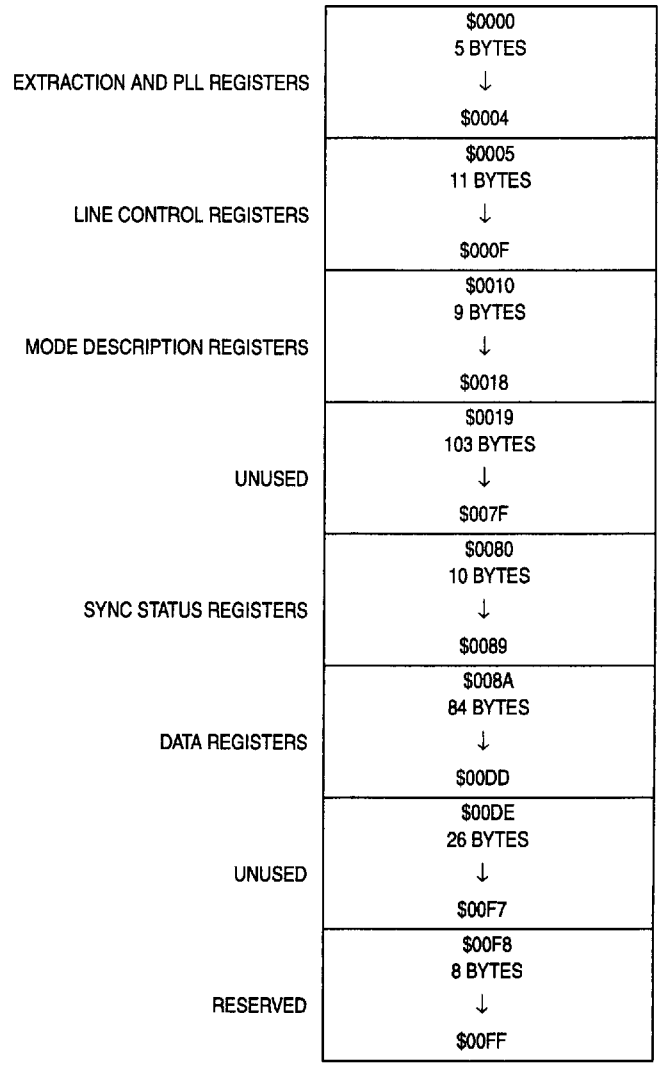


Figure 2-1. MC68HC68VBI Memory Map

2.4 Control Registers $00–$18

Addr	Name
$00	Miscellaneous Register
$01	Extraction PLL Divider Register
$02	Sync Status/Control Register
$03	Sampling Clock Control
$04	Extraction Control Register
$05	Line Control 7/8 Register
$06	Line Control 9/10 Register
$07	Line Control 11/12 Register
$08	Line Control 13/14 Register
$09	Line Control 15/16 Register
$0A	Line Control 17/18 Register
$0B	Line Control 19/20 Register
$0C	Line Control 21/22 Register
$0D	Line Control 23/24 Register
$0E	Line Control 25/26 Register
$0F	Line Control 27/28 Register
$10	Mode 0 Description 1 Register
$11	Mode 0 Description 2 Register
$12	Mode 0 Description 3 Register
$13	Mode 1 Description 1 Register
$14	Mode 1 Description 2 Register
$15	Mode 1 Description 3 Register
$16	Mode 2 Description 1 Register
$17	Mode 2 Description 2 Register
$18	Mode 2 Description 3 Register

Figure 2-2. MC68HC68VBI Control Registers Description

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00	Miscellaneous (MISC)	Read:	SYS	0	0	0	0	PFLD	RSS	RPSAV
		Write:								
$01	Extraction PLL Divider (EPLLD)	Read:	C7	C6	C5	C4	C3	C2	C1	C0
		Write:								
$02	Sync Control/Status (SCST)	Read:	SCHK	0	0	PCLD	SSL3	SSL2	SSL1	SSL0
		Write:								
$03	Sampling Clock Control (SCCTR)	Read:	0	A2	A1	A0	B3	B2	B1	B0
		Write:								
$04	Extraction Control (EXCTR)	Read:	EIF	EB	0	0	0	0	0	EEN
		Write:			EIC					
$05	Line Control 7/8 (LCR7/LCR8)	Read:	EN7	0	L7M1	L7M0	EN8	0	L8M1	L8M0
		Write:								
$06	Line Control 9/10 (LCR9/LCR10)	Read:	EN9	0	L9M1	L9M0	EN10	0	L10M1	L10M0
		Write:								
$07	Line Control 11/12 (LC11/LCR12)	Read:	EN11	0	L11M1	L11M0	EN12	0	L12M1	L12M0
		Write:								
$08	Line Control 13/14 (LCR13/LCR14)	Read:	EN13	0	L13M1	L13M0	EN14	0	L14M1	L14M0
		Write:								
$09	Line Control 15/16 (LCR15/LCR16)	Read:	EN15	0	L15M1	L15M0	EN16	0	L16M1	L16M0
		Write:								
$0A	Line Control 17/18 (LCR17/LCR18)	Read:	EN17	0	L17M1	L17M0	EN18	0	L18M1	L18M0
		Write:								
$0B	Line Control 19/20 (LCR19/LCR20	Read:	EN19	0	L19M1	L19M0	EN20	0	L20M1	L20M0
		Write:								
$0C	Line Control 21/22 (LCRR21/LCR22)	Read:	EN21	0	L21M1	L21M0	EN22	0	L22M1	L22M0
		Write:								
$0D	Line Control 23/24 (LCR23/LCR24)	Read:	EN23	0	L23M1	L23M0	EN24	0	L24M1	L24M0
		Write:								
$0E	Line Control 25/26 (LCR25/LCR26)	Read:	EN25	0	L25M1	L25M0	EN26	0	L26M1	L26M0
		Write:								
$0F	Line Control 27/28 (LCR27/LCR28)	Read:	EN27	0	L27M1	L27M0	EN28	0	L28M1	L28M0
		Write:								

U = Unimplemented

Figure 2-3. Control Register $00:$0F

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$10	Mode 0 Description 0 (M0D0)	Read:	0	M0C6	M0C5	M0C4	M0C3	M0C2	M0C1	M0C0
		Write:								
$11	Mode 0 Description 1 (M0D1)	Read:	M0PDC	M0S2	M0B5	M0B4	M0B3	M0B2	M0B1	M0B0
		Write:								
$12	Mode 0 Description 2 (M0D2)	Read:	M0SL3	M0SL2	M0SL1	M0SL0	M0RF	M0LEN	M0REN	M0OEN
		Write:								
$13	Mode 1 Description 0 (M1D0)	Read:	0	M1C6	M1C5	M1C4	M1C3	M1C2	M1C1	M1C0
		Write:								
$14	Mode 1 Description 1 (M1D1)	Read:	M1PDC	M1S2	M1B5	M1B4	M1B3	M1B2	M1B1	M1B0
		Write:								
$15	Mode 1 Description 2 (M1D2)	Read:	M1SL3	M1SL2	M1SL1	M1SL0	M1RF	M1LEN	M1REN	M1OEN
		Write:								
$16	Mode 2 Description 0 (M2D0)	Read:	0	M2C6	M2C5	M2C4	M2C3	M2C2	M2C1	M2C0
		Write:								
$17	Mode 2 Description 1 (M2D1)	Read:	M2PDC	M2S2	M2B5	M2B4	M2B3	M2B2	M2B1	M2B0
		Write:								
$18	Mode 2 Description 2 (M2D2)	Read:	M2SL3	M2SL2	M2SL1	M2SL0	M2RF	M2LEN	M2REN	M2OEN
		Write:								

U = Unimplemented

Figure 2-4. Control Register $10:$18

2.5 Status/Data Registers $80–$DD

Addr	Name
$80	Field Sync/Line 7 Sync Register
$81	Line 8/Line 9 Sync Register
$82	Line 10/Line 11 Sync Register
$83	Line 12/Line 13 Sync Register
$84	Linbe 14/Line 15 Sync Register
$85	Line 16/Line 17 Sync Register
$86	Line 18/Line 19 Sync Register
$87	Line 20/Line 21 Sync Register
$88	Line 22/Line 23 Sync Register
$89	PDC Address Register
$8A	Data Register 0
$8B	Data Register 1
$8C	Data Register 2
$8D	Data Register 3
$8E	Data Register 4
$8F	Data Register 5
$90	Data Register 6
$91	Data Register 7
$92	Data Register 8
$93	Data Register 9
$94	Data Register 10
$95	Data Register 11
$96	Data Register 12
$97	Data Register 13
$98	Data Register 14
$99	Data Register 15

Addr	Name
$AF	Data Register 37
$B0	Data Register 38
$B1	Data Register 39
$B2	Data Register 40
$B3	Data Register 41
$B4	Data Register 42
$B5	Data Register 43
$B6	Data Register 44
$B7	Data Register 45
$B8	Data Register 46
$B9	Data Register 47
$BA	Data Register 48
$BB	Data Register 49
$BC	Data Register 50
$BD	Data Register 51
$BE	Data Register 52
$BF	Data Register 53
$C0	Data Register 54
$C1	Data Register 55
$C2	Data Register 56
$C3	Data Register 57
$C4	Data Register 58
$C5	Data Register 59
$C6	Data Register 60
$C7	Data Register 61
$C8	Data Register 62

Figure 2-5. MC68HC68VBI Status/Data Registers Description

Addr	Name
$9A	Data Register 16
$9B	Data Register 17
$9C	Data Register 18
$9D	Data Register 19
$9E	Data Register 20
$9F	Data Register 21
$A0	Data Register 22
$A1	Data Register 23
$A2	Data Regiser 24
$A3	Data Register 25
$A4	Data Register 26
$A5	Data Register 27
$A6	Data Register 28
$A7	Data Register 29
$A8	Data Register 30
$A9	Data Register 31
$AA	Data Register 32
$AB	Data Register 33
$AC	Data Register 34
$AD	Data Register 35
$AE	Data Regiser 36

Addr	Name
$C9	Data Register 63
$CA	Data Register 64
$CB	Data Register 65
$CC	Data Register 66
$CD	Data Register 67
$CE	Data Register 68
$CF	Data Register 69
$D0	Data Register 70
$D1	Data Register 71
$D2	Data Register 72
$D3	Data Register 73
$D4	Data Register 74
$D5	Data Register 75
$D6	Data Register 76
$D7	Data Register 77
$D8	Data Register 78
$D9	Data Register 79
$DA	Data Register 80
$DB	Data Register 81
$DC	Data Register 82
$DD	Data Register 83

Figure 2-5. MC68HC68VBI Status/Data Registers Description (Continued)

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$80	Field Sync/Line 7 (FSL7)	Read:	0	FLD	LRPL	SCHK	L7C3	L7C2	L7C1	L7C0
		Write:								
$81	Line 8/Line 9 (L8/L9)	Read:	L8C3	L8C2	8LC1	L8C0	L9C3	L9C2	L9C1	L9C0
		Write:								
$82	Line 10/Line 11 (L10/L11)	Read:	L10C3	10C2	L10C1	L10C0	L11C3	L11C2	L11C1	L11C0
		Write:								
$83	Line 12/Line 13 (L12/L13)	Read:	L12C3	L12C2	12LC1	L12C0	L13C3	L13C2	L13C1	L13C0
		Write:								
$84	Line 14/Line 15 (L14/L15)	Read:	L14C3	L14C2	L14C1	L14C0	L15C3	L15C2	L15C1	L15C0
		Write:								
$85	Line 16/Line 17 (L16/L17)	Read:	L16C3	L16C2	L16C1	L16C0	L17C3	L17C2	L17C1	L17C0
		Write:								
$86	Line 18/Line 19 (L18/L19)	Read:	L18C3	L18C2	L18C1	L18C0	L19C3	L19C2	L19C1	L19C0
		Write:								
$87	Line 20/Line 21 (L20/L21)	Read:	L20C3	L20C2	L20C1	L20C0	L21C3	L21C2	L21C1	LC210
		Write:								
$88	Line 22/Line 23 (L22/L23)	Read:	L22C3	L22C2	L22C1	L22C0	L23C3	L23C2	L23C1	L23C0
		Write:								
$89	PDC Address (PAR)	Read:	MULT	PAR6	PAR5	PAR4	PAR3	PAR2	PAR1	PAR0
		Write:								
$8A	Read Data 0 (RD0)	Read:	R0B7	R0B6	R0B5	R0B4	R0B3	R0B2	R0B1	R0B0
		Write:								
$8B	Read Data 1 (RD1)	Read:	R1B7	R1B6	R1B5	R1B4	R1B3	R1B2	R1B1	R1B0
		Write:								
$8C	Read Data 2 (RD2)	Read:	R2B7	R2B6	R2B5	R2B4	R2B3	R2B2	R2B1	R2B0
		Write:								
$8D	Read Data 3 (RD3)	Read:	R3B7	R3B6	R3B5	R3B4	R3B3	R3B2	R3B1	R3B0
		Write:								
$8E	Read Data 4 (RD4)	Read:	R4B7	R4B6	R4B5	R4B4	R4B3	R4B2	R4B1	R4B0
		Write:								
$8F	Read Data 5 (RD5)	Read:	R5B7	R5B6	R5B5	R5B4	R5B3	R5B2	R5B1	R5B0
		Write:								

U = Unimplemented

Figure 2-6. Status/Data Register $80:$8F

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$90	Read Data 6 (RD6)	Read:	R6B7	R6B6	R6B5	R6B4	R6B3	RB2	R6B1	R6B0
		Write:								
$91	Read Data 7 (RD7	Read:	R7B7	R7B6	R7B5	R7B4	R7B3	R7B2	R7B1	R7B0
		Write:								
$92	Read Data 8 (RD8)	Read:	R8B7	R8B6	R8B5	R8B4	R8B3	R8B2	R8B1	R8B0
		Write:								
$93	Read Data 9 (RD9)	Read:	R9B7	R9B6	R9B5	R9B4	R9B3	R9B2	R9B1	R9B0
		Write:								
$94	Read Data 10 (RD10)	Read:	R10B7	R10B6	R10B5	R10B4	R10B3	R10B2	R10B1	R10B0
		Write:								
$95	Read Data 11 (RD11)	Read:	R11B7	R11B6	R11B5	R11B4	R11B3	R11B2	R11B1	R11B0
		Write:								
$96	Read Data12 (RD12)	Read:	R12B7	R12B6	R12B5	R12B4	R12B3	R12B2	R12B1	R12B0
		Write:								
$97	Read Data 13 (RD13)	Read:	R13B7	R13B6	R13B5	R13B4	R13B3	R13B2	R13B1	R13B0
		Write:								
$98	Read Data 14 (RD14)	Read:	R14B7	R14B6	R14B5	R14B4	R14B3	R14B2	R14B1	R14B0
		Write:								
$99	Read Data 15 (RD15)	Read:	R15B7	R15B6	R15B5	R15B4	R15B3	R15B2	R15B1	R15B0
		Write:								
$9A	Read Data 16 (RD16)	Read:	R16B7	R16B6	R16B5	R16B4	R16B3	R16B2	R16B1	R16B0
		Write:								
$9B	Read Data 17 (RD17)	Read:	R17B7	R17B6	R17B5	R17B4	R17B3	R17B2	R17B1	R17B0
		Write:								
$9C	Read Data 18 (RD18)	Read:	R18B7	R18B6	R18B5	R18B4	R18B3	R18B2	R18B1	R18B0
		Write:								
$9D	Read Data 19 (RD19)	Read:	R19B7	R19B6	R19B5	R19B4	R19B3	R19B2	R19B1	R19B0
		Write:								
$9E	Read Data 20 (RD20)	Read:	R20B7	R20B6	R20B5	R20B4	R20B3	R20B2	R20B1	R20B0
		Write:								
$9F	Read Data 21 (RD21)	Read:	R21B7	R21B6	R21B5	R21B4	R21B3	R21B2	R21B1	R21B0
		Write:								

U = Unimplemented

Figure 2-7. Status/Data Register $90:$9F

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$B0	Read Data 38 (RD38)	Read:	R38B7	R38B6	R38B5	R38B4	R38B3	R38B2	R38B1	R38B0
		Write:								
$B1	Read Data 39 (RD39)	Read	R39B7	R39B6	R39B5	R39B4	R39B3	R39B2	R39B1	R39B0
		Write:								
$B2	Read Data 40 (RD40)	Read:	R40B7	R40B6	R40B5	R40B4	R40B3	R40B2	R40B1	R40B0
		Write:								
$B3	Read Data 41 (RD41)	Read:	R41B7	R41B6	R41B5	R41B4	R41B3	R41B2	R41B1	R41B0
		Write:								
$B4	Read Data 42 (RD42)	Read:	R42B7	R42B6	R42B5	R42B4	R42B3	R42B2	R42B1	R42B0
		Write:								
$B5	Read Data 43 (RD43)	Read:	R43B7	R43B6	R43B5	R43B4	R43B3	R43B2	R43B1	R43B0
		Write:								
$B6	Read Data 44 (RD44)	Read:	R44B7	R44B6	R44B5	R44B4	R44B3	R44B2	R44B1	R44B0
		Write:								
$B7	Read Data 45 (RD45)	Read:	R45B7	R45B6	R45B5	R45B4	R45B3	R45B2	R45B1	R45B0
		Write:								
$B8	Read Data 46 (RD46)	Read:	R46B7	R46B6	R46B5	R46B4	R46B3	R46B2	R46B1	R46B0
		Write:								
$B9	Read Data 47 (RD47)	Read:	R47B7	R47B6	R47B5	R47B4	R47B3	R47B2	R47B1	R47B0
		Write:								
$BA	Read Data 48 (RD48)	Read:	R48B7	R48B6	R48B5	R48B4	R48B3	R48B2	R48B1	R48B0
		Write:								
$BB	Read Data 49 (RD49)	Read:	R49B7	R49B6	R49B5	R49B4	R49B3	R49B2	R49B1	R49B0
		Write:								
$BC	Read Data 50 (RD50)	Read:	R50B7	R50B6	R50B5	R50B4	R50B3	R50B2	R50B1	R50B0
		Write:								
$BD	Read Data 51 (RD51)	Read:	R51B7	R51B6	R51B5	R51B4	R51B3	R51B2	R51B1	R51B0
		Write:								
$BE	Read Data 52 (RD52)	Read:	R52B7	R52B6	R2B5	R52B4	R52B3	R52B2	R52B1	R52B0
		Write:								
$BF	Read Data 53 (RD53)	Read:	R53B7	R53B6	R53B5	R53B4	R53B3	R53B2	R53B1	R53B0
		Write:								

U = Unimplemented

Figure 2-8. Status/Data Register $B0:$BF

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$C0	Read Data 54 (RD54)	Read:	R54B7	R54B6	R54B5	R54B4	R54B3	R54B2	R54B1	R54B0
		Write:								
$C1	Read Data 55 (RD55)	Read:	R55B7	R55B6	R55B5	R55B4	R55B3	R55B2	R55B1	R55B0
		Write:								
$C2	Read Data56 (RD56)	Read:	R56B7	R56B6	R56B5	R56B4	R56B3	R56B2	R56B1	R56B0
		Write:								
$C3	Read Data 57 (RD57)	Read:	R57B7	R57B6	R57B5	R57B4	R57B3	R57B2	R57B1	R57B0
		Write:								
$C4	Read Data 58 (RD58)	Read:	R58B7	R58B6	R58B5	R58B4	R58B3	R58B2	R58B1	R58B0
		Write:								
$C5	Read Data 59 (RD59)	Read:	R59B7	R59B6	R59B5	R59B4	R59B3	R59B2	R59B1	R59B0
		Write:								
$C6	Read Data 60 (RD60)	Read:	R60B7	R60B6	R60B5	R60B4	R60B3	R60B2	R60B1	R60B0
		Write:								
$C7	Read Data 61 (RD61)	Read:	R61B7	R61B6	R61B5	R1B4	R61B3	R61B2	R61B1	R61B0
		Write:								
$C8	Read Data 62 (RD62)	Read:	R62B7	R62B6	R62B5	R62B4	R62B3	R62B2	R62B1	R62B0
		Write:								
$C9	Read Data 63 (RD63)	Read:	R63B7	R63B6	R63B5	R63B4	R63B3	R63B2	R63B1	R63B0
		Write:								
$CA	Read Data 64 (RD64)	Read:	R64B7	R64B6	R64B5	R64B4	R64B3	R64B2	R64B1	R64B0
		Write:								
$CB	Read Data 65 (RD65)	Read:	R65B7	R65B6	R65B5	R65B4	R65B3	R65B2	R65B1	R65B0
		Write:								
$CC	Read Data 66 (RD66)	Read:	R66B7	R66B6	R66B5	R66B4	R66B3	R6B2	R66B1	R66B0
		Write:								
$CD	Read Data 67 (RD67)	Read:	R67B7	R67B6	R67B5	R67B4	R67B3	R67B2	R67B1	R67B0
		Write:								
$CE	Read Data 68 (RD68)	Read:	R68B7	R68B6	R68B5	R68B4	R68B3	R68B2	R68B1	R68B0
		Write:								
$CF	Read Data 69 (RD69)	Read:	R69B7	R69B6	R69B5	R69B4	R69B3	R69B2	R69B1	R69B0
		Write								

U = Unimplemented

Figure 2-9. Status/Data Register $C0:$CF

Addr	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$D0	Read Data 70 (RD70)	Read:	R70B7	R70B6	R70B5	R70B4	R70B3	R70B2	R70B1	R70B0
		Write:								
$D1	Read Data 71 (RD71)	Read:	R71B7	R71B6	R71B5	R71B4	R71B3	R71B2	R71B1	R71B0
		Write:								
$D2	Read Data 72 (RD72)	Read:	R72B7	R72B6	R72B5	R72B4	R72B3	R72B2	R72B1	R72B0
		Write:								
$D3	Read Data 73 (RD73)	Read:	R73B7	R73B6	R73B5	R73B4	R73B3	R73B2	R73B1	R73B0
		Write:								
$D4	Read Data 74 (RD74)	Read:	R74B7	R74B6	R74B5	R74B4	R74B3	R74B2	R74B1	R74B0
		Write:								
$D5	Read Data 75 (RD75)	Read:	R75B7	R75B6	R75B5	R75B4	R75B3	R75B2	R75B1	R75B0
		Write:								
$D6	Read Data 76 (RD76)	Read:	R76B7	R76B6	R76B5	R76B4	R76B3	R76B2	R76B1	R76B0
		Write:								
$D7	Read Data 77 (RD77)	Read:	R77B7	R77B6	R77B5	R77B4	R77B3	R77B2	R77B1	R77B0
		Write:								
$D8	Read Data 78 (RD78)	Read:	R78B7	R78B6	R78B5	R78B4	R78B3	R78B2	R78B1	R78B0
		Write:								
$D9	Read Data 79 (RD79)	Read:	R79B7	R79B6	R79B5	R79B4	R79B3	R79B2	R79B1	R79B0
		Write:								
$DA	Read Data 80 (RD80)	Read:	R80B7	R80B6	R80B5	R80B4	R80B3	R80B2	R80B1	R80B0
		Write:								
$DB	Read Data 81 (RD81)	Read:	R81B7	R81B6	R81B5	R81B4	R81B3	R81B2	R81B1	R81B0
		Write:								
$DC	Read Data 82 (RD82)	Read:	R82B7	R82B6	R82B5	R82B4	R82B3	R82B2	R82B1	R82B0
		Write:								
$DD	Read Data 83 (RD83)	Read:	R83B7	R83B6	R83B5	R83B4	R83B3	R83B2	R83B1	R83B0
		Write:								

U = Unimplemented

Figure 2-10. Data/Status Register $D0:$DD

Section 3. Phase-Locked Loop (PLL)

3.1 Contents

3.2 Introduction

The MC68HC68VBI has an on-chip PLL for generation of synchronous clock signals for use in the data extraction module. (See **Figure 3-1**.)

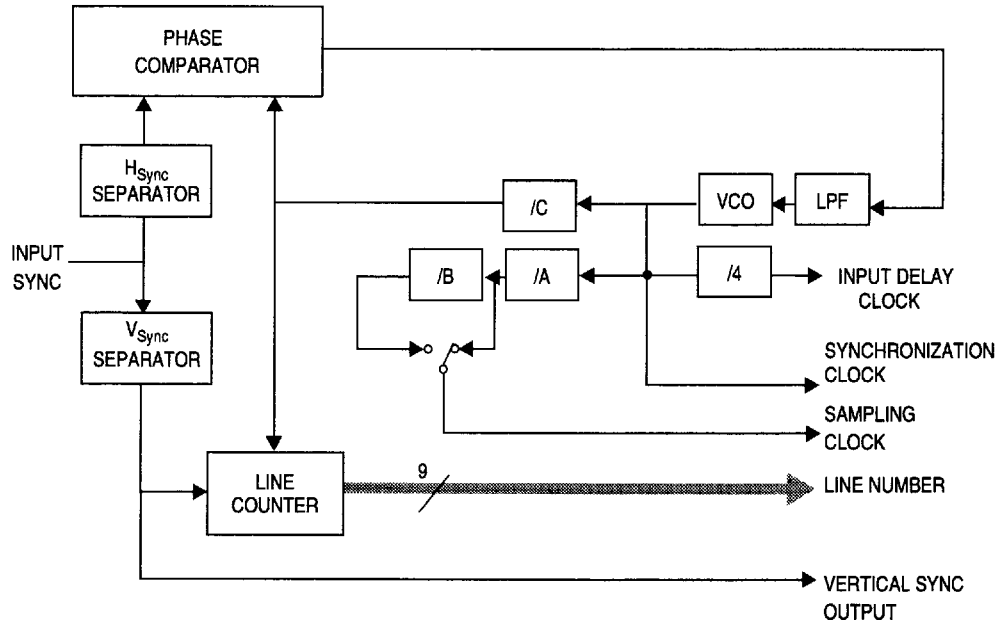


Figure 3-1. PLL Block Diagram

The PLL has three programmable dividers and a clock switch which are used to determine the sampling clock and synchronization clock frequency. The PLL control registers 1 and 2, located at $01 and $03 of the control registers, determine the value of the dividers. The position of the clock switch is determined by MxS2 of the mode description registers.

Table 3-1 summarizes divider values for several input data types.

Table 3-1. PLL Output Frequency Examples

Vertical Blanking Interval Data Type	Divide Ratio			Register Value			MxS2	Sampling Frequency
	A	B	C	A	B	C		
Closed Caption	7	8	1792	6	7	$3F	1	32 x f_H
Video ID, 525 Lines	8	8	1820	7	7	$5B	1	28.43 x f_H
Moji Tajuu	5	N/A	1820	4	N/A	$5B	0	364 x f_H
Teletext	4	N/A	1776	3	N/A	$2F	0	444 x f_H
VPS	6	N/A	1920	5	N/A	$BF	0	320 x f_H

If low power consumption is desired during periods when the PLL is not being used, the power save bit, RPSAV, located in the miscellaneous register at $00, can be set. This bit disables the PLL. Operation may be resumed by clearing this bit.

The lock state of the PLL can be determined by LRPL in the field sync/line 7 sync register located at $80 of the status/data registers. The LRPL bit is set only at the leading edge of vertical sync when the PLL is locked. The LRPL bit guarantees that the PLL has not become unlocked during the vertical blanking interval. If a disturbance as shown in **Figure 3-2** should occur, the LRPL bit would not be set when read following line 30, although it would be locked at that time. The LRPL bit would not be set again until the next leading edge of vertical sync that the PLL was locked.

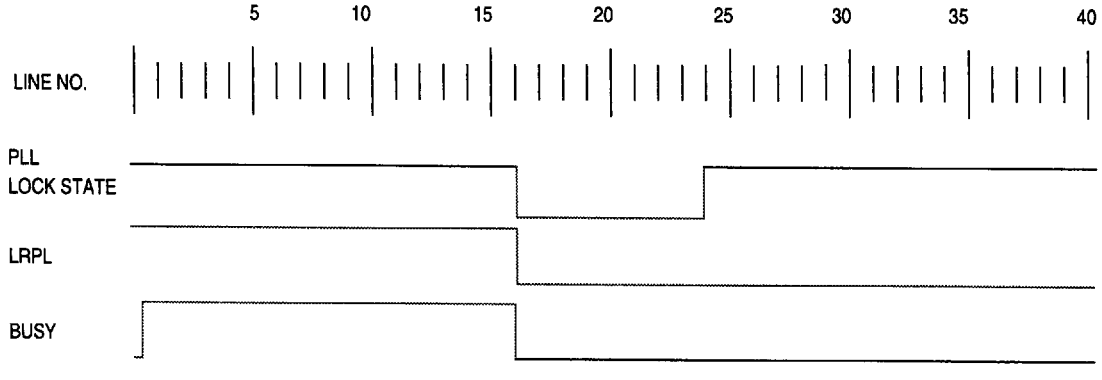


Figure 3-2. LRPL Bit Timing Example

The input signal selected by RSS is used for sampling clock generation and line counting. The user may select either externally or internally separated vertical and horizontal sync for the input to the PLL. The PLL is used for generation of sampling clocks used in the VBI data extraction module. Sampling clocks are built using the horizontal input signal selected for the PLL by the sync select bit (RSS) in the miscellaneous register located at $00 of the control register. See **Figure 3-3**.

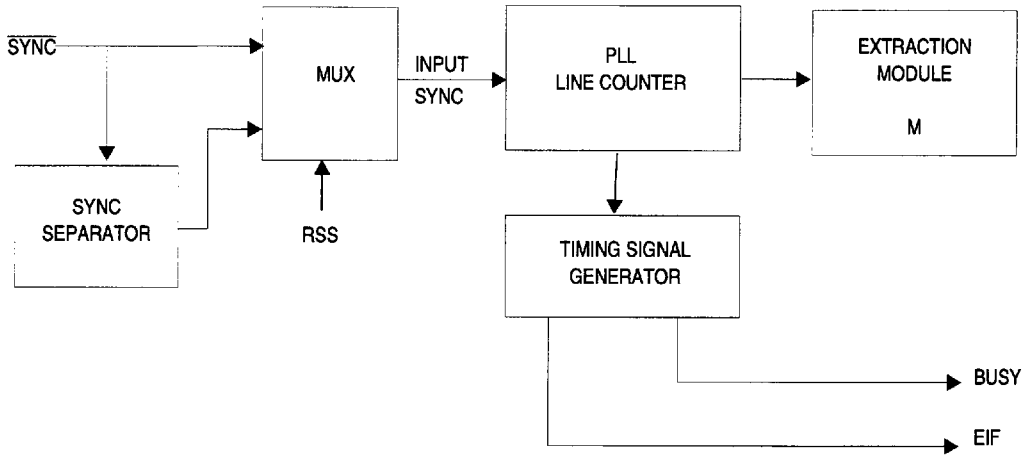


Figure 3-3. PLL Clock Signal Distribution

3.3 Line Number Definitions

Figure 3-4, Figure 3-5, Figure 3-6, and **Figure 3-7** show line number definitions for NTSC and PAL signals. All references to line numbers will be as defined for VBI unless otherwise specified.

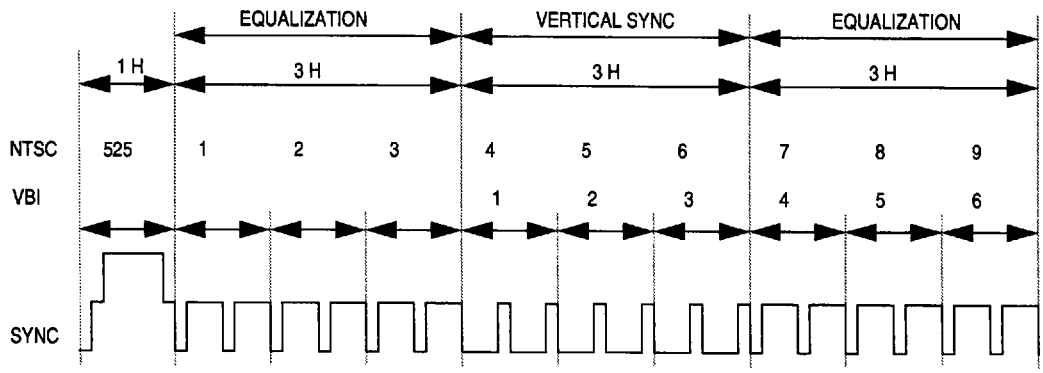


Figure 3-4. NTSC First Field

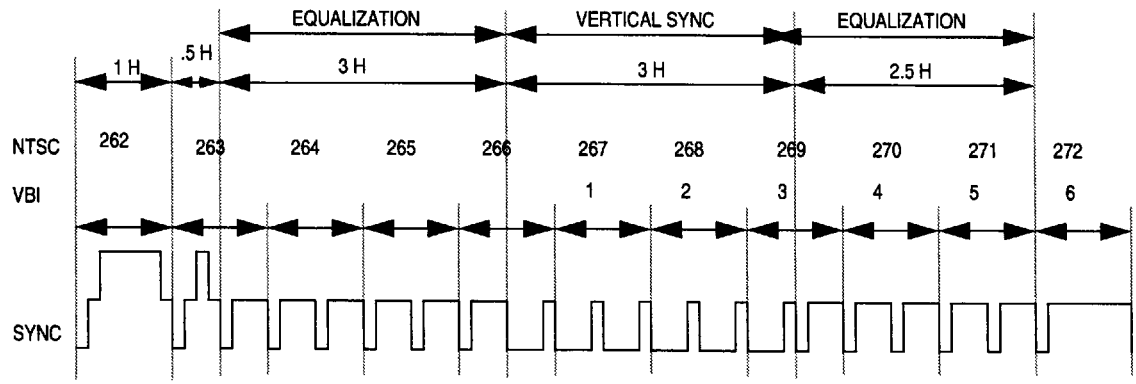


Figure 3-5. NTSC Second Field

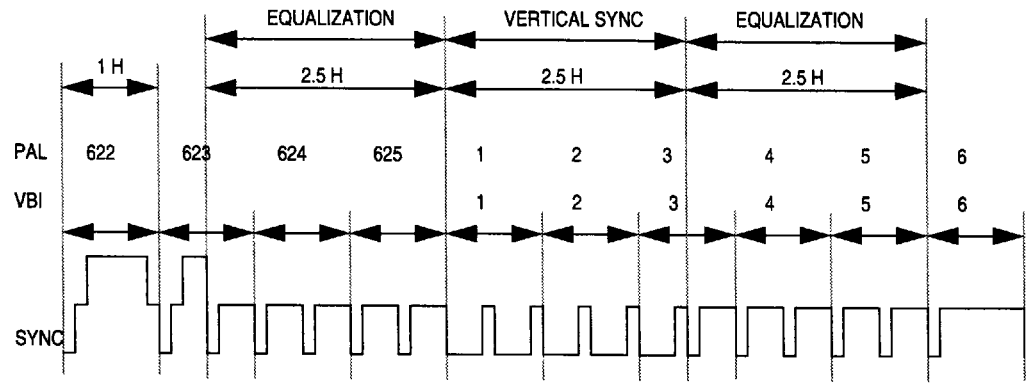


Figure 3-6. PAL First Field

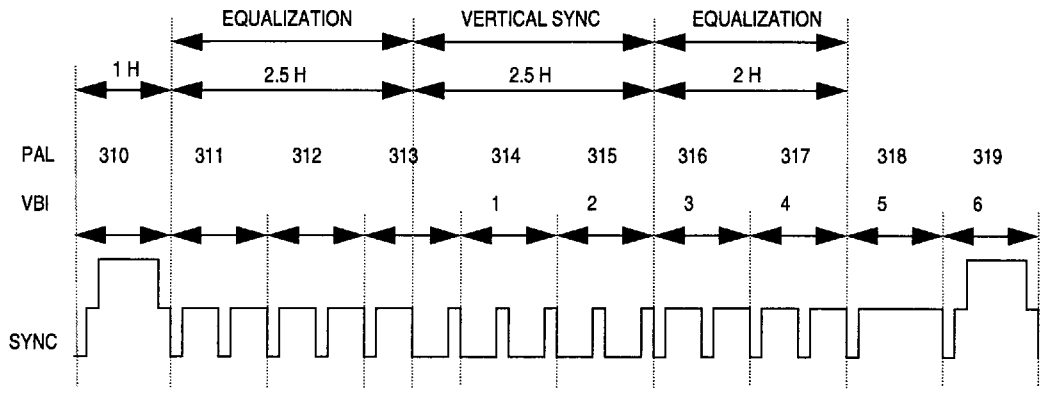


Figure 3-7. PAL Second Field

3.4 PLL State Description

The PLL will be in one of four modes depending on the input signal conditions. The PLL forms a window at the expected location of the horizontal sync signal. The four states are:

1. Unlock – No relationship between input sync frequency and PLL output frequency
2. Lock – Input sync frequency and PLL output frequency related according to C7:C0
3. Comp – Single missing horizontal sync compensated for by PLL. If a horizontal sync is missing prior to near line 253 at SYS = 0 or line 303 at SYS = 1 in either field, this mode will insert a horizontal sync. If two consecutive lines are missing horizontal sync pulses, the PLL will return to the unlocked state.
4. Hold – Compensates for phase jumps caused by playback head switching commonly found in signals produced by video cassette players. This mode disables the phase comparator, holds the frequency of the PLL, and repositions the window according to vertical sync. The output frequency of PLL is held if a discontinuity in the phase of horizontal sync pulses occurs immediately prior to vertical sync. For SYS = 0, this time is near line 253. For SYS = 1, this time is near line 303.

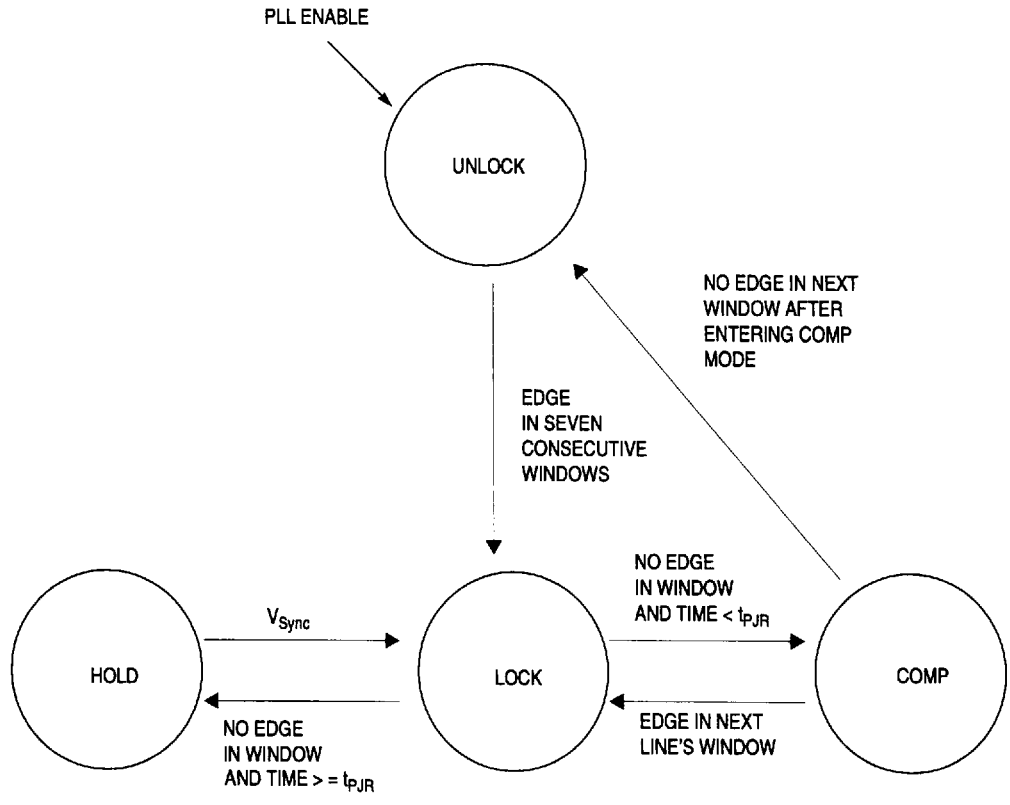


Figure 3-8. PLL State Diagram

3.5 Sampling Clock Control Register

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	A2	A1	A0	B3	B2	B1	B0
Write:								
Reset:	0	1	1	1	1	1	1	1

= Unimplemented

Figure 3-9. Sampling Control Register (SCCTR)

Bit 7 — Reserved

This bit is not used and always reads 0.

A0:A2 — A counter

These bits set the divide ratio of the PLL's divider A. Values from 0 to 7 may be written. One less than the desired divide ratio should be written to these bits. If zero is written, the counter will divide by 1.

B0:B3 — B counter

These bits set the divide ratio of the PLL's divider B. Values from 0 to 15 may be written. One less than the desired divide ratio should be written to these bits. If zero is written, the counter will divide by 1.

NOTE: *If MxS2 = 1, then (A+1)(B+1) must be greater than 4. If MxS2 = 0, then (A+1) must be greater than 4 to ensure proper operation.*

3.6 Extraction PLL Divider

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	C7	C6	C5	C4	C3	C2	C1	C0
Reset:	1	1	1	1	1	1	1	1

Figure 3-10. Extraction PLL Divider (EPLLD)

C0:C7 — C Counter Adjust

These bits determine the divide ratio of the PLL's divider C; 1729 less than the desired divide ratio should be written to this register.

The value of the C divider will be the contents of the counter adjust register plus a fixed offset of 1728. Divide ratios from 1729 to 1984 may be selected.

3.7 Sync Control/Status

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SCHK	0	0	PCLD	SSL3	SSL2	SSL1	SSL0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 3-11. Sampling Control Register (SCST)

SCHK — Sync Check

Same as $80 SCHK bit. This bit cleared by read of $80 or by read of $02.

Bits 6:5 — Reserved

These bits are not used and always read 0.

PCLD — Pedestal Clamp Large Driver Disable

Pedestal clamp large driver control

1 = Pedestal clamp large driver disabled

0 = Pedestal clamp large driver enabled

SSL3:SSL0 — Sync Slice Level

These bits determine the voltage level at which sync information will be sliced.

3.8 Miscellaneous Register

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SYS	0	0	0	0	PFLD	RSS	RPSAV
Write:								
Reset:	0	0	0	0	0	0	0	1

= Unimplemented

Figure 3-12. Sampling Control Register (MISC)

SYS — SYStem

This bit determines which system type the peripheral will use.

1 = 625 line system
0 = 525 line system

PFLD — PLL Filter Large Driver Disable

This bit determines if enable and disable of the PLL filter's large driver will be under automatic or manual control.

Write:

1 = PLL filter large driver always enabled
0 = PLL filter large driver dibbled automatically

Bits 6:2 — Reserved

These bits are not used and always read 0.

RSS — Read Sync Select

This bit determines if the internal sync separator will be enabled or not. If direct coupled CMOS level negative true composite sync is used, the sync separator should be bypassed. If capacitively coupled video sync is used, the sync separator should be enabled.

Write:

1 = Direct coupled negative true composite sync (disabled)
0 = Internally separated sync (enabled)

RPSAV — Power Save Mode

Power save mode is entered using this bit.

Write:

1 = Power save mode

0 = Normal operation

Section 4. VBI Data Extraction Module

4.1 Contents

4.2 Introduction

The data extraction module of the MC68HC68VBI is a high-frequency sampling circuit for use with low-level composite video signals. Input signal parameters are programmable, allowing the user to define the input data formats. Sampling clock frequency can be programmed using the phase-locked loop (PLL) system. Data may be extracted from NTSC (National Television System Committee), PAL (phase alternating line system), or sequential color and memory system (SECAM) composite video signals. Up to four modes can be extracted on lines 7 through 28. A maximum of 84 8-bit bytes can be extracted and stored by this module in each field.

Features of the data extraction module include:

- Extraction of:
  - Closed Caption, EDS
  - Video Identification
  - Program Delivery Control (PDC)
  - Moji Tajuu, Japanese Closed Captioning in Kanji
  - Video Programming System (VPS)
  - User-Defined Data Formats
- Real-Time Sampling Clock Resynchronization
- Quasi-Horizontal Sync Detection
- Field Detection
- Packet 8/30 Format 1, Format 2 PDC Mode with Format Determined Hamming Decode

4.3 General Operation

Since the data extraction module relies only on the user-defined mode description, the user is not confined to sampling pre-defined data formats only. **Figure 4-1** illustrates those parameters of the signal that the user defines for a typical waveform.

Voltage slicing levels are defined for data and sync portions of the signal. The sync slice level bits, SSL3:SSL0, define the voltage slice level used to extract the sync signals. The data slice level bits, MxSL3:MxSL0, define the voltage slice level used to extract data from the signal. The data slice level is defined in reference to the pedestal level. The sync slice level is defined in reference to the sync tip level.

The clock synchronization edge is determined by MxRF in the mode description registers and is used for initial clock synchronization and maintenance of clock synchronization. This edge should be chosen so that an accurate, unambiguous sampling clock can be found.

The clock delay bits, MxC6:MxC0, define the number of input delay clock cycles from the leading edge of horizontal until sampling is started. Care should be taken that this expires when the signal is at the proper polarity before the first sampled data bit. The sampling clock is resynchronized on each selected edge after the clock delay expires.

The MxB bits are used to count the number of bytes that are entered into the data registers after sampling has started. After the number of bytes indicated by the MxB bits have been sampled, no more data is entered into the data registers.

Once the data formats to be sampled have been defined, the user may indicate which lines to sample in a given format using the line control registers. The user should specify the mode to be sampled by the corresponding mode description group.

If more than one line of data is read during a given field, the data will be stored contiguously in the read data registers. That is, the first byte of the second line of data will immediately follow the last byte of the first line of data.

Data is entered into the read data registers starting at read data 0 and progressing to higher addresses as data is sampled. Data is sampled least significant bit first and entered into read data registers least significant bit (LSB) first.

If sampling is terminated in the middle of a byte, the bits for that byte will be entered into the data register from the least significant bit (LSB) and the remaining bits will be 0.

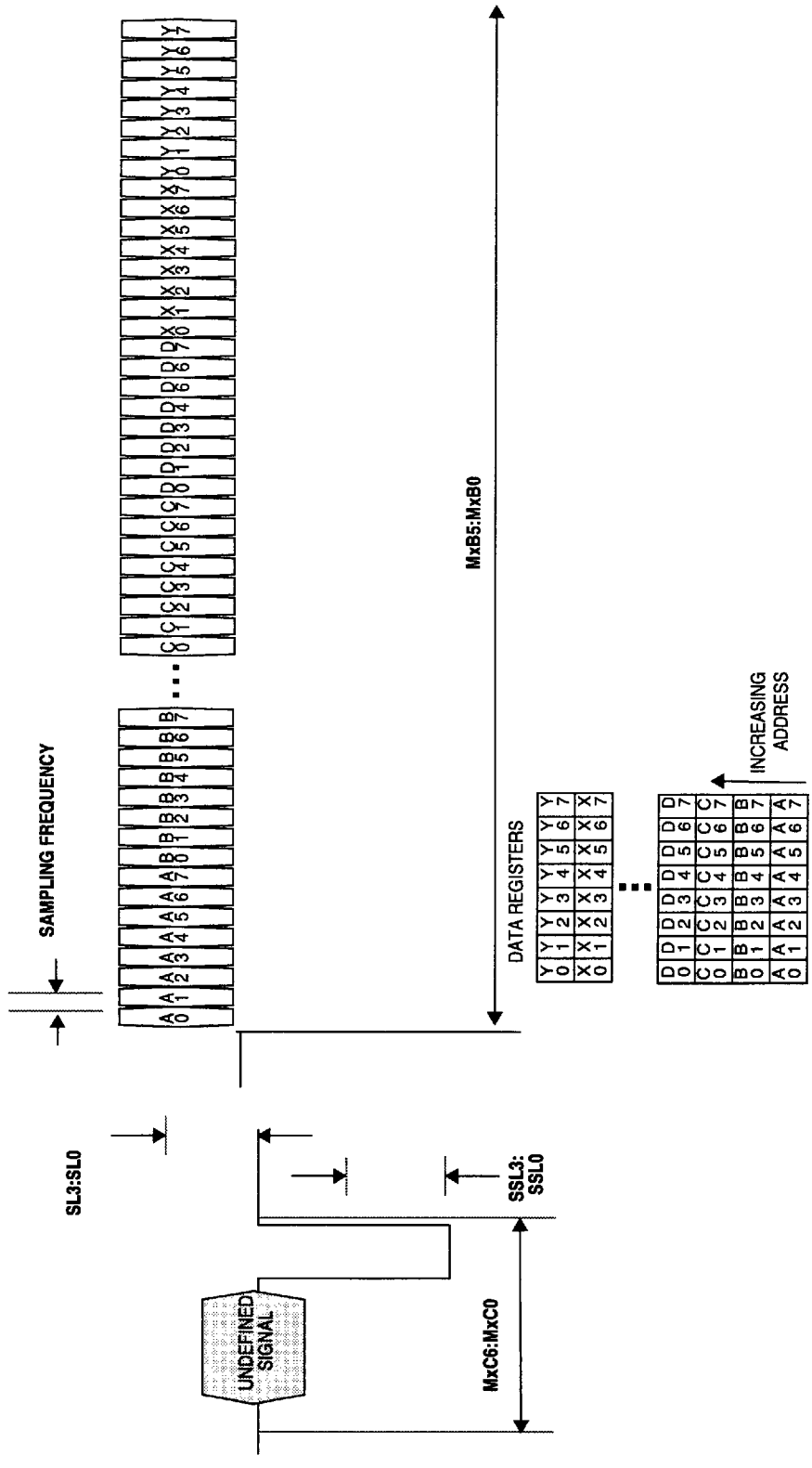
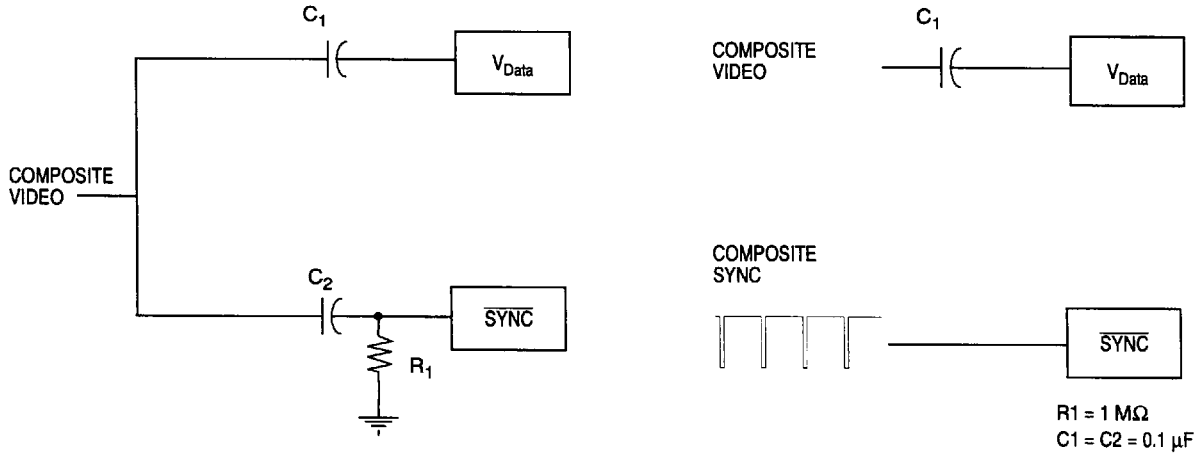


Figure 4-1. Data Extraction Timing Diagram

4.4 Signal Connection

The video signal can be connected to the extraction module in one of two ways:

1. Using the internal sync separator
2. Bypassing the internal sync separator and using a CMOS level negative true composite sync signal directly applied to the SYNC pin. See **Figure 4-2(a)** and **Figure 4-2(b)**.



RSS = 0
A) CONNECTION USING INTERNAL SYNC SEPARATOR

RSS = 1
B) CONNECTION USING EXTERNAL SYNC SEPARATOR

Figure 4-2. External Video Signal Connections

4.5 Data Slicer Output Signals

When serial mode is activated, three outputs of the data slicer are available to the user. **Figure 4-3** shows a representation of the generation of these signals.

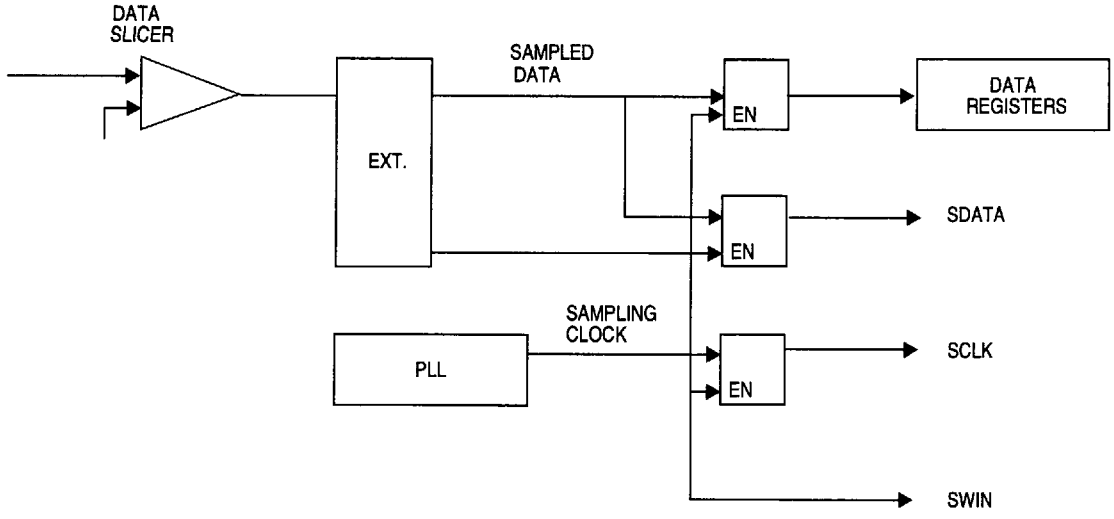
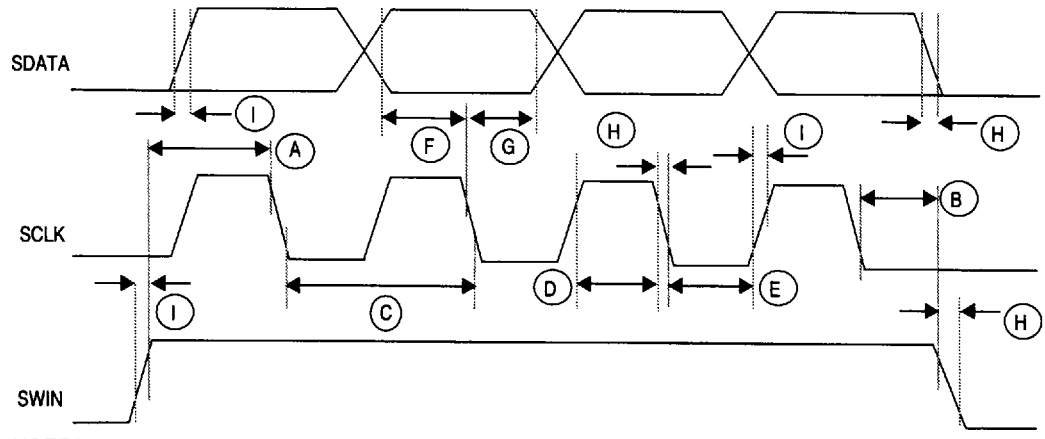


Figure 4-3. Data Slicer Output Signal Block Diagram

The slicer window output, SWIN, will go active high for all sampled data that is entered into the data registers.

Slicer sampling clock, SCLK, is the sampling clock used in the data slicer to sample the video signal on V_{Data}. Due to clock resynchronization, a 50% duty cycle waveform will not always be present.

The slicer data output, SDATA, is the sampled data. This data also will be entered into the data registers.



NOTES:
A = SWIN leading edge to clock
B = Clock to SWIN trailing edge
C = SCLK period
D = SCLK high time
E = SCLK low time
F = Data setup time
G = Data hold time
H = Signal falling time
I = Signal rising time

Figure 4-4. Data Slicer Output Signal Timing Diagram

Immediately after expiration of the count in the clock delay register, the leading edge of SWIN will occur on the line designated for sampling of a mode with MxOEN = 1. After the initial synchronization of the sampling clock on this line, SCLK and SDATA will become active. The trailing edge of SWIN will occur when the number of bytes expires or the next horizontal synchronization pulse expires, whichever occurs first.

4.6 BUSY Signal

This signal assists the user in interfacing with the host device at the appropriate time. While the busy signal is high, attempts to read the data registers may result in unknown data.

The leading edge of BUSY will occur during the line 1 interval. The trailing edge of BUSY will occur eight VCO clocks after the leading edge of the line 30 horizontal sync.

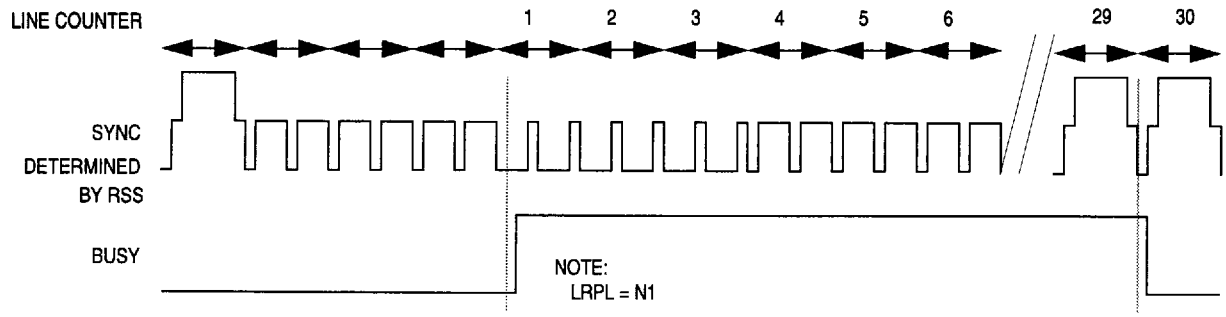


Figure 4-5. BUSY Timing Diagram for Normal Sync Condition

If a disturbance in the PLL occurs during the vertical sync interval, BUSY will remain high until the end of the vertical sync interval and then fall. If a disturbance occurs after the vertical sync interval, the BUSY signal, if still high, will fall immediately.

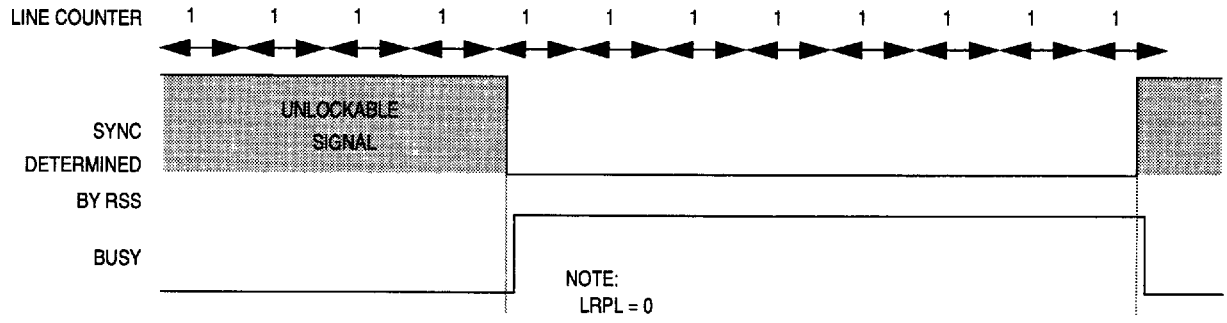


Figure 4-6. BUSY Timing Diagram for PLL Unlocked Condition 1

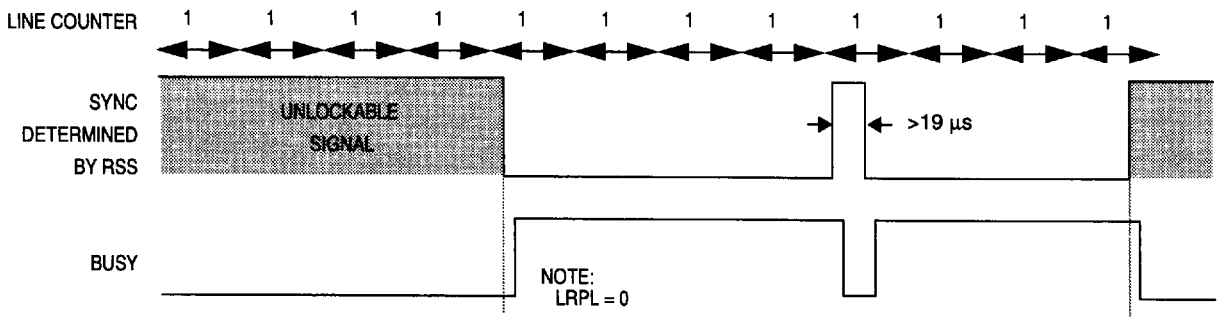


Figure 4-7. BUSY Timing Diagram for PLL Unlocked Condition 2

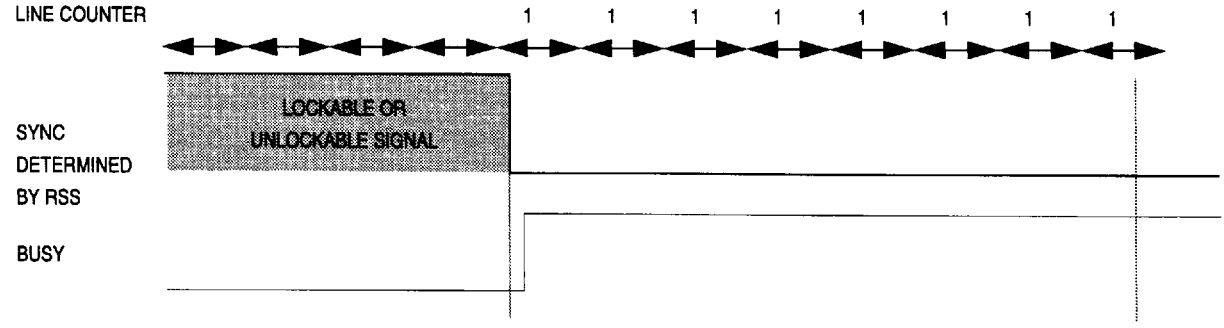


Figure 4-8. BUSY Timing Diagram for No Signal Condition

4.6.1 Register Readability During BUSY

When the BUSY signal is high, access to all registers is not permitted. Control registers and the four most significant bits in the status registers are always readable and writable. However, the remaining registers are only readable while the BUSY signal is low.

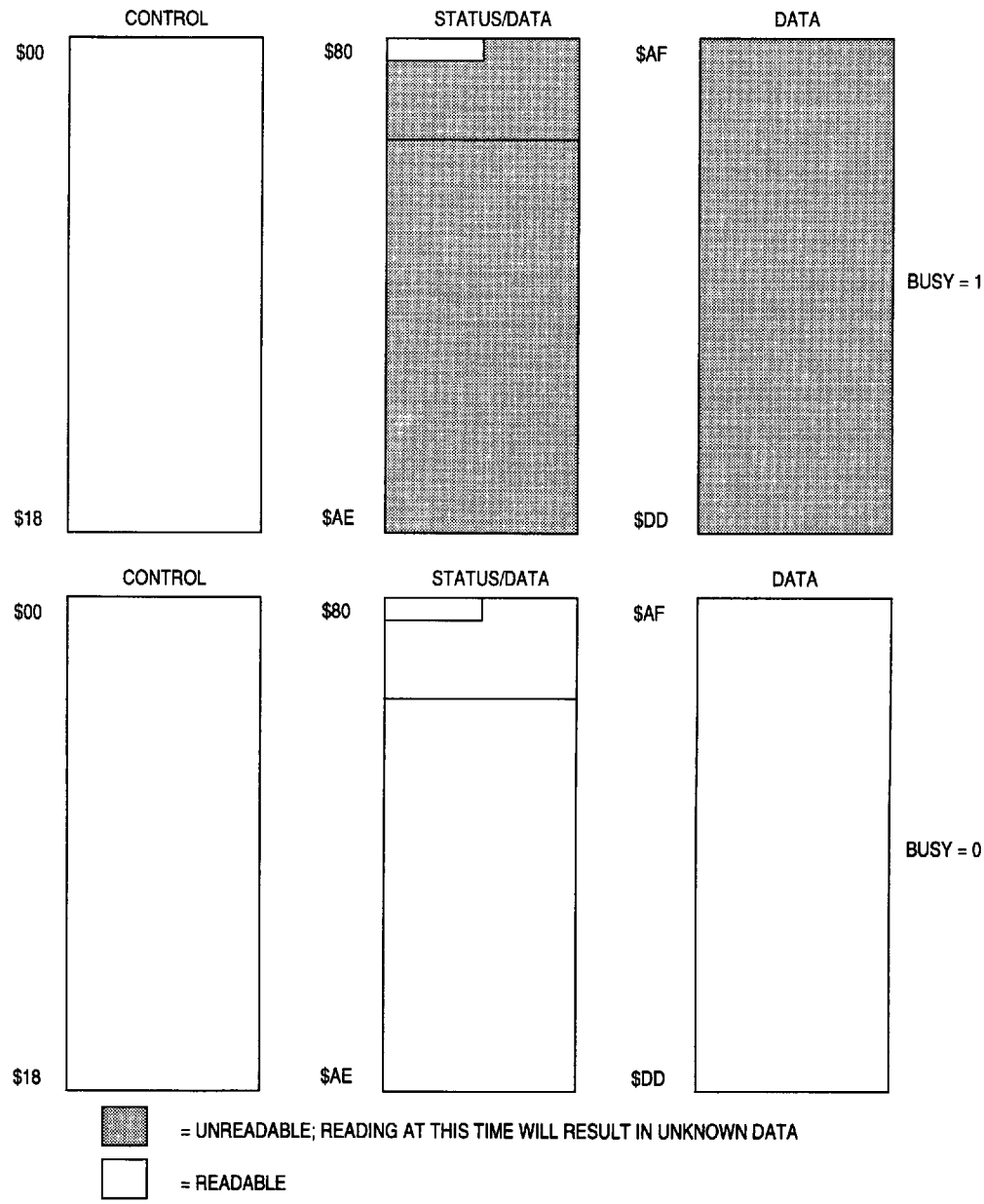


Figure 4-9. Register Readability During BUSY

4.7 Quasi-Horizontal Sync Detection

Quasi-horizontal sync pulses may be counted in lines 7 through 23. Quasi-horizontal sync pulses are falling edges below the sync slice level occurring between genuine horizontal sync pulses. Genuine horizontal sync pulses are defined in the active display region. See **Figure 4-10** for NTSC first field example. For second field and PAL signals, quasi-horizontal sync pulses are also counted in lines 7 through 23. If the PLL is not locked, quasi-horizontal sync pulses cannot be detected.

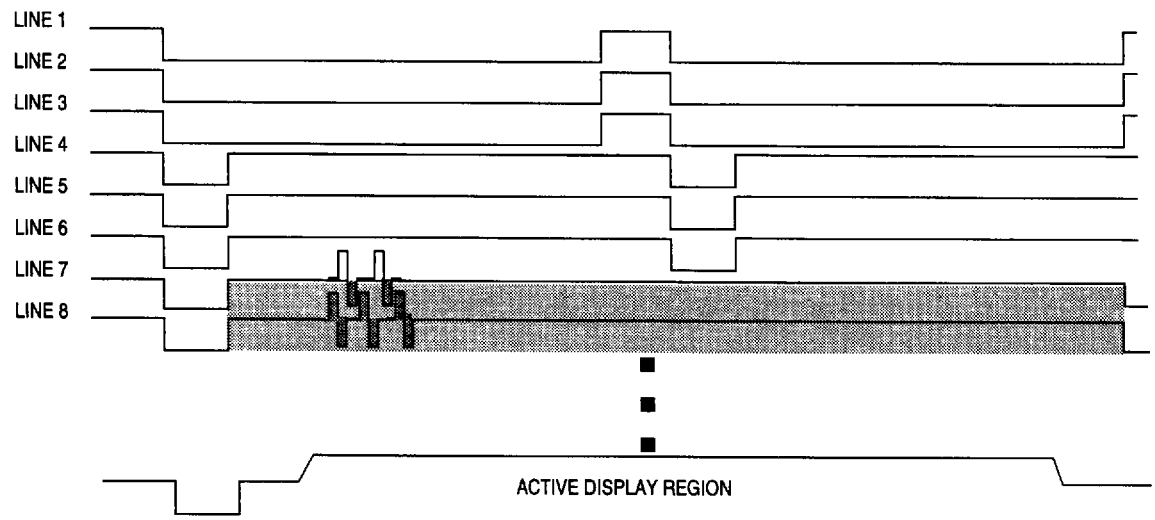


Figure 4-10. Quasi-H Sync Timing for NTSC First Field

4.8 Field Detection

The most recent field of display is indicated by the field bit, FLD.

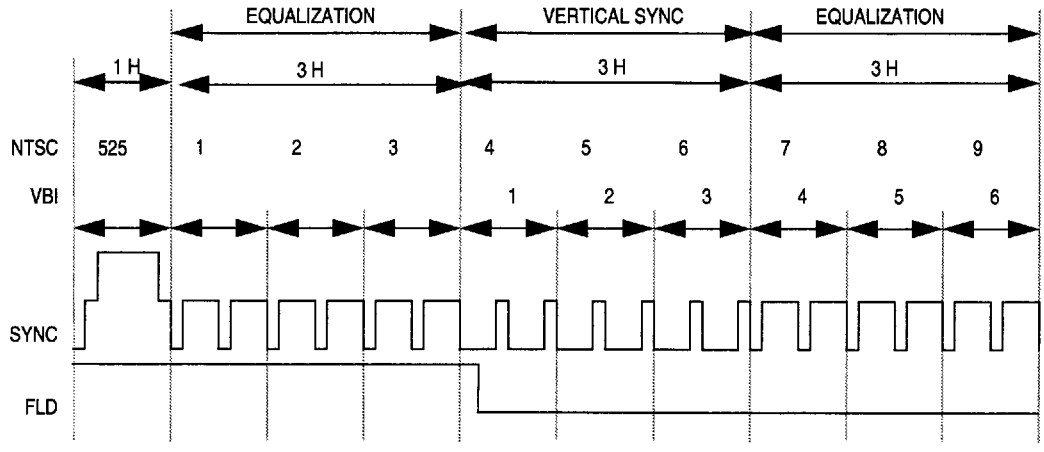


Figure 4-11. NTSC First Field

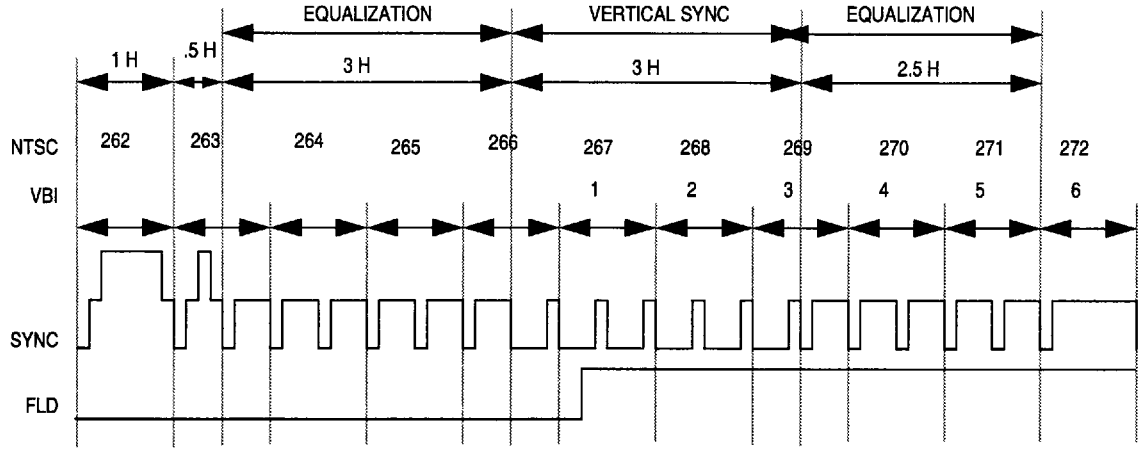


Figure 4-12. NTSC Second Field

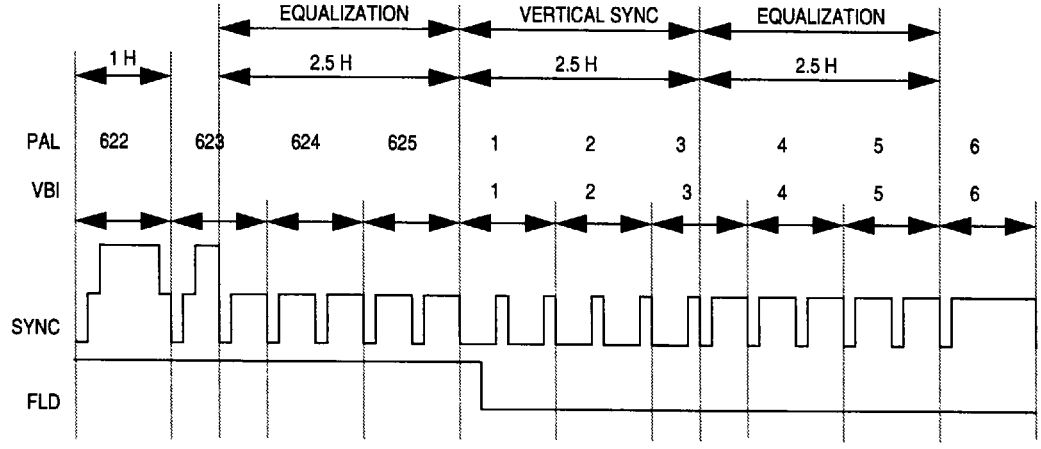


Figure 4-13. PAL First Field

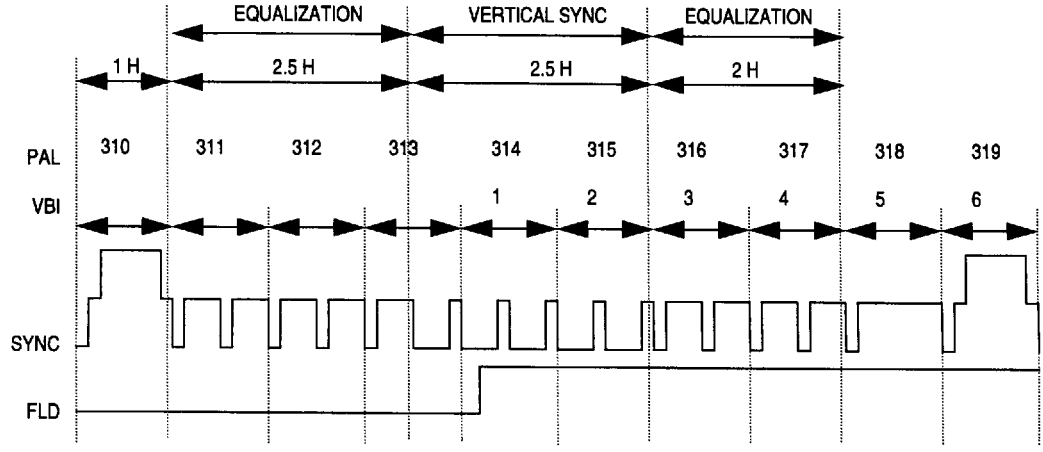


Figure 4-14. PAL Second Field

4.9 Data Extraction Input Signal Description

A description of the input signal to the data extraction module on $\overline{\text{SYNC}}$ is shown in **Figure 4-15, Figure 4-16, Table 4-1,** and **Table 4-2.** Limits on these signal parameters are in **7.7 Data Extraction Characteristics.**

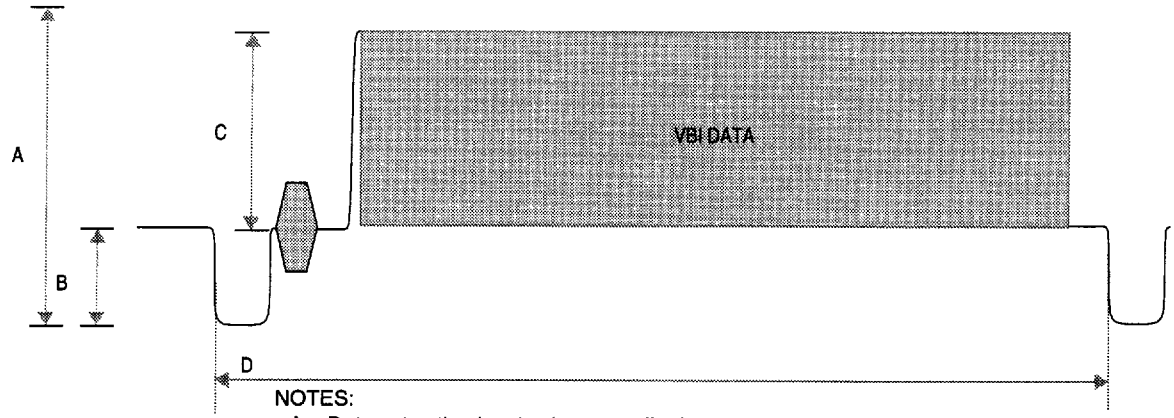


Figure 4-15. Data Extraction Input Line Description

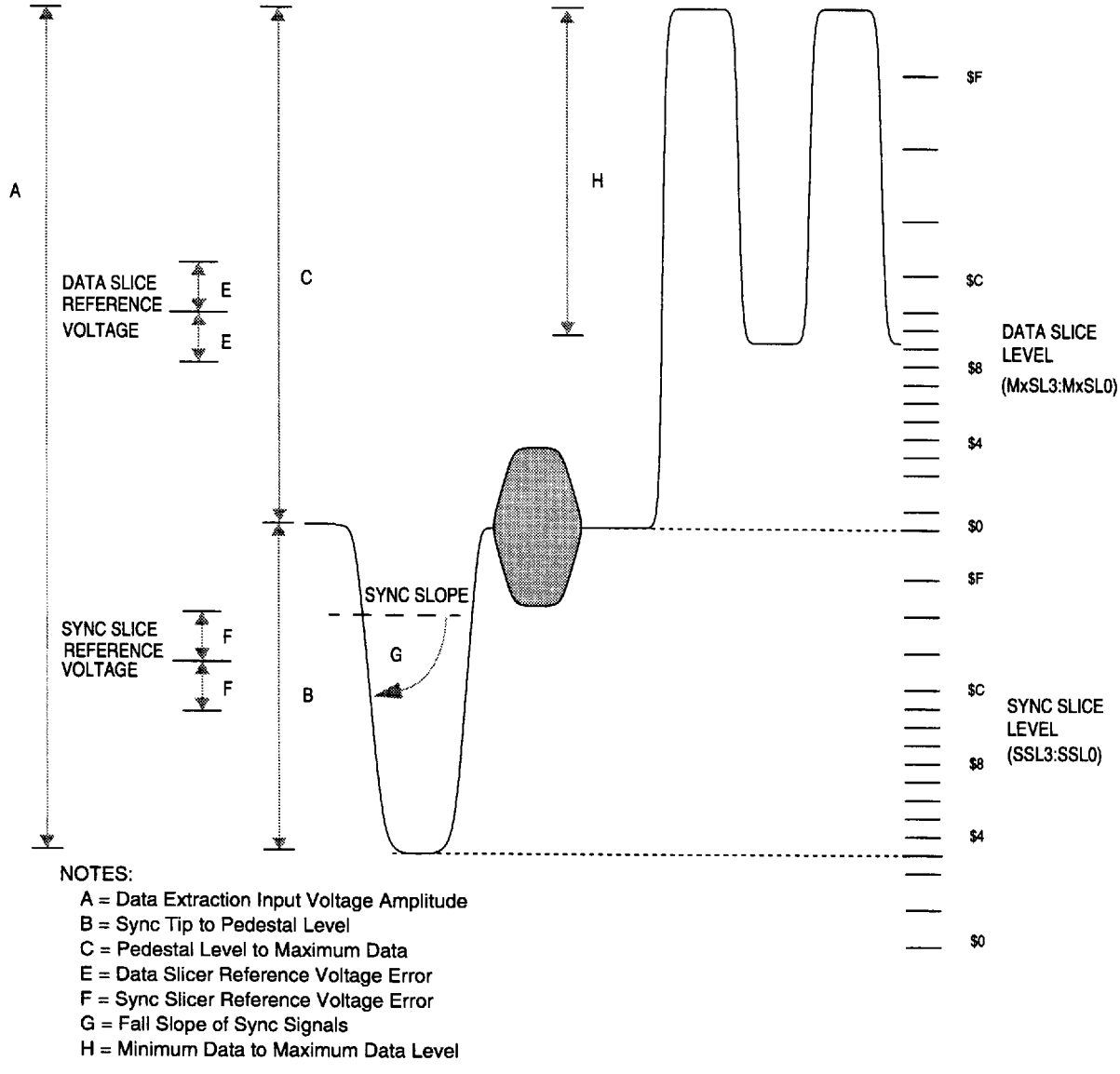


Figure 4-16. Data Extraction Slice Level Description

Data and sync slice levels must be selected by the user based on the characteristics of the input signal. See **Figure 4-15** and **Figure 4-16**.

The sync slice level is selected using the SSL3:SSL0 bits in the sync control/status register located at $02 of the control registers. The sync slice level is referenced to the sync tip clamp level. There is a possible error of ±F millivolts in the sync slice reference voltage. Care must be taken when selecting the sync slice reference voltage to ensure that only

those signals considered to be composite sync or quasi-sync pulses cross this reference.

The pedestal level is clamped during lines four and five of each field as shown in **Figure 4-17** and **Figure 4-18**. If the pedestal voltage change between lines 4 and 28 is less than 12.5 mV, the data slice level need not be adjusted to compensate for this change.

Table 4-1. Sync Slice Levels

SSL3: SSL0	Tap	D	Sync Slice Reference Voltage for $V_{DD2} - V_{SS2}$ =			SSL3: SSL0	Tap	D	Sync Slice Reference Voltage for $V_{DD2} - V_{SS2}$ =		
			4.5 V	5.0 V	5.5 V				4.5 V	5.0 V	5.5 V
$0	55	–5	–108 mV	–120	–133	$8	65	5	108 mV	120	133
$1	57	–3	–65	–72	–80	$9	66	6	129	144	159
$2	59	–1	–22	–24	–27	$A	67	7	151	168	186
$3	60	0	0	0	0	$B	68	8	172	192	212
$4	61	1	22	24	27	$C	69	9	194	216	239
$5	62	2	43	48	53	$D	71	11	237	264	292
$6	63	3	65	72	80	$E	73	13	280	312	345
$7	64	4	86	96	106	$F	75	15	323	360	398

The data slice level is selected using the MxSL3:MxSL0 bits in the individual mode select registers. The data slice level is referenced to the pedestal clamp level. There is a possible error of ±E millivolts in the data slice reference voltage. Care must be taken when selecting the data slice reference voltage to ensure that during the vertical blanking interval lines selected for data extraction only those signals considered to be valid data pulses cross this reference.

Table 4-2. Data Slice Levels

MxSL3: MxSL0	Tap	D	Data Slice Reference Voltage for $V_{DD2} - V_{SS2}$ =			MxSL3: MxSL0	Tap	D	Sync Slice Reference Voltage for $V_{DD2} - V_{SS2}$ =		
			4.5 V	5.0 V	5.5 V				4.5 V	5.0 V	5.5 V
$0	61	1	22 mV	24	27	$8	70	10	215 mV	240	265
$1	63	3	65	72	80	$9	71	11	237	264	292
$2	64	4	86	96	106	$A	72	12	258	288	318
$3	65	5	108	120	133	$B	73	13	280	312	345
$4	66	6	129	144	159	$C	75	15	323	360	398
$5	67	7	151	192	186	$D	78	18	387	432	477
$6	68	8	172	216	212	$E	82	22	473	528	583
$7	69	9	194	240	239	$F	86	26	559	624	689

Average sync and data slice levels can be calculated for any power supply voltage using the variable D included in the above tables.

$$V_{Slice} = ((V_{DD2} - V_{SS2}) - 200\ mV) \times D/200$$

Where V_{Slice} is the data or sync slice level. These voltages represent average values with no tolerance. Actual voltages may vary slightly.

4.9.1 Pedestal Clamp and Data Slicer Circuit Diagram

Figure 4-17 illustrates the pedestal clamp and data slicer circuit for the 68HC68VBI. The sync slice circuit is not shown in the diagram.

The pedestal clamp level is an internal fixed reference level not available to the user. The data slice level reference voltage is determined by MxSL3:MxSL0. The four transistors that compose the large buffer and small buffer are used to accurately determine and clamp the pedestal voltage level and hold it on the capacitor attached to the V_{Data} pin.

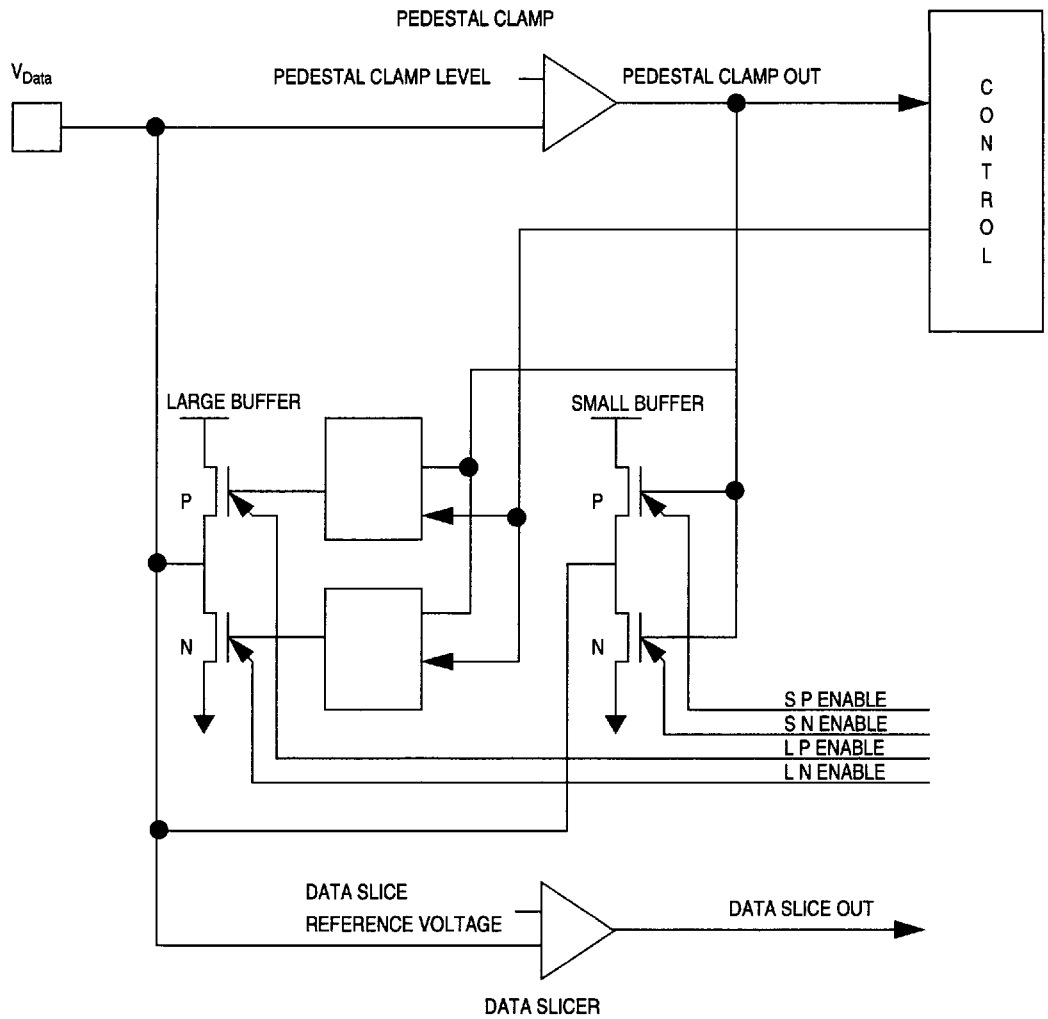


Figure 4-17. Pedestal Clamp and Data Slicer

4.9.2 Pedestal Clamp Timing Diagram

The pedestal level is clamped during lines 4 and 5. **Figure 4-18** illustrates the active clamping time for the large P and large N transistors. The small P and small N are similarly active in the line 5 interval.

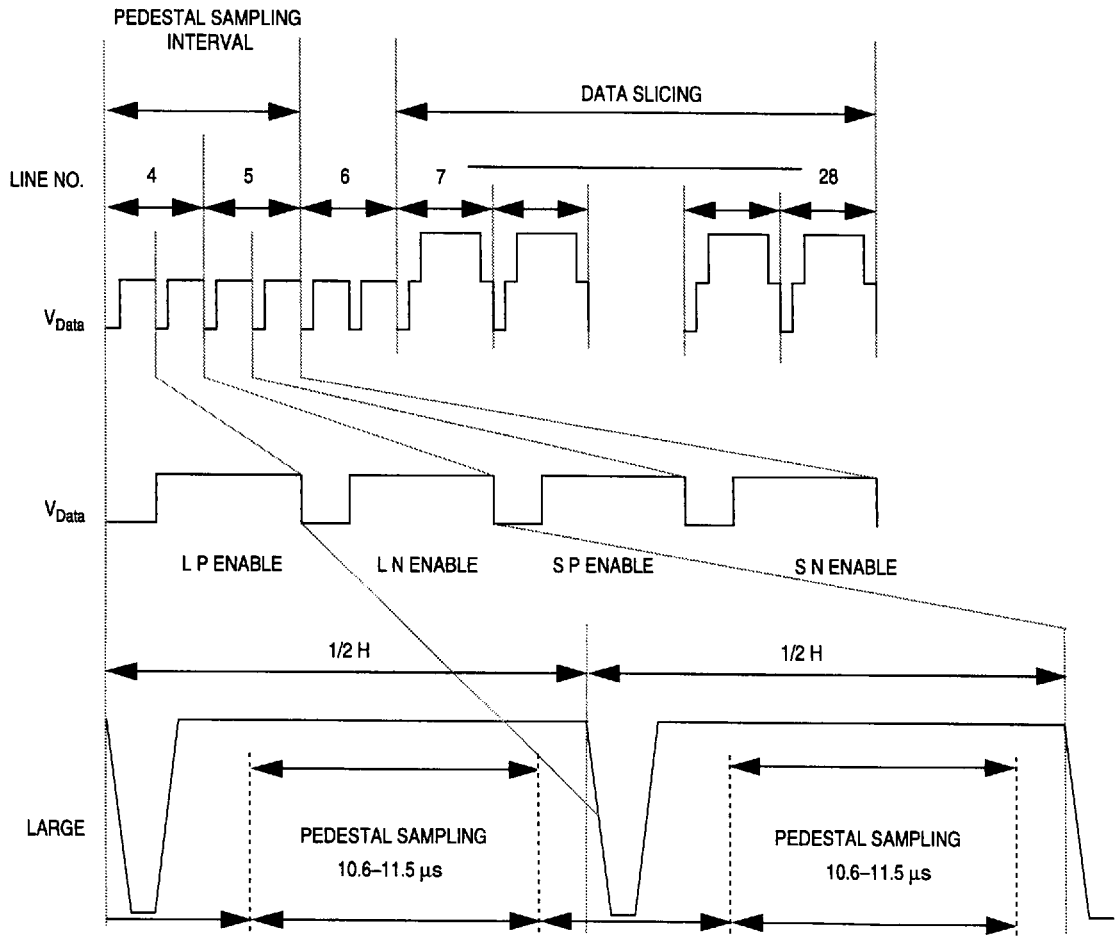


Figure 4-18. Pedestal Clamp Timing

4.10 Extraction Control Register

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	EIF	EB	0	0	0	0	0	EEN
Write:			EIC					
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-19. Extraction Control Register (EXCTR)

EIF — Extraction Interrupt Flag

This bit is set by detection of line 30 by the extraction module line counter based on the sync selected by RSS. This read only bit is cleared by writing a 1 to the EIC bit. Reset clears this bit.

EB — Extraction Module BUSY

This bit is set from line one to line 30 by the extraction module line counter based on the sync selected by RSS. Reset clears this bit.

EIC — Extraction Interrupt Clear

The EIC bit is write only and always reads as 0. Writing a 1 to this bit clears EIF. Writing 0 to this bit has no effect.

1 = Clear EIF
0 = No effect

Bits 4:1 — Reserved

These bits are not used and always read 0.

EEN — Extraction Module Enable

The EEN bit enables the data extraction module.
Reset clears this bit.

1 = Extraction module enabled
0 = Extraction module disabled

4.11 Mode Description Registers

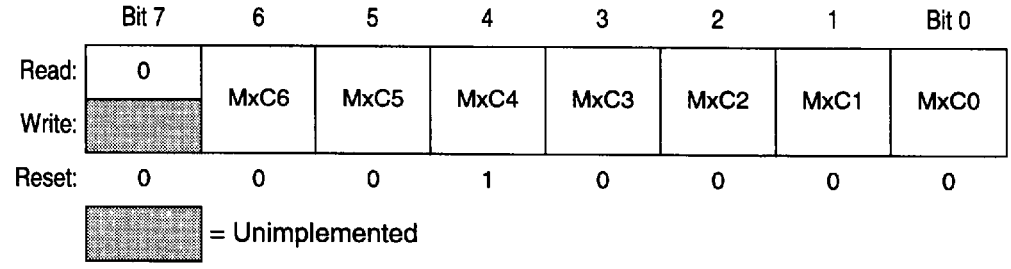


Figure 4-20. Mode Description Register 0 (MxD0, MxD1, and MxD2)

Bit 7 — Reserved

This bit is not used and always reads 0.

MxC6:MxC0 — Mode x Clock Delay

These bits determine how many counts of the input delay clock, extraction VCO frequency divided by four, will be delayed from the leading edge of the horizontal sync pulse before the clock synchronization edge detect circuit is enabled. This register should not be set to less than 16, its reset state.

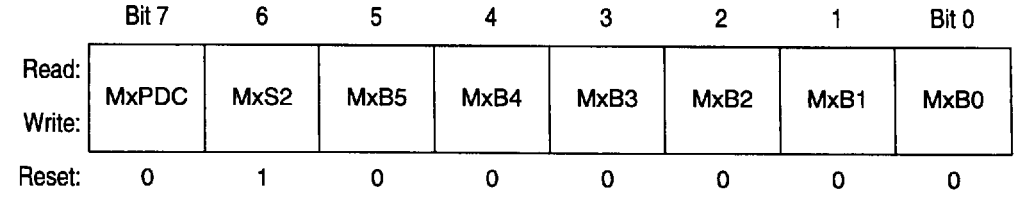


Figure 4-21. Mode Description Register 1 (MxD1)

MxPDC — Mode x PDC select

This bit selects PDC mode.

Write:

1 = PDC mode

0 = Normal mode

MxS2 — Mode x Switch 2

This bit determines the setting of PLL's clock switch.

Write:

1 = Sampling clock is output of B divider.

0 = Sampling clock is output of A divider.

MxB5:MxB0 — Mode x number of Bytes per line

These bits give the number of bytes per line for the specified mode. For PDC mode (MxPDC = 1), this count starts from and includes the framing code. For non-PDC modes (MxPDC = 0), this count starts from the first byte.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MxSL3	MxSL2	MxSL1	MxSL0	MxRF	MxLEN	MxREN	MxOEN
Reset:	0	0	0	0	0	0	0	0

Figure 4-22. Mode Description Register 2 (MxD2)

MxSL3:MxSL0 — Mode x Slice Level

These bits determine the voltage level at which the vertical blanking information data will be sliced.

MxRF — Mode x Rising/Falling edge clock synchronization

This bit determines the edge on which the sampling clock is synchronized.

Write:

1 = Clock synchronization edge is falling edge of video signal.

0 = Clock synchronization edge is rising edge of video signal.

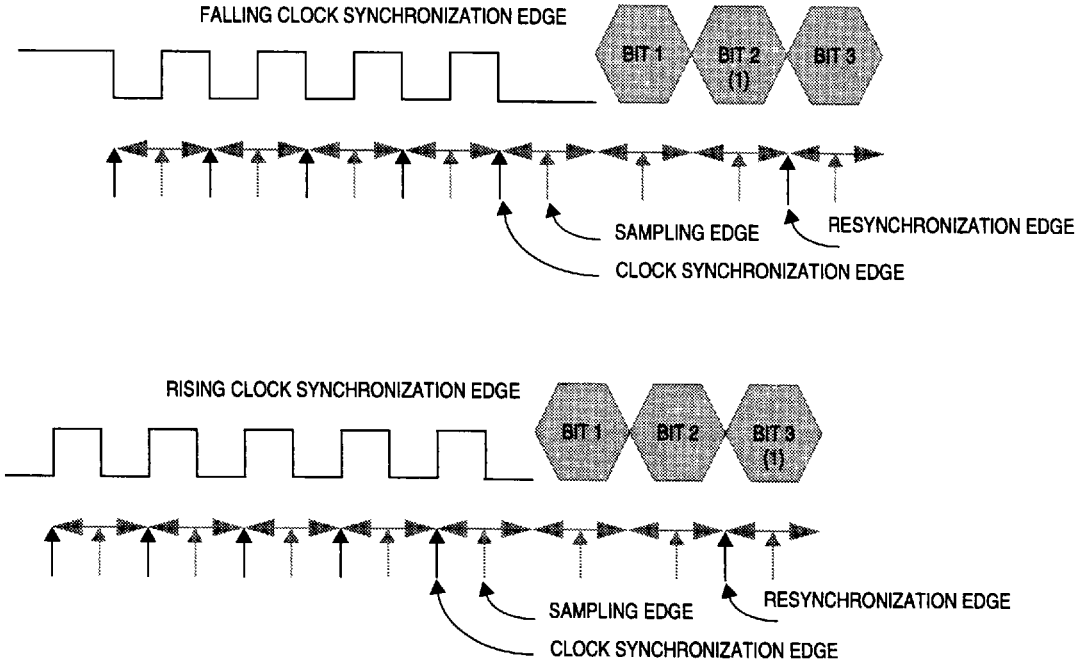


Figure 4-23. Clock Synchronization Edge

MxLEN — Mode x Digital Low Pass Filter Enable

This bit enables the V_{Data} digital low pass filter.

Write:

1 = Filter enabled
0 = Filter disabled

A digital low pass filter has been included in the data slicer signal chain to improve performance under noisy conditions. Since this filter will remove signal pulses with a duration of less than four VCO clocks, it is not suitable for very high frequency data and care should be exercised in its application.

The maximum noise duration is $4/(f_{Sync} * C)$. Where f_{Sync} is the frequency of the horizontal sync input on the $\overline{SYNC}$ pin and C is the value of C0:C7 in the EPLLD register plus 1728. Any pulse, negative or positive, having a duration of less than $4/(f_{Sync} * C)$ will be considered noise and will be removed.

The minimum signal duration is $4/(f_{Sync} * C)$. All pulses having a duration of greater than $4/(f_{Sync} * C)$ will be considered as data bits and not removed.

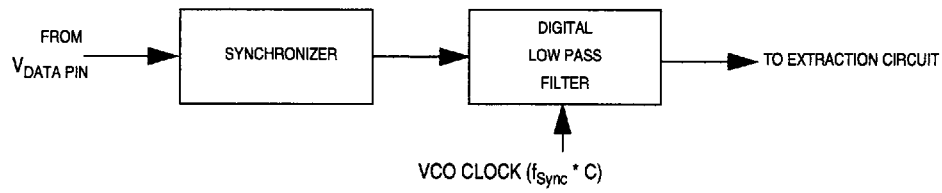


Figure 4-24. Digital Low Pass Filter Block Diagram

MxREN — Mode x Resynchronization Circuit Enable

This bit enables the extraction module clock resynchronization circuit.

Write:

1 = Resynchronization disabled
0 = Resynchronization enabled

If this bit is set, the resynchronization circuit will be disabled. After expiration of the count in the clock delay register and resynchronization to the first rising edge, no clock resynchronization will be done.

If this bit is clear, resynchronization will be performed on every edge specified by MxRF as illustrated in **Figure 4-23**.

MxOEN — Mode x Data Slicer Output Enable

This bit enables the extraction module data slicer outputs SDATA, SCLK, and SWIN.

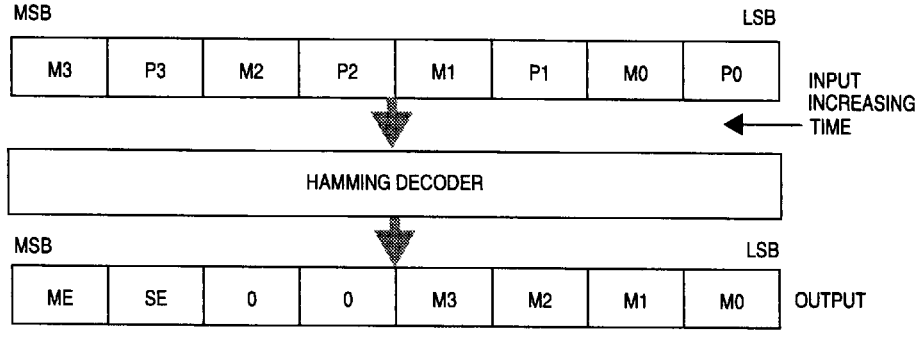
Write:

1 = Data slicer output signal enabled for mode x enabled
0 = Data slicer output signal disabled for mode x disabled

In serial mode, when this bit is set, SDATA, SCLK, and SWIN are enabled. These signals will become active as described in **Figure 4-4**. In serial mode, when this bit is clear SDATA,SCLK, and SWIN will be fixed low. In parallel mode, this bit has no effect.

4.12 Teletext Hamming Decoder

The extraction module includes a teletext Hamming decoder for use in PDC mode. The decoder is used for single error detection and correction of bytes 4 through 12 in format 8/30 packets and bytes 4 through 25 in format 2 8/30 packets. Additionally, multiple errors are detected.



The input byte consists of four message bits (M3, M2, M1, and M0) and four protection bits (P3, P2, P1, and P0). If a single error occurs in any of these bits, the error will be corrected in the output byte and the single error bit, SE, will be set in the output byte. If multiple errors occur, the multiple error bit, ME, will be set. If multiple errors are present, they cannot be corrected.

Table 4-3. Teletext Hamming Decoder

Input Byte								Output Nibble			
M3	P3	M2	P2	M1	P1	M0	P0	M3	M2	M1	M0
0	0	0	1	0	1	0	1	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	1	0	0	1	0	0	1	0
0	1	0	1	1	1	1	0	0	0	1	1
0	1	1	0	0	1	0	0	0	1	0	0
0	1	1	1	0	0	1	1	0	1	0	1
0	0	1	1	1	0	0	0	0	1	1	0
0	0	1	0	1	1	1	1	0	1	1	1
1	1	0	1	0	0	0	0	1	0	0	0
1	1	0	0	0	1	1	1	1	0	0	1
1	0	0	0	1	1	0	0	1	0	1	0
1	0	0	1	1	0	1	1	1	0	1	1
1	0	1	0	0	0	0	1	1	1	0	0
1	0	1	1	0	1	1	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	0	1	1	1	1

4.13 PDC Mode

This mode allows the user to select data based on detection of extension data packets of type 8/30. Additionally, teletext Hamming decode will be performed as shown in **Figure 4-25**.

This sequence will be followed:

1. Those lines selected for PDC mode (MxPDC = 1), will be sampled into the circuitry according to the sampling clock and mode description for that line.
2. The data stream will be searched for a match to the teletext framing code. When at least seven of eight bits match the framing

code, the framing code will be entered into the data registers without any error correction. If no framing code is detected before the leading edge of the next line's horizontal sync, one byte of data 00 is entered into the data registers and the process stops.

3. Following Hamming decode, bytes 4 and 5, the magazine row and address group, are compared to the 8/30 format code. If the magazine and row address group do not match the 8/30 format code, these bytes are not entered into the data registers and the process stops. If a match occurs, these bytes are entered into the data registers and the process continues.

4. Following Hamming decode, byte 6, the designation code, is compared to the format 2 designation code. If the designation code is format 2, PDC mode will be assumed and bytes 7 through 25 are Hamming decoded and entered into the data registers. If the designation code is other than format 2, only bytes 7 through 12 will be Hamming decoded and entered into the data registers.

5. The remaining bytes, counted from the framing code until expiration of MxB5:MxB0, are entered into the data register without Hamming decode. See **Figure 4-26.**

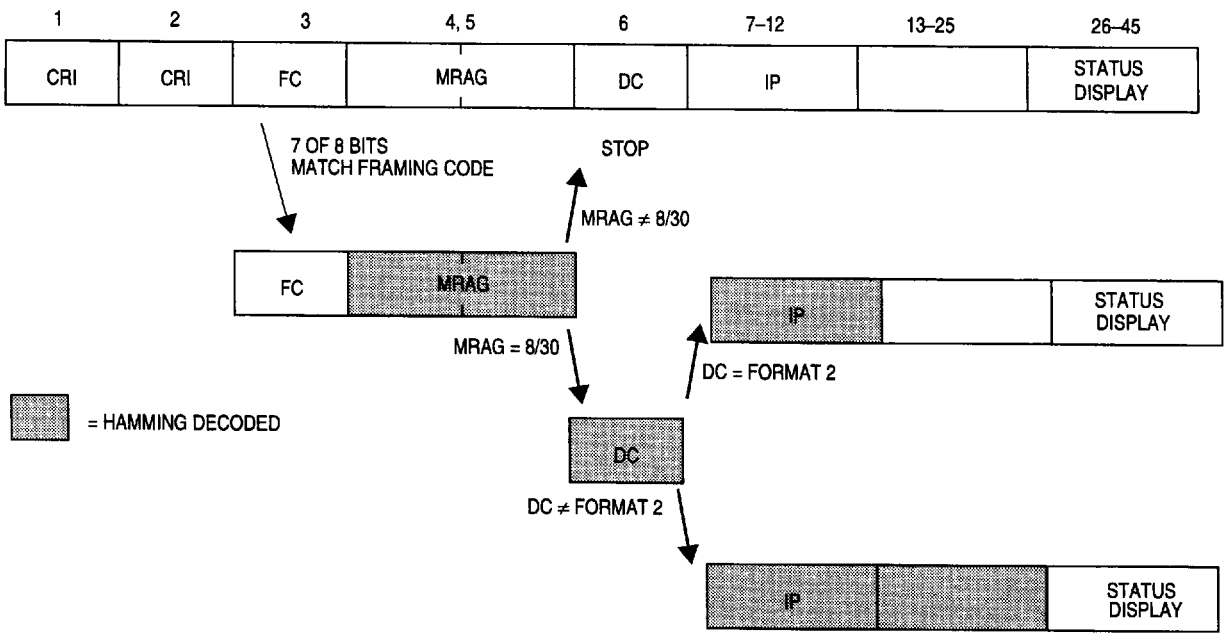


Figure 4-25. PDC Mode Teletext Hamming Decode Enable Diagram

4.13.1 Framing Code Synchronization

The third byte of every data line comprises the framing code 11100100. This code can be used to establish byte synchronization even if one bit of the framing code has been wrongly received. **Figure 4-26** indicates how incoming data are compared with the framing code pattern. It shows that a test for any seven corresponding bits will give a correct indication of the framing code in the presence of a single error.

The framing code is not Hamming decoded. However, a single bit error is allowed. After seven of the eight bits of the framing code have been located in the bit stream, the framing code is entered into the data registers with no error correction.

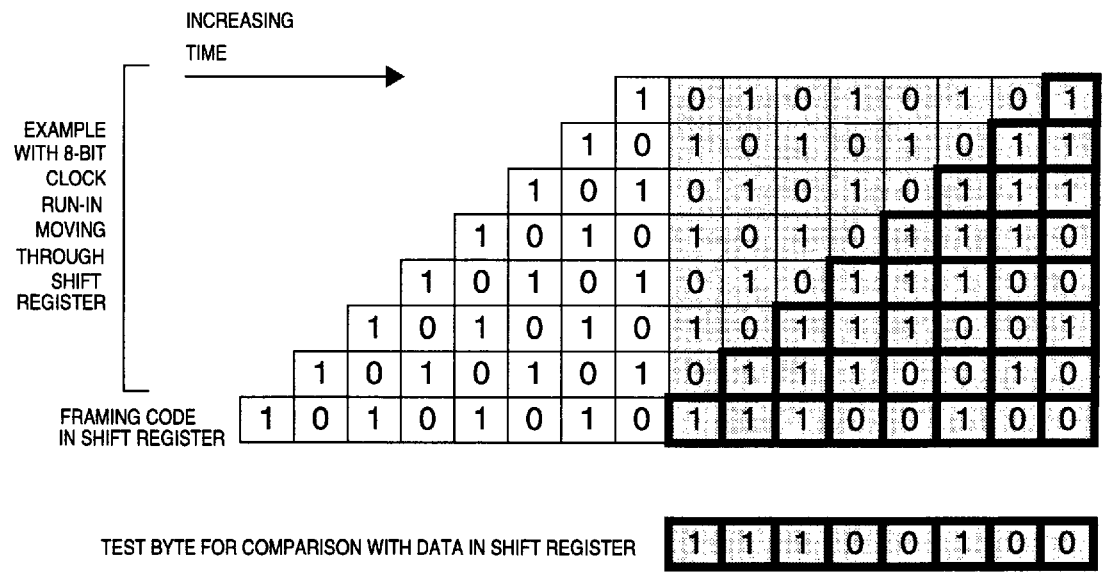


Figure 4-26. Operation of Framing Code Synchronization

4.13.2 8/30 Magazine and Row Address Group Match

The forth and fifth bytes of every data line are the magazine and row address group. These codes are used to determine if a line is 8/30 format or not. **Figure 4-27** indicates how incoming data are compared with the 8/30 format pattern. It shows that the bytes are first teletext Hamming decoded before the comparison is performed, allowing for a single correctable bit error in each byte. If this code is not matched, an error is assumed and no further data is entered into the data registers.

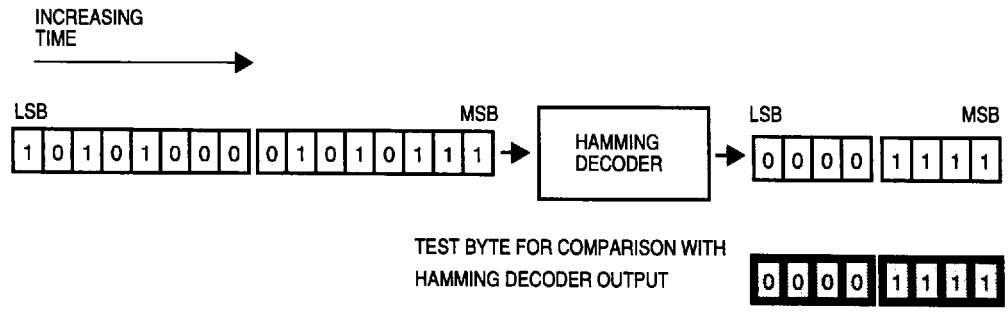


Figure 4-27. Operation of 8/30 MRAG Comparison

4.13.3 Format 2 Designation Code Match

The sixth byte of 8/30 format data lines is the designation code. This code is used to determine if a line is format 2 or not. **Figure 4-27** indicates how incoming data is compared with the format 2 pattern. It shows that the bytes are first teletext Hamming decoded before the comparison is performed, allowing for a single correctable bit error. If this code is matched, format 2 will be assumed and, if read, bytes 7 through 25 will be Hamming decoded. If this code is not matched, bytes 7 through 12 will be Hamming decoded, but the remaining bytes will not be Hamming decoded.

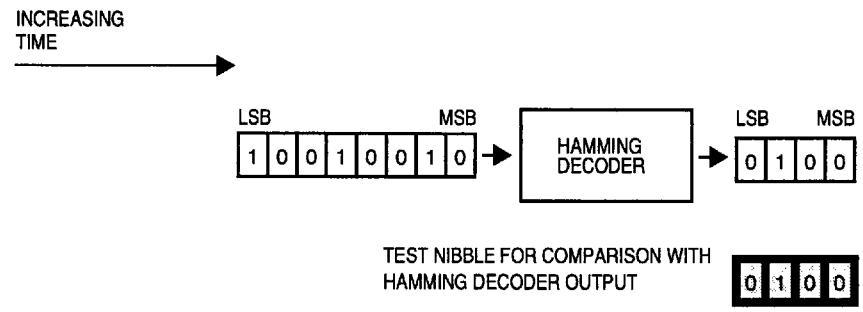


Figure 4-28. Operation of Format 2 Designation Code Comparison

4.14 Line Control Registers

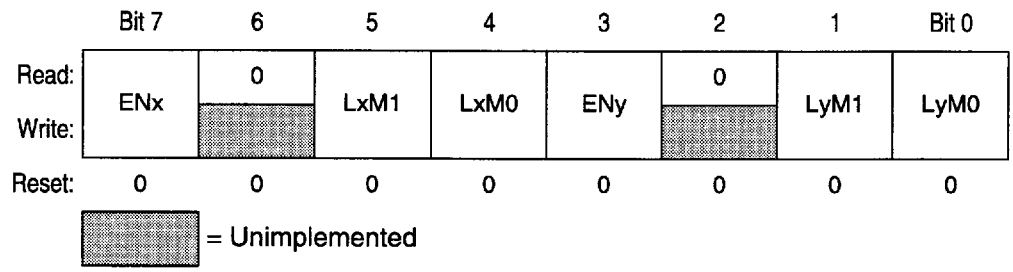


Figure 4-29. Line Control Registers x/y (LCRx/LCRy)

ENx and ENy — Line output enable bits

These bits enable data acquisition for the indicated line number, x or y.

LxM1:LxM0 and LyM1:LyM0 — Line x/y mode bits

These bits determine the mode number for the line number indicated, x or y.

4.15 Field Sync Line 7 Sync Registers

Address: $0080

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	—	FLD	LRPL	SCHK	L7C3	L7C2	L7C1	L7C0
Write:								
Reset:	0	0	0	0	U	U	U	U

= Unimplemented U = Unaffected

Figure 4-30. Field Sync Line 7 Sync Registers (FSL7)

Bit 7 — Reserved

These bit is not used. Reading this bit can yield 1 or 0.

FLD — FieLD

This bit indicates the most recently sampled field of display.

Read:

1 = Field 2
0 = Field 1

LRPL — Lock state of PLL

This bit indicates if the PLL is locked to the input signal. See the description in **3.4 PLL State Description**.

Read:

1 = Locked
0 = Not locked

SCHK — Sync Check

This bit is set when the clamped input signal on the $\overline{\text{SYNC}}$ pin is less than the voltage reference determined by SSL3:SSL0 including comparator offset. This bit is cleared by a read of $80 or by a read of $02.

L7C3:L7C0 — Line 7 Quasi-Sync Count

These bits give the number of quasi-sync pulses counted in line 7 of the most recently sampled field of display.

4.16 Quasi-Sync Line Count Registers

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LxC3	LxC2	LxC1	LxC0	LyC3	LyC2	LyC1	LyC0
Write:								
Reset:	U	U	U	U	U	U	U	U

= Unimplemented U = Unaffected

Figure 4-31. Line Control Register x/y (L8/L9–L22/L23)

LxC3:LxC0 — Line x Quasi-Sync Count

These bits give the number of quasi-sync pulses counted in line *x* of the most recently sampled field of display.

LyC3:LyC0 — Line x Quasi-Sync Count

These bits give the number of quasi-sync pulses counted in line *y* of the most recently sampled field of display.

4.17 PDC Address Register

Address: $0089

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MULT	PAR6	PAR5	PAR4	PAR3	PAR2	PAR1	PAR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-32. PDC Address Register (PAR)

MULT — Multiple Error

This bit indicates if multiple errors have occurred in any of the teletext Hamming decoded bytes in the present field.

Read:

1 = Multiple error

0 = No multiple error

This read-only bit is cleared by vertical sync.

PAR6:PAR0 — PDC Address Match

These bits are an offset from location $80 to the location of the designation code of the extracted PDC data in the data registers. These bits are cleared by vertical sync detection. If no 8/30 magazine and row address group occurs, these bits will remain 0 to indicate this.

4.18 Read Data x Registers

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RxB7	RxB6	RxB5	RxB4	RxB3	RxB2	RxB1	RxB0
Write:								
Reset:	U	U	U	U	U	U	U	U

= Unimplemented U = Unaffected

Figure 4-33. Read Data Registers (RD0–RD83)

RxB7:RxB0 – Read Data

These registers contain the data extracted from the most recent field. These registers are cleared by detection of a vertical sync. They are not cleared by reset.

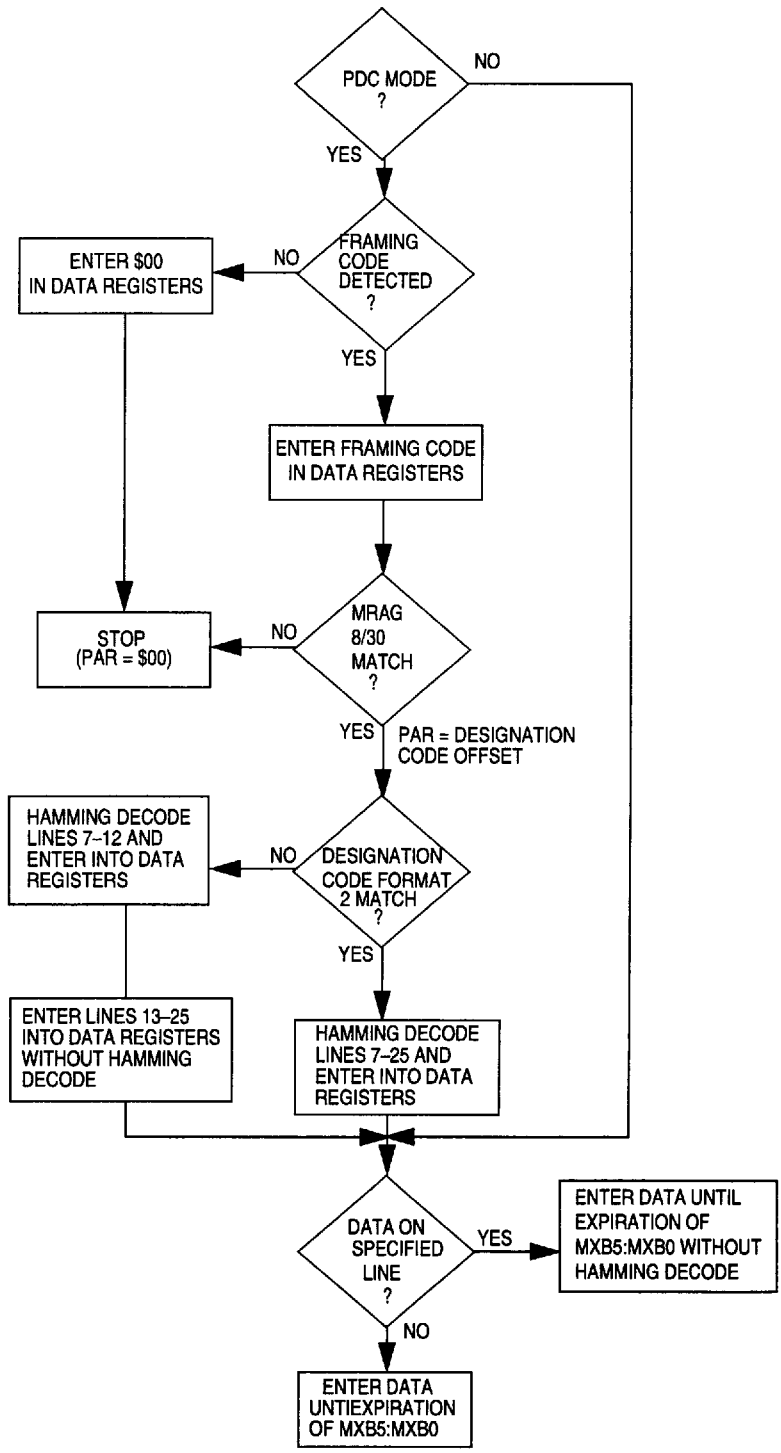


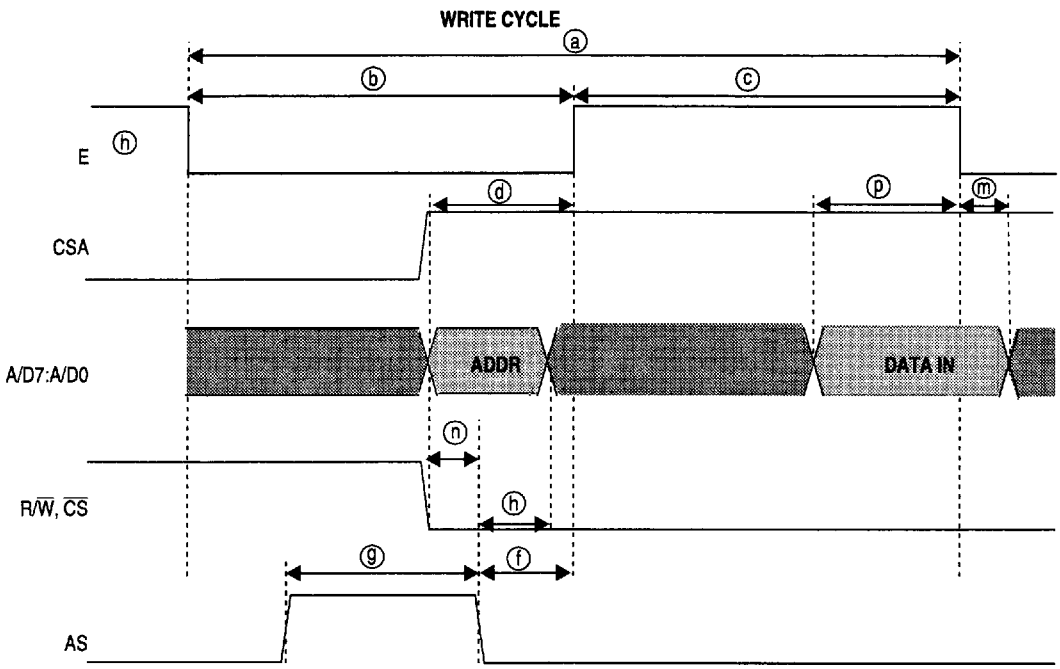
Figure 4-34. Data Entry Flow Diagram

Section 5. Multiplexed Expansion Bus

5.1 Contents

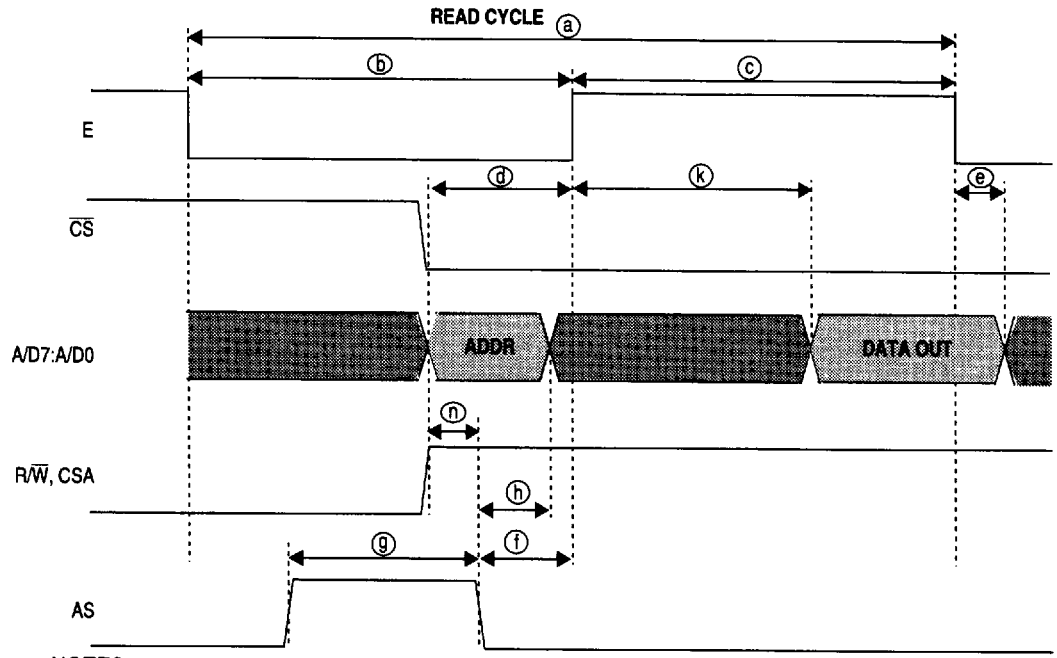
5.2 Introduction

The MC68HC68VBI has an 8-bit, multiplexed, expanded interface for exchange of information between the host MCU and the internal status/data and control registers.



NOTES:
a = Expanded mode input clock (E) period
b = Expanded mode input clock (E) low time
c = Expanded mode input clock (E) high time
d = Address valid signal to E rising edge
f = Delay time, AS to E rising edge
g = AS pulse width
h = Address hold time
m = Input data hold time
n = Address setup time
p = Write data valid signal to E falling edge

Figure 5-1. Multiplexed Expansion Bus Write Cycle Timing



NOTES:
a = Expanded mode input clock (E) period
b = Expanded mode input clock (E) low time
c = Expanded mode input clock (E) high time
d = Address valid signal to E rising edge
e = Output data hold time
f = Delay time, AS to E rising edge
g = AS pulse width
h = Address hold time
k = E rising edge to valid data
n = Address setup time

Figure 5-2. Multiplexed Expansion Bus Read Cycle Timing

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Section 6. Serial Peripheral Interface (SPI)

6.1 Contents

6.2 Introduction

The MC68HC68VBI has a full-duplex serial peripheral interface (SPI) for exchange of information between the host MCU and the internal status/data and control registers. The serial clock (SCK) and chip select ($\overline{CS}$) are provided by the host MCU. Serial data input (SDI) is input only. Serial data output (SDO) is open-drain output only. See **Figure 6-1**.

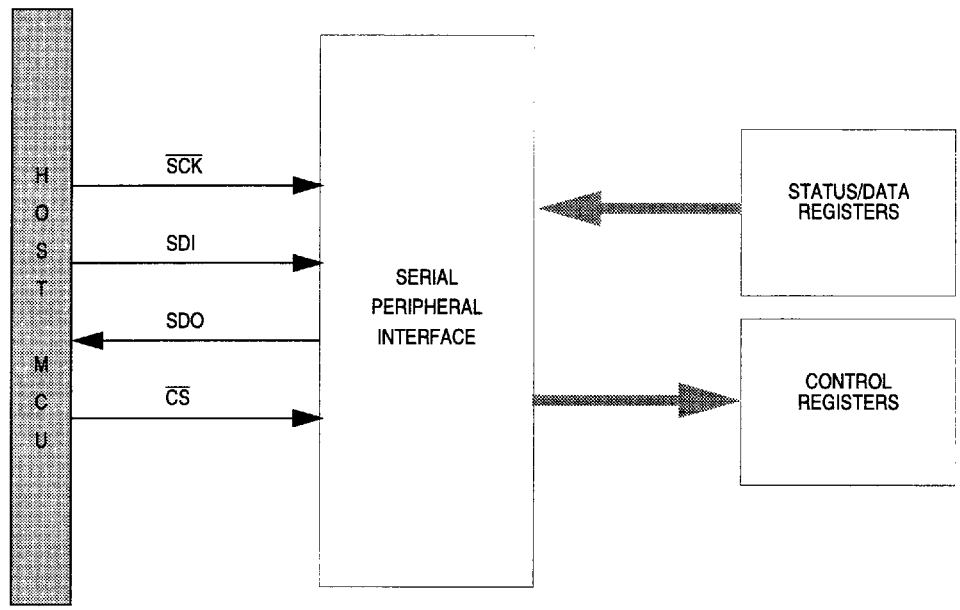


Figure 6-1. SPI Block Diagram

6.3 SPI Memory Access

No registers control the operation of the SPI. However, there is flexibility in how both read and write operations are executed. The start and stop addresses of data written to the control registers are determined by the first two data bytes input to the SPI. Data is always read from address $80 of the status/data registers, but the end address may be selected by terminating the connection. See **Figure 6-2**. Data is sent and received least significant bit (LSB) first as illustrated in **Figure 6-3**.

Before the falling edge of $\overline{CS}$, the $\overline{SCK}$ pin must be held high externally. After chip select is asserted, the first two bytes clocked into the SPI are the write start (STA) and write ignore (IGN) address. Thereafter, data is clocked into the write-only registers starting from address STA. At the ignore address (IGN), data is no longer entered into the memory. Clocks must be applied for a full byte at the ignore address to enter the previous data into the register.

The SPI will enter data sequentially into control registers from the start address until address IGN is reached. The data clocked in at address

IGN can be any data since it will not be entered into the control registers. However, this final byte must be clocked to ensure that all previous bytes have been entered into the control registers.

After the dummy data at address IGN has been clocked in, information exchange can be terminated, if desired. However, if reading of the status/data registers is not complete, additional clocks will not enter data into the control registers after the IGN address.

Starting from the first clock used to clock in address STA, data is clocked out of the read-only registers from address $80. Even after address IGN has been reached, data can be clocked from the SDO pin.

When address $DD of the status/data registers is reached, the data at this address will be clocked out. If clocks are applied after this address, data will continue to be clocked out sequentially. Following data at $FF, data at $00 will be clocked out.

When the serial peripheral interface is selected, the data acquisition module cannot access the internal status/data registers. It is the host processor's responsibility to ensure that the serial peripheral interface is not selected during the vertical blanking interval.

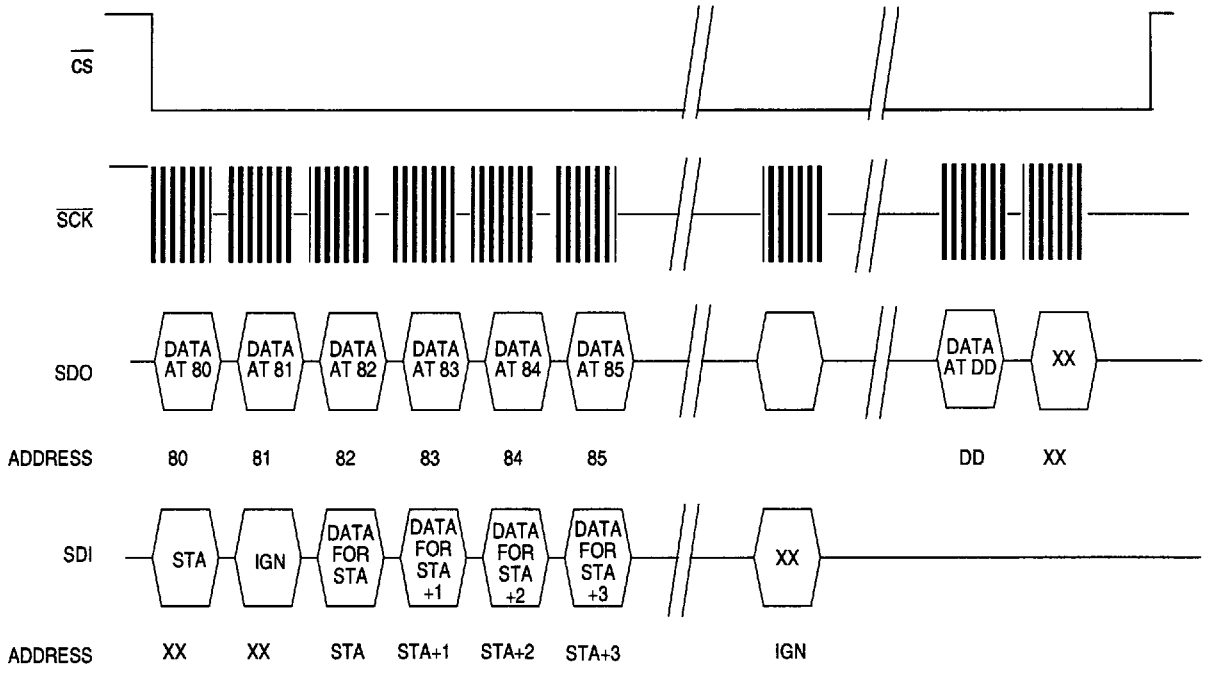
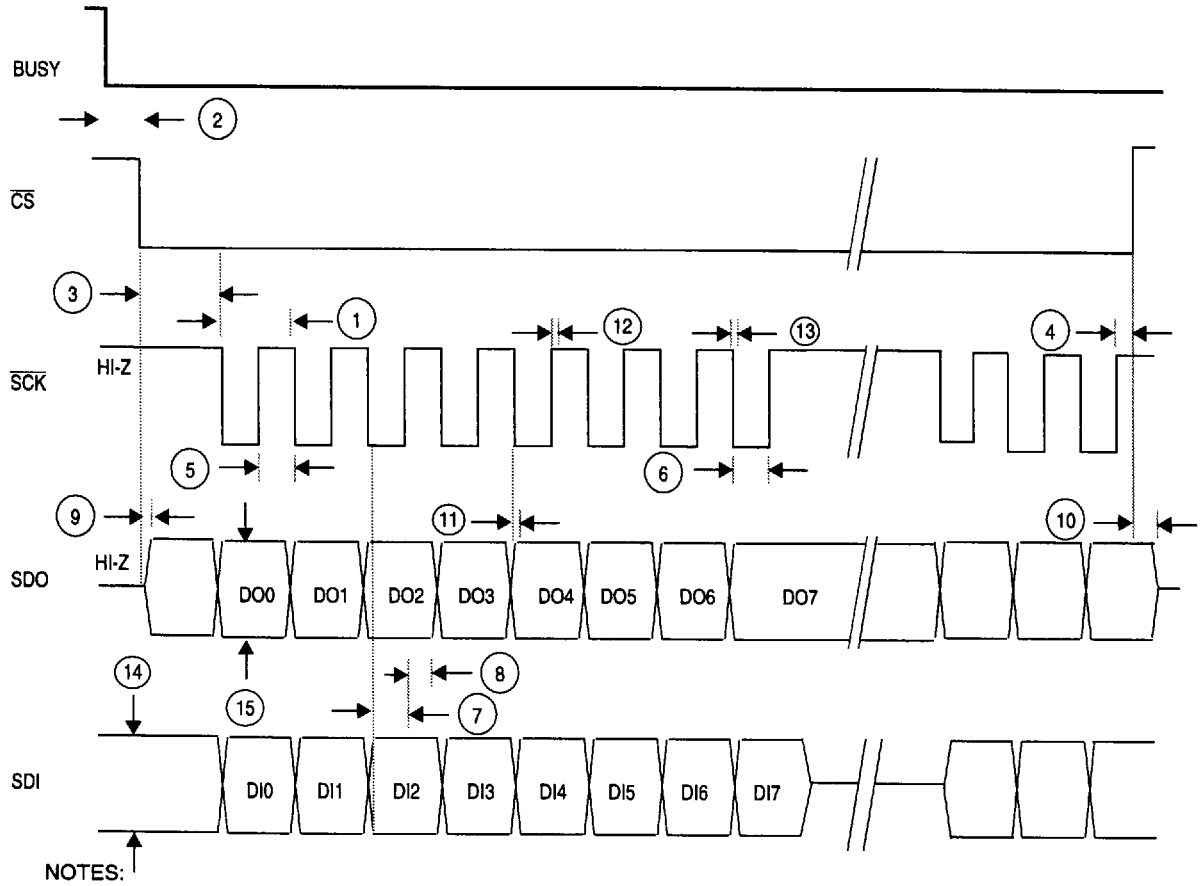


Figure 6-2. SPI Interface Description



NOTES:

1. Cycle time – Time for one cycle of SCK
2. BUSY low to chip selet low time – Wait time required after BUSY low to chip select
3. Chip select lead time – Wait time required after CS low before first clock
4. Chip select lag time – Wait time required after last clock before CS high
5. Clock high time – Time clock is high
6. Clock low time – Time clock is low
7. Data setup time – Time from change in data until rising edge
8. Data hold time – Time from rising edge until data may change
9. Access time – Time high impedance state to active data
10. Disable time – Time from active data to high impedance
11. Data valid –Time from falling edge to active data
12. Rise time – Time from 20% V_{DD} to 70% V_{DD}
13. Fall time – Time from 70% V_{DD} to 20% V_{DD}
14. Input amplitude – V_{IH} and V_{IL} levels of input signal
15. Output amplitude – V_{OH} and V_{OL} levels of output signal

Figure 6-3. SPI Timing Diagram

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Section 7. Electrical Specifications

7.1 Contents

7.2 Introduction

This section contains electrical and timing specifications.

7.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Keep V_{In} and V_{Out} within the range $V_{SS} < (V_{In}$ or $V_{Out}) < V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} + 0.3	V
Current Drain Per Pin, Excluding V_{DD} and V_{SS}	I	25	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE:
1. Voltages referenced to V_{SS}

7.4 Operating Temperature Range

Rating	Symbol	Value	Unit
Operating Temperature Range MC68HC68VBI (Standard)	T_A	T_L to T_H –5 to +70	°C

7.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance 32-Pin Quad Flat Pack (QFP)	θ_{JA}	195	°C

7.6 5.0 V DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage I_{Load} = ±10.0 µA AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC2	V_{OL} V_{OH}	— V_{DD}–0.1	— —	0.1 —	V
Output High Voltage (I_{Load} = –0.8 mA) AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC2	V_{OH}	V_{DD}–0.8	—	—	V
Output Low Voltage (I_{Load} = 1.6 mA) AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC2	V_{OL}	—	—	0.4	V
Input High Voltage $\overline{RESET}$, CSA SDI/AS, SCK/E, CS (Serial Activated)	V_{IH}	2.0		V_{DD}	V
Input Low Voltage $\overline{RESET}$, CSA SDI/AS, SCK/E, CS (Serial Activated)	V_{IL}	V_{SS}	—	0.8	V
Output Low Voltage (I_{Load} = 1.6 mA) SDO/$\overline{RW}$, BUSY	V_{OL}	—	—	0.4	V
Input High Voltage AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC1,PAR/SER TEST, SDO/RW, SDI/AS, SCK/E, CS (Parallel Activated) SDI/AS, SCK/E, CS (Serial Activated)	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC1, PAR/SER TEST, SDO/RW, SDI/AS, SCK/E, CS (Parallel Activated)	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply Current (See NOTES) Run Power Save 25 °C 0 C to +70 °C (Standard)	I_{DD1} $+I_{DD2}$ $+I_{DD3}$	— — —	13 1 2	18 20 30	mA µA µA
Hi-Z Leakage Current TEST, PAR/SER, RESET, SDI/AS CK/E, CS, CSA, OSC1, AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7	I_L	—	—	± 10	µA
Capacitance AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7, OSC2, BUSY TEST, PAR/SER, RESET, SDI/AS SCK/E, CS, CSA, OSC1, AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7	C_{Out} C_{In}	— —	— —	8 12	pF
Pull-Down Current AD0/SCLK, AD1/SDATA, AD2/SWIN, AD3:AD7 (Serial Mode)	I_{OH}	–10	—	–100	µA

NOTES:

1. V_{DD} = 5.0 V ±10%, T_A = –5 °C to +70 °C
2. Typical values at midpoint of voltage range, 25 °C only.
3. Run supply current measurements made with all modes enabled and PLLs at nominal frequenties.
4. Power save supply current measurements made with all I/O pins configured as inputs, V_{IL} = 0.2 Vdc, V_{IH} = V_{DD} –0.2 Vdc.

7.7 Data Extraction Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Data Extraction Input Voltage Amplitude[1]	A[2]	0.6	1.0	1.5	V
Sync Tip to Pedestal Level	B[2]	143	286	500	mV
Pedestal Level to Maximum Data	C[2]	357	714	1000	mV
Minimum Data to Maximum Data Level	H[2]	200	—	C	mV
Horizontal Line Frequency (525-Line System)	D[2]	15,655	15,734	15,813	Hz
Horizontal Line Frequency (625-Line System)	D[2]	15,546	15,625	15,703	Hz
Data Slicer Reference Voltage Error	E[2]	—	—	100	mV
Sync Slicer Reference Voltage Error	F[2]	—	—	75	mV
Pedestal Voltage Change (Lines 4–28)	—			12.5	mV
Quasi-Horizontal Sync Duration	—	0.25	2	6.1	µs
Vertical Sync Duration	—	19	—	—	µs
Fall Slope of Sync Signals (H_{Sync}, V_{Sync}, Equal Pulse)[3]	G[2]	0.2	1.0	—	mV/ns

NOTES:
1. V_{DD} = 5.0 V ±10%, T_A = –5 °C to +70 °C
2. Refer to **Figure 4-16. Data Extraction Slice Level Description**.
3. 10% to 90% transition slope (This is a calculated recommendation value for proper operation and is not tested.)

7.8 Expanded Interface Characteristic

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Expanded Mode Input Clock (E) Period 10	a	500	500	—	ns
Expanded Mode Input Clock (E) Low Time	b	227	250	—	ns
Expanded Mode Input Clock (E) High Time	c	222	250	—	ns
Address Valid Signal to E Rising Edge	d	84	—	—	ns
Output Data Hold Time	e	33	—	—	ns
Delay Time, AS to E Rising Edge	f	53	—	—	ns
AS Pulse Width	g	96	—	—	ns
Address Hold Time	h	33	—	—	ns
E Rising Edge to Valid Data	k	—	—	128	ns
Input Data Hold Time	m	0	—	—	ns
Address Setup Time	n	26	—	—	ns
Write Data Valid Signal to E Falling Edge	p	40	—	—	ns

NOTES:
1. V_{DD} = 5.0 V ±10%, T_A = –5 °C to +70 °C. Refer to **Figure 5-1. Multiplexed Expansion Bus Write Cycle Timing** and **Figure 5-2. Multiplexed Expansion Bus Read Cycle Timing**.

7.9 Data Slicer Output Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SWIN Leading Edge to Clock	A	170	—	—	ns
Clock to SWIN Trailing Edge	B	29	—	—	ns
SCLK Period	C	139	174	—	ns
SCLK High Time	D	29	84	—	ns
SCLK Low Time	E	29	50	—	ns
Data Setup Time	F	29	84	—	ns
Data Hold Time	G	29	50	—	ns
Signal Falling Time	H	—	20	40	ns
Signal Rising Time	I	—	20	40	ns

NOTES:
1. V_{DD} = 5.0 V ±10%, T_A = –5 °C to +70 °C
2. This table is valid only for Moji Tajuu frequency signals with five or more VCO samplings per data bit.
3. C_{Load} = 90 pF
4. Refer to **Figure 4-4. Data Slicer Output Signal Timing Diagram**.

7.10 Serial Peripheral Interface Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Cycle Time	t_{cyc}	500	—	—	ns
Busy Low to Chip Select Low Time	t_{BCS}	500	—	—	ns
Chip Select Lead Time	t_{Lead}	240	—	—	ns
Chip Select Lag Time	t_{LAG}	240	—	—	ns
Clock High Time	t_H	190	—	—	ns
Clock Low Time	t_L	190	—	—	ns
Data Setup Time	t_{SU}	100	—	—	ns
Data Hold Time	t_{HO}	100	—	—	ns
Access Time	t_A	0	—	120	ns
Disable Time	t_{DIS}	—	—	240	ns
Data Valid	t_V	—	—	240	ns
Rise Time	t_R	—	—	100	ns
Fall Time	t_F	—	—	100	ns

NOTES:
1. V_{DD} = 5.0 V ± 10%, T_A = –5 °C to +70 °C
2. Refer to **Figure 6-3. SPI Timing Diagram.**

7.11 Phase-Locked Loop Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Phase Jump Ready Time SYS = 0 and f_{OSC} = 3.57 MHz SYS = 1 and f_{OSC} = 4.43 MHz	t_{PJR}	— —	16.0374 19.417	— —	ms

NOTE:
1. Refer to **Figure 3-8.**

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Section 8. Mechanical Specifications

8.1 Contents

8.2 Introduction

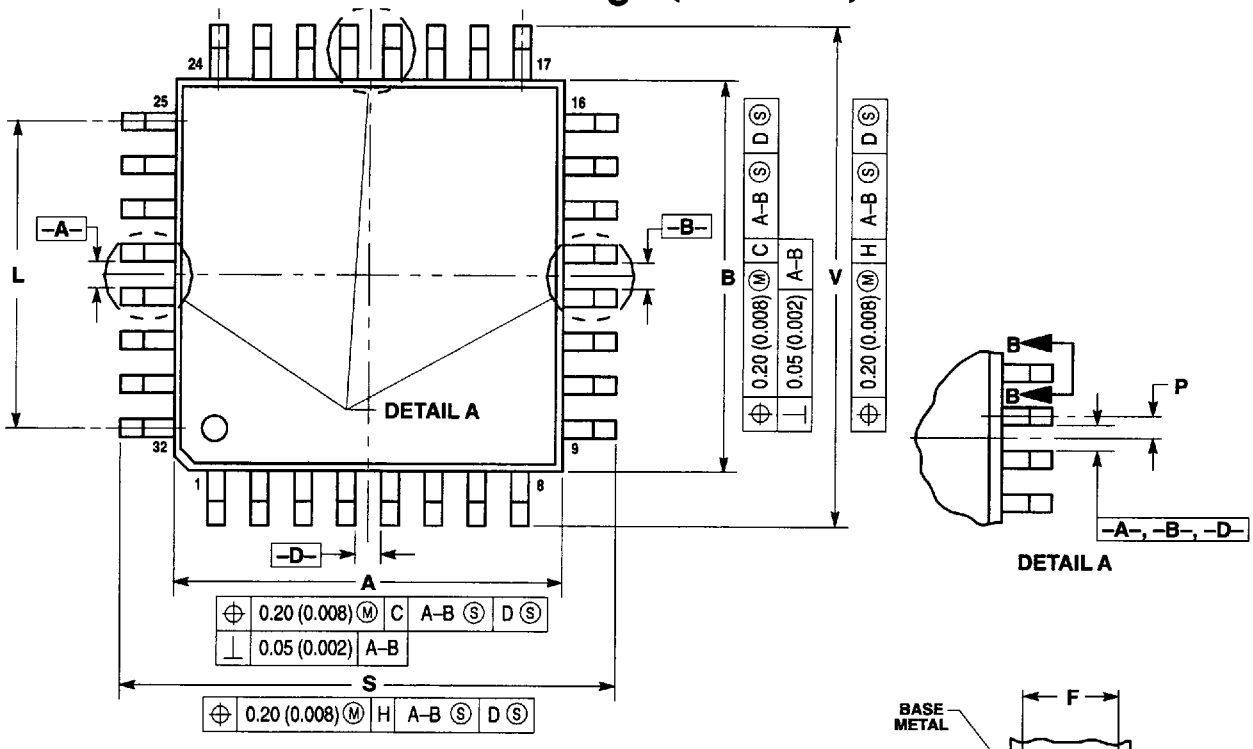
This section describes the dimensions of the dual in-line package (DIP) and small outline integrated circuit (SOIC) MCU packages.

The following figure shows the latest package information at the time of this publication. To make sure that you have the latest package specifications, contact one of the following:

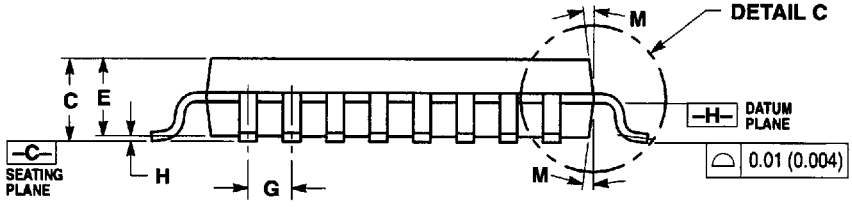
- Local Motorola Sales Office
- Motorola Fax Back System (Mfax™)
  - Phone 1-602-244-6609
  - EMAIL RMFAX0@email.sps.mot.com; http://sps.motorola.com/mfax/
- Worldwide Web (wwweb) home page at http://motorola.com/sps/

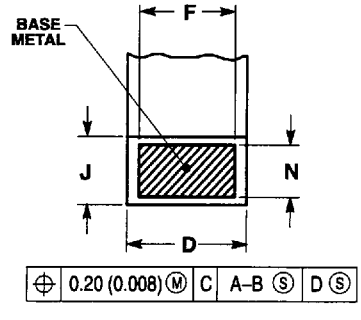
Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.

8.3 28-Pin Plastic Dual In-Line Package (Case 873)

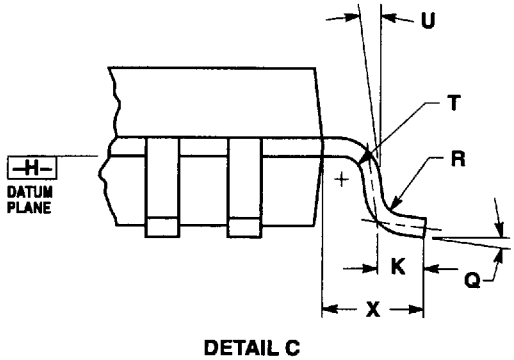


DETAIL A





SECTION B–B
VIEW ROTATED 90 ° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

Section 9. Ordering Information

9.1 Contents

9.2 Introduction

This section contains ordering information for the MC68HC68VBI.

9.3 MC Order Number

Table 9-1 shows the MC order number for the available package type.

Table 9-1. MC Order Number

Package Type	Operating Temperature Range	MC Order Number
28-Pin Plastic Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HC68VBIFB