SECTION 7
ELECTRICAL CHARACTERISTICS

7.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage	V_{in}	– 0.3 to + 7.0	V
Operating Temperature Range MC68302	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to his high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD})

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.

7.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for TQFP	θ_{JA}	52.8	°C/W
	θ_{JC}	10.4	°C/W

$T_J = T_A + (P_D \cdot \theta_{JA})$
$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

where:
$P_{I/O}$ is the power dissipation on pins.
For T_A = 70°C and $P_{I/O}$ = 0 W, 20.48 MHz, 5.25 V, and TQFP package, the worst case value of T_J is:
T_J = 70°C + (5.25 V · 30 mA · 52.8°C/W) = 78.3C

7.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction to Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts—Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected.

If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.4 POWER DISSIPATION

Characteristic	Symbol	Typ	Max	Unit
Power Dissipation at 20.48 MHz	I_{DD}	30	60	mA
Power Dissipation: WAIT Mode	I_{DD}	5		mA
Power Dissipation: STOP Mode	I_{DD}	100		µA

NOTES:

1. Values measured with maximum loading of 130 pF on all output pins. Typical means 5.0 V at 25°C. Maximum means guaranteed maximum over maximum temperature (70°C) and voltage (5.25 V).

7.5 DC ELECTRICAL CHARACTERISTICS

Table 7-1. DC Electrical Characteristics (V_{CC} = 5.0V ±5%)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage for non-Schmitt Trigger Input Pins (Except for EXTAL)	V_{IH}	2.0	V_{DD}	V
Input Low Voltage (Except for RESET, PIO[15:0], LA(23:20), L1RXD, L1CLK, L1SYNC, L1GRNT, SCPRXD and EXTAL)	V_{IL}	V_{SS}–0.3	0.8	V
Input High Voltage for pins that have Schmitt trigger. (RESET, PIO[15:0], LA(23:20), L1RXD, L1CLK, L1SYNC, L1GRNT, SCPRXD)	V_{IH}	2.2	V_{DD}	V
Input Low Voltage for pins that have Schmitt trigger inputs (RESET, PIO[15:0], LA(23:20), L1RXD, L1CLK, L1SYNC, L1GRNT, SCPRXD).	V_{IL}	V_{SS}–0.3	0.8	V

Table 7-1. DC Electrical Characteristics (V_{CC} = 5.0V ±5%)

Input High Voltage (EXTAL)	V_{CIH}	0.8*V_{DD}	V_{DD}+0.3	V
Input Low Voltage (EXTAL)	V_{CIL}	V_{SS}–0.3	0.6	V
Input Undershoot Voltage	-	–	–0.8	V
Input Leakage Current	I_{IN}	–	20	µA
Input Capacitance All Pins	C_{IN}	–	20	pF
Three-State Leakage Current, including Open Drain outputs when not driving Low level.	I_{TSL}	-	20	µA
Output High Voltage (I_{OH}=–400[µA])	V_{OH}	2.4	-	V
Output Low Voltage (I_{OL}=3.2 mA) PA[0–15], SCPTxD,SCPCLK, L1GRNT,L1RQ,CLKO (I_{OL}=5.0 mA) L1TxD,TxD (I_{OL}=7.0 mA) L1TxD,TxD (I_{OL}=9.0 mA) PCMCIA mode: PC_D[0–15], IRQSEL,IRQO,PC_IREQ PC_STSCHG,PC_WAIT,PC_CISCS (I_{OL}=24.0 mA) ISA mode: SD[0–15], IRQSEL,IRQO,IRQ3 IOCS16,IOCHRDY,MEMCS16	V_{OL} V_{OL} V_{OL} V_{OL} V_{OL}	- - - - -	0.5 0.5 0.6 0.5 0.5	V
Output Drive CLKO Output Drive All Other Pins	O_{CLK} O_{ALL}	- -	50 100	pF pF
Power	V_{DD}	4.75	5.25	V
Common	V_{SS}	0	0	V

7.6 AC ELECTRICAL SPECIFICATIONS

7.6.1 CLKOUT Timing Specifications

Table 7-2. CLKOUT Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{clk1}	EXTAL Period	65.1		48.8		ns
t_{clk2}	EXTAL Duty Cycle	49	51	49	51	%
t_{clk3}	EXTAL Duty Cycle	49	51	49	51	%
t_{clk4}	CLKOUT to EXTAL Delay	10	31	–	0	ns
t_{clk5}	CLKOUT High Width for CLKOUT=EXTAL cycle	31.5	33.5	23.5	25.5	ns
t_{clk6}	CLKOUT Low Width for CLKOUT=EXTAL cycle	31.5	33.5	23.5	25.5	ns
t_{clk7}	CLKOUT Period for CDIV=00	65	65	48	48.8	ns
t_{clk8}	CLKOUT to EXTAL Delay	13.5	40	–	0	ns
t_{clk9}	CLKOUT High Width for CLKOUT=EXTAL/2 Cycle (CDIV=10)	63.5	66.5	48	50	ns
t_{clk10}	CLKOUT Low Width for CLKOUT=EXTAL/2 Cycle (CDIV=10)	65.5	66.5	48	50	ns
t_{clk11}	CLKOUT Period for CDIV=10	130	130.5	97.6	98	ns
t_{clk12}	CLKOUT Low Width for a Deleted CLKOUT High Cycle			70.5	76.5	ns

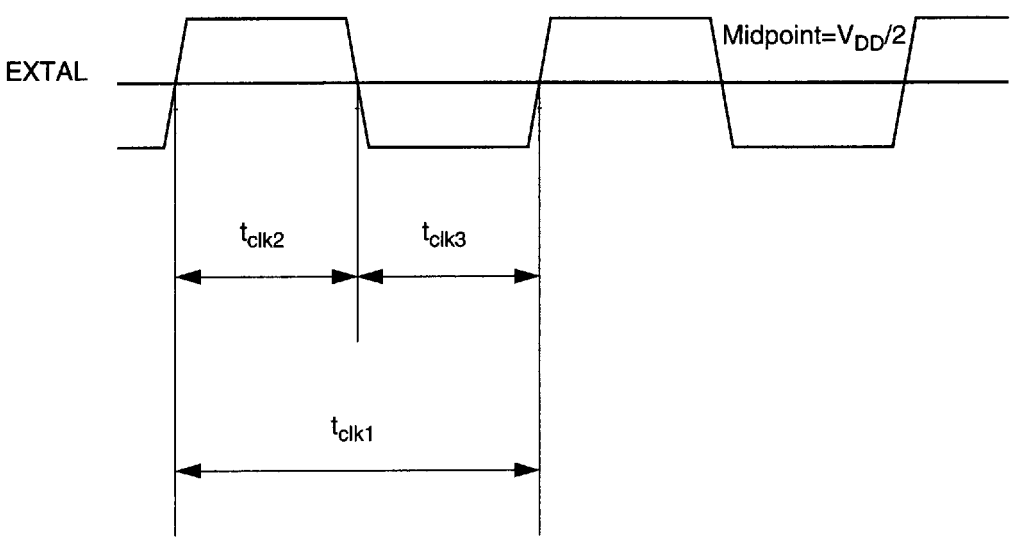


Figure 7-1. CLKOUT Timing Specifications

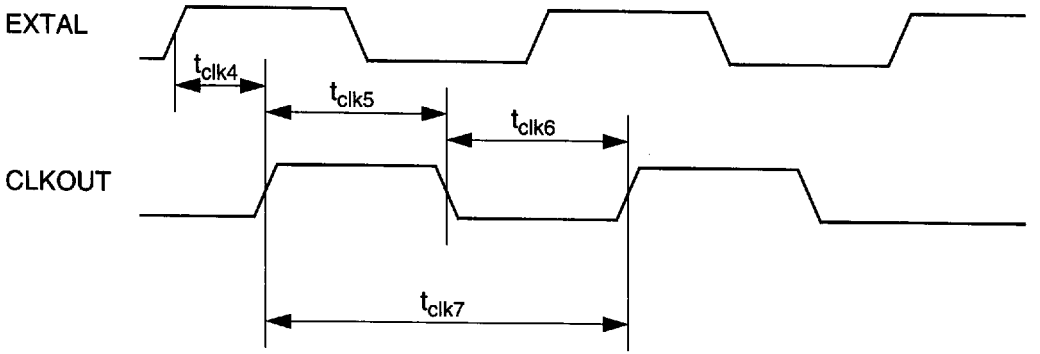


Figure 7-2. CLKOUT Timing for CDIV 1-0=00 in CLKCNT

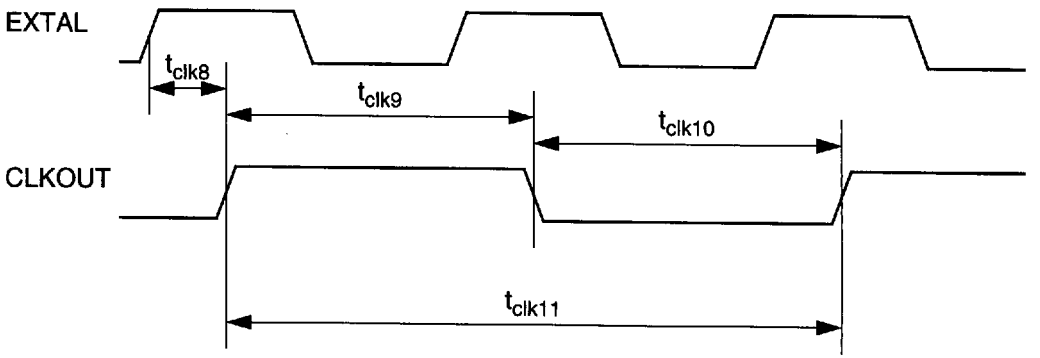


Figure 7-3. CLKOUT Timing for CDIV 1-0=10 in CLKCNT

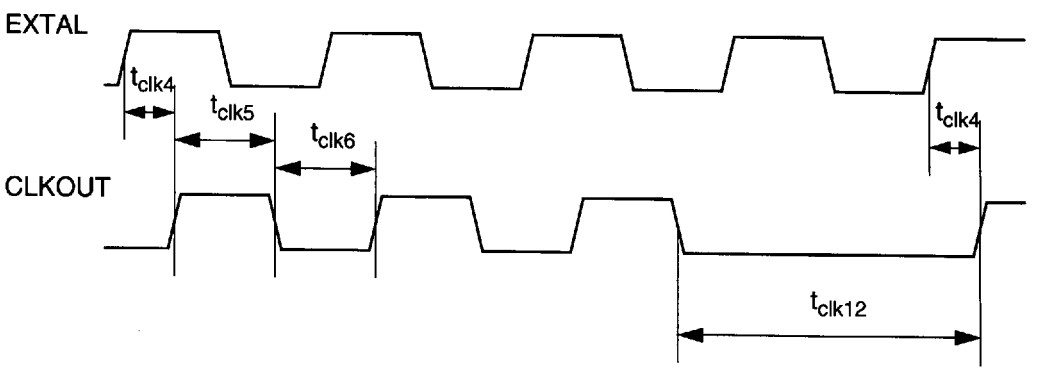


Figure 7-4. CLKOUT Timing for CDIV 1-0=01 in CLKCNT

7.6.2 ISA Host Interface Timing Specifications

7.6.2.1 ISA RESET TIMING SPECIFICATIONS.

Table 7-3. ISA Reset Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{irst1}	RESET pulse width	9	-	9	-	µs
t_{irst2}	RESET inactive to first WRITE access setup time	2	-	2	-	ms
t_{irst3}	$\overline{IOW}$ inactive to RESET inactive setup time	1	-	1	-	µs
t_{irst4}	RESET inactive to first READ access set-up time	2	-	2	-	ms
t_{irst5}	$\overline{IOR}$ inactive to RESET inactive setup time	1	-	1	-	µs
t_{irst6}	0.9 V_{CC} to reset inactive setup	9	-	9	-	µs

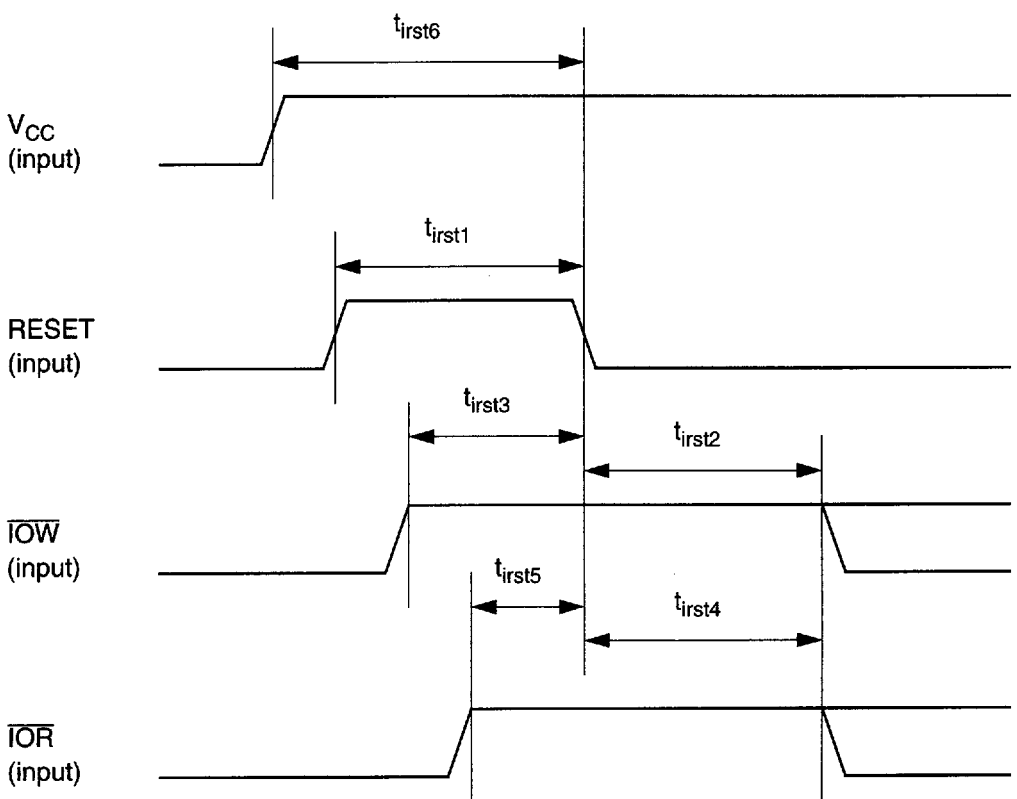


Figure 7-5. ISA Reset Timing Specifications

7.6.2.2 ISA IO SPACE READ ACCESS.

Table 7-4. IO Address Space Read Access (Internal Space)

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{ir1}	SA[15:0], AEN, $\overline{SBHE}$ to $\overline{IOR}$ active setup	22		22		ns
t_{ir2}	SA[15:0], AEN, $\overline{SBHE}$ hold from $\overline{IOR}$ inactive	25		25		ns
t_{ir3}	$\overline{IOR}$ active to inactive	98		75		ns
t_{ir4}	$\overline{IOW}$ / $\overline{IOR}$ to $\overline{IOR}$ delay, No Wait States (Special case: Coupled Accesses)	131	202	100	145	ns
t_{ir5}	$\overline{IOW}$ / $\overline{IOR}$ to Data Valid, No Wait States (Special case: Coupled Accesses)		252		195	ns
t_{ir6}	Data Hold time from $\overline{IOR}$ rising edge	0		0		ns
t_{ir7}	$\overline{IOCS16}$ Active from SA[15:0], AEN and $\overline{SBHE}$ valid		42		42	ns
t_{ir8}	$\overline{IOR}$ active to data out valid		50		50	ns
t_{ir9}	$\overline{IOW}$ / $\overline{IOR}$ to $\overline{IOR}$ delay for non Coupled Accesses, No Wait States	202		145		ns
t_{ir10}	$\overline{IOR}$ active to IOCHRDY falling edge (Inactive)		42		42	ns
t_{ir11}	IOCHRDY inactive (Low) pulse width	160	200	120		ns
t_{ir12}	$\overline{IOR}$ active (Low) hold from IOCHRDY active (High)	0		0		ns
t_{ir13}	Valid read data from IOCHRDY active (Rising edge)		0		0	ns
t_{ir14}	$\overline{IOW}$/$\overline{IOR}$ to $\overline{IOR}$ delay, with Wait States	70		50		ns
t_{ir15}	$\overline{IOR}$ active or inactive to $\overline{NMSICS}$ active or inactive delay		40		40	ns

Table 7-5. PnP Address Space Read Access

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{pnpr1}	SA[15:0], AEN, $\overline{SBHE}$ to $\overline{IOR}$ active setup	22		22		ns
t_{pnpr2}	SA[15:0], AEN, $\overline{SBHE}$ hold from $\overline{IOR}$ inactive	25		25		ns
t_{pnpr3}	$\overline{IOR}$ active to inactive	98		75		ns
t_{pnpr4}	$\overline{IOW}$ to $\overline{IOR}$ delay (Special case: Coupled Accesses)	98	150	75	110	ns
t_{pnpr5}	$\overline{IOW}$ to Data Valid (Special case: Coupled Accesses)		195		155	ns
t_{pnpr6}	Data Hold time from $\overline{IOR}$ rising edge	0		0		ns
t_{pnpr8}	$\overline{IOR}$ active to data out valid		45		45	ns
t_{pnpr9}	$\overline{IOW}$ to $\overline{IOR}$ delay for non Coupled Accesses	140		100		ns

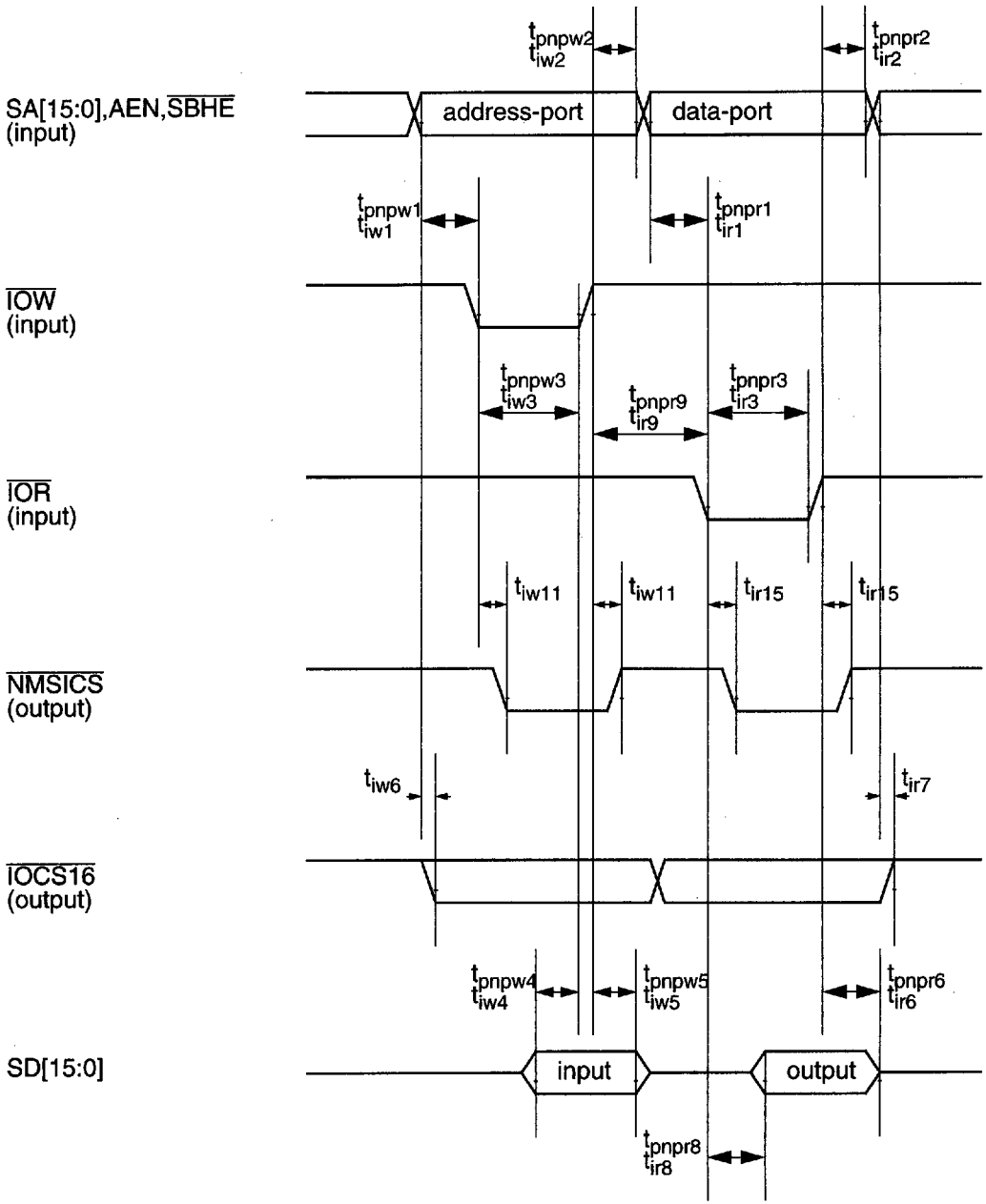


Figure 7-6. IO Space Read Access without Wait States for PnP and Internal Space

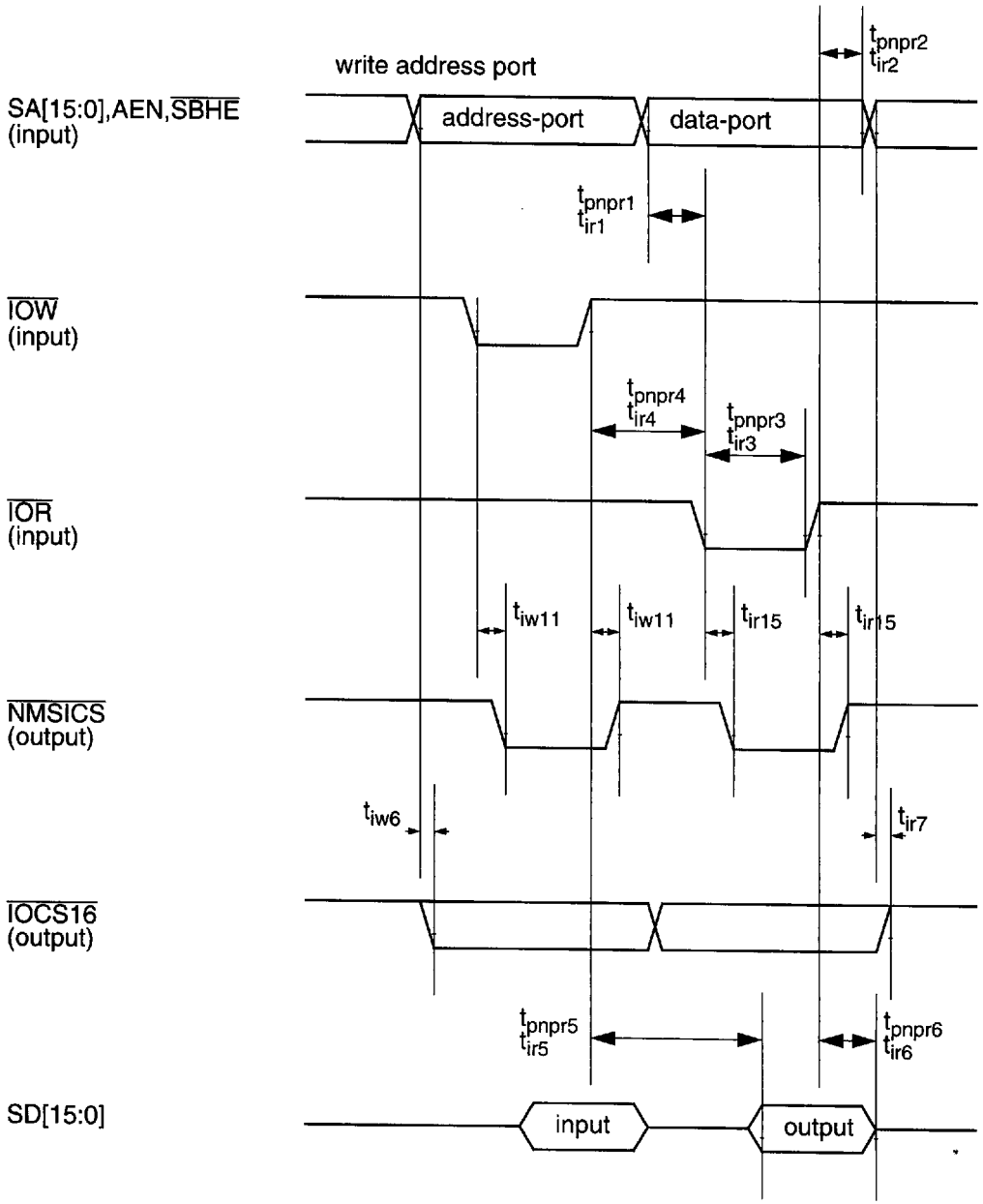


Figure 7-7. IO Space Read Access without Wait States (PnP and Internal Space) - the Special Case of Coupled Accesses

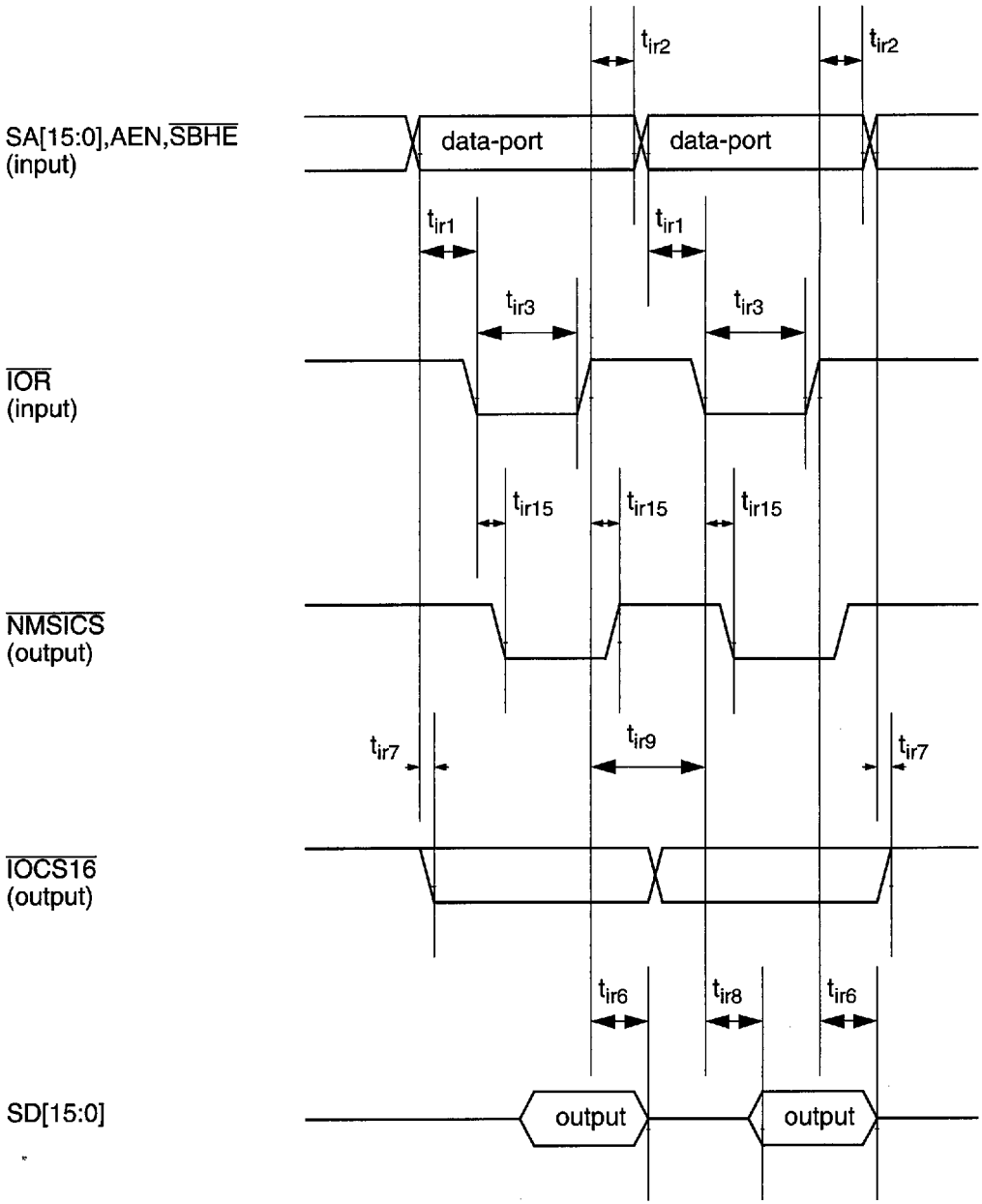


Figure 7-8. IO Space Read Access without Wait States (Internal Space)

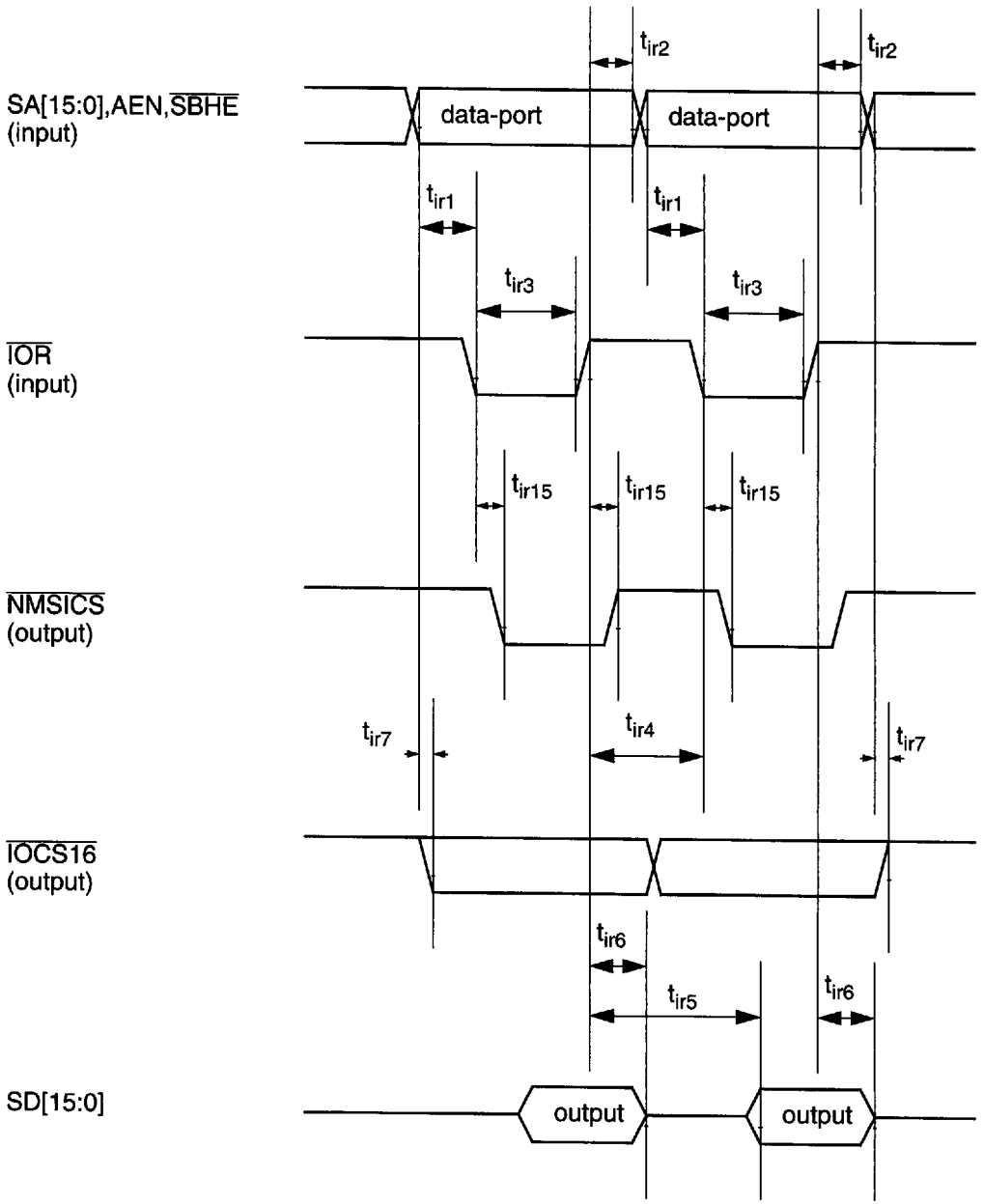


Figure 7-9. IO Space Read Access without Wait States (Internal Space) - the Special Case of Coupled Read Accesses

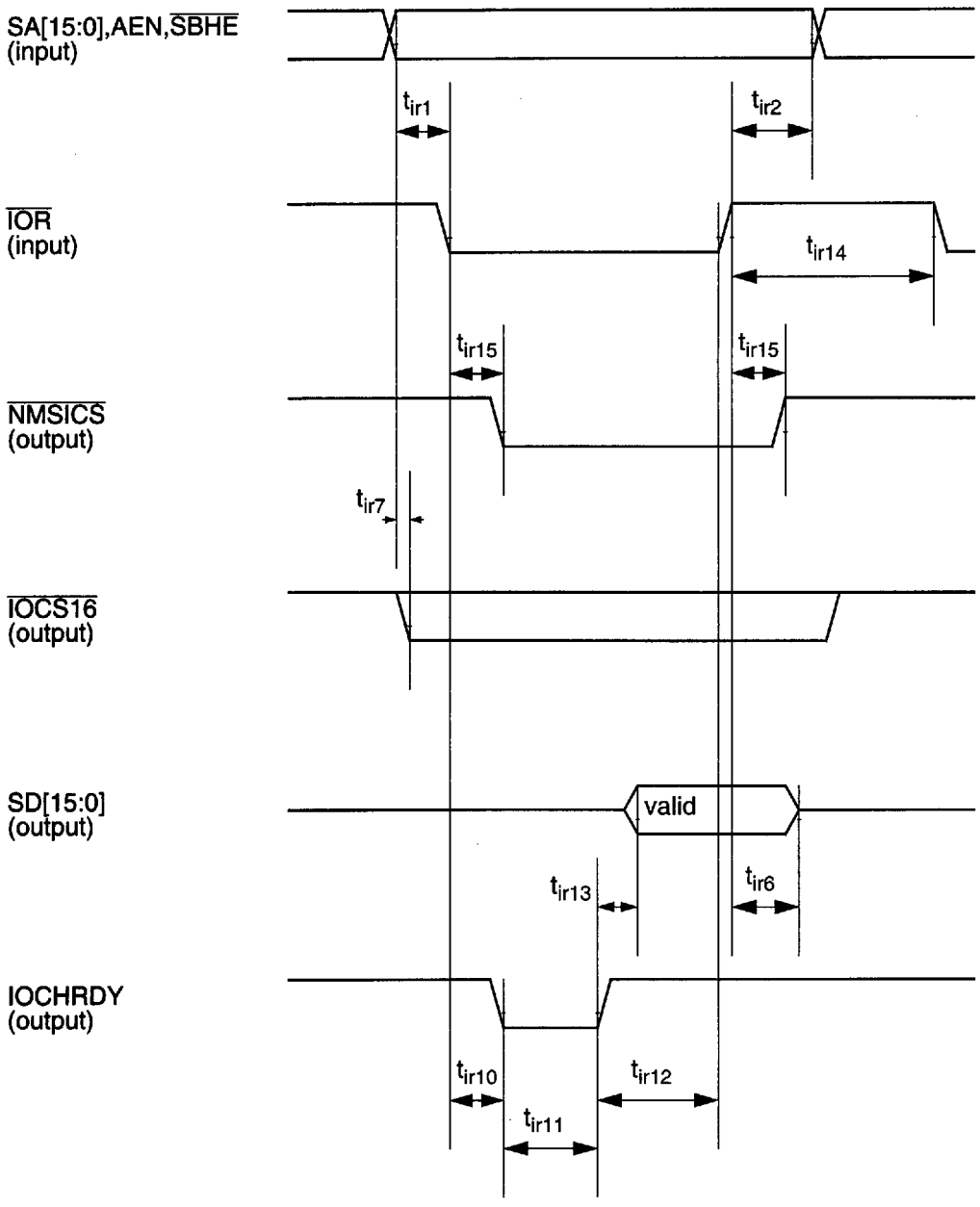


Figure 7-10. IO Space Read Access with Wait States

7.6.2.3 IO SPACE WRITE ACCESS.

Table 7-6. IO Address Space Write Access (Internal Space)

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{iw1}	SA[15:0], AEN, $\overline{SBHE}$ to $\overline{IOW}$ active setup	22		22		ns
t_{iw2}	SA[15:0], AEN, $\overline{SBHE}$ hold from $\overline{IOW}$ inactive	25		25		ns
t_{iw3}	$\overline{IOW}$ active to inactive	98		75		ns
t_{iw4}	Data valid setup to $\overline{IOW}$ rising edge (Inactivation)	40		40		ns
t_{iw5}	Data hold time from $\overline{IOW}$ rising edge (Inactivation)	15		15		ns
t_{iw6}	$\overline{IOCS16}$ Active from SA[15:0], AEN and $\overline{SBHE}$ valid		42		42	ns
t_{iw7}	$\overline{IOW}$ inactive time	131		100		ns
t_{iw8}	$\overline{IOW}$ active (Low) hold from IOCHRDY active (High)	0		0		ns
t_{iw9}	$\overline{IOW}$ active to IOCHRDY falling edge (Inactive)		42		42	ns
t_{iw10}	IOCHRDY inactive (Low) pulse width	120		160		ns
t_{iw11}	$\overline{IOW}$ active or inactive to $\overline{NMSICS}$ active or inactive delay		40		40	ns

Table 7-7. PnP Address Space Write Access

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{pnpw1}	SA[15:0], AEN, $\overline{SBHE}$ to $\overline{IOW}$ active setup	22		22		ns
t_{pnpw2}	SA[15:0], AEN, $\overline{SBHE}$ hold from $\overline{IOW}$ inactive	25		25		ns
t_{pnpw3}	$\overline{IOW}$ active to inactive	98		75		ns
t_{pnpw4}	Data valid setup to $\overline{IOW}$ rising edge (Inactivation)	40		40		ns
t_{pnpw5}	Data hold time from $\overline{IOW}$ rising edge (Inactivation)	15		15		ns
t_{pnpw7}	$\overline{IOW}$ inactive time	98		75		ns

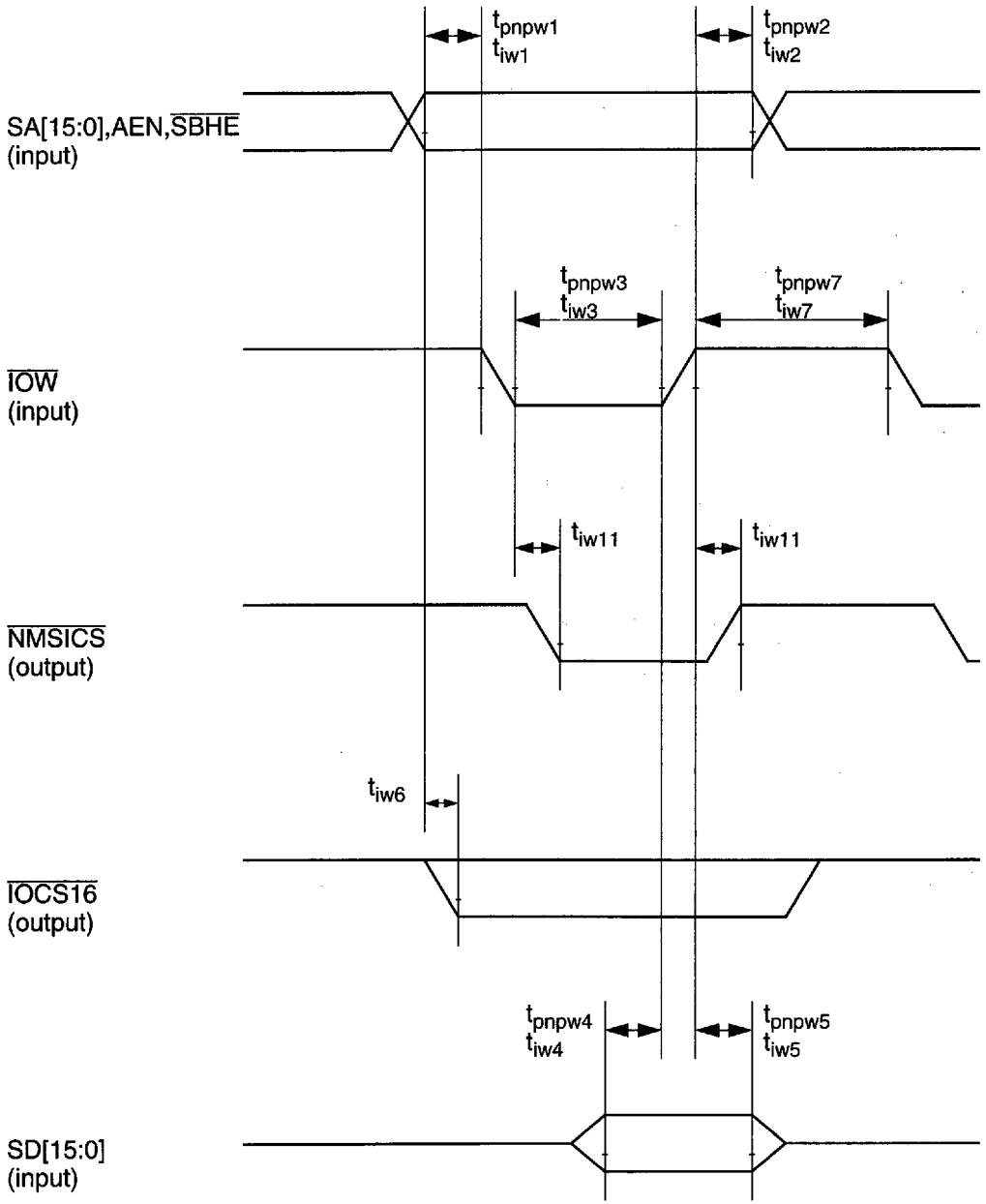


Figure 7-11. IO Space Write Access without Wait states (PnP and Internal Space)

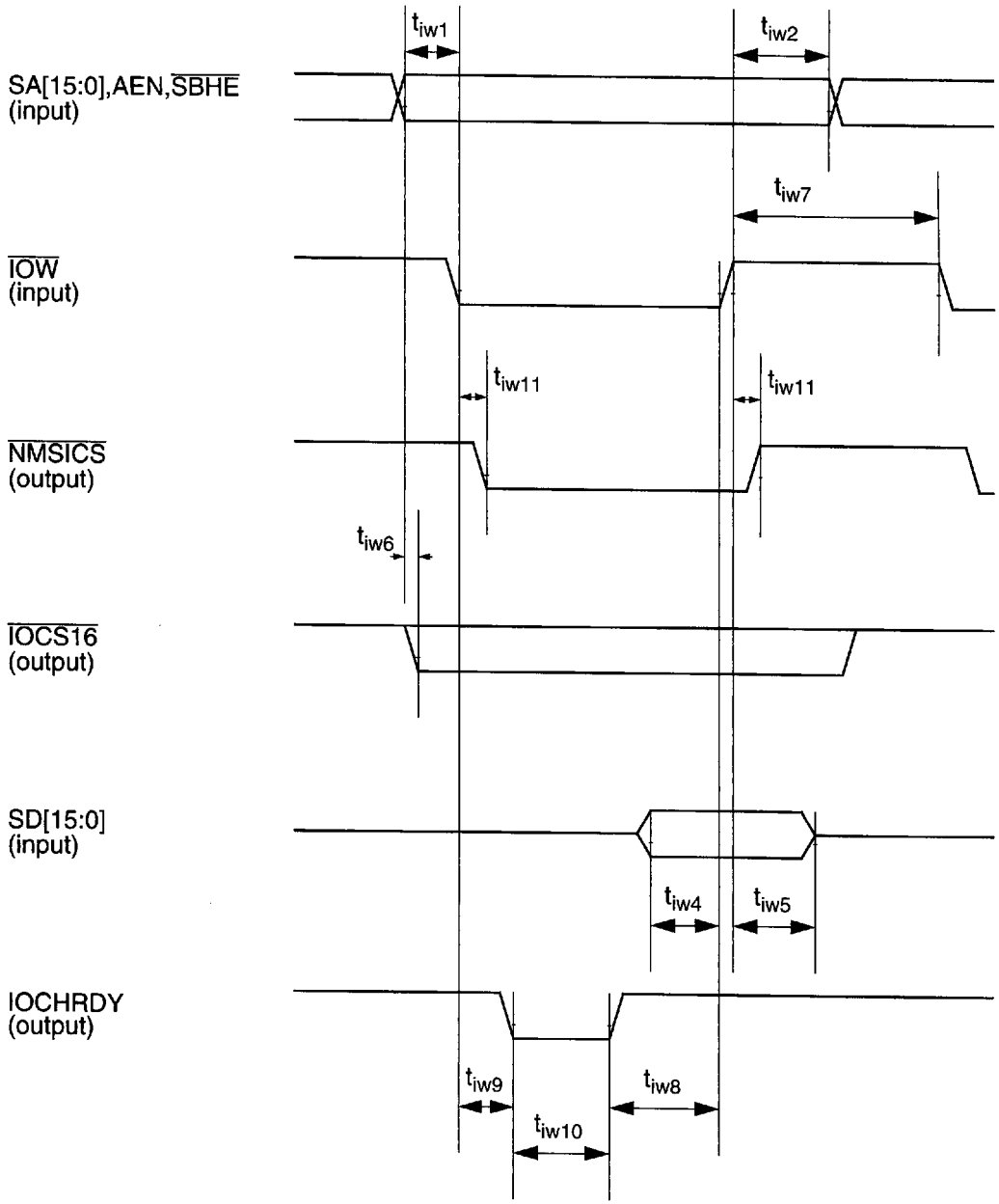


Figure 7-12. IO Space Write Access with Wait States - Internal Space

7.6.2.4 MEMORY SPACE READ ACCESS.

Table 7-8. Memory Space Read Access

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{mr1}	LA[23:17] setup to BALE inactive (Falling edge)	50		50		ns
t_{mr2}	BALE Active to Inactive (Assertion length)	35		35		ns
t_{mr3}	LA[23:17] hold from BALE inactive (Falling edge)	10		10		ns
t_{mr4}	LA[23:17] setup to $\overline{\text{MEMR}}$ active (Falling edge)	50		50		ns
t_{mr5}	$\overline{\text{MEMCS16}}$ valid from LA[23:17]		50		50	ns
t_{mr6}	$\overline{\text{MEMCS16}}$ valid hold from LA[23:17] nonvalid	0		0		ns
t_{mr7}	SA[16:0], $\overline{\text{SBHE}}$ to $\overline{\text{MEMR}}$ active setup time	22		22		ns
t_{mr8}	$\overline{\text{MEMR}}$ active to inactive (Assertion length)	200		170		ns
t_{mr9}	SA[16:0], $\overline{\text{SBHE}}$ to BALE inactive (Falling edge)	25		25		ns
t_{mr10}	Data out valid from $\overline{\text{MEMR}}$ active (Falling edge)		203		162	ns
t_{mr11}	$\overline{\text{MEMR}}$ inactive to active (Rising to falling edge delay), no wait states	100		75		ns
t_{mr12}	Data out hold time from $\overline{\text{MEMR}}$ negation (Rising edge)	0		0		ns
t_{mr13}	BALE active from $\overline{\text{MEMR}}$ inactive (Rising edge)	40		40		ns
t_{mr14}	$\overline{\text{REF}}$ setup to $\overline{\text{MEMR}}$ active (Falling edge)	60		60		ns
t_{mr15}	$\overline{\text{REF}}$ hold from $\overline{\text{MEMR}}$ inactive (Rising Edge)	10		10		ns
t_{mr16}	$\overline{\text{REF}}$ setup to BALE inactive (Falling edge)	25		25		ns
t_{mr17}	SA[16:0], $\overline{\text{SBHE}}$ hold from $\overline{\text{MEMR}}$ inactive	25		25		ns
t_{mr18}	$\overline{\text{MEMR}}$ active to IOCHRDY falling edge (Inactive)		45		45	ns
t_{mr19}	IOCHRDY inactive (Low) pulse width	120		120		ns
t_{mr20}	$\overline{\text{MEMR}}$ active (Low) hold from IOCHRDY active (High)	0		0		ns
t_{mr21}	Valid read data from IOCHRDY active (Rising edge)		0		0	ns
t_{mr22}	$\overline{\text{MEMR}}$ active or inactive to $\overline{\text{NMSICS}}$ active or inactive delay		42		42	ns
t_{mr23}	$\overline{\text{MEMR}}$ inactive to active (Rising to falling edge delay) with wait states	70		50		ns

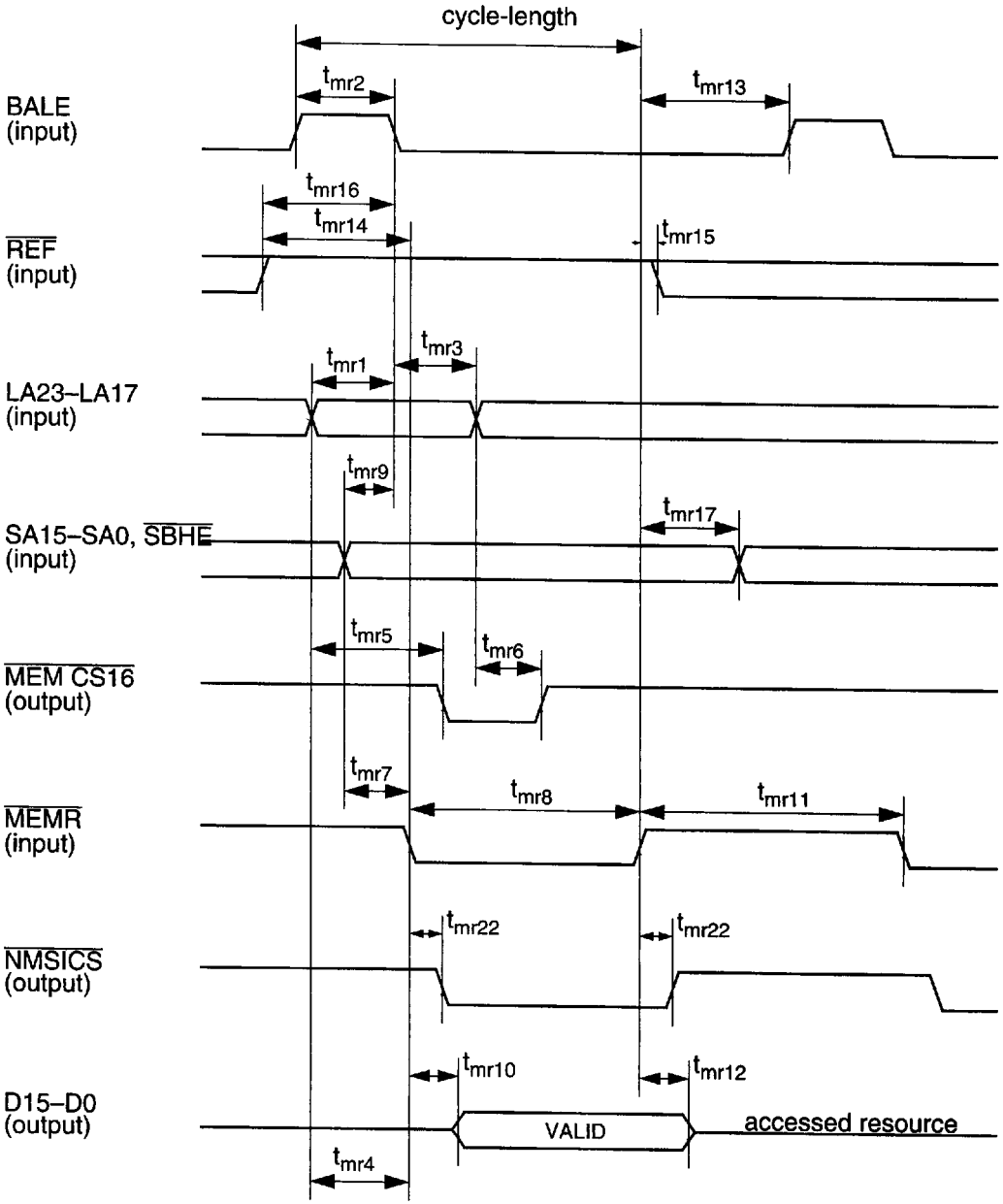


Figure 7-13. Memory Space Read Access without Wait States

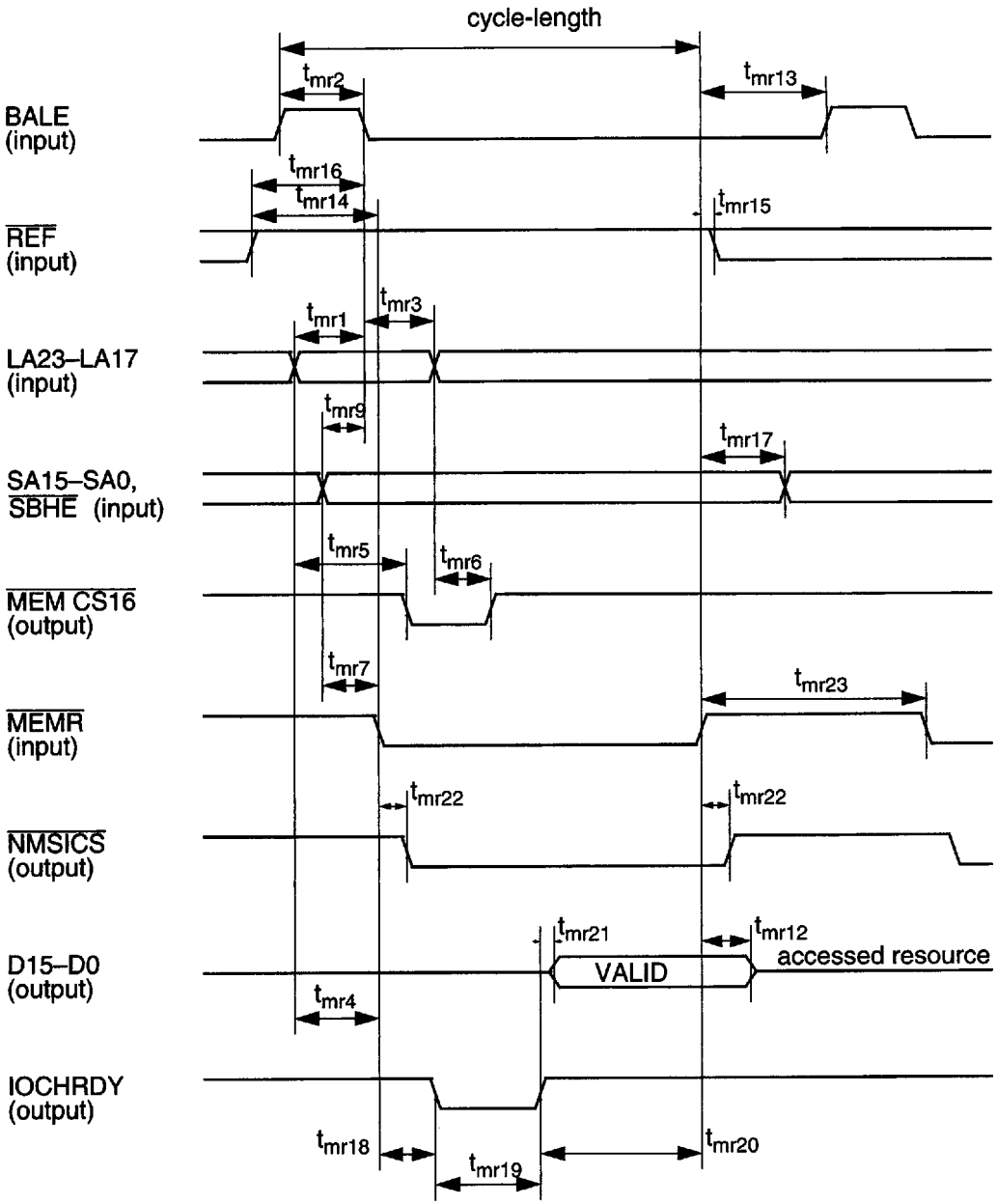


Figure 7-14. Memory Space Read Access with Wait States

7.6.2.5 MEMORY SPACE WRITE ACCESS .

Table 7-9. Memory Space Write Access

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{mw1}	LA[23:17] setup to BALE inactive (Falling edge)	50		50		ns
t_{mw2}	BALE Active to Inactive (Assertion length)	35		35		ns
t_{mw3}	LA[23:17] hold from BALE inactive (Falling edge)	10		10		ns
t_{mw4}	LA[23:17] setup to $\overline{\text{MEMW}}$ active (Falling edge)	50		50		ns
t_{mw5}	$\overline{\text{MEMCS16}}$ valid from LA[23:17]		50		50	ns
t_{mw6}	$\overline{\text{MEMCS16}}$ valid hold from LA[23:17] nonvalid	0		0		ns
t_{mw7}	SA[16:0], $\overline{\text{SBHE}}$ to $\overline{\text{MEMW}}$ active setup time	22		22		ns
t_{mw8}	$\overline{\text{MEMW}}$ active to inactive (Assertion length)	200		150		ns
t_{mw9}	SA[16:0], $\overline{\text{SBHE}}$ to BALE inactive (Falling edge)	25		25		ns
t_{mw10}	Data setup to $\overline{\text{MEMW}}$ rising edge (Inactivation)	40		40		ns
t_{mw11}	$\overline{\text{MEMW}}$ inactive to active (Rising to falling edge delay) no wait states	100		75		ns
t_{mw12}	Data in hold time from $\overline{\text{MEMW}}$ negation (Rising edge)	7		7		ns
t_{mw13}	BALE active from $\overline{\text{MEMW}}$ inactive (Rising edge)	40		40		ns
t_{mw14}	$\overline{\text{REF}}$ setup to $\overline{\text{MEMW}}$ active (Falling edge)	60		60		ns
t_{mw15}	$\overline{\text{REF}}$ hold from $\overline{\text{MEMW}}$ inactive (Rising Edge)	10		10		ns
t_{mw16}	$\overline{\text{REF}}$ setup to BALE inactive (Falling edge)	25		25		ns
t_{mw17}	SA[16:0], $\overline{\text{SBHE}}$ hold from $\overline{\text{MEMW}}$ inactive	25		25		ns
t_{mw18}	$\overline{\text{MEMW}}$ active to IOCHRDY falling edge (Inactive)		45		45	ns
t_{mw19}	IOCHRDY inactive (Low) pulse width	120		120		ns
t_{mw20}	$\overline{\text{MEMW}}$ active (Low) hold from IOCHRDY active (High)	0		0		ns
t_{mw21}	$\overline{\text{MEMW}}$ active or inactive to $\overline{\text{NMSICS}}$ active or inactive delay		43		43	ns
t_{mw22}	$\overline{\text{MEMW}}$ inactive to active (Rising to falling edge delay) with wait states	70		50		ns

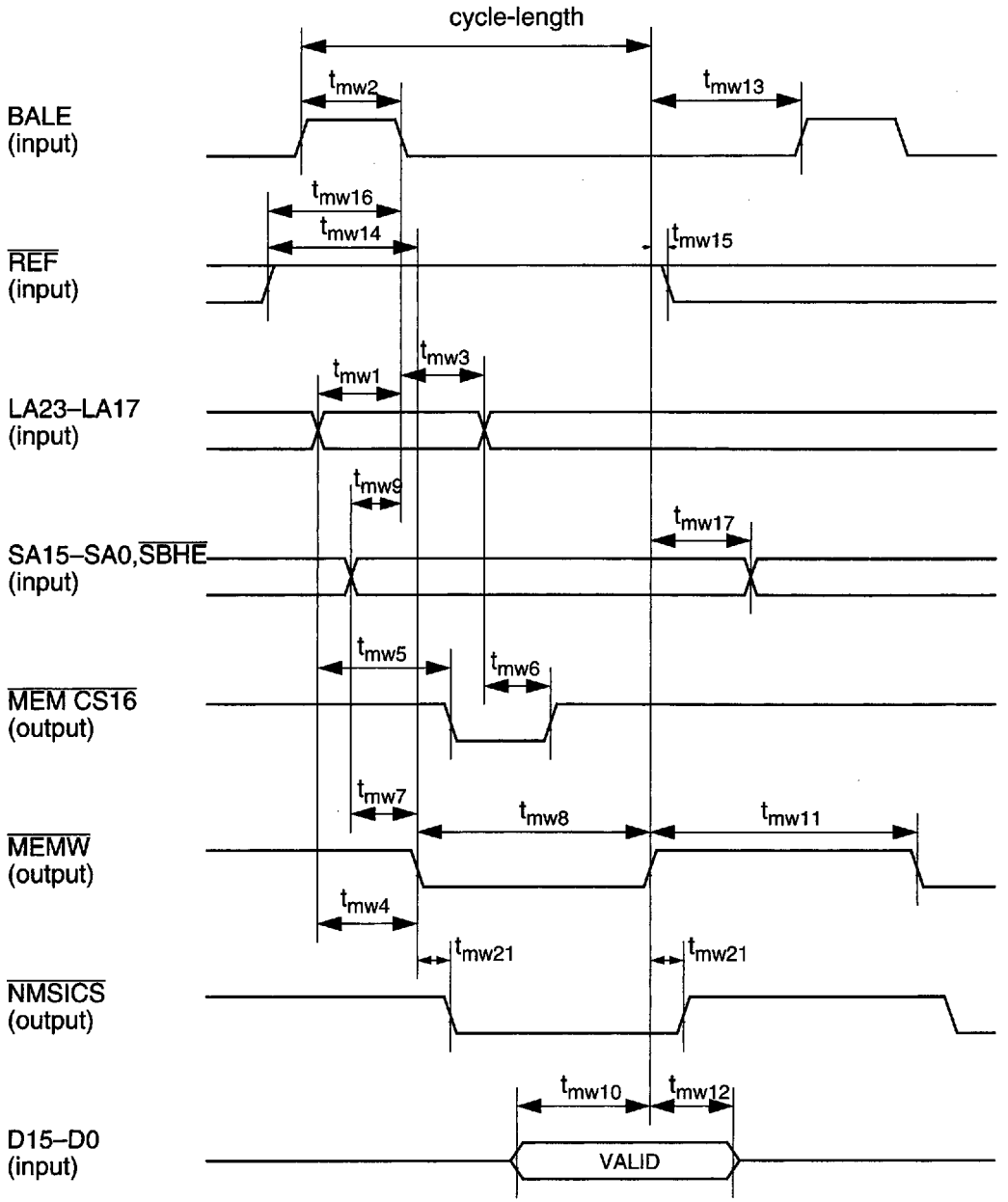


Figure 7-15. Memory Space Write Access without Wait States

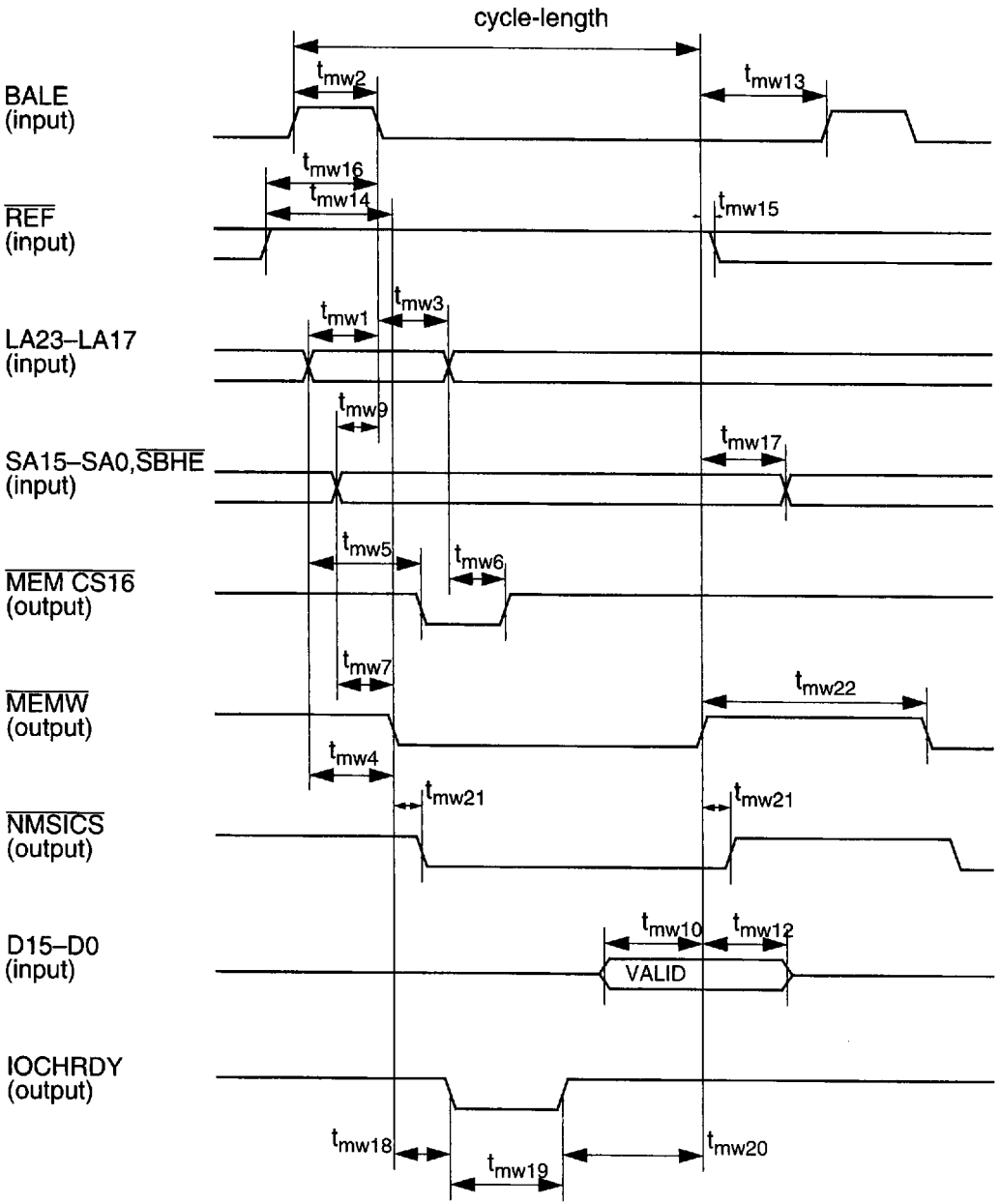


Figure 7-16. Memory Space Write Access with Wait States

7.6.3 PCMCIA Host Interface Timing Specifications

7.6.3.1 PCMCIA READ ACCESS WITH/WITHOUT WAIT STATES.

Table 7-10. PCMCIA Read Access with/without Wait States

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{pr1}	Read Cycle Length (Without wait states)	200		150		ns
t_{pr2}	Address and $\overline{REG}$ Hold time from $\overline{OE}$ negation (Rising edge)	15		15		ns
t_{pr3}	$\overline{CE1}$ and $\overline{CE2}$ to $\overline{OE}$ assertion setup time	0		0		ns
t_{pr4}	Address and $\overline{REG}$ valid to $\overline{OE}$ assertion (Falling edge) set-up	25		25		ns
t_{pr5}	Data Valid from $\overline{OE}$ assertion (Falling edge) delay ($\overline{WAIT}$ negated)		45		45	ns
t_{pr6}	$\overline{CE1}$ and $\overline{CE2}$ from $\overline{OE}$ negation (Rising edge) hold time	15		15		ns
t_{pr7}	$\overline{WAIT}$ valid from $\overline{OE}$ assertion (Falling edge) delay		35		35	ns
t_{pr8}	$\overline{WAIT}$ pulse width	160	200	120	150	ns
t_{pr9}	$\overline{OE}$ negation (Rising edge) hold time from $\overline{WAIT}$ negation	0		0		ns
t_{pr10}	Data valid to $\overline{WAIT}$ negation (Rising edge) setup time	0		0		ns
t_{pr11}	Data valid from $\overline{OE}$ negation (Rising edge) hold time	0		0		ns
t_{pr12}	$\overline{CISCS}$ from $\overline{OE}$ delay		40		40	ns
t_{pr13}	$\overline{NMSICS}$ from $\overline{OE}$ delay		42		42	ns

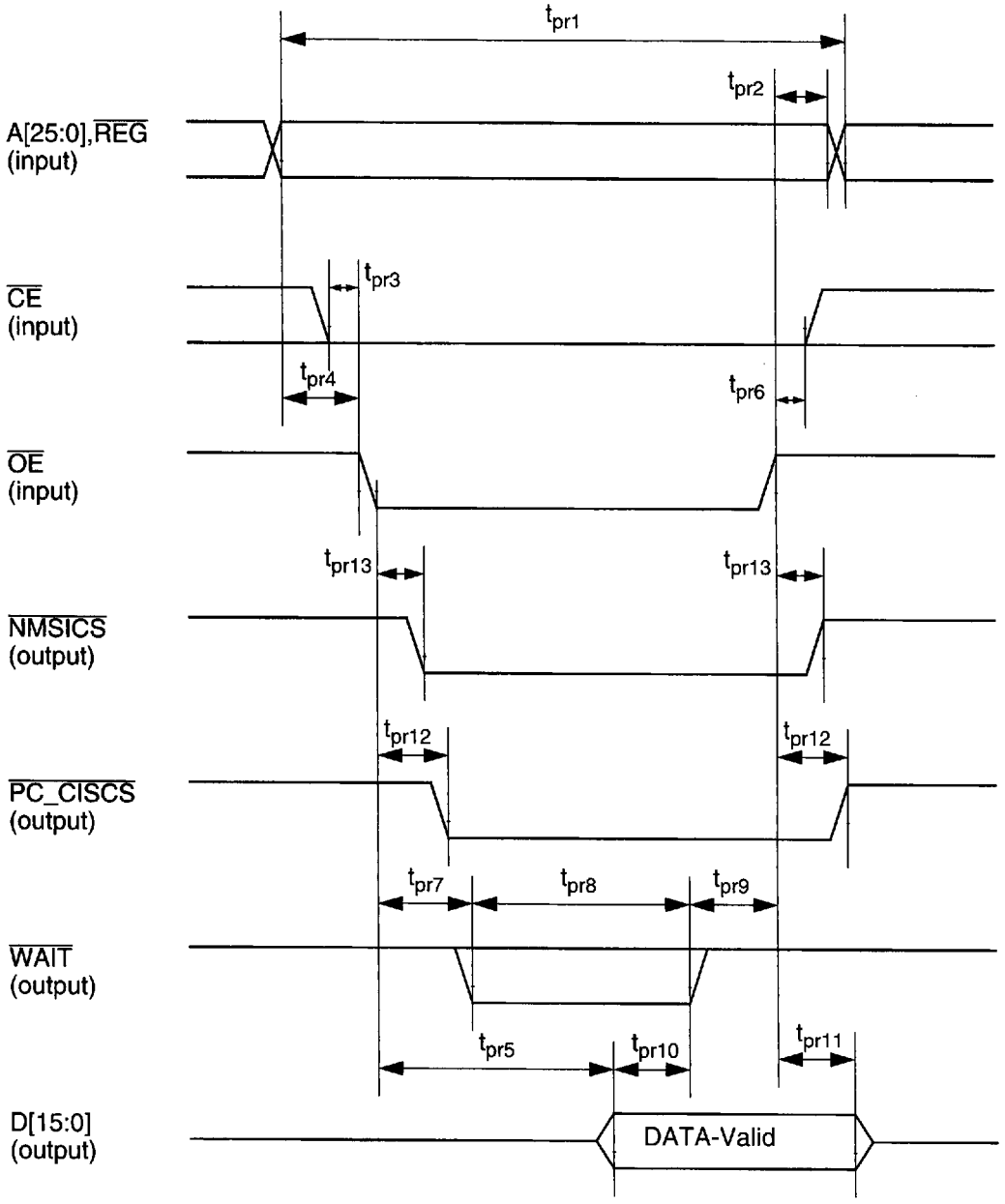


Figure 7-17. PCMCIA Read Access with/without Wait States

7.6.3.2 PCMCIA WRITE ACCESS WITH/WITHOUT WAIT STATES.

Table 7-11. PCMCIA Write Access with/without Wait States

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{pw1}	Write Cycle Length (Without wait states)	200		150		ns
t_{pw2}	$\overline{CE1}$ and $\overline{CE2}$ to $\overline{WE}$ assertion setup time	0		0		ns
t_{pw3}	$\overline{CE1}$ and $\overline{CE2}$ from $\overline{WE}$ negation (Rising edge) hold time	15		15		ns
t_{pw4}	Address and $\overline{REG}$ valid to $\overline{WE}$ assertion (Falling edge) setup	25		25		ns
t_{pw5}	Write pulse width	135		100		ns
t_{pw6}	Address and $\overline{REG}$ Hold time from $\overline{WE}$ negation (Rising edge)	15		15		ns
t_{pw7}	$\overline{WAIT}$ valid from $\overline{WE}$ assertion (Falling edge) delay		35		35	ns
t_{pw8}	$\overline{WAIT}$ pulse width	160	200	120	150	ns
t_{pw9}	$\overline{WE}$ (Rising edge) hold time from $\overline{WAIT}$ negation	0		0		ns
t_{pw10}	$\overline{OE}$ high hold time from $\overline{WE}$ rising edge	25		25		ns
t_{pw11}	$\overline{OE}$ high to $\overline{WE}$ active setup time	10		10		ns
t_{pw12}	Data Valid to $\overline{WE}$ negation setup time	50		50		ns
t_{pw13}	Data Valid from $\overline{WE}$ negation hold time	25		25		ns
t_{pw14}	$\overline{CISCS}$ from $\overline{WE}$ delay		40		40	ns
t_{pw15}	$\overline{NMSICS}$ from $\overline{WE}$ delay		43		43	ns

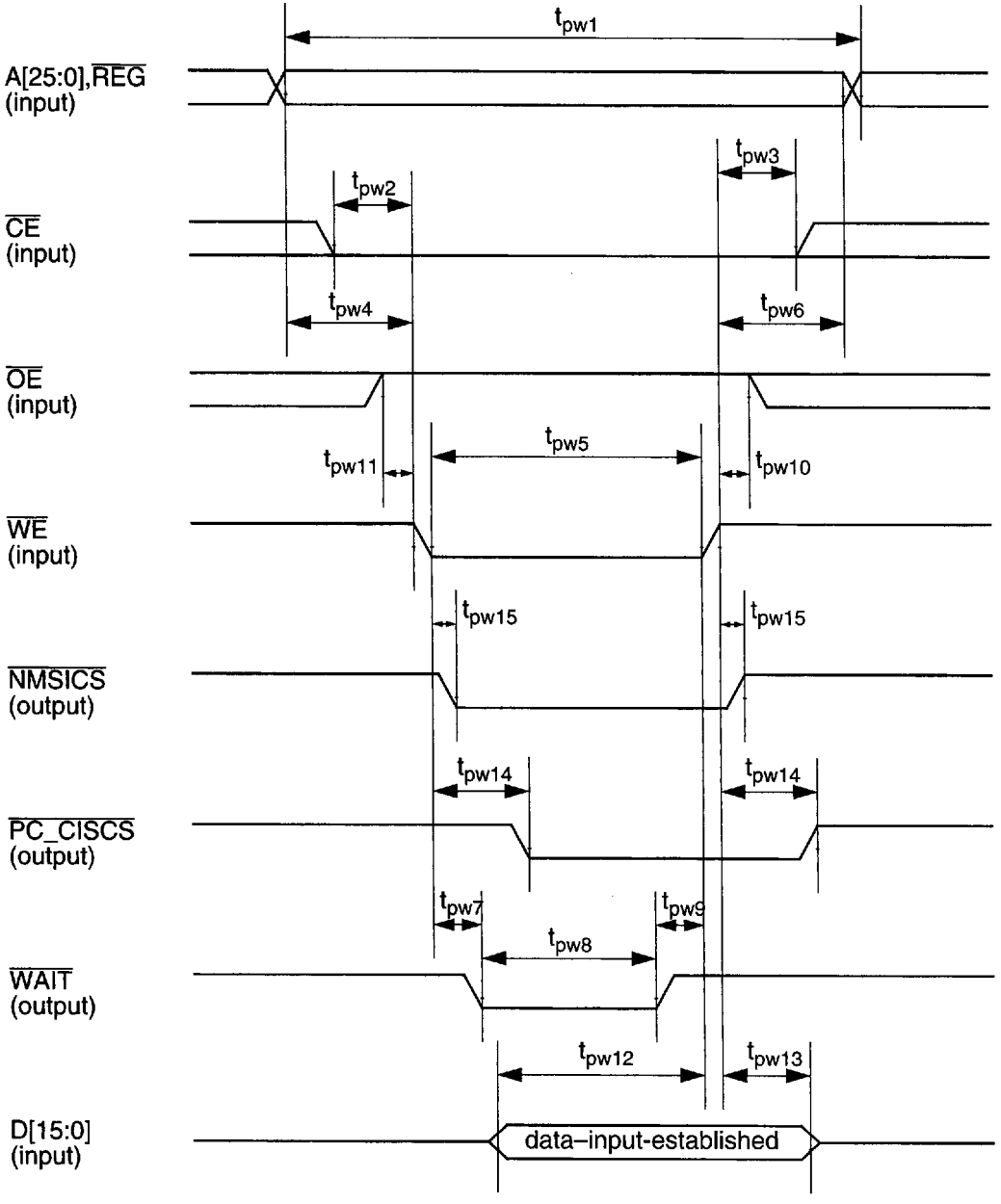


Figure 7-18. PCMCIA Write Access with/without Wait States

7.6.3.3 PCMCIA RESET TIMING SPECIFICATIONS.

Table 7-12. PCMCIA Reset Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{prst1}	RESET pulse width	9	-	9	-	µs
t_{prst2}	$\overline{Mode}$ from RESET pulse inactive hold time	1	-	1	-	µs
t_{prst3}	$\overline{Mode}$ to RESET inactive setup time	1	-	1	-	µs
t_{prst4}	RESET inactive to first access setup time	18	-	18	-	ms
t_{prst5}	E2E from RESET inactive hold time	1	-	1	-	µs
t_{prst6}	E2E to RESET inactive setup time	1	-	1	-	µs
t_{prst7}	0.9 V_{CC} to reset inactive setup	9	-	9	-	µs

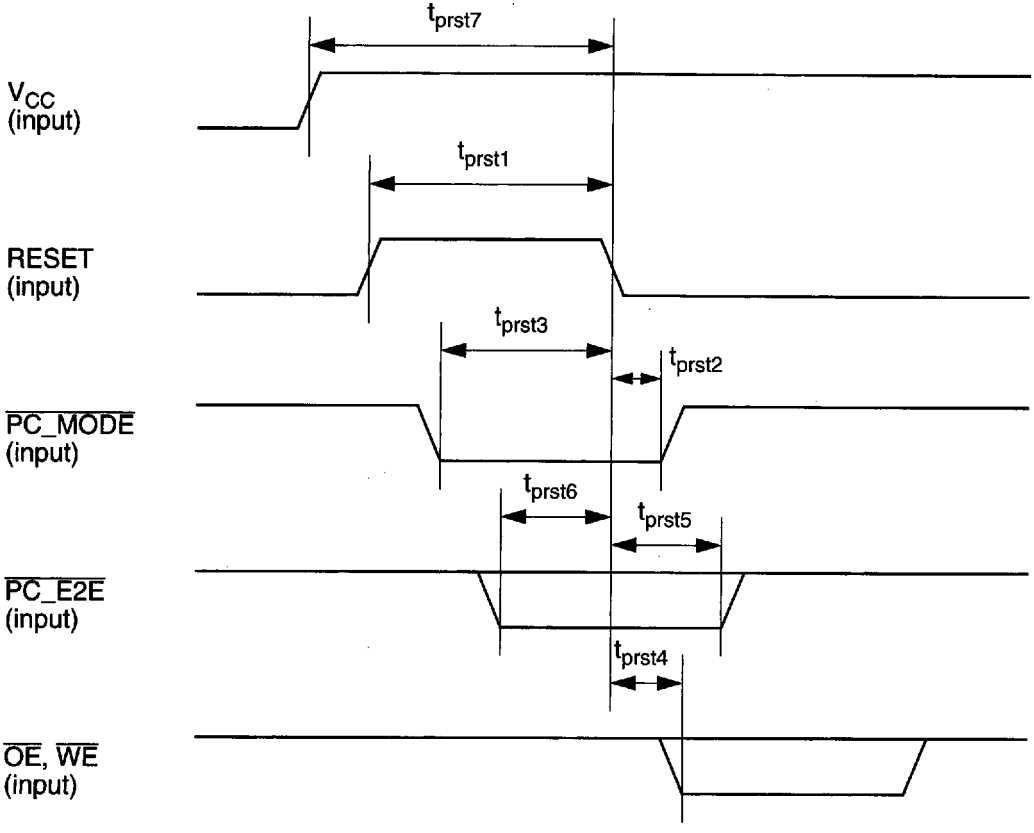


Figure 7-19. PCMCIA Reset Timing Specifications

7.6.4 Serial Interface Timing Specifications

7.6.4.1 SCP TIMING SPECIFICATIONS.

Table 7-13. SCP Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{scp1}	Scpclk Clock Output Period	4	64	4	64	Clks
t_{scp2}	Scpclk Clock High or Low Time	2	32	2	32	Clks
t_{scp3}	ScpRxD Data Setup Time	30	-	30	-	ns
t_{scp4}	ScpRxD Data Hold Time	8	-	8	-	ns
t_{scp5}	ScpTxD Data Valid (after clk Edge)	0	30	0	30	ns
t_{scp7}	Scpclk Rise Time	0	15	0	15	ns
t_{scp8}	Scpclk Fall Time	0	15	0	15	ns

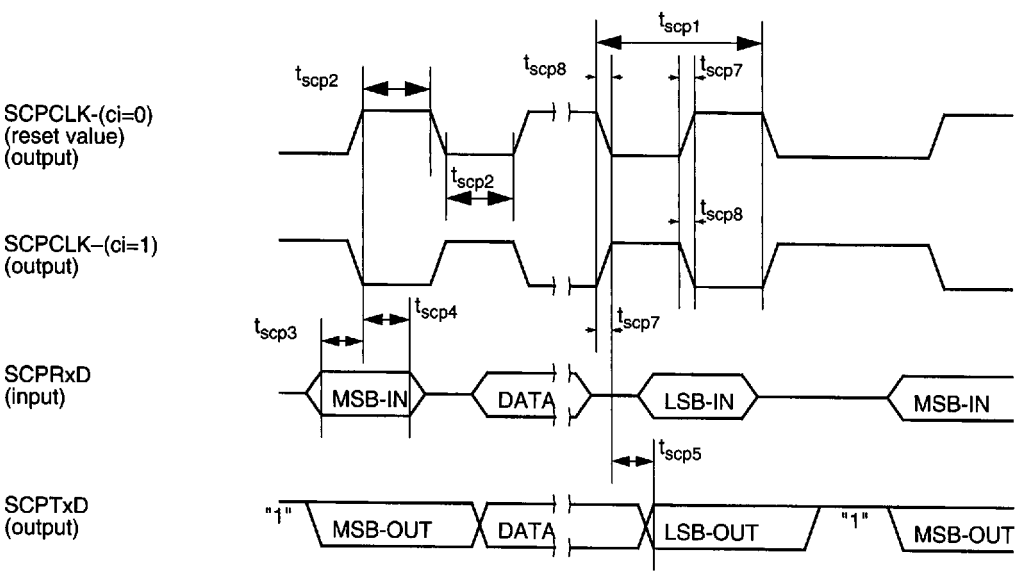


Figure 7-20. SCP Timing (cp=0, Reset Value)

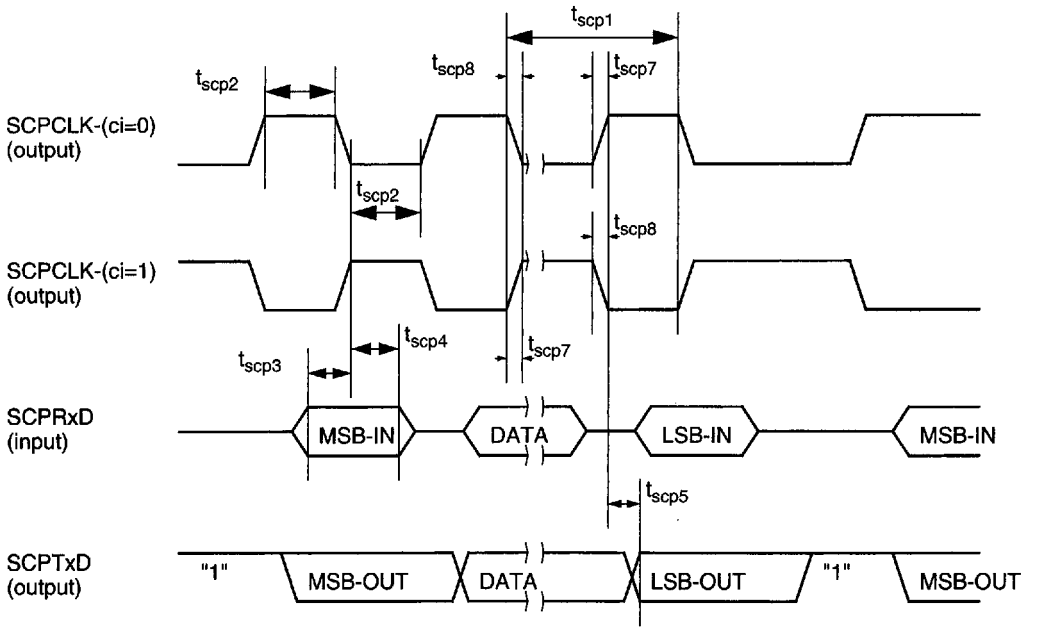


Figure 7-21. SCP Timing (cp=1)

7.6.4.2 SERIAL EEPROM TIMING SPECIFICATIONS.

Table 7-14. SERIAL EEPROM Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{e2p1}	Scpclk Clock Output Period	44		44		Clks
t_{e2p2}	Scpclk Clock High or Low Time	20		20		Clks
t_{e2p3}	ScpRxD Setup Time	30		30		ns
t_{e2p4}	ScpRxD Hold Time	8		8		ns
t_{e2p5}	ScpTxD Data Valid (after scpclk Edge)	0	30	0	30	ns
t_{e2p7}	Scpclk Rise Time	0	15	0	15	ns
t_{e2p8}	Scpclk Fall Time	0	15	0	15	ns
t_{e2p9}	E2EN Negation After Last Scpclk Edge	1		1		Clks
t_{e2p10}	E2EN and ScpEN3–1 Assert/Negate to Scpclk Edge	22		22		Clks
t_{e2p11}	ScpTxD First Bit Valid to Scpclk Edge	20		20		Clks

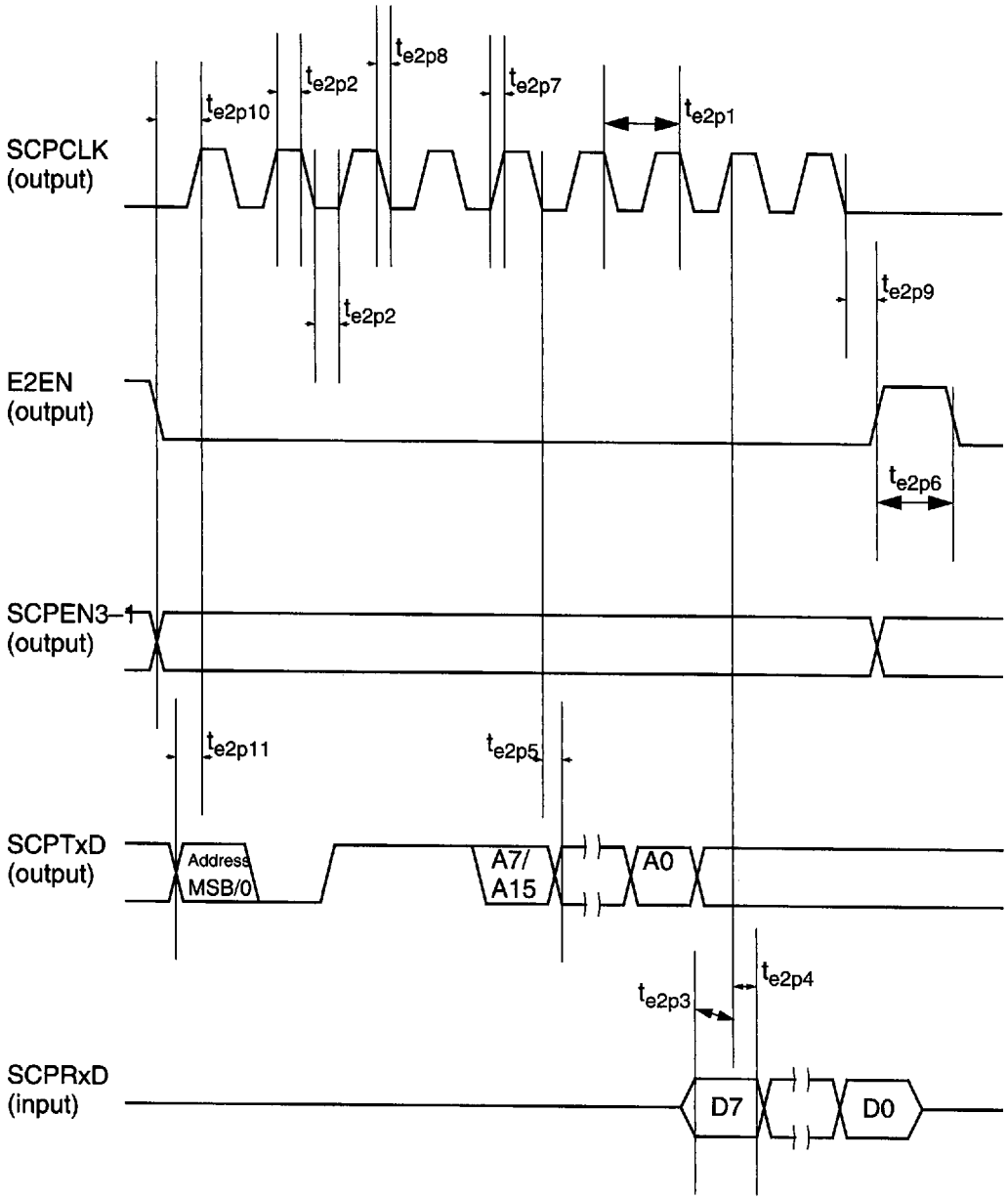


Figure 7-22. Serial EEPROM (SCP Type) Timing Specifications (with Initial Reset Value of spmode)

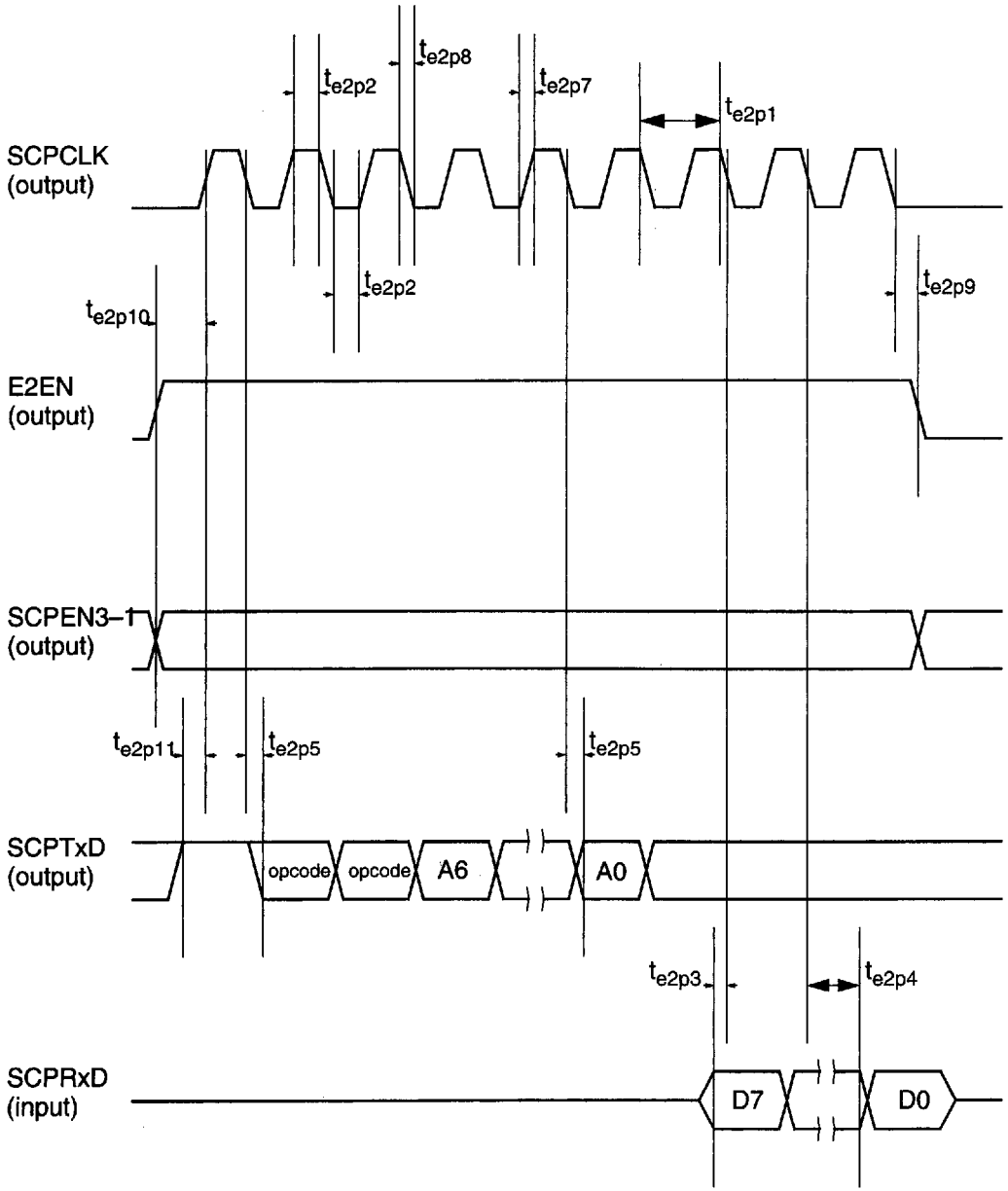


Figure 7-23. Serial EEPROM (93C46 TYPE) TIMING SPECIFICATIONS (With Initial Reset Value of spmode)

7.6.4.3 IDL TIMING SPECIFICATIONS.

Table 7-15. IDL Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{idl1}	L1CLK(idl clock) Frequency (see Note 1)	-	6	-	6	MHz
t_{idl2}	L1CLK width Low	60	-	60	-	ns
t_{idl3}	L1CLK width High (see Note 3)	p+10	-	p+10	-	ns
t_{idl4}	L1TxD,L1RQ,SDS1–SDS2 Rising/Falling time	-	17	-	17	ns
t_{idl5}	L1SYNC setup Time (to L1CLK Falling Edge)	25	-	25	-	ns
t_{idl6}	L1SYNC Hold Time (from L1CLK Falling Edge)	40	-	40	-	ns
t_{idl7}	L1SYNC Inactive Before 4th L1CLK	0	-	0	-	ns
t_{idl8}	L1TxD Active Delay (from L1CLK Rising Edge)	0	65	0	65	ns
t_{idl9}	L1TxD to High Impedance (from L1CLK Rising Edge) (see Note 2)	0	50	0	50	ns
t_{idl10}	L1RxD Setup Time (to L1CLK Falling Edge)	42	-	42	-	ns
t_{idl11}	L1RxD Hold Time (from L1Clk Falling Edge)	42	-	42	-	ns
t_{idl12}	Time Between Successive IDL syncs	20	-	20	-	L1CLK
t_{idl13}	L1RQ Setup Time (to L1SYNC Falling Edge)	1	-	1	-	L1CLK
t_{idl14}	L1GRNT Setup Time (to L1SYNC Falling Edge)	42	-	42	-	ns
t_{idl15}	L1GRNT Hold Time (from L1SYNC Falling Edge)	42	-	42	-	ns
t_{idl16}	SDS1–SDS2 Active Delay from L1CLK Rising Edge	10	65	10	65	ns
t_{idl17}	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	65	10	65	ns

NOTES:

1. The ratio EXTAL/L1CLK must be greater then 2.5/1.
2. High impedance is measured at the 30% and 70% of V_{DD} points, with the line at $V_{DD}/2$ through 10k in parallel with 130 pF.
3. Where P=1/EXTAL Thus, for a 20.48-MHz EXTAL rate, P=48.8 ns.

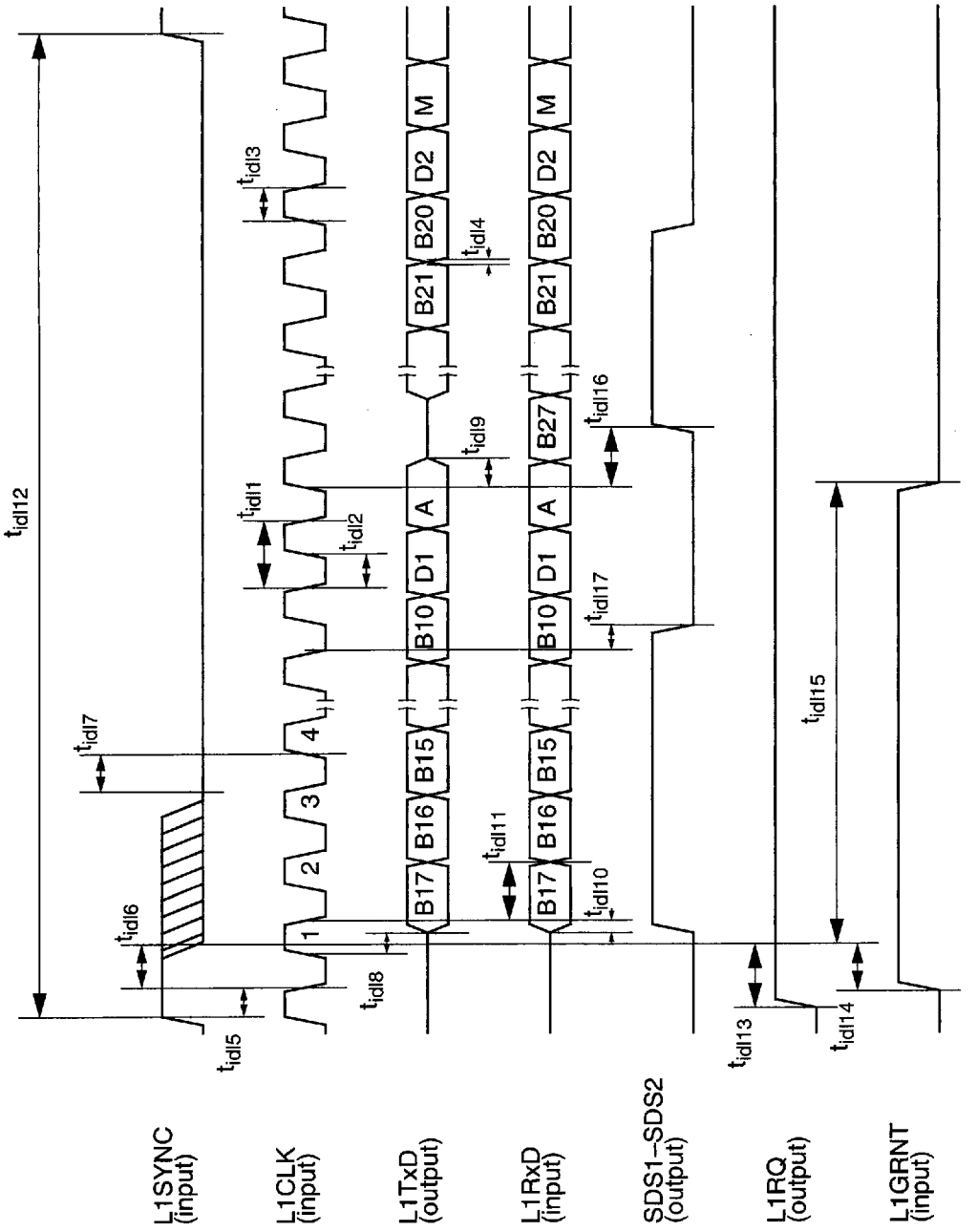


Figure 7-24. IDL Timing Specifications

7.6.4.4 GCI TIMING SPECIFICATIONS.

Table 7-16. GCI Timing Specifications

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
	L1CLK(gci clock) Frequency (Normal Mode) (see Note 1)	-	512	-	512	KHz
t_{gci1n}	L1CLK Clock Period Normal Mode (see Note 1)	1800	2100	1800	2100	ns
t_{gci2n}	L1CLK width Low Normal Mode	840	1450	840	1450	ns
t_{gci3n}	L1CLK width High Normal Mode	840	1450	840	1450	ns
	L1CLK(gci clock) Period (Mux Mode) (see Note 1)	-	6	-	6	MHz
t_{gci1m}	L1CLK Clock Period Mux Mode (see Note 1)	175	-	175	-	ns
t_{gci2m}	L1CLK width Low Mux Mode	75	-	75	-	ns
t_{gci3m}	L1CLK width High Mux Mode	p+10	-	p+10	-	ns
t_{gci4}	L1SYNC setup Time (to L1CLK Falling Edge)	25	-	25	-	ns
t_{gci5}	L1SYNC Hold Time (from L1CLK Falling Edge)	42	-	42	-	ns
t_{gci6}	L1TxD Active Delay (from L1CLK Rising Edge)	0	100	0	100	ns
t_{gci7}	L1TxD Active Delay (from L1SYNC Rising Edge) (see Note 2)	0	100	0	100	ns
t_{gci8}	L1RxD Setup Time (to L1CLK Rising Edge)	17	-	17	-	ns
t_{gci9}	L1RxD Hold Time (from L1Clk Rising Edge)	42	-	42	-	ns
t_{gci10}	Time Between Successive L1SYNC in Normal SCIT Mode	64 192	- -	64 192	- -	L1CLK L1CLK
t_{gci11}	SDS1–SDS2 Active Delay from L1CLK Rising Edge (see Note 3)	10	75	10	75	ns
t_{gci12}	SDS1–SDS2 Active Delay from L1SYNC Rising Edge (see Note 3)	10	75	10	75	ns
t_{gci13}	SDS1–SDS2 Inactive Delay from L1CLK Falling Edge	10	75	10	75	ns
t_{gci14}	GCIDCL (gci Data Clock) Active Delay	0	42	0	42	ns

NOTES:

1. The ratio CLKO/L1CLK must be greater than 2.5/1.
2. Condition CL=150 pF

   L1TxD becomes valid after the L1CLK rising edge or L1SYNC, whichever is later.
3. SDS1–SDS2 becomes valid after the L1CLK rising edge or L1SYNC, whichever is later.
4. Where P=1/CLKO. Thus, for a 20.48 MHz CLKO rate, P=48.8 ns.

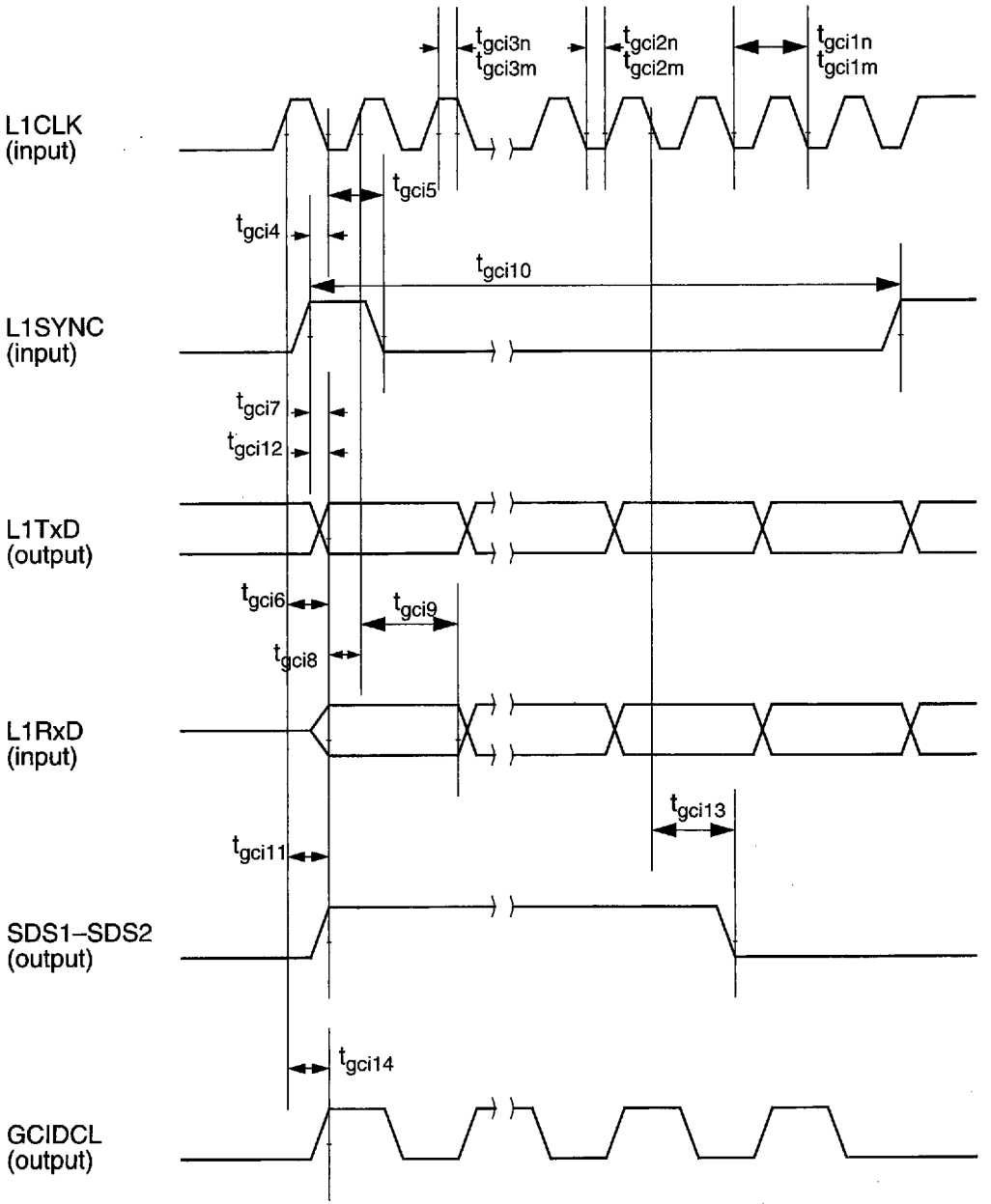


Figure 7-25. GCI Timing Specifications

7.6.4.5 PCM TIMING SPECIFICATIONS.

Table 7-17. PCM Timing

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_{pcm0}	L1CLK (PCM Clock) Frequency (see Note 1)		6		6	MHz
t_{pcm1}	L1clk Width Low	55	-	55	-	ns
t_{pcm1a}	L1CLK Width High (see Note 4)	p+10	-	p+10	-	ns
t_{pcm2}	L1SYNC/PSYNC Setup Time to L1clk Rising Edge	20	-	20	-	ns
t_{pcm3}	L1SYNC/PSYNC Hold Time from L1clk Falling Edge	40	-	40	-	ns
t_{pcm4}	L1SYNC/PSYNC Width Low	1	-	1	-	L1CLK
t_{pcm5}	Time Between Successive Sync Signals (Short Frame)	8	-	8	-	L1CLK
t_{pcm6}	L1TxD Data Valid after L1CLK Rising Edge (see Note 2)	0	70	0	70	ns
t_{pcm7}	L1TxD to High Impedance (from L1CLK Rising Edge)	0	50	0	50	ns
t_{pcm8}	L1RxD Setup Time (to L1CLK Falling Edge) (see Note 3)	20	-	20	-	ns
t_{pcm9}	L1RxD Hold Time (from L1CLK Falling Edge) (see Note 3)	50	-	50	-	ns

NOTES:

1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. L1TxD becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used. This note should only be used if the user can guarantee that only one sync pin (L1SYNC and PSYNC) is changed simultaneously in the selection and deselection of the desired PCM channel time slot. A safe example of this is using only PCM CH-1. Another example is using CH-1 and CH-2 only, where CH-1 and CH-2 are not contiguous on the PCM highway.
3. Specification valid for both sync methods.
4. Where p=1/CLKO. Thus, for a 20.48-MHz CLKO rate, p=48.8 ns.
5. If L1SYNC/PSYNC is guaranteed to make a smooth low to high transition (no spikes) while L1CLK is high, setup time can be measured to L1CLK falling edge.

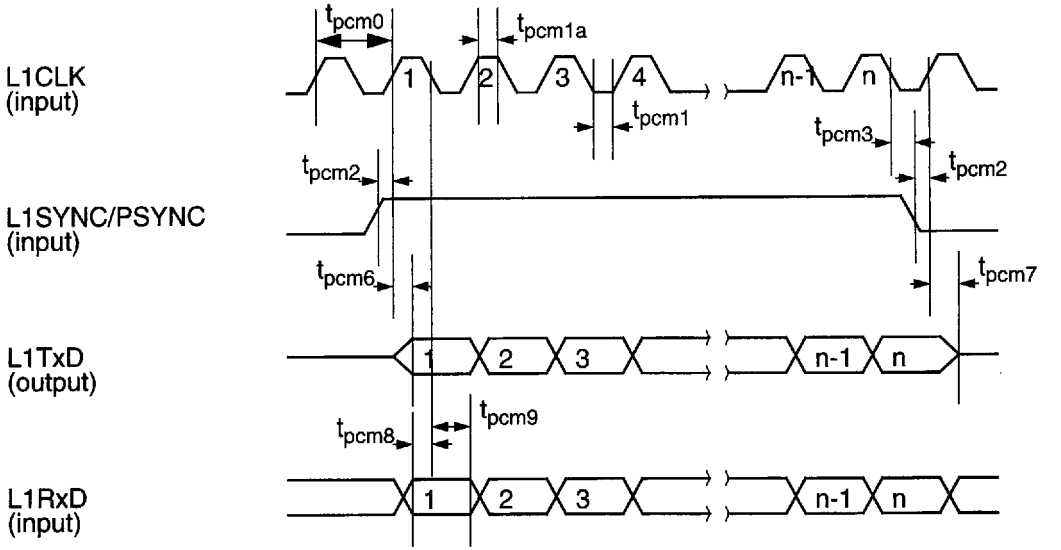


Figure 7-26. PCM Timing Diagram (SYNC Envelopes Data)

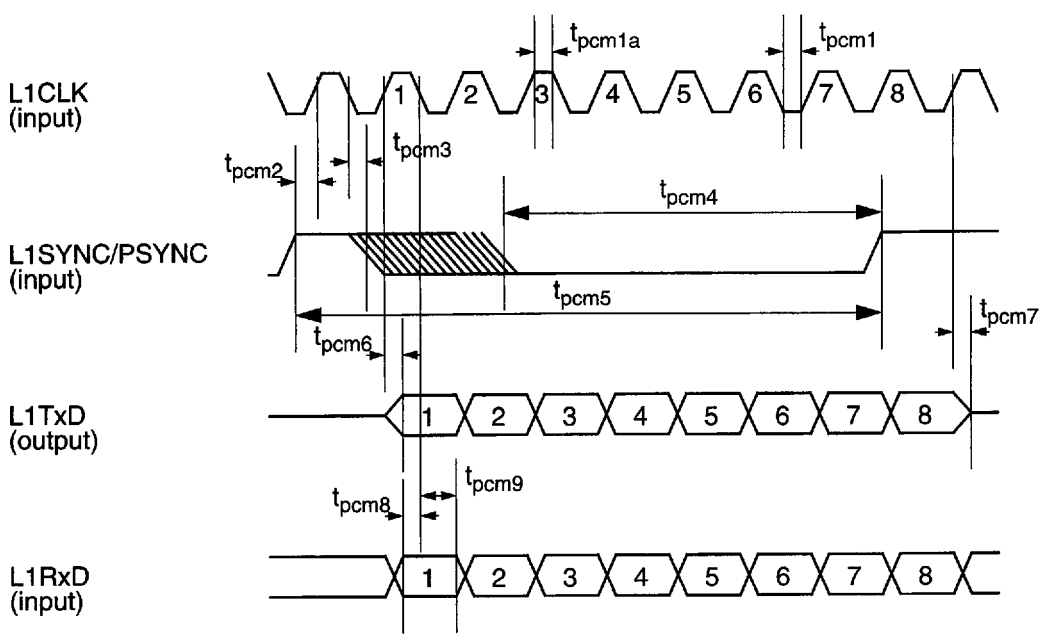


Figure 7-27. PCM Timing Diagram (SYNC Prior to 8-bit Data)

7.6.4.6 NMSI TIMING SPECIFICATIONS.

Table 7-18. NMSI Timing Specifications (External Clock)

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
$t_{nm\text{-}ext1}$	CLKRX and CLKTX Frequency (see Note1)		6.14		6.14	MHz
$t_{nm\text{-}ext2}$	CLKRX and CLKTX Low (see Note 2)	p+10	-	p+10	-	ns
$t_{nm\text{-}ext3}$	CLKRX and CLKTX High (see Note 2)	p+10	-	p+10	-	ns
$t_{nm\text{-}ext4}$	CLKRX and CLKTX Rise/Fall Time	-	-	-	-	ns
$t_{nm\text{-}ext5}$	TXD Active Delay from CLKTX Falling Edge	0	70	0	70	ns
$t_{nm\text{-}ext6}$	RXD Setup Time to CLKRX Rising Edge	10	-	10	-	ns
$t_{nm\text{-}ext7}$	RXD Hold Time from CLKRX Rising Edge	50	-	50	-	ns

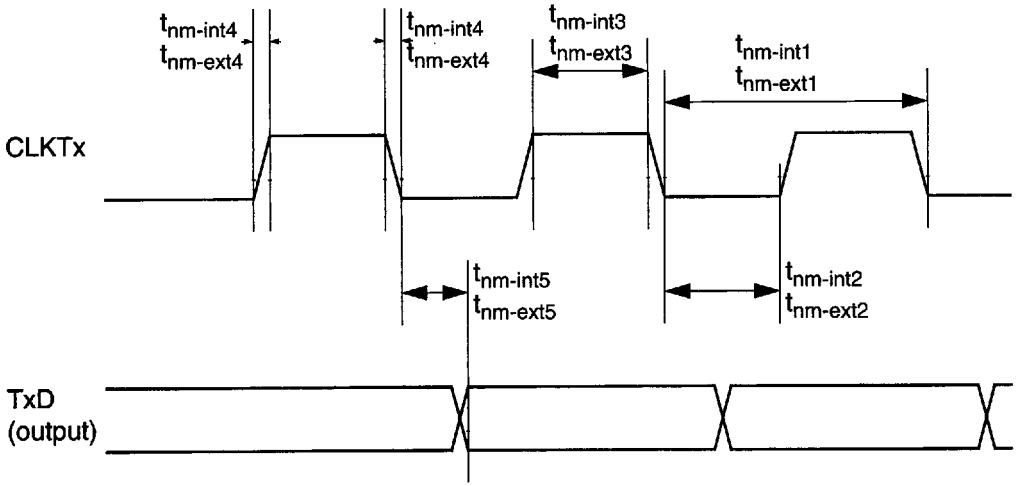
Table 7-19. NMSI Timing Specifications (Internal Clock)

PARAMETER	CHARACTERISTICS	15.36MHZ		20.48MHZ		UNITS
		MIN	MAX	MIN	MAX	
$t_{nm\text{-}int1}$	CLKRX and CLKTX Frequency (see Note1)		5.13		6.83	MHz
$t_{nm\text{-}int2}$	CLKRX and CLKTX Low (see Note 2)	p+10	-	p+10	-	ns
$t_{nm\text{-}int3}$	CLKRX and CLKTX High (see Note 2)	p+10	-	p+10	-	ns
$t_{nm\text{-}int4}$	CLKRX and CLKTX Rise/Fall Time	-	20	-	20	ns
$t_{nm\text{-}int5}$	TXD Active Delay from CLKTX Falling Edge	0	40	0	40	ns
$t_{nm\text{-}int6}$	RXD Setup Time to CLKRX Rising Edge	50	-	50	-	ns
$t_{nm\text{-}int7}$	RXD Hold Time from CLKRX Rising Edge	10	-	10	-	ns

NOTES:

1. The ratio CLKO/CLKTX and CLKO/CLKRX must be greater than or equal to 2.5/1 for external clock. The input clock to the baud rate generator may be either an internal clock or TIN1, and may be faster as EXTAL. However, the output of the baud rate generator must provide a CLKO/CLKTX and CLKO/CLKRX ratio greater than or equal to 3/1.

2. Where p=1/CLKO. Thus, for a 20.48-MHz CLKO rate, p=48.8 ns.



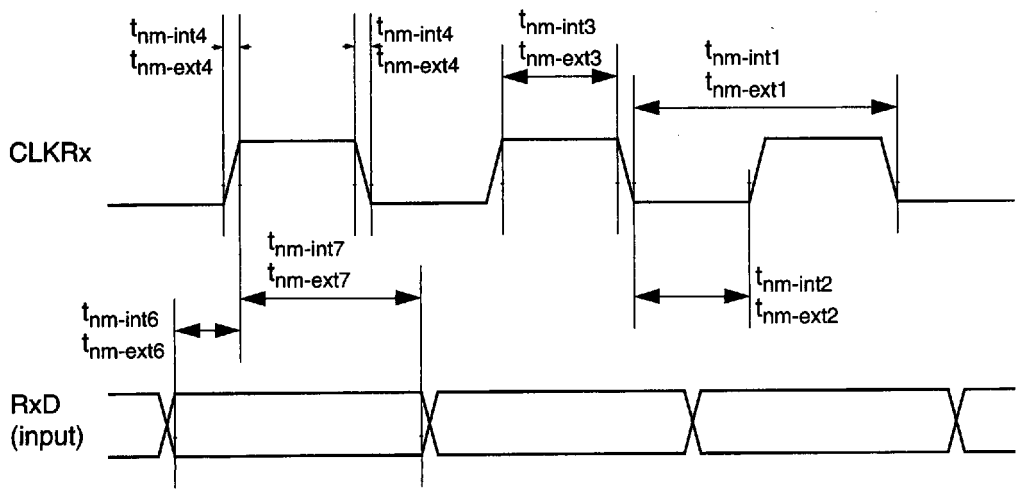


Figure 7-28. NMSI Timing Specifications