DECADE COUNTER

MC5490 • MC7490
MC9390 • MC8390

ISSUE 3

Add Suffix F for TO-86 ceramic flat package (Case 607).
Suffix L for TO-116 dual in-line ceramic package (Case 632).
Suffix P for TO-116 dual in-line plastic package (Case 646) MC7490, MC8390

RESET/COUNT TRUTH TABLE

R0		R9		OUTPUT			
Pin 2	Pin 3	Pin 6	Pin 7	Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

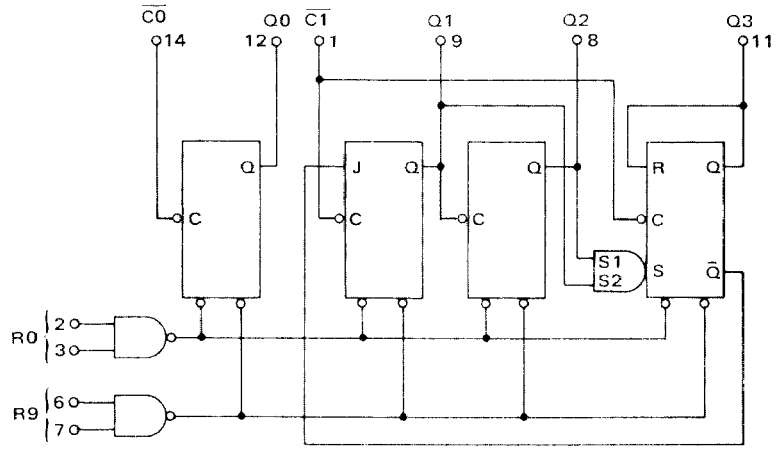
X = Don't care.

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to $\overline{C1}$.

These 4-bit counters are comprised of a divide-by-two section and a divide-by-five section. These sections can be used independently, or can be connected to perform the counting function or the simple divide-by-ten function. Two sets of direct RESET inputs are provided to allow setting all outputs to a logic "0" or to the BCD count of 9.



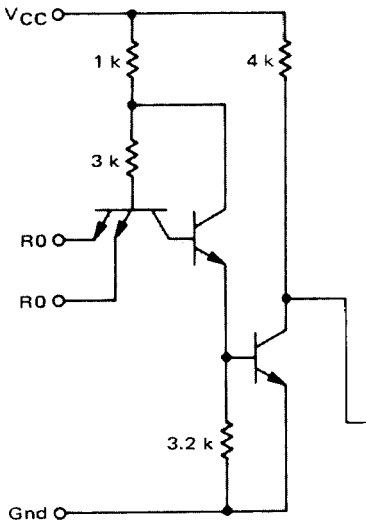
Input Loading Factor:
R0, R9 = 1
$\overline{C0}$ = 2
$\overline{C1}$ = 4

Output Loading Factor = 10

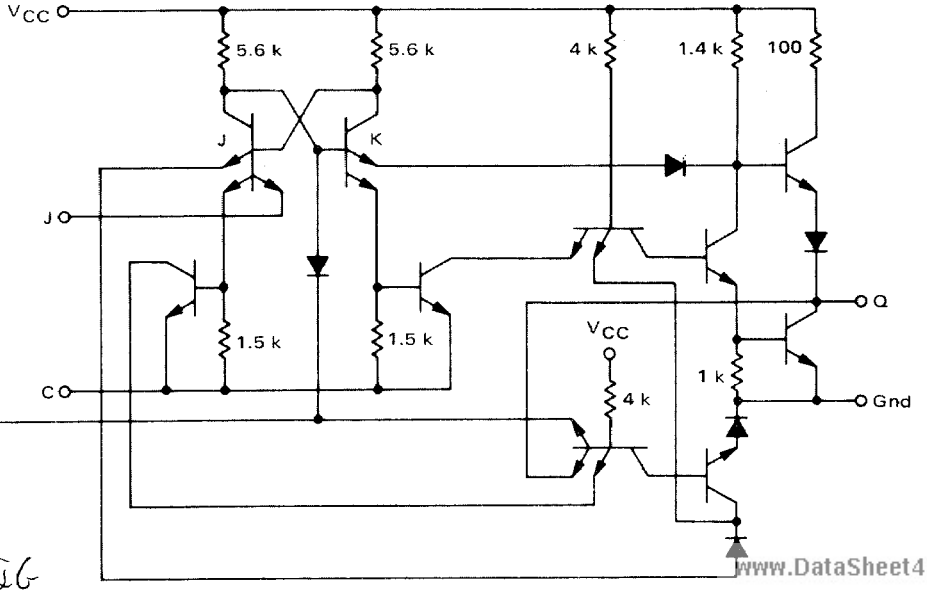
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 20 ns typ/bit

V_{CC} = Pin 5
Gnd = Pin 10

TYPICAL RESET GATE



TYPICAL FLIP-FLOP



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ORIG

004478

4478

1 of

ELECTRICAL CHARACTERISTICS

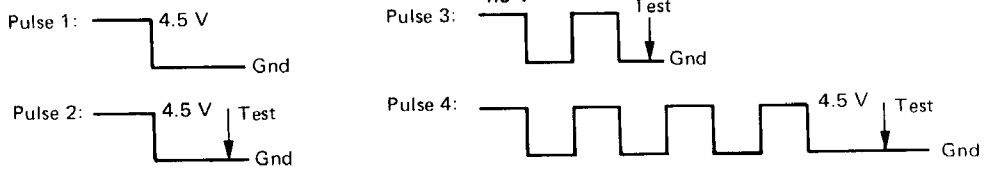
Test procedures are shown for only one input of each reset gate. The other input of each reset gate is tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{ILT1}	V_{ILT2}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}
MC5490, MC9390	16	-0.4	0.4	2.4	5.5	4.5	0.8	0.7	2.0	5.0	4.5	5.5
MC7490, MC8390	16	-0.4	0.4	2.4	5.5	4.5	0.8	0.8	2.0	5.0	4.75	5.25

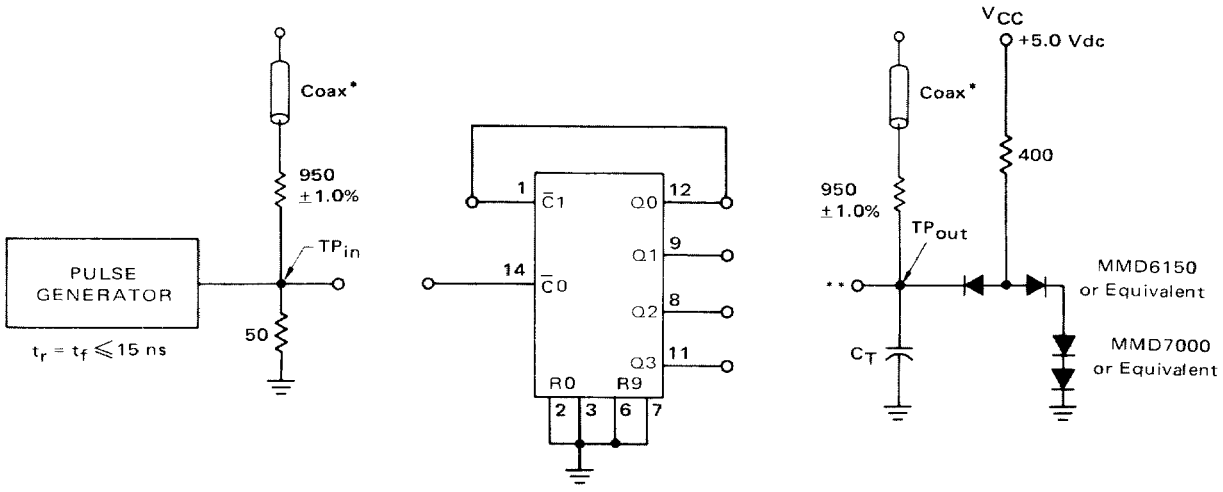
Characteristic	Symbol	Pin Under Test	MC5490/MC9390 Test Limits -55 to +125°C Min	Max	Unit	MC7490/MC8390 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{ILT1}	V_{ILT2}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Pulse 2, 3, 4	Gnd
Input																							
Forward Current R0	I_{IL}	2	–	-1.6	mAdc	-	-1.6	mAdc	–	–	2	–	–	3						5			
R9		6	–	-1.6	↓	–	-1.6	↓	–	–	6	–	–	7	–	–				↓			7,10
C0		14	–	-3.2		–	-3.2		–	–	14	–	–		–	–							9,10
C1		1	–	-6.4		–	-6.4		–	–	1	–	–		–	–							8,10
Leakage Current R0	I_{IH}	2	–	40	μAdc	–	40	μAdc	–	–	–	2	–	–	–	–	–	–		5			3,5
R9		6	–	40	↓	–	40	↓	–	–	–	6	–	–	–	–	–	–		↓			7,10
C0		14	–	80		–	80		–	–	–	14	–	–	–	–	–	–					9,10
C1		1	–	160		–	160		–	–	–	1	–	–	–	–	–	–					8,10
R0	I_{IHH}	2	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	2	–	–	–	–	–		5			3,10
R9		6	–	↓	↓	–	↓	↓	–	–	–	–	6	–	–	–	–	–		↓			7,10
C0		14	–			–			–	–	–	–	14	–	–	–	–	–					9,10
C1		1	–			–			–	–	–	–	1	–	–	–	–	–					8,10
Output*																							
Output Voltage Q0	V_{OL}	12	–	0.4	Vdc	–	0.4	Vdc	12	–	–	–	–	–	6,7	–	2,3	–	5				10
Short-Circuit Current Pulse 2	I_{OS}†		-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	–	–	–	–	–	5	2,3	14	10,12
Output Voltage Pulse 2	V_{OH}	↓	2.4	–	Vdc	2.4	–	Vdc	–	12	–	–	–	–	↓	–	–	–	5		2,3	14	10
Q1	V_{OL}	9	–	0.4	Vdc	–	0.4	Vdc	9	–	–	–	–	–	6,7	–	2,3	–	5	–			10
Pulse 2	I_{OS}†	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	↓	–	–	–	–	5	2,3	1	9,10
Pulse 2	V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	9	–	–	–	–		–	–	–	5	–	2,3	1	10
Q2	V_{OL}	8	–	0.4	Vdc	–	0.4	Vdc	8	–	–	–	–	–	6,7	1	2,3	–	5				10
Pulse 3	I_{OS}†	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	↓	–	–	–	–	5	2,3	1	8,10
Pulse 3	V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	8	–	–	–	–		1	–	–	5	–	2,3	1	10
Q3	V_{OL}	11	–	0.4	Vdc	–	0.4	Vdc	11	–	–	–	–	–	6,7	1	2,3	–	5				10
Pulse 4	I_{OS}†	↓	-20	-57	mAdc	-18	-57	mAdc	–	–	–	–	–	–	↓	↓	–	–	–	5	2,3	1	10,11
Pulse 4	V_{OH}		2.4	–	Vdc	2.4	–	Vdc	–	11	–	–	–	–			–	–	5	–	2,3	1	10
Power Requirements (Total Device)																							
Power Supply Drain	I_{CC}	5	–	46	mAdc	–	53	mAdc	–	–	–	–	–	–	–	–	–	–	–	5	2,3	–	1,6,7,10,14

*Pulse 1 applied prior to Pulse 2, 3, and 4.

†Only one output should be shorted at a time.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



f_{tog} = 10 MHz min

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe.

**A load is connected to each output during the test.