

12-Stage Binary Ripple Counter

MC74AC4040

The MC74AC4040 consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4040 for some designs.

Features

- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity
- These are Pb-Free Devices

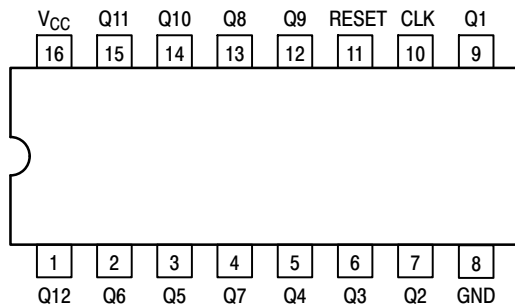


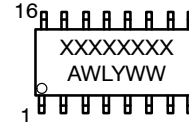
Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low



MARKING DIAGRAM



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MC74AC4040

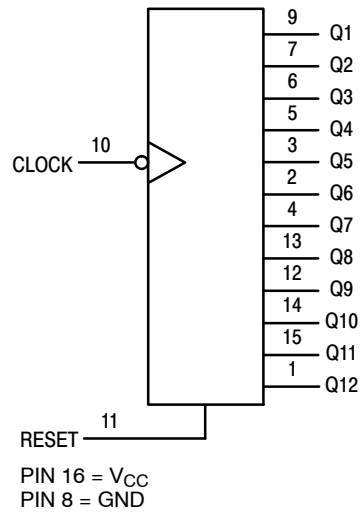


Figure 2. Logic Diagram

MC74AC4040

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V
V _I	DC Input Voltage	-0.5 ≤ V _{CC} +0.5	V
V _O	DC Output Voltage (Note 1)	-0.5 ≤ V _{CC} +0.5	V
I _{IK}	DC Input Diode Current	±20	mA
I _{OK}	DC Output Diode Current	±50	mA
I _O	DC Output Sink/Source Current	±50	mA
I _{CC}	DC Supply Current per Output Pin	±50	mA
I _{GND}	DC Ground Current per Output Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	126	°C/W
P _D	Power Dissipation in Still Air at 25°C	995	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model > 2000 Charged Device Model > 1000	V
I _{Latch-Up}	Latch-Up Performance (Note 4)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} /V _{OUT}	Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	-
T _A	Operating Temperature, All Package Types	-40	+85	°C
t _r /t _f	Input Rise/Fall Time (Figure 1)	V _{CC} = 3.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 5.5 V 0	150 40 25	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Conditions	Value	Unit
I_{CC}	Maximum Quiescent Supply Voltage	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5$ V, $T_A =$ Worst Case	80	μ A
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND $V_{CC} = 5.5$ V, $T_A = 25^\circ$ C	8.0	μ A

DC CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	74AC		74AC		Unit
				$T_A = +25^\circ$ C		$T_A = -40^\circ$ C to $+85^\circ$ C		
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	3.0	–	2.1	2.1	V	
			4.5	–	3.15	3.15		
			5.5	–	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	3.0	–	0.9	0.9	V	
			4.5	–	1.35	1.35		
			5.5	–	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	$I_{OUT} = -50$ μ A	3.0	2.99	2.9	2.9	V	
			4.5	4.49	4.4	4.4		
			5.5	5.49	5.4	5.4		
		$*V_{IN} = V_{IL}$ or V_{IH} –12 mA	I_{OH} –24 mA	3.0	–	2.56	2.46	V
				4.5	–	3.86	3.76	
5.5	–	4.86	4.76					
V_{OL}	Maximum Low Level Output Voltage	$I_{OUT} = 50$ μ A	3.0	0.002	0.1	0.1	V	
			4.5	0.001	0.1	0.1		
			5.5	0.001	0.1	0.1		
		$*V_{IN} = V_{IL}$ or V_{IH} 12 mA	I_{OL} 24 mA	3.0	–	0.36	0.44	V
				4.5	–	0.36	0.44	
5.5	–	0.36	0.44					
I_{IN}	Maximum Input Leakage Current	$V_I = V_{CC},$ GND	5.5	–	± 0.1	± 1.0	μ A	
I_{OLD}	Minimum Dynamic Output Current†	$V_{OLD} = 1.65$ V Max	5.5	–	–	75	mA	
I_{OHD}		$V_{OHD} = 3.85$ V Min	5.5	–	–	–75	mA	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	Conditions	V _{CC} * (V)	74AC			74AC		Unit
				T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
				Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency		3.3 5.0	110 130	120 140	– –	100 120	– –	MHz
t _{CP} to Q1	Propagation Delay n _{CP} to Q1		3.3 5.0	2.0 2.0	– –	11 8.0	2.0 2.0	14 10	ns
Q _n to Q _{n+1}	Propagation Delay Q _n to Q _{n+1}		3.3 5.0	0 0	– –	5.5 3.5	0 0	6.5 4.5	ns
MR to Q t _{HL}	Propagation Delay MR to Q		3.3 5.0	3.0 3.0	– –	12 10	3.0 3.0	15 12	ns
t _{rec} n _{CP} to MR	Recovery Time		3.3 5.0	0 0	-2.5 -1.5	– –	0 0	– –	ns
t _w n _{CP}	Minimum Pulse Width Clock Pin		3.3 5.0	4.0 3.0	3.5 2.5	– –	4.5 3.5	– –	ns
t _w MR	Minimum Pulse Width Master Reset		3.3 3.0	4.0 3.0	3.5 2.5	– –	4.5 3.5	– –	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

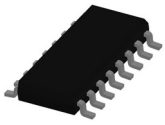
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Conditions	Value Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.0 V	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0 V	50	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74AC4040DR2G	AC4040G	SOIC-16 (Pb-Free)	2,500 Tape & Reel

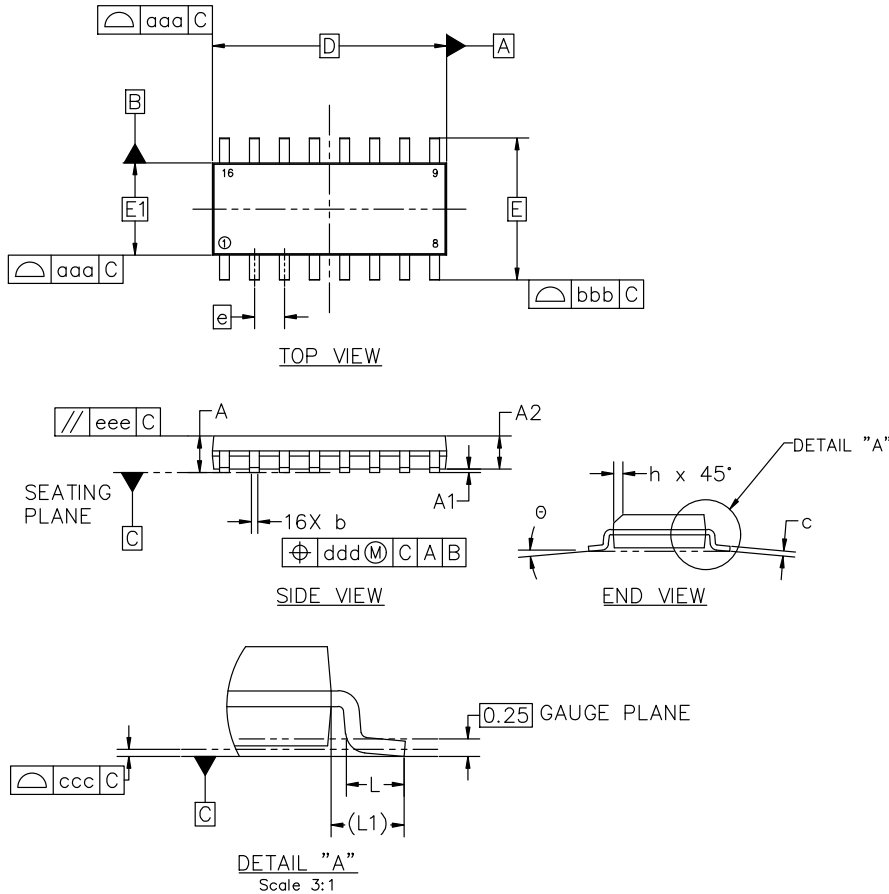


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

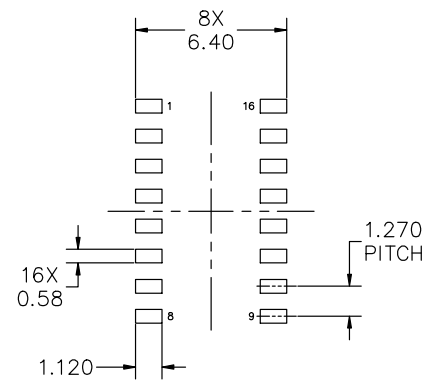
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

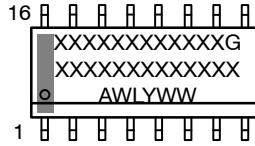
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CASE 751B
ISSUE M

DATE 18 OCT 2024

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p>	

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