

# MC74AC109, MC74ACT109



**ON Semiconductor™**

<http://onsemi.com>

## Dual JK̄ Positive Edge-Triggered Flip-Flop

The MC74AC109/74ACT109 consists of two high-speed completely independent transition clocked JK̄ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK̄ design allows operation as a D flip-flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and K̄ inputs together.

### Asynchronous Inputs:

- LOW input to  $\overline{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\overline{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\overline{C}_D$  and  $\overline{S}_D$  makes both Q and  $\overline{Q}$  HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 Has TTL Compatible Inputs

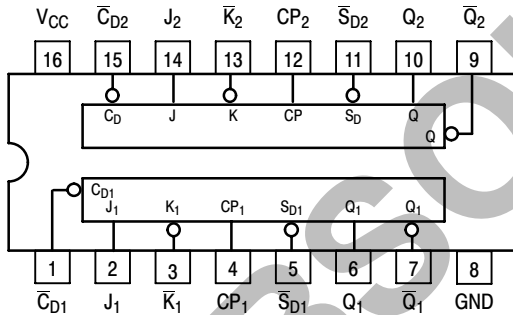
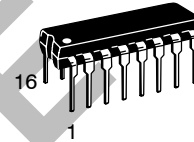


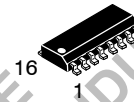
Figure 1. Pinout; 16-Lead Packages Conductors (Top View)

### PIN ASSIGNMENT

PIN	FUNCTION
J <sub>1</sub> , J <sub>2</sub> , K̄ <sub>1</sub> , K̄ <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
$\overline{C}_D1$ , $\overline{C}_D2$	Direct Clear Inputs
$\overline{S}_D1$ , $\overline{S}_D2$	Direct Set Inputs
Q <sub>1</sub> , Q <sub>2</sub> , Q̄ <sub>1</sub> , Q̄ <sub>2</sub>	Outputs



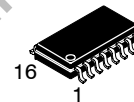
DIP-16  
N SUFFIX  
CASE 648



SO-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



EIAJ-16  
M SUFFIX  
CASE 966

### ORDERING INFORMATION

Device	Package	Shipping
MC74AC109N	PDIP-16	25 Units/Rail
MC74ACT109N	PDIP-16	25 Units/Rail
MC74AC109D	SOIC-16	48 Units/Rail
MC74ACT109D	SOIC-16	48 Units/Rail
MC74AC109DR2	SOIC-16	2500 Tape & Reel
MC74ACT109DR2	SOIC-16	2500 Tape & Reel
MC74AC109DT	TSSOP-16	96 Units/Rail
MC74ACT109DT	TSSOP-16	96 Units/Rail
MC74AC109DTR2	TSSOP-16	2500 Tape & Reel
MC74ACT109DTR2	TSSOP-16	2500 Tape & Reel
MC74AC109M	EIAJ-16	50 Units/Rail
MC74ACT109M	EIAJ-16	50 Units/Rail
MC74AC109MEL	EIAJ-16	2000 Tape & Reel
MC74ACT109MEL	EIAJ-16	2000 Tape & Reel

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

# MC74AC109, MC74ACT109

## TRUTH TABLE

Inputs					Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\downarrow$	L	L	L	H
H	H	$\downarrow$	H	L	Toggle	
H	H	$\downarrow$	L	H	$Q_0$	$\bar{Q}_0$
H	H	$\downarrow$	H	H	H	L
H	H	L	X	X	$Q_0$	$\bar{Q}_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 $\downarrow$  = LOW-to-HIGH Clock Transition  
 X = Immaterial  
 $Q_0(\bar{Q}_0)$  = Previous  $Q_0(\bar{Q}_0)$  before  
 LOW-to-HIGH Transition of Clock

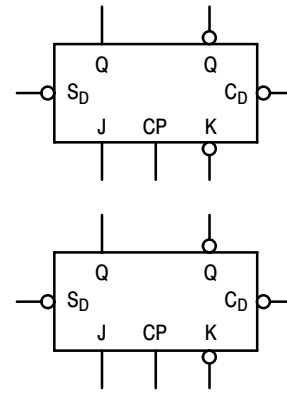
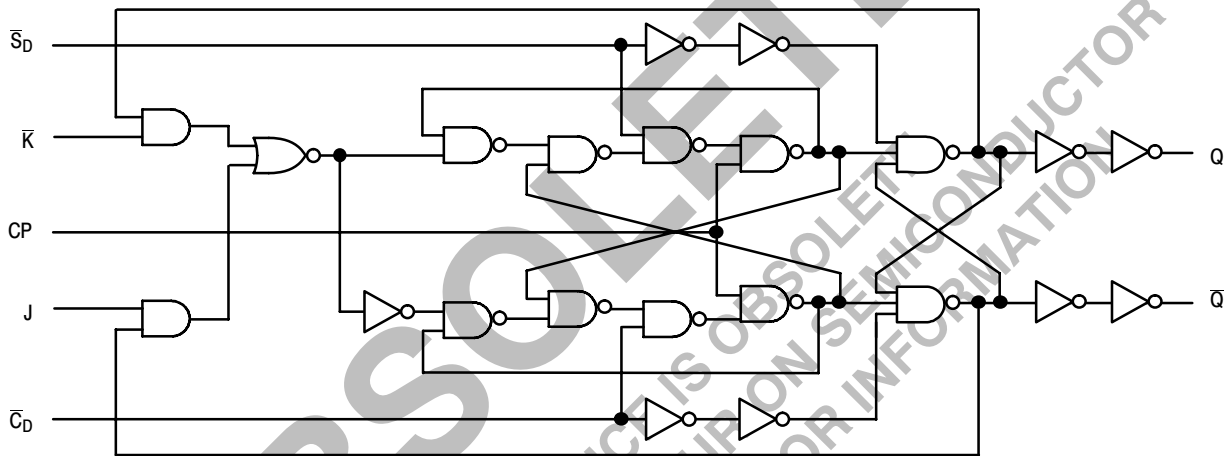


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram  
 (One Half Shown)

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{OUT}$	DC Output Sink/Source Current, per Pin	$\pm 50$	mA
$I_{CC}$	DC $V_{CC}$ or GND Current per Output Pin	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

# MC74AC109, MC74ACT109

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V <sub>CC</sub>	V	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V <sub>CC</sub> @ 3.0 V	–	150	–	ns/V
		V <sub>CC</sub> @ 4.5 V	–	40	–	
		V <sub>CC</sub> @ 5.5 V	–	25	–	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V <sub>CC</sub> @ 4.5 V	–	10	–	ns/V
		V <sub>CC</sub> @ 5.5 V	–	8.0	–	
T <sub>J</sub>	Junction Temperature (PDIP)	–	–	140	°C	
T <sub>A</sub>	Operating Ambient Temperature Range	–40	25	85	°C	
I <sub>OH</sub>	Output Current – High	–	–	–24	mA	
I <sub>OL</sub>	Output Current – Low	–	–	24	mA	

- V<sub>IN</sub> from 30% to 70% V<sub>CC</sub>; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V<sub>IN</sub> from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74AC		74ACT		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = –40°C to +85°C			
			Typ	Guaranteed Limits	Typ	Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0	–	2.56	2.46	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> –12 mA I <sub>OH</sub> –24 mA –24 mA	
		4.5	–	3.86	3.76			
		5.5	–	4.86	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0	–	0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA	
		4.5	–	0.36	0.44			
		5.5	–	0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V <sub>OLD</sub> = 1.65 V Max	
I <sub>OHD</sub>		5.5	–	–	–75	mA	V <sub>OHD</sub> = 3.85 V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.

# MC74AC109, MC74ACT109

**AC CHARACTERISTICS** (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			74AC		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	125 150	– –	– –	100 125	– –	MHz	3–3
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	3.3 5.0	4.0 2.5	– –	13.5 10.0	3.5 2.0	16.0 10.5	ns	3–6
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	3.3 5.0	3.0 2.0	– –	14.0 10.0	3.0 1.5	14.5 10.5	ns	3–6
t <sub>PLH</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	3.3 5.0	3.0 2.5	– –	12.0 9.0	2.5 2.0	13.0 10.0	ns	3–6
t <sub>PHL</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	3.3 5.0	3.0 2.0	– –	12.0 9.5	3.0 2.0	13.5 10.5	ns	3–6

\*Voltage Range 3.3 V is 3.3 V ±0.3 V.

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC		74AC		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Set-up Time, HIGH or LOW J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	3.3 5.0	– –	6.5 4.5	7.5 5.0	ns	3–9	
t <sub>h</sub>	Hold Time, HIGH or LOW J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	3.3 5.0	– –	0 0.5	0 0.5	ns	3–9	
t <sub>w</sub>	Pulse Width CP <sub>n</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$	3.3 5.0	– –	4.0 3.5	4.5 3.5	ns	3–6	
t <sub>rec</sub>	Recovery Time $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP	3.3 5.0	– –	0 0	0 0	ns	3–9	

\*Voltage Range 3.3 V is 3.3 V ±0.3 V.

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		74ACT		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	–	3.86	3.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -24 mA	
		5.5	–	4.86	4.76			

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

# MC74AC109, MC74ACT109

## DC CHARACTERISTICS (continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		74ACT		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 24 mA I <sub>OL</sub> = 24 mA	
		5.5	-	0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
ΔI <sub>CC</sub>	Additional Max. I <sub>CC</sub> /Input	5.5	0.6	-	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V	
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V <sub>OLD</sub> = 1.65 V Max	
I <sub>OHD</sub>		5.5	-	-	-75	mA	V <sub>OHD</sub> = 3.85 V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	-	4.0	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			74ACT		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	145	-	-	125	-	MHz	3-3
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	5.0	4.0	-	11.0	3.5	13.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	5.0	3.0	-	10.0	2.5	11.5	ns	3-6
t <sub>PLH</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	5.0	2.5	-	9.5	2.0	10.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	5.0	2.5	-	10.0	2.0	11.5	ns	3-6

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		74ACT		Unit	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Set-up Time, HIGH or LOW J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	5.0	-	2.0	2.5	ns	3-9	
t <sub>h</sub>	Hold Time, HIGH or LOW J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	5.0	-	2.0	2.0	ns	3-9	
t <sub>w</sub>	Pulse Width CP <sub>n</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$	5.0	-	5.0	6.0	ns	3-6	

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC109, MC74ACT109

## AC OPERATING REQUIREMENTS (continued)

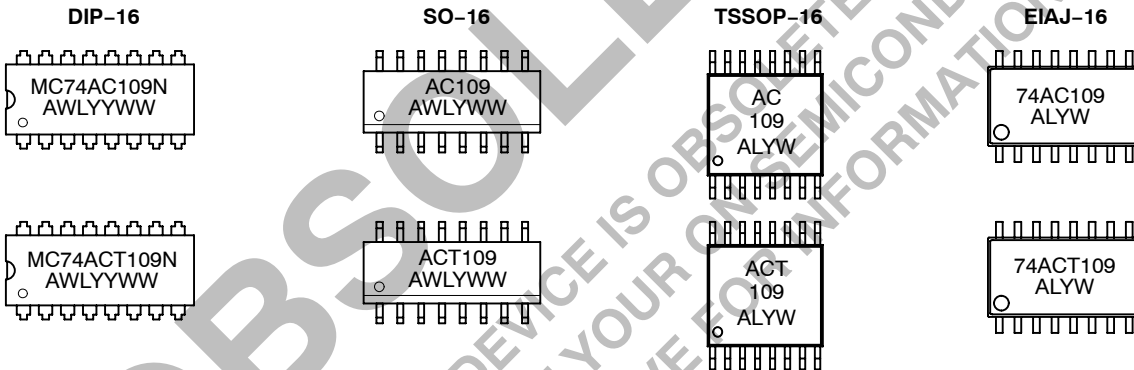
Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		Unit	Fig. No.		
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF				T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum				
t <sub>rec</sub>	Recovery Time C <sub>Dn</sub> or S <sub>Dn</sub> to CP	5.0	-	0	0	ns	3-9	

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	35	pF	V <sub>CC</sub> = 5.0 V

## MARKING DIAGRAMS

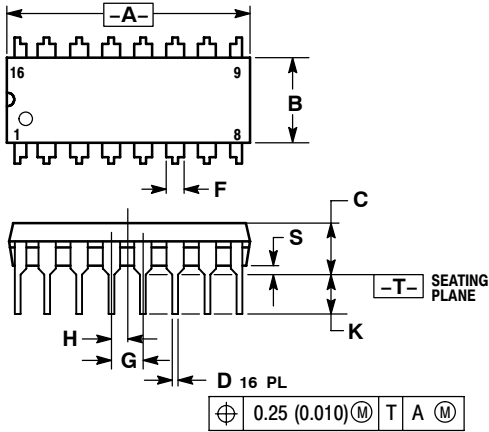


A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week

# MC74AC109, MC74ACT109

## PACKAGE DIMENSIONS

### PDIP-16 N SUFFIX 16 PIN PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

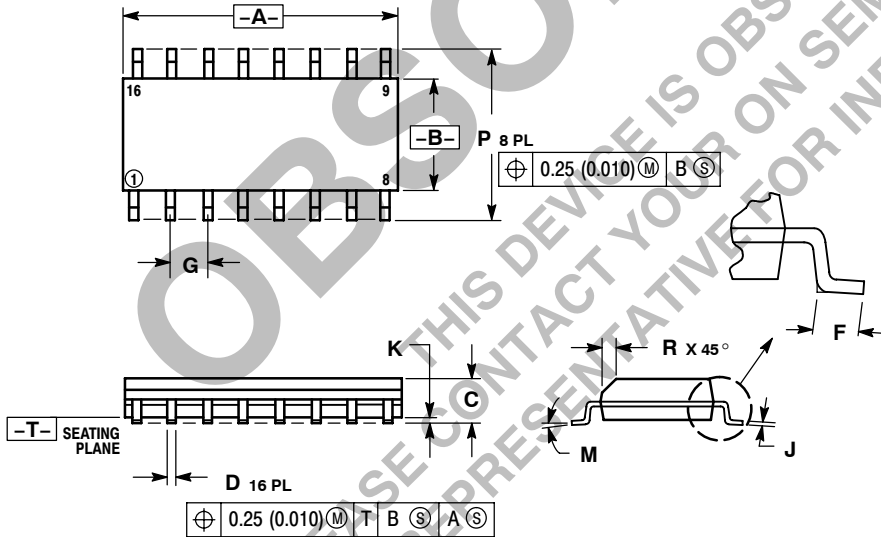


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

### SO-16 D SUFFIX 16 PIN PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

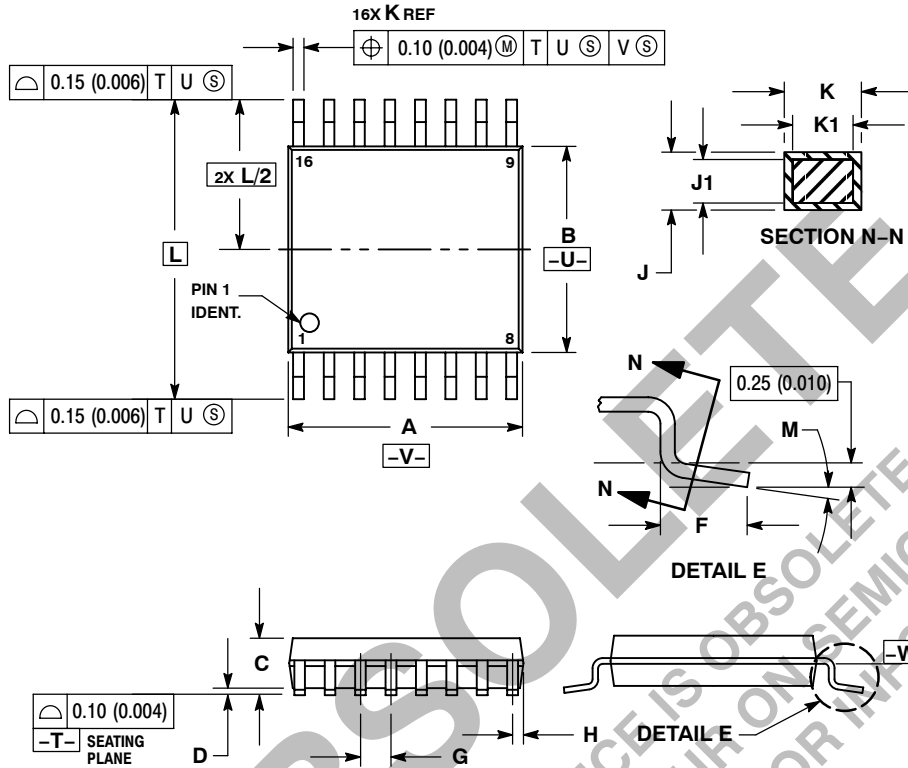
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# MC74AC109, MC74ACT109

## PACKAGE DIMENSIONS

**TSSOP-16**  
**DT SUFFIX**  
 16 PIN PLASTIC TSSOP PACKAGE  
 CASE948F-01  
 ISSUE O

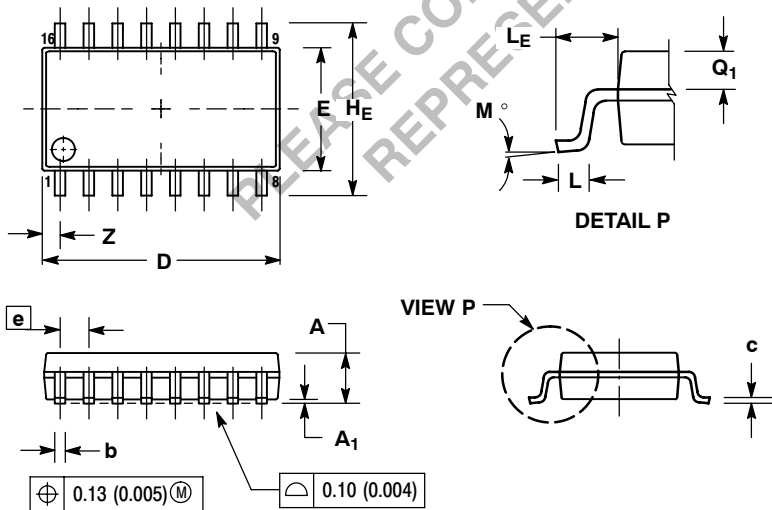


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**EIAJ-16**  
**M SUFFIX**  
 16 PIN PLASTIC EIAJ PACKAGE  
 CASE966-01  
 ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031



**OBSOLETE**  
THIS DEVICE IS OBSOLETE  
PLEASE CONTACT YOUR ON SEMICONDUCTOR  
REPRESENTATIVE FOR INFORMATION

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative