MOTOROLA

MC74F2961A
MC74F2962A

Advance Information

4-BIT CORRECTION MULTIPLE BUS BUFFERS

DESCRIPTION — The MC74F2961A and MC74F2962A are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the MC74F2960/A Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The MC74F2961A provides an inverting data path beween the data bus (B_i) and the MC74F2960/A error correction data input (Y_i) and the MC74F2962A provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the MC74F2960/A and memory data bus, thereby optimizing internal data path speeds.

The MC74F2961A and MC74F2962A are 4-bit devices. Four devices are used to interface each 16-bit MC74F2960/A Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

- Provides complete data path interface between the MC74F2960/A Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- 3-State 24 mA Output to Data Bus
- 3-State Data Output to Memory
- Inverting Data Bus for MC74F2961A and Noninverting for MC74F2962A
- Data Bus Latches Allow Operation with Multiplexed Buses
- Space Saving 24-Pin 0.3" Package

System Performance Improvement
Motorola 'A' System versus AMD Standard System

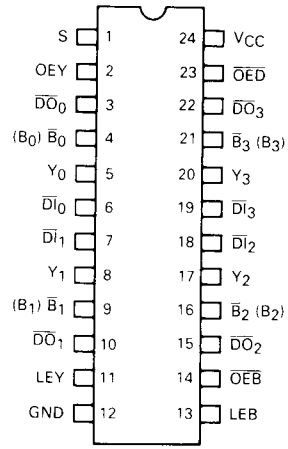
Mode	Device	Path	Am2960 Am2961	MC74F2960A/ 2961A	% Improvement with 'A'-System
Generate	2961/A	B to Y	25	12	52%
	2960/A	Data to S/C	32	20	38%
		Total Delay	**57**	**32**	**44%**
Detect	2961/A	D to Y	15	10	33%
	2960/A	Data to Error	32	19	41%
		Total Delay	**47**	**29**	**38%**
Correct	2961/A	D to Y	15	10	33%
	2960/A	Data to Data	65	42	35%
	2961/A	Y to B	20	13	35%
		Total Delay	**100**	**65**	**35%**

All delays are in nanoseconds and are manufacturer's published specifications.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4-BIT ERROR CORRECTION MULTIPLE BUS BUFFERS

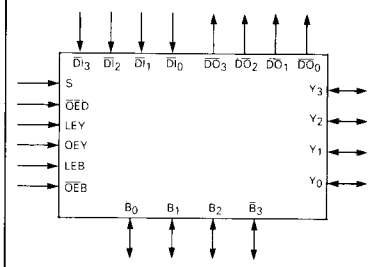
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

N Suffix — Case 724-02 (Plastic)
J Suffix — Case 758-01 (Ceramic)

LOGIC SYMBOL



B-Bus is noninverting for MC74F2962A

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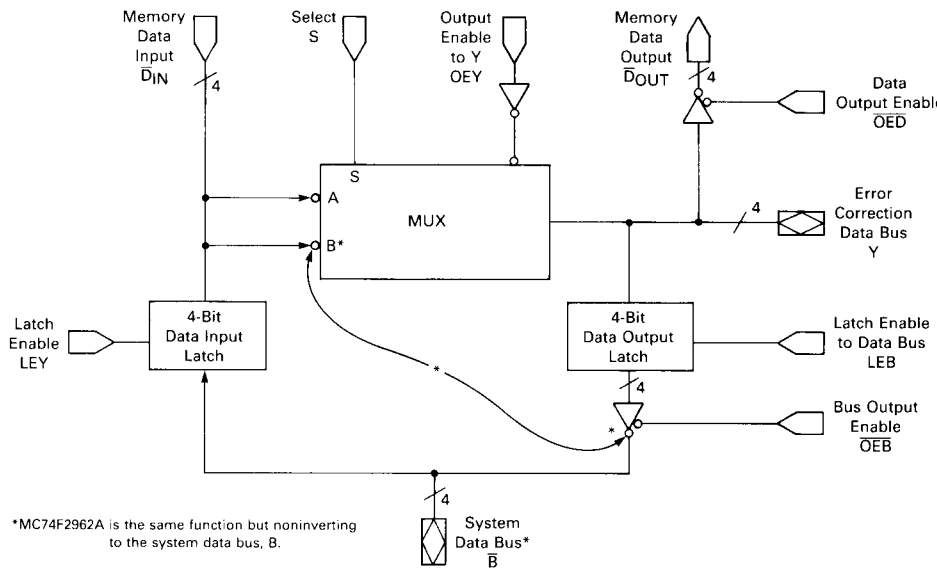
BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 9, 16, 21	B_0, B_1, B_2, B_3	I/O	The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the MC74F2961A ($\overline{B}_i$) and noninverting for the MC74F2962A (B_i).
14	$\overline{OEB}$	I	The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW, data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH, the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.
13	LEB	I	Latch Enable for the Data Output Latch. When LEB is HIGH, the latch is transparent and Y-Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.
5, 8, 17, 20	Y_0, Y_1, Y_2, Y_3	I/O	The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.
11	LEY	I	The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.
2	OEY	I	Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH, data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW, the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.
1	S	I	The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).
3, 10, 15, 22	$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$	O	The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.
23	$\overline{OED}$	I	Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.
6, 7, 18, 19	$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$	I	The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI_i}$	$\overline{B_i}$* MC74F2961A	B_i* MC74F2962A	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

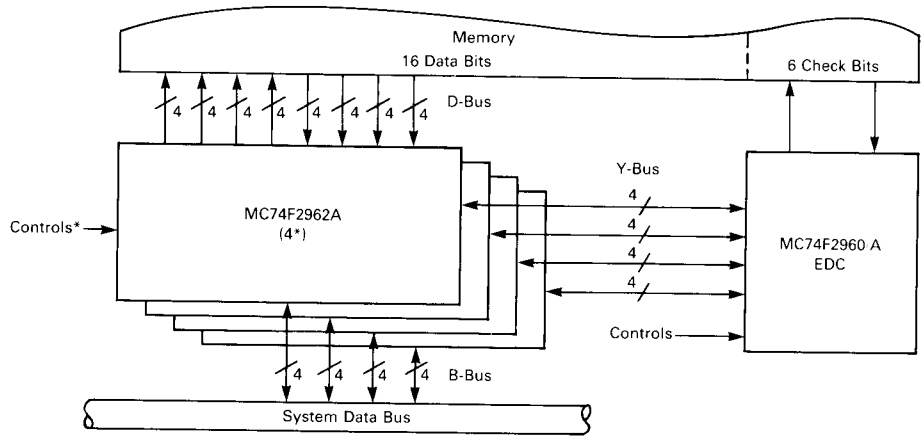
Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ MC74F2961A	B MC74F2962A
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

APPLICATION



*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65°C to +150°C
Ambient Temperature Under Bias
Power Applied . . . . . 55°C to +125°C
Supply Voltage to Ground Potential
Continuous . . . . . −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
High Output State . . . . . 0.5 V to V_{CC} Max
DC Input Voltage . . . . . 5.5 V
DC Output Current, Into Outputs . . . . . 30 mA
DC Input Current . . . . . −30 mA to +5.0 mA

Stress above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature . . . . . 0°C to +70°C
Supply Voltage . . . . . +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
Y BUS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0 mA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4 V	OEY = LOW			−1.2	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7 V	OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5 V	OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4 V			−1.2	mA
			V_O = 2.4 V			+100	μA
B BUS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4 V	$\overline{OEB}$ = HIGH			−0.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7 V	$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5 V	$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4 V			−0.6	μA
			V_O = 2.4 V			+100	
DO OUTPUTS							
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1.0 mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4 V			−50	μA
			V_O = 2.4 V			+50	
DI INPUTS AND CONTROLS							
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4 V	DI Inputs			−0.6	mA
			Controls			−0.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0 V				100	μA
POWER SUPPLY							
I_{CC}	Power Supply Current	V_{CC} = MAX			60	75	mA

NOTES: 1. For conditions as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING TEST CIRCUIT

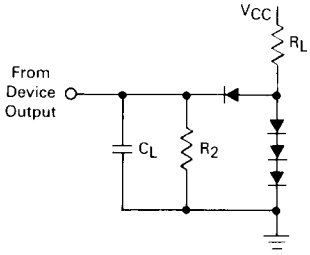


FIGURE 1.

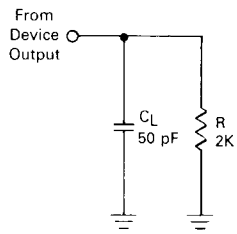


FIGURE 2.

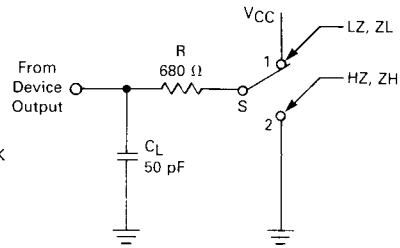


FIGURE 3.

MC74F261A SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions		COMMERCIAL Min	COMMERCIAL Max	Units
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1, C_L = 5.0 pF, R_L = 390 Ω, R_2 = 1.0 kΩ			12	ns
t_{PHL}					12	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)				10	ns
t_{PHL}					10	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)				13	ns
t_{PHL}					13	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)				16	ns
t_{PHL}					16	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y				14	ns
t_{PZL}					14	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y				14	ns
t_{PLZ}					14	ns
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ			16	ns
t_{PHL}					16	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)				13	ns
t_{PHL}					13	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1, C_L = 300 pF, R_L = 270 Ω, R_2 = 1.0 kΩ			23	ns
t_{PHL}					23	ns
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ			14	ns
t_{PZL}					14	ns
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$				14	ns
t_{PHZ}					14	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2, C_L = 50 pF, R = 2.0 kΩ			11	ns
t_{PHL}					11	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	Figure 3, C_L = 50 pF, R = 680 Ω	S = 2		14	ns
t_{PZL}			S = 1		14	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		S = 2		14	ns
t_{PLZ}			S = 1		14	ns
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1, C_L = 50 pF, R_L = 390 Ω, R_2 = 1.0 kΩ		4		ns
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)			6		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ		4		ns
t_H	Y to LEB Hold Time (OEY = LOW)			6		ns

MC74F262A SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	COMMERCIAL		Units
			Min	Max	
t_{PLH}	Propagation Delay B to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1, C_L = 5.0 pF, R_L = 390 Ω, R_2 = 1.0 kΩ		13	ns
t_{PHL}				13	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)			10	ns
t_{PHL}				10	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)			14	ns
t_{PHL}				14	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)			16	ns
t_{PHL}				16	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y			14	ns
t_{PZL}				14	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y			14	ns
t_{PLZ}				14	ns
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ		16	ns
t_{PHL}				16	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)			14	ns
t_{PHL}				14	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1, C_L = 300 pF, R_L = 270 Ω, R_2 = 1.0 kΩ		24	ns
t_{PHL}				24	ns
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ		14	ns
t_{PZL}				14	ns
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B			14	ns
t_{PHZ}				14	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2, C_L = 50 pF, R = 2.0 kΩ		11	ns
t_{PHL}				11	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	S = 2		14	ns
t_{PZL}		S = 1		14	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$	S = 2		14	ns
t_{PLZ}		S = 1		14	ns
		Figure 3, C_L = 50 pF, R = 680 Ω			
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1, C_L = 50 pF, R_L = 390 Ω, R_2 = 1.0 kΩ	4		ns
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)		6		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1, C_L = 50 pF, R_L = 270 Ω, R_2 = 1.0 kΩ	4		ns
t_H	Y to LEB Hold Time (OEY = LOW)		6		ns

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