

Single 2-Input NAND Gate

MC74HC1G00

The MC74HC1G00 is a high speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G00 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: $t_{PD} = 7 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity
- Balanced Propagation Delays ($t_{pLH} = t_{pHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL} = 2 \text{ mA}$)
- Chip Complexity: < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

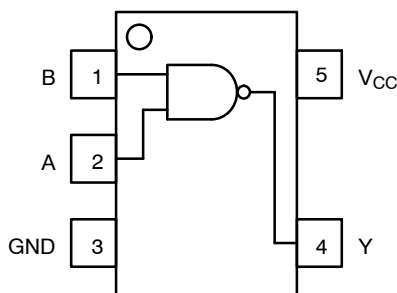


Figure 1. Pinout

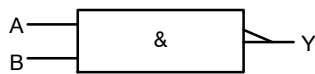


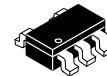
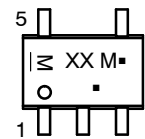
Figure 2. Logic Symbol

| PIN ASSIGNMENT | |
|----------------|----------|
| 1 | B |
| 2 | A |
| 3 | GND |
| 4 | Y |
| 5 | V_{CC} |

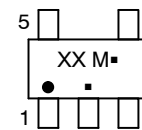


SC-88A
DF SUFFIX
CASE 419A

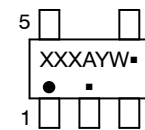
MARKING DIAGRAMS



TSOP-5
DT SUFFIX
CASE 483



Commercial



NLV Prefix

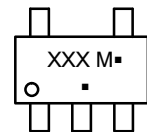
XXX = Device Code
M = Date Code*
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.



SC-74A
DBV SUFFIX
CASE 318BQ



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

MC74HC1G00

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | |
|-------------------------------------|---|--|----------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +6.5 | V | |
| V _{IN} | DC Input Voltage | -0.5 to V _{CC} +0.5 | V | |
| V _{OUT} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V | |
| I _{IK} | DC Input Diode Current | ±20 | mA | |
| I _{OK} | DC Output Diode Current | ±20 | mA | |
| I _{OUT} | DC Output Source/Sink Current | ±12.5 | mA | |
| I _{CC} or I _{GND} | DC Supply Current per Supply Pin or Ground Pin | ±25 | mA | |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C | |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C | |
| T _J | Junction Temperature Under Bias | +150 | °C | |
| θ _{JA} | Thermal Resistance (Note 1) | SC-88A SC-74A | 377 320 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C | SC-88A SC-74A | 332 390 | mW |
| MSL | Moisture Sensitivity | Level 1 | | |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | 2000 1000 | V |
| I _{LATCHUP} | Latchup Performance (Note 3) | | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow per JESD51-7.
2. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

MC74HC1G00

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|-----------------------------|----------------------------------|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 6.0 | V |
| V _{IN} | DC Input Voltage | 0.0 | V _{CC} | V |
| V _{OUT} | DC Output Voltage | 0.0 | V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time | | | ns/V |
| | | V _{CC} = 2.0 V | 0 | 20 |
| | | V _{CC} = 2.3 V to 2.7 V | 0 | 20 |
| | | V _{CC} = 3.0 V to 3.6 V | 0 | 10 |
| | | V _{CC} = 4.5 V to 6.0 V | 0 | 5 |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|-----------------|---------------------------|--|------------------------|-----------------------|------|------|-------------------------------|------|--------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | 3.0 | 2.1 | - | - | 2.1 | - | 2.1 | - | |
| | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | |
| | | | 6.0 | 4.20 | - | - | 4.20 | - | 4.20 | - | |
| V _{IL} | Low-Level Input Voltage | | 2.0 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | 3.0 | - | - | 0.9 | - | 0.9 | - | 0.9 | |
| | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | |
| | | | 6.0 | - | - | 1.80 | - | 1.80 | - | 1.80 | |
| V _{OH} | High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OH} = -20 μA | 2.0 | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | | 3.0 | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | |
| | | | 4.5 | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | |
| | | | 6.0 | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | |
| | | 4.5 | 4.18 | 4.31 | - | 4.13 | - | 4.08 | - | | |
| | | 6.0 | 5.68 | 5.80 | - | 5.63 | - | 5.58 | - | | |
| V _{OL} | Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 20 μA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 3.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 4.5 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 6.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | 4.5 | - | 0.17 | 0.26 | - | 0.33 | - | 0.40 | | |
| | | 6.0 | - | 0.18 | 0.26 | - | 0.33 | - | 0.40 | | |
| I _{IN} | Input Leakage Current | V _{IN} = 6.0 V or GND | 6.0 | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | V _{IN} = V _{CC} or GND | 6.0 | - | - | 1.0 | - | 10 | - | 40 | μA |

MC74HC1G00

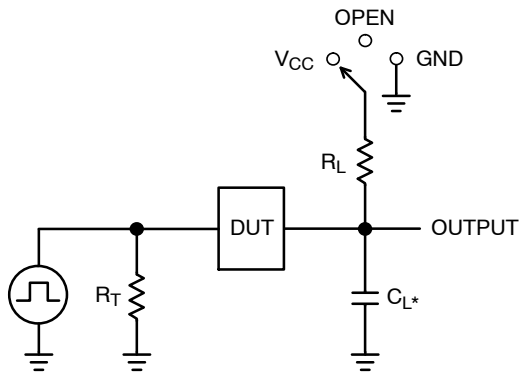
AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|--|-------------------------------------|--|-----------------------|-----|-----|-------------------------------|-----|--------------------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, (A or B) to Y | V _{CC} = 5.0 V C _L = 15 pF | - | 3.5 | 15 | - | 20 | - | 25 | ns |
| | | V _{CC} = 2.0 V C _L = 50 pF | - | 20 | 100 | - | 125 | - | 155 | |
| | | V _{CC} = 3.0 V | - | 11 | 27 | - | 35 | - | 90 | |
| | | V _{CC} = 4.5 V | - | 8 | 20 | - | 25 | - | 35 | |
| | | V _{CC} = 6.0 V | - | 7 | 17 | - | 21 | - | 26 | |
| t _{TLH} , t _{THL} | Output Transition Time | V _{CC} = 5.0 V C _L = 15 pF | - | 3 | 10 | - | 15 | - | 20 | ns |
| | | V _{CC} = 2.0 V C _L = 50 pF | - | 25 | 125 | - | 155 | - | 200 | |
| | | V _{CC} = 3.0 V | - | 16 | 35 | - | 45 | - | 60 | |
| | | V _{CC} = 4.5 V | - | 11 | 25 | - | 31 | - | 38 | |
| | | V _{CC} = 6.0 V | - | 9 | 21 | - | 26 | - | 32 | |
| C _{IN} | Input Capacitance | | - | 5 | 10 | - | 10 | - | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 4) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|--|---|--|----|
| | | 10 | | |
| | | | | |

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74HC1G00



* C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1 \text{ MHz}$

Figure 3. Test Circuit

| Test | Switch Position | C_L , pF | R_L , Ω |
|------------------------------|-----------------|------------------------------|------------------|
| t_{PLH} / t_{PHL} | Open | See AC Characteristics Table | X |
| t_{TLH} / t_{THL} (Note 5) | Open | | X |
| t_{PLZ} / t_{PZL} | V_{CC} | | 1 k |
| t_{PHZ} / t_{PZH} | GND | | 1 k |

X - Don't Care

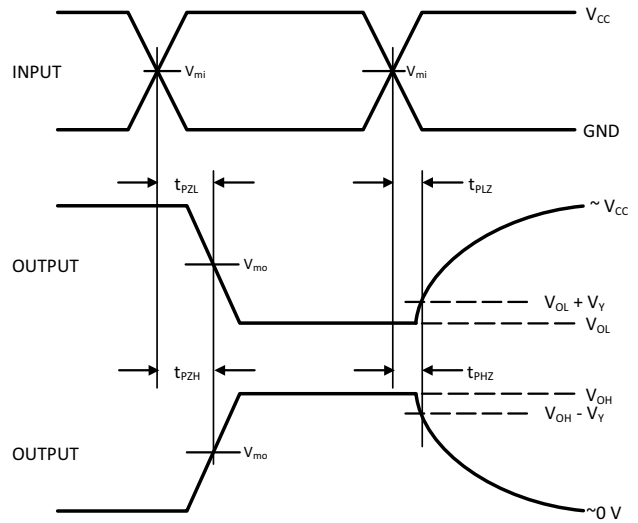
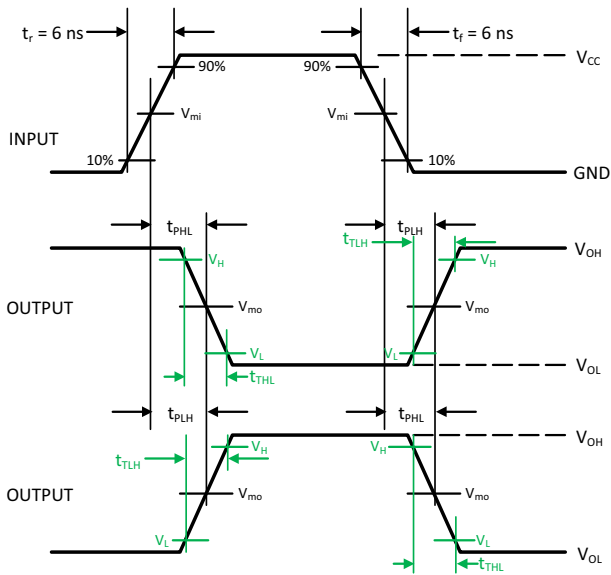


Figure 4. Switching Waveforms

| V_{CC} , V | V_{mi} , V | V_{m0} , V | | V_L , V | V_H , V | V_Y , V |
|--------------|--------------|-----------------------|---|----------------------------------|----------------------------------|-----------|
| | | t_{PLH} , t_{PHL} | t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ} | | | |
| 3.0 to 3.6 | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{OL} + 0.1 (V_{OH} - V_{OL})$ | $V_{OL} + 0.9 (V_{OH} - V_{OL})$ | 0.3 |
| 4.5 to 5.5 | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{OL} + 0.1 (V_{OH} - V_{OL})$ | $V_{OL} + 0.9 (V_{OH} - V_{OL})$ | 0.3 |

5. t_{TLH} and t_{THL} are measured from 10% to 90% of $(V_{OH} - V_{OL})$, and 90% to 10% of $(V_{OH} - V_{OL})$, respectively.

MC74HC1G00

ORDERING INFORMATION

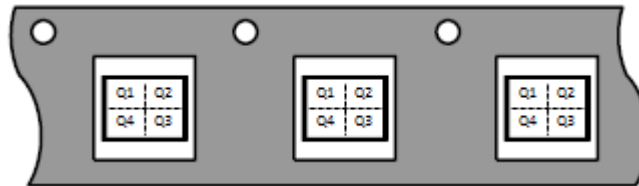
| Device | Packages | Specific Device Code | Pin 1 Orientation (See below) | Shipping [†] |
|---------------------|----------|----------------------|----------------------------------|-----------------------|
| MC74HC1G00DFT1G | SC-88A | H1 | Q2 | 3000 / Tape & Reel |
| MC74HC1G00DFT1G-Q* | SC-88A | H1 | Q2 | 3000 / Tape & Reel |
| MC74HC1G00DFT2G | SC-88A | H1 | Q4 | 3000 / Tape & Reel |
| MC74HC1G00DFT2G-Q* | SC-88A | H1 | Q4 | 3000 / Tape & Reel |
| MC74HC1G00DBVT1G | SC-74A | H1 | Q4 | 3000 / Tape & Reel |
| MC74HC1G00DBVT1G-Q* | SC-74A | H1 | Q4 | 3000 / Tape & Reel |

[†]For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

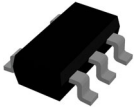
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PIN 1 ORIENTATION IN TAPE AND REEL

Direction of Feed

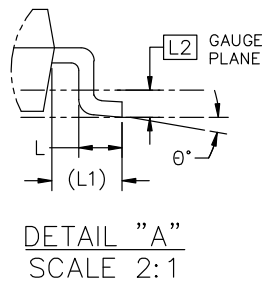
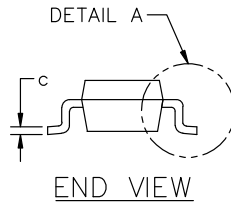
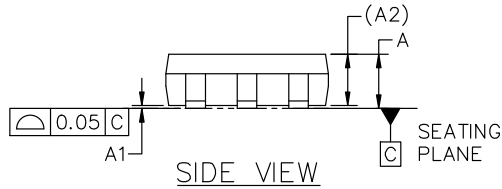
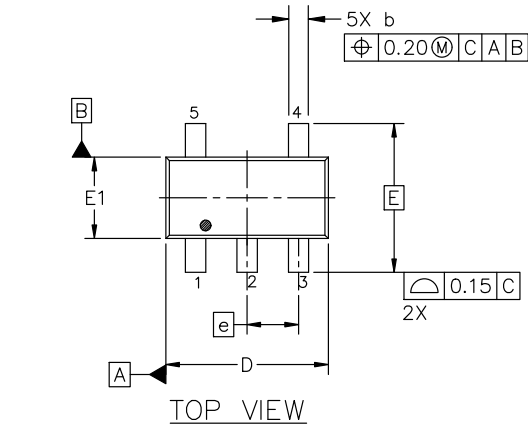


MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

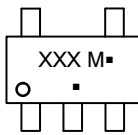


SC-74A-5 3.00x1.50x0.95, 0.95P
CASE 318BQ
ISSUE C

DATE 26 FEB 2024



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

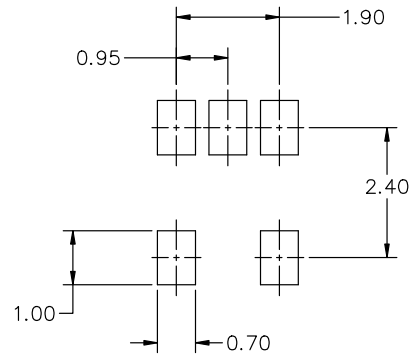
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.18 | 0.10 |
| A2 | 0.95 REF. | | |
| b | 0.25 | 0.37 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.85 | 3.00 | 3.15 |
| E | 2.75 BSC | | |
| E1 | 1.35 | 1.50 | 1.65 |
| e | 0.95 BSC | | |
| L | 0.20 | 0.40 | 0.60 |
| L1 | 0.62 REF. | | |
| L2 | 0.25 BSC | | |
| θ | 0° | 5° | 10° |



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| | | |
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| DESCRIPTION: | SC-74A-5 3.00x1.50x0.95, 0.95P | PAGE 1 OF 1 |

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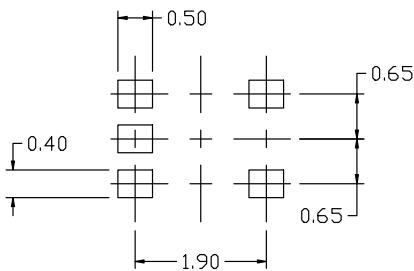
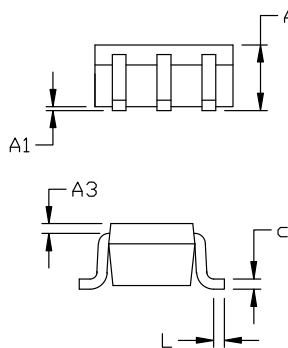
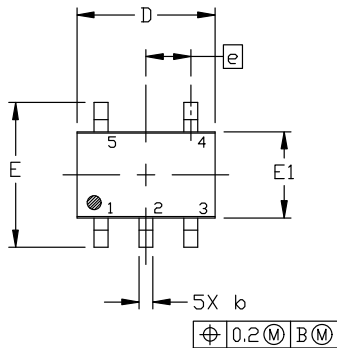
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

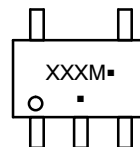
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:

1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|-------------------------|---------------------------------|---|
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| DESCRIPTION: | SC-88A (SC-70-5/SOT-353) | PAGE 1 OF 1 |

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