

Low-Voltage CMOS
16-Bit Buffer
With 5V-Tolerant Inputs and Outputs
(3-State, Inverting)

The MC74LCX16240A is a high performance, inverting 16-bit buffer operating from a 2.7 to 3.6V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16240A inputs to be safely driven from 5V devices. The LCX16240A is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24mA at the outputs. The Output Enable (OEn) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

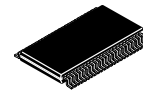
- Designed for 2.7 to 3.6V V_{CC} Operation
- 4.9ns Maximum t_{pd}
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- JEDEC Standard JESD-36 Compatible www.DataSheet4U.com
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

The MC74LCX16240A contains sixteen inverting buffers with 3-state 5V-tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16-bit operation. The 3-state outputs are controlled by an Output Enable (OEn) input for each nibble. When OEn is LOW, the outputs are on. When OEn is HIGH, the outputs are in the high impedance state.

MC74LCX16240A

LCX

LOW-VOLTAGE
CMOS 16-BIT BUFFER



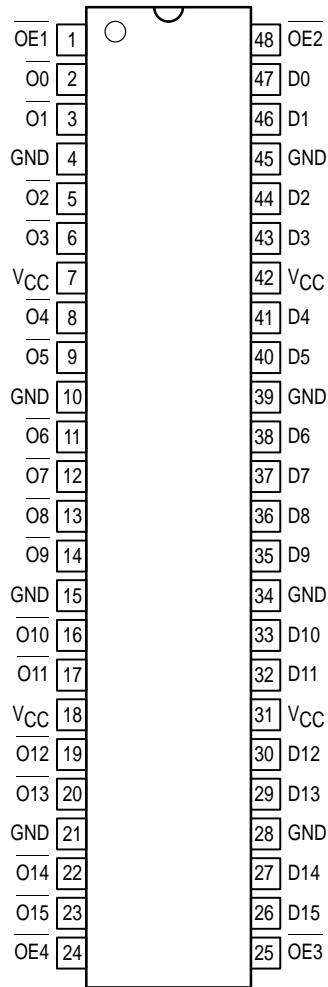
DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 1201-01

PIN NAMES

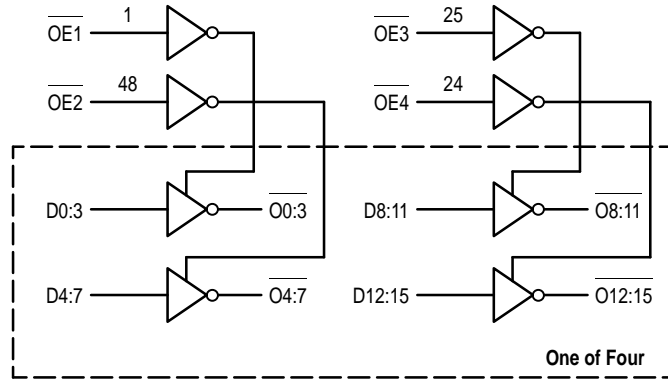
Pins	Function
OEn	Output Enable Inputs
D0-D15	Inputs
O0-O15	Outputs



MC74LCX16240A



LOGIC DIAGRAM



OE1	D0:3	O0:3	OE2	D4:7	O4:7	OE3	D8:11	O8:11	OE4	D12:15	O12:15
L	L	H	L	L	H	L	L	H	L	L	H
L	H	L	L	H	L	L	H	L	L	H	L
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1.	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V _I	Input Voltage	0		5.5	V	
V _O	Output Voltage (HIGH or LOW State) (3-State)	0		V _{CC}	V	
		0		5.5		
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0V – 3.6V			-24	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 3.0V – 3.6V			24	mA	
I _{OH}	HIGH Level Output Current, V _{CC} = 2.7V – 3.0V			-12	mA	
I _{OL}	LOW Level Output Current, V _{CC} = 2.7V – 3.0V			12	mA	
T _A	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8V to 2.0V, V _{CC} = 3.0V	0		10	ns/V	

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V	2.0		V
V _{IL}	LOW Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V		0.8	V
V _{OH}	HIGH Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OH} = -100μA	V _{CC} - 0.2		V
		V _{CC} = 2.7V; I _{OH} = -12mA	2.2		
		V _{CC} = 3.0V; I _{OH} = -18mA	2.4		
		V _{CC} = 3.0V; I _{OH} = -24mA	2.2		
V _{OL}	LOW Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OL} = 100μA		0.2	V
		V _{CC} = 2.7V; I _{OL} = 12mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 16mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 24mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
I _I	Input Leakage Current	2.7V ≤ V _{CC} ≤ 3.6V; 0V ≤ V _I ≤ 5.5V		±5.0	μA
I _{OZ}	3-State Output Current	2.7 ≤ V _{CC} ≤ 3.6V; 0V ≤ V _O ≤ 5.5V; V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0V; V _I or V _O = 5.5V		10	μA
I _{CC}	Quiescent Supply Current	2.7 ≤ V _{CC} ≤ 3.6V; V _I = GND or V _{CC}		20	μA
		2.7 ≤ V _{CC} ≤ 3.6V; 3.6 ≤ V _I or V _O ≤ 5.5V		±20	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 ≤ V _{CC} ≤ 3.6V; V _{IH} = V _{CC} - 0.6V		500	μA

AC CHARACTERISTICS (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T _A = -40°C to +85°C			
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V	
			Min	Max	Max	
t _{PLH} t _{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.9 4.9	5.9 5.9	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	6.5 6.5	7.5 7.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	5.5 5.5	6.5 6.5	ns
t _{OSSL} t _{OSLH}	Output-to-Output Skew (Note 3.)			1.0 1.0		ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

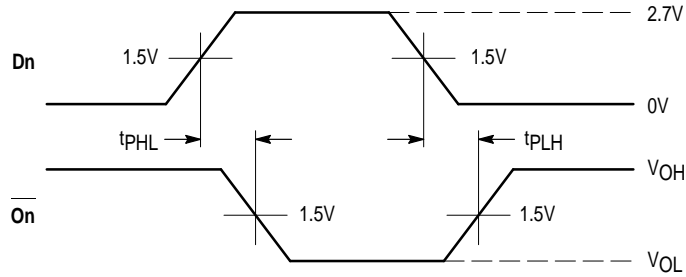
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V

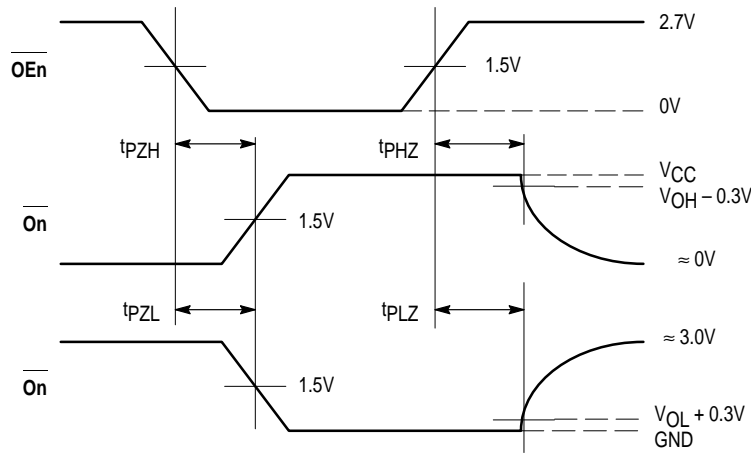
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
CPD	Power Dissipation Capacitance	10MHz, V _{CC} = 3.3V, V _I = 0V or V _{CC}	20	pF

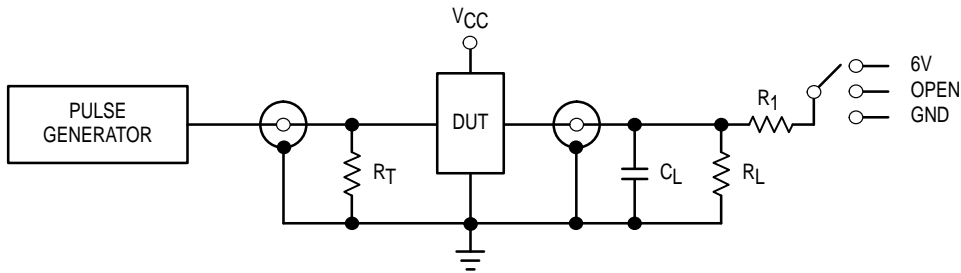


WAVEFORM 1 – PROPAGATION DELAYS
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 1. AC Waveforms



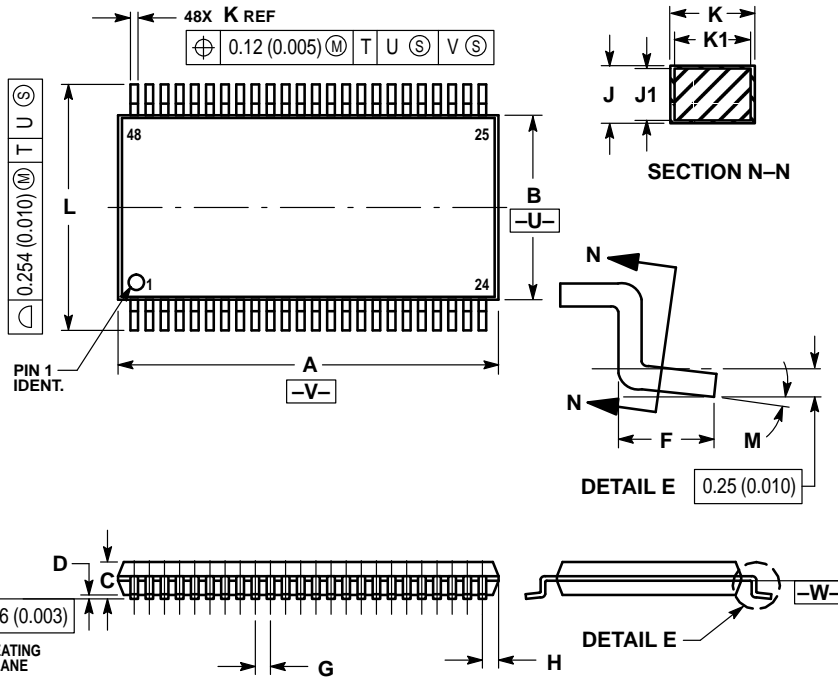
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 1201-01
 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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