Low-Voltage CMOS 18-Bit Universal Bus Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16501

LCX

LOW–VOLTAGE CMOS 18–BIT UNIVERSAL BUS TRANSCEIVER

The MC74LCX16501 is a high performance, non–inverting 18–bit universal bus transceiver operating from a 2.7 to 3.6V supply. This part is not byte controlled; it is "18–bit" controlled. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16501 inputs to be safely driven from 5V devices. The MC74LCX16501 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data flow in each direction is controlled by Output Enable (OEAB, OEBA), Latch Enable (LEAB, LEBA) and Clock inputs (CAB, CBA). When LEAB is HIGH, the A–to–B dataflow is transparent. When LEAB is LOW, and CAB is held at LOW or HIGH, the data A is latched; on the LOW–to–HIGH transition of CAB the A–data is stored in the latch/flip–flop. The outputs are active when OEAB is HIGH. When OEAB is LOW the B–outputs are in 3–state. Similarly, the LEBA, OEBA and CBA control the B–to–A dataflow. Please note that the output enables are complementary; OEAB is active HIGH, OEBA is active LOW.

DT SUFFIX
56–LEAD PLASTIC TSSOP PACKAGE
CASE 1202–01

- Designed for 2.7 to 3.6V V_{CC} Operation
- 6ns t_{pd} Maximum
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

PIN NAMES

Pins	Function
OEAB, $\overline{\text{OEBA}}$	Output Enable Inputs
CAB, CBA	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
A0–A17	Side A Inputs/Outputs
B0–B17	Side B Inputs/Outputs

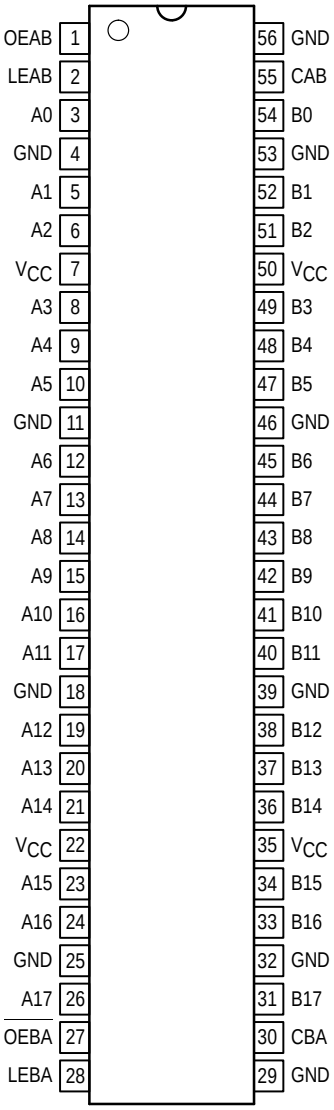


Figure 1. 56-Lead Pinout
(Top View)

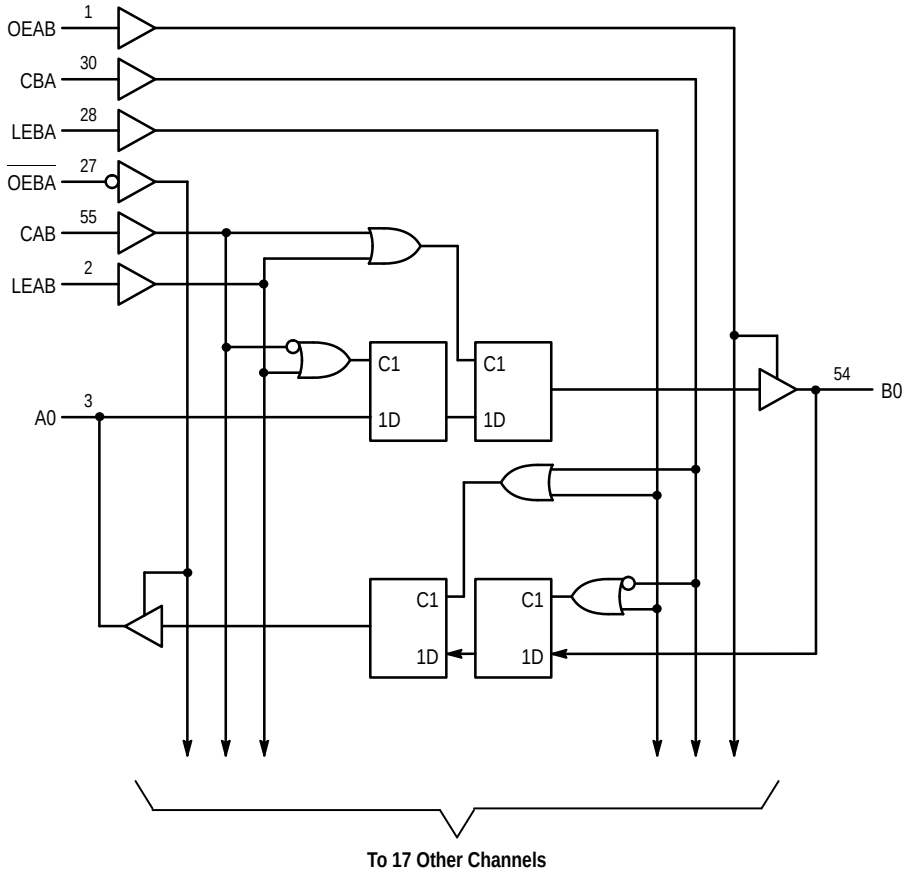


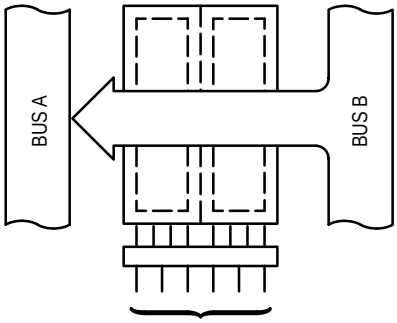
Figure 2. Logic Diagram

FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEAB	**$\overline{OEBA}$**	**LEAB**	**LEBA**	**CAB**	**CBA**	**An**	**Bn**	
L	H					Input	Input	
		L	L	H or L	H or L	X	X	Hold Data; A and B Outputs Disabled
				↑	↑	l h	l h	Clock A and/or B Data; A and B Outputs Disabled
H	H					Input	Output	
		L	X	H or L	X*	X	QA	Hold and Display B Data
				↑	X*	l h	L H	Clock A Data to B Bus; Store A Data
		H	X	X	X*	L H	L H	A Data to B Bus; (Transparent)
L	L					Output	Input	
		X	L	X*	H or L	QB	X	Hold and Display A Data
				X*	↑	L H	l h	Clock B Data to A Bus; Store B Data
		X	H	X*	X	L H	L H	B Data to A Bus; (Transparent)
H	L					Output	Output	
		L	L	H or L	H or L	QB	QA	Stored A Data to B Bus; Stored B Data to A Bus

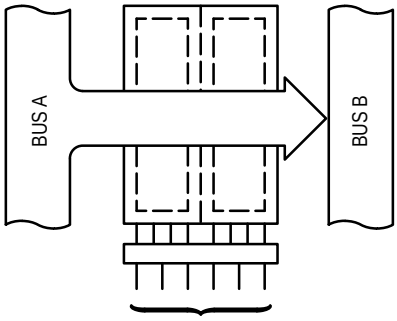
H = High Voltage Level; L = Low Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Clock Low–to–High Transition; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Clock Low–to–High Transition; X = Don't Care; ↑ = Low–to–High Clock Transition; QA = A input storage register; QB = B input storage register; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

Real Time Transfer – Bus B to Bus A



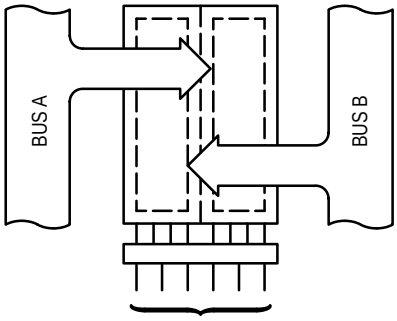
OEAB	OEBA	CAB	CBA	LEAB	LEBA
L	L	X	X	X	H

Real Time Transfer – Bus A to Bus B



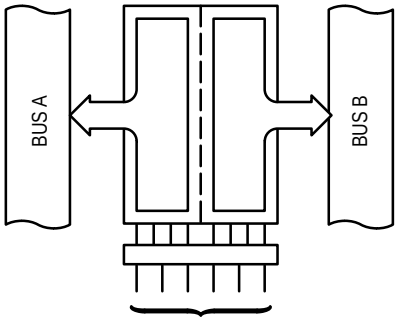
OEAB	OEBA	CAB	CBA	LEAB	LEBA
H	H	X	X	H	X

Store Data from Bus A, Bus B or Bus A and Bus B



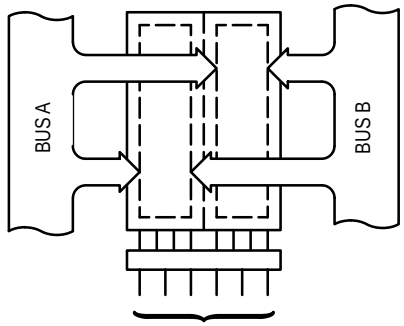
OEAB	OEBA	CAB	CBA	LEAB	LEBA
X	H	↑	X	L	X
L	X	X	↑	X	L
L	H	X	X	L	L

Transfer A Stored Data to Bus B or B Stored Data to Bus A or Both at the Same Time



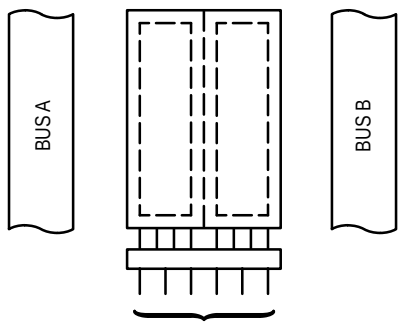
OEAB	OEBA	CAB	CBA	LEAB	LEBA
H	H	↑	X	L	X
L	L	X	↑	X	L
H	L	H or L	H or L	L	L

Store Bus A in Both Registers or Store Bus B in Both Registers



OEAB	OEBA	CAB	CBA	LEAB	LEBA
H	H	X	X	L	L
L	L	X	X	L	L

Isolation



OEAB	OEBA	CAB	CBA	LEAB	LEBA
L	H	H or L	H or L	L	L

Figure 3. Bus Applications

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$–0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$–0.5 \le V_O \le +7.0$	Output in 3–State	V
		$–0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 100µA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $0V \le V_I \le 5.5V$		±5.0	μA
I_{OZ}	3–State Output Current	$2.7 \le V_{CC} \le 3.6V$; $0V \le V_O \le 5.5V$; $V_I = V_{IH}$ or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	μA
I_{CC}	Quiescent Supply Current	$2.7 \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	μA
		$2.7 \le V_{CC} \le 3.6V$; $3.6 \le V_I$ or $V_O \le 5.5V$		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \le V_{CC} \le 3.6V$; $V_{IH} = V_{CC} – 0.6V$		500	μA

AC CHARACTERISTICS (Note 3.; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3	170				MHz
t_{PHL} t_{PLH}	Propagation Delay Input to Output	1	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Output	3	1.5 1.5	6.7 6.7	1.5 1.5	8.0 8.0	ns
t_{PHL} t_{PLH}	Propagation Delay LExx to Output	4	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.2 7.2	1.5 1.5	8.2 8.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t_s	Setup Time	3,4	2.5		2.5		ns
t_h	Hold Time	3,4	1.5		1.5		ns
t_w	Pulse Width Time	3,4	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 4.)			1.0 1.0			ns

3. These AC parameters are preliminary and may be modified prior to release.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

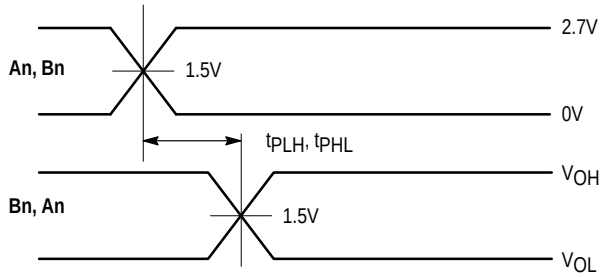
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 5.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 5.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

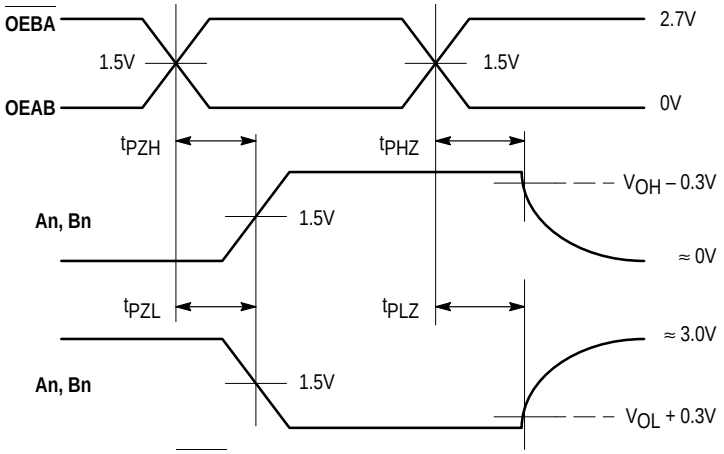
5. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	20	pF

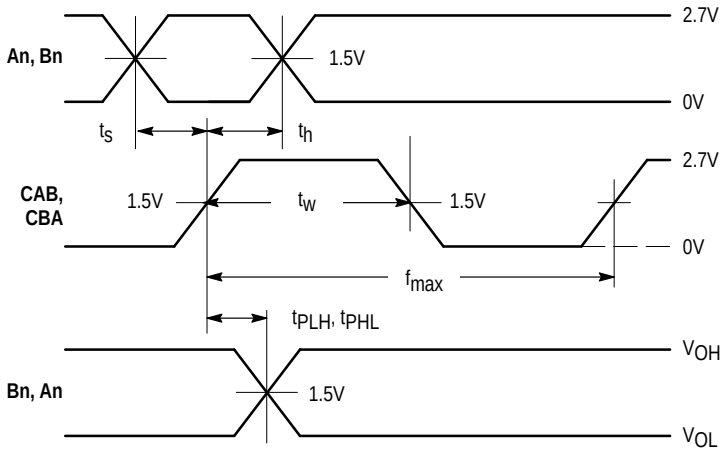


WAVEFORM 1 – An to Bn PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



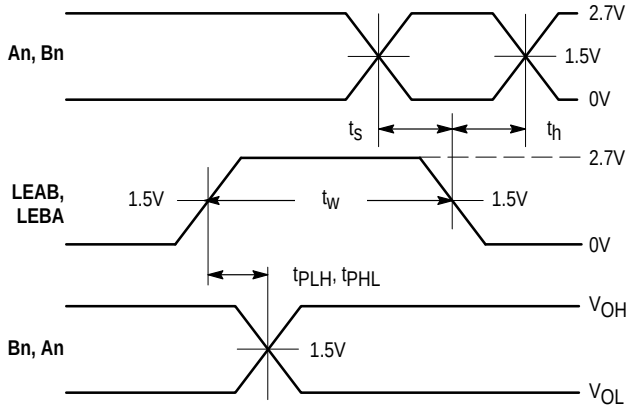
WAVEFORM 2 – $\overline{OEBA}$/OEAB to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 4. AC Waveforms



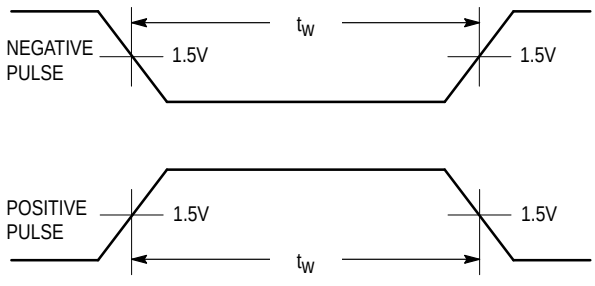
WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted



WAVEFORM 4 – LExx to An, Bn PROPAGATION DELAYS, LExx MINIMUM PULSE WIDTH, An, Bn to LExx SETUP AND HOLD TIMES

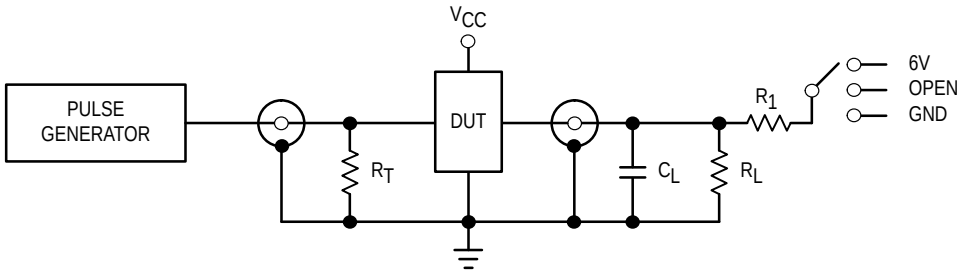
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted



WAVEFORM 5 – INPUT PULSE DEFINITION

$t_R = t_F$ = 2.5ns, 10% to 90% of 0V to 2.7V

Figure 5. AC Waveforms (continued)



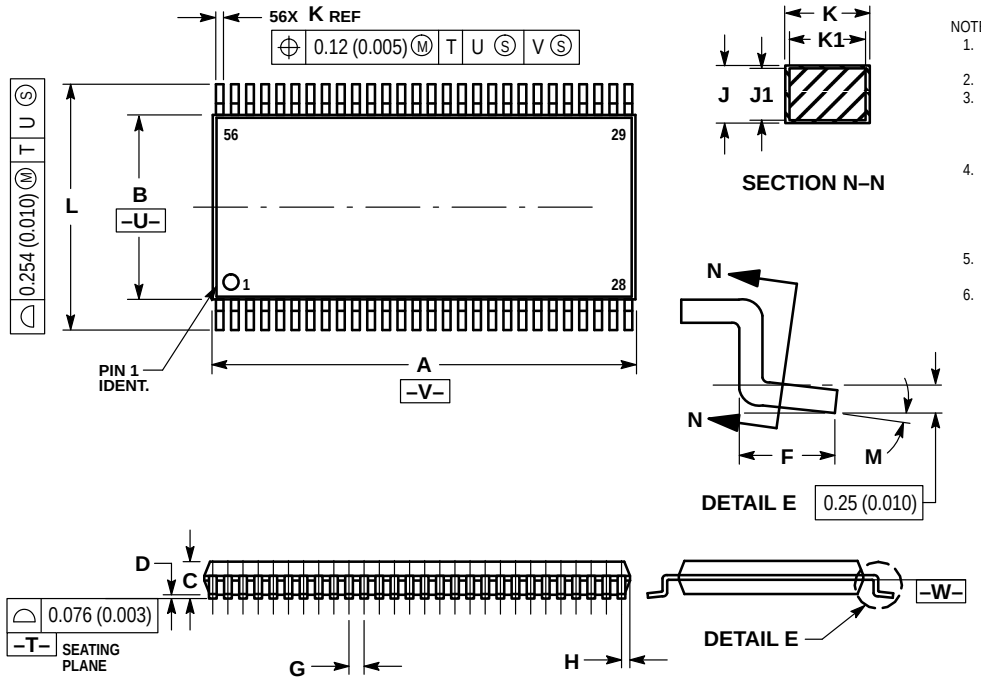
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 6. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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