Advance Information

Low-Voltage CMOS 16-Bit Transceiver/Registered Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16646

LCX

LOW–VOLTAGE CMOS 16–BIT TRANSCEIVER/ REGISTERED TRANSCEIVER

The MC74LCX16646 is a high performance, non–inverting 16–bit transceiver/registered transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16646 inputs to be safely driven from 5V devices. The MC74LCX16646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable (OEn) and Direction Control (DIRn) pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBAn, SABn) can multiplex stored and real–time (transparent mode) data. The DIR determines which bus will receive data when OE is active LOW. In the isolation mode (OE HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

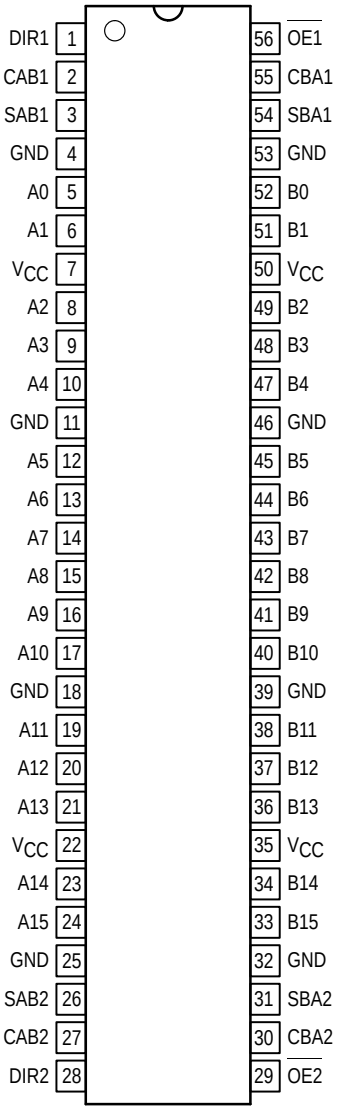
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5.2ns Maximum t_{pd}
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

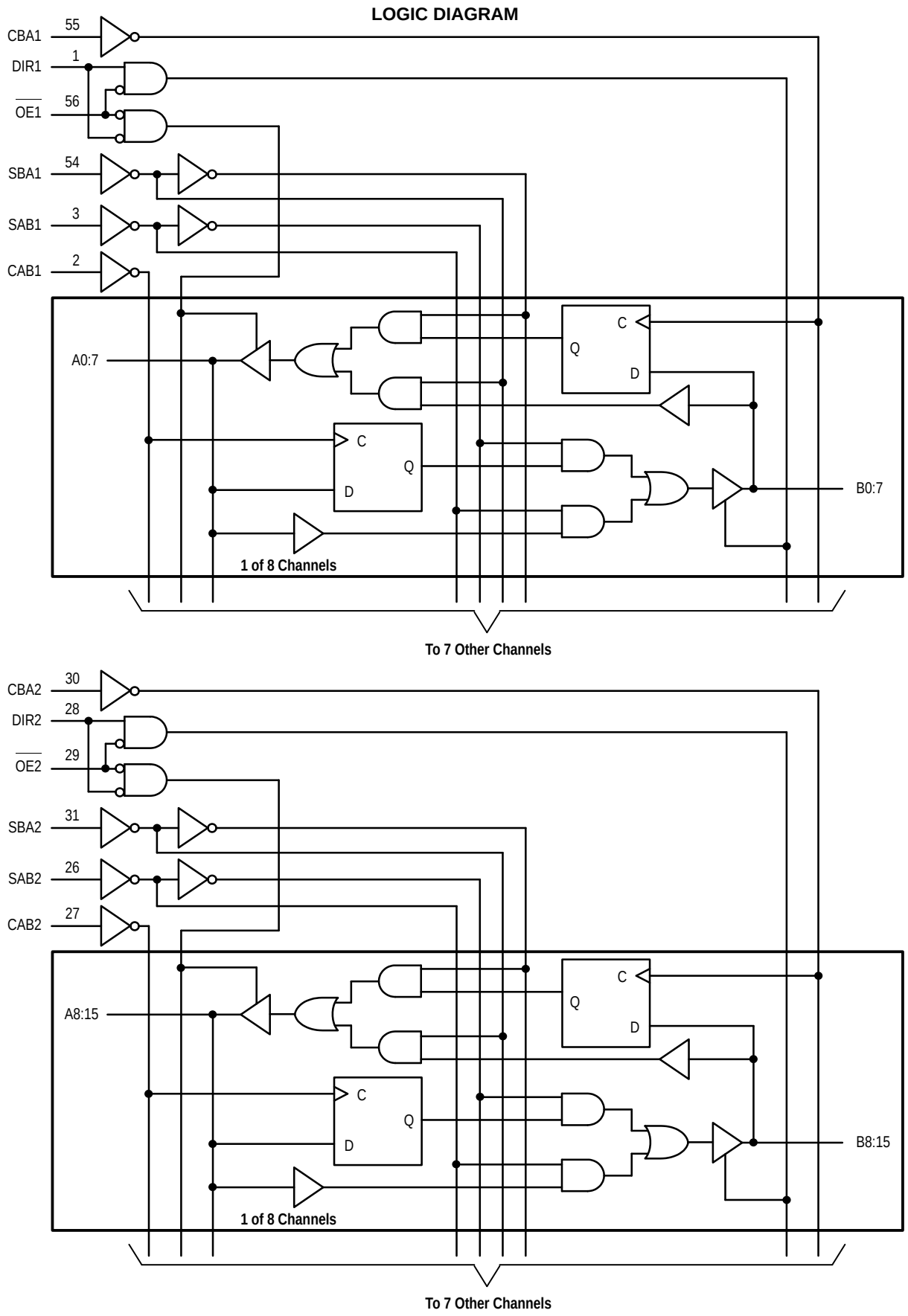
PIN NAMES

Pins	Function
A0–A15	Side A Inputs/Outputs
B0–B15	Side B Inputs/Outputs
CABn, CBAn	Clock Pulse Inputs
SABn, SBAn	Select Control Inputs
DIRn, OEn	Output Enable Inputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

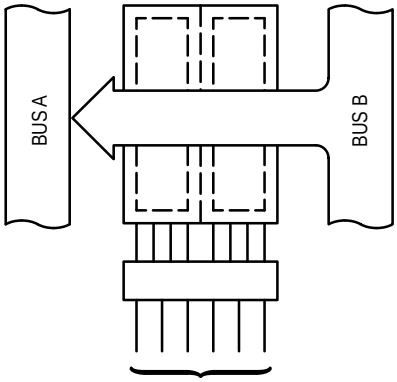

DIR1 1
CAB1 2
SAB1 3
GND 4
A0 5
A1 6
VCC 7
A2 8
A3 9
A4 10
GND 11
A5 12
A6 13
A7 14
A8 15
A9 16
A10 17
GND 18
A11 19
A12 20
A13 21
VCC 22
A14 23
A15 24
GND 25
SAB2 26
CAB2 27
DIR2 28
56 OE1
55 CBA1
54 SBA1
53 GND
52 B0
51 B1
50 VCC
49 B2
48 B3
47 B4
46 GND
45 B5
44 B6
43 B7
42 B8
41 B9
40 B10
39 GND
38 B11
37 B12
36 B13
35 VCC
34 B14
33 B15
32 GND
31 SBA2
30 CBA2
29 OE2

LOGIC DIAGRAM



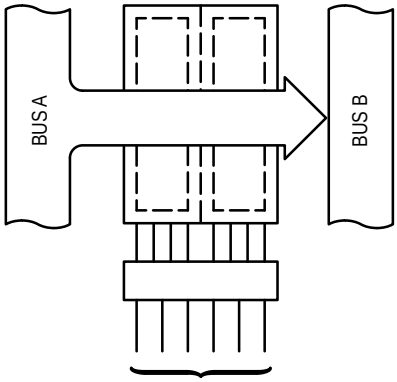
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



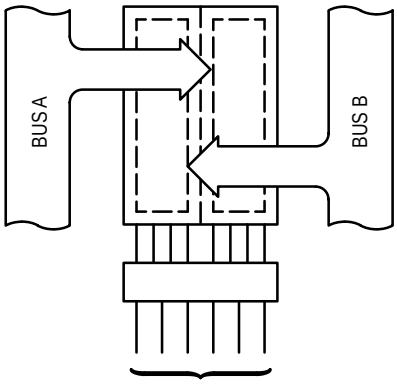
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



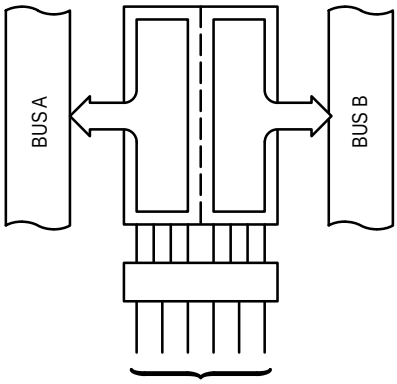
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

Store Data from Bus A, Bus B or Busses A and B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer Storage Data to Bus A or Bus B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

Inputs						Data Ports		Operating Mode
$\overline{OEn}$	DIRn	CABn	CBAn	SABn	SBAn	An	Bn	
H	X					**Input**	**Input**	
		↥	↥	X	X	X	X	Isolation, Hold Storage
		↑	↑	X	X	l h X X	X X l h	Store A and/or B Data
L	H					**Input**	**Output**	
		↥	X*	L	X	L H	L H	Real Time A Data to B Bus
				H	X	X	QA	Stored A Data to B Bus
		↑	X*	L	X	l h	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	QA QA	Clock A Data to B Bus; Store A Data
L	L					**Output**	**Input**	
		X*	↥	X	L	L H	L H	Real Time B Data to A Bus
				X	H	QB	X	Stored B Data to A Bus
		X*	↑	X	L	L H	l h	Real Time B Data to A Bus; Store B Data
				X	H	QB QB	L H	Clock B Data to A Bus; Store B Data

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; X = Don't Care; ↑ = Low–to–High Clock Transition; ↥ = NOT Low–to–High Clock Transition; QA = A input storage register; QB = B input storage register; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3–State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V_{CC} ≤ 3.6V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	2.7V ≤ V_{CC} ≤ 3.6V		0.8	V
V_{OH}	HIGH Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OH} = –100μA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –18mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OL} = 100μA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 12mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 16mA		0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	μA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	μA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		20	μA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (Note 3.; $t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40°C$ to $+85°C$				
			$V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	3	170				MHz
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_s	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5		ns
t_h	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5		ns
t_w	Clock Pulse Width, HIGH or LOW	3	3.0		3.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 4.)			1.0 1.0			ns

3. These AC parameters are preliminary and may be modified prior to release.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

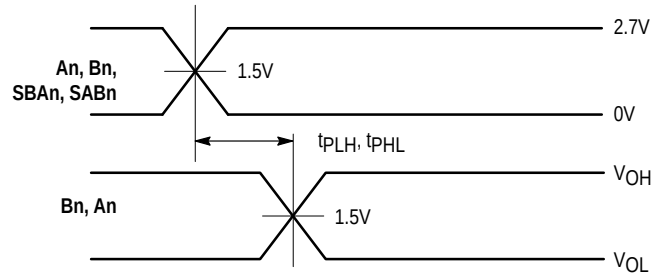
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 5.)	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 5.)	$V_{CC} = 3.3V$, $C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$		0.8		V

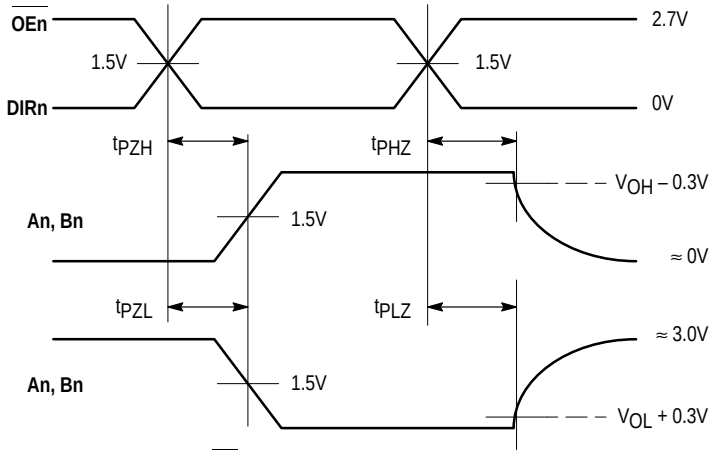
5. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	20	pF

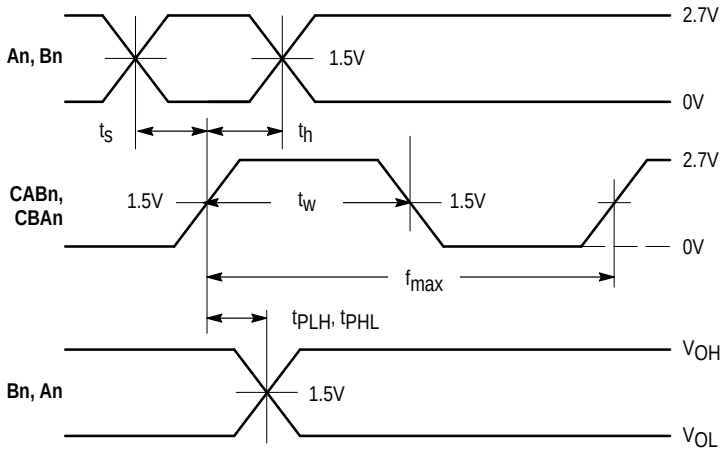


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



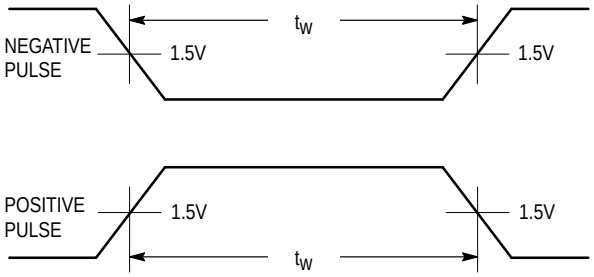
WAVEFORM 2 – $\overline{OE}$/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

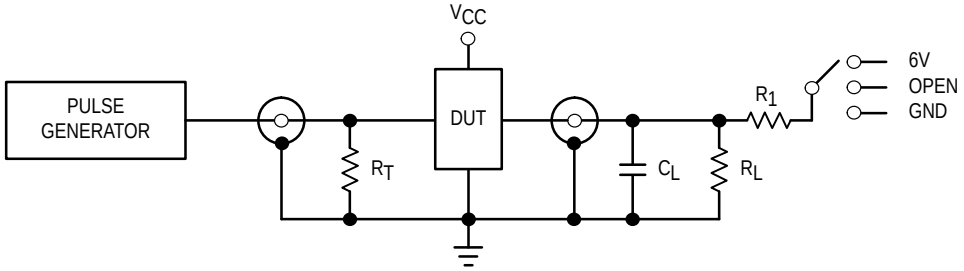
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F$ = 2.5ns, 10% to 90% of 0V to 2.7V

Figure 1. AC Waveforms (continued)



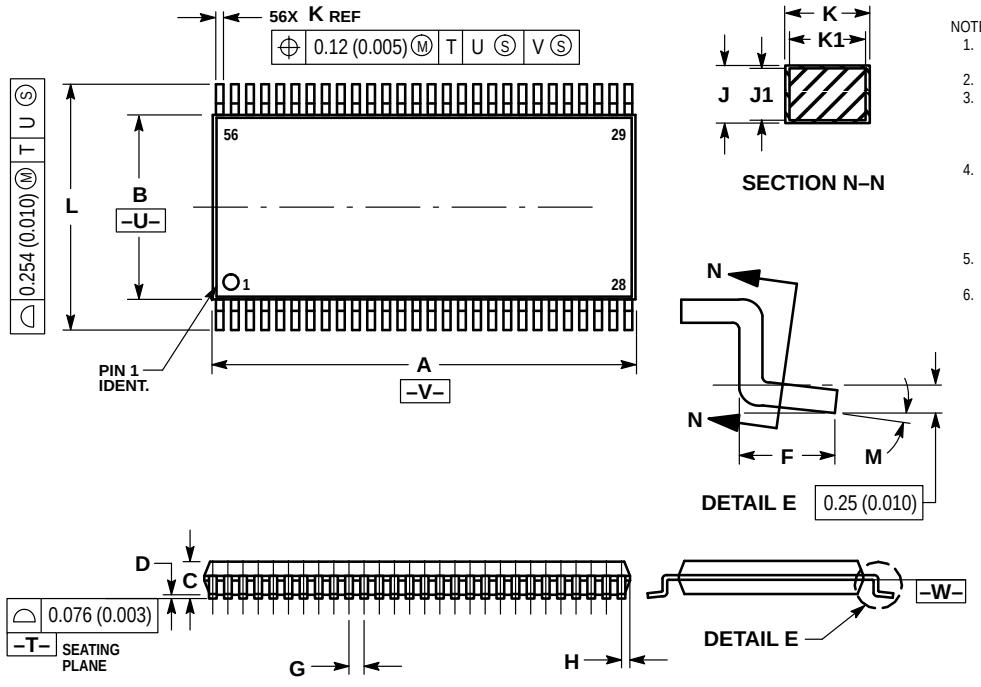
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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