Low-Voltage CMOS Octal Buffer

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX244A

The MC74LCX244A is a high performance, non–inverting octal buffer operating from a 1.65 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $\rm V_I$ specification of 5.5 V allows MC74LCX244A inputs to be safely driven from 5 V devices. The MC74LCX244A is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable (\overline{OE}) input, when HIGH, disables the output by placing them in a HIGH Z condition.

Features

- Designed for 1.65 to 3.6 V V_{CC} Operation
- 5 V Tolerant Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0 \text{ V}$
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA)
 Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
 - ♦ Human Body Model >2000 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



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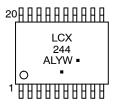




TSSOP-20 DT SUFFIX CASE 948E

QFN20 MN SUFFIX CASE 485CB

MARKING DIAGRAMS



TSSOP-20



QFN20 - 485CB

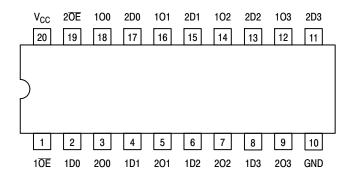
A = Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.



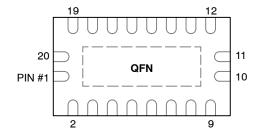


Figure 1. Pinouts: 20-Lead (Top View)

PIN NAMES

PINS	FUNCTION
nOE	Output Enable Inputs
1Dn, 2Dn	Data Inputs
10n, 20n	3-State Outputs

TRUTH TABLE

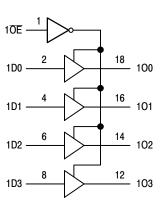
INP	UTS	OUTPUTS
1 <u>0E</u> 2 <u>0E</u>	1Dn 2Dn	10n, 20n
L	L	L
L	Н	Н
Н	Х	Z

H = High Voltage Level

L = Low Voltage Level

Z = High Impedance State X = High or Low Voltage Level and Transitions are Acceptable

For I_{CC} reasons, DO NOT FLOAT Inputs



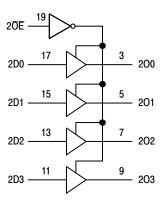


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
VI	DC Input Voltage (Note 1)		-0.5 to +6.5	V
Vo	DC Output Voltage (Note 1) Active-Mode (High o	r Low State)	-0.5 to V _{CC} + 0.5	V
	Tri-	-State Mode	-0.5 to +6.5	
	Power-Down Mode	(V _{CC} = 0 V)	-0.5 to +6.5	
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA
l _{ok}	DC Output Diode Current	/ _{OUT} < GND	-50	mA
Io	DC Output Source/Sink Current		±50	mA
I _{CC}	DC Supply Current Per Supply Pin		±100	mA
I _{GND}	DC Supply Current Per Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating Oxygen Inc	lex: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}		Body Model evice Model	> 2000 N/A	V
I _{LATCHUP}	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

- 2. HBM tested to EIA/JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

 3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Тур	Max	Unit	
V _{CC}	Supply Voltage Operating		1.65	3.3	3.6	V
	Data Retention Only		1.5	3.3	3.6	
VI	Digital Input Voltage		0	_	5.5	V
Vo	Output Voltage Active Mode (High or Low State)		0	_	V _{CC}	V
	Tri-State Mode		0	_	5.5	
	Power Down Mode (V _{CC} = 0 V)		0	_	5.5	
T _A	Operating Free-Air Temperature		-40	_	+125	°C
t _r , t _f	Input Transition Rise or Fall Rate V_I = from 0.8 V to 2.0 V, V_{CC} = 3.0 V		0	=	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

				$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$		
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Min	Max	Unit
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V _{CC}	-	0.65 x V _{CC}	-	V
			2.3 to 2.7	1.7	-	1.7	_	
			2.7 to 3.6	2.0	-	2.0	_	
V _{IL}	Low-Level Input Voltage		1.65 to 1.95	-	0.35 x V _{CC}	-	0.35 x V _{CC}	V
			2.3 to 2.7	-	0.7	-	0.7	
			2.7 to 3.6	-	0.8	-	0.8	
V _{OH}	High-Level	$V_I = V_{IH}$ or V_{IL}						V
	Output Voltage	I _{OH} = -100 μA	1.65 to 3.6	V _{CC} - 0.2	-	V _{CC} - 0.2	-	
		I _{OH} = -4 mA	1.65	1.2	-	1.2	-	
		I _{OH} = -8 mA	2.3	1.8	-	1.8	-	
		I _{OH} = -12 mA	2.7	2.2	-	2.2	_	
		I _{OH} = -16 mA	3.0	2.4	-	2.4	_	
		I _{OH} = -24 mA	3.0	2.2	-	2.2	-	
V _{OL}	Low-Level	$V_I = V_{IH} \text{ or } V_{IL}$						V
	Output Voltage	I _{OL} = 100 μA	1.65 to 3.6	_	0.2	_	0.2	
		I _{OL} = 4 mA	1.65	_	0.45	_	0.45	
		I _{OL} = 8 mA	2.3	-	0.6	-	0.6	
		I _{OL} = 12 mA	2.7	-	0.4	-	0.4	
		I _{OL} = 16 mA	3.0	_	0.4	_	0.4	
		I _{OL} = 24 mA	3.0	-	0.55	-	0.6	
l _l	Input Leakage Current	V _I = 0 to 5.5 V	3.6	-	±5.0	-	±5.0	μΑ
l _{OZ}	3-State Output Leakage Current	$V_I = V_{IH} \text{ or } V_{IL},$ $V_O = 0 \text{ V to } 5.5 \text{ V}$	3.6	-	±5.0	-	±5.0	μΑ
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V or V _O = 5.5 V	0	-	10	-	20	μΑ
Icc	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	-	10	-	10	μΑ
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6 V	2.3 to 3.6	-	500	-	500	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

				T _A = -40°	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		C to +125°C	
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, D to O	See Figures 3 and 4	1.65 to 1.95	-	10.3	-	10.3	ns
			2.3 to 2.7	-	7.8	-	7.8	
			2.7	-	7.5	-	7.5	
			3.0 to 3.6	-	6.5	-	6.5	
t _{PZH} , t _{PZL}	Output Enable Time, OE to O	See Figures 3 and 4	1.65 to 1.95	-	13.0	-	13.0	ns
			2.3 to 2.7	-	10.0	-	10.0	
			2.7	-	9.0	-	9.0	
			3.0 to 3.6	-	8.0	-	8.0	
t _{PHZ} , t _{PLZ}	Output Disable Time, OE to O	See Figures 3 and 4	1.65 to 1.95	-	11.0	-	11.0	ns
			2.3 to 2.7	-	8.4	-	8.4	
			2.7	-	8.0	-	8.0	
			3.0 to 3.6	-	7.0	-	7.0	
t _{OSHL} , t _{OSLH}	Output to Output Skew		1.65 to 1.95	-	-	-	-	ns
			2.3 to 2.7	-	-	-	-	
			2.7	-	-	-	-	
			3.0 to 3.6	-	1.0	-	1.0	

DYNAMIC SWITCHING CHARACTERISTICS

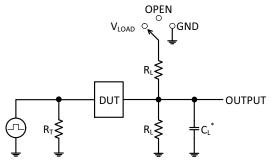
				T _A = +25°C			
Symbol	Parameter	Test Condition	V _{CC} (V)	Min	Тур	Max	Unit
V _{OLP}	Dynamic LOW Peak Voltage	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	-	0.8	-	V
	(Note 4)	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	2.5	-	0.6	-	
V _{OLV}	Dynamic LOW Valley Voltage	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	_	-0.8	-	V
	(Note 4)	$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$	2.5	_	-0.6	-	

^{4.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T _A = 25°C)	Unit
C _{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C _{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	25	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

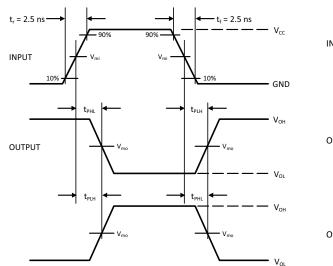


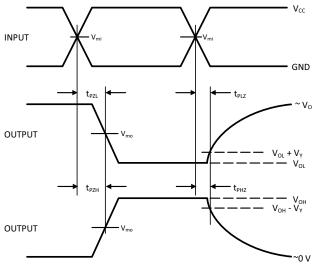
Test Switch Position t_{PLH} / t_{PHL} Open V_{LOAD}

 C_L includes probe and jig capacitance

 R_T is Z_{OUT} of pulse generator (typically 50 Ω) f = 1 MHz

Figure 3. Test Circuits





V _{CC} , V	R_L,Ω	C _L , pF	V_{LOAD}	V _{mi} , V	V _{mo} , V	V _Y , V
1.65 to 1.95	500	30	2 x V _{CC}	V _{CC} /2	V _{CC} /2	0.15
2.3 to 2.7	500	30	2 x V _{CC}	V _{CC} /2	V _{CC} /2	0.15
2.7	500	50	6 V	1.5	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	1.5	0.3

Figure 4. Switching Waveforms

ORDERING INFORMATION

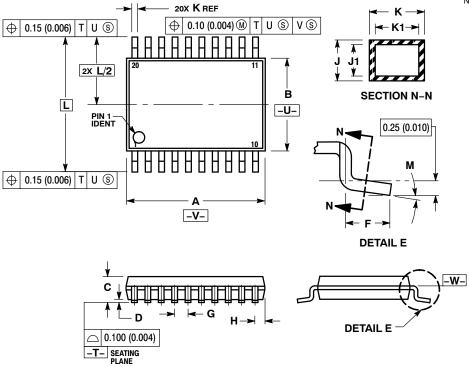
Device	Package	Shipping [†]
MC74LCX244ADTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC74LCX244AMN2TWG (Contact ON Semiconductor)	QFN20, 2.5x3.5 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

PACKAGE DIMENSIONS

TSSOP-20 CASE 948E ISSUE D



NOTES:

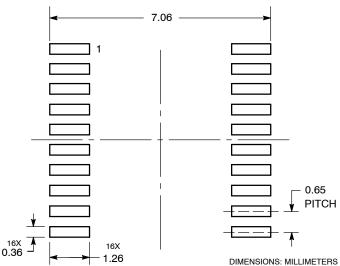
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.

- MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
- CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE -W-.

	PETERIMINED AT DATOM FEAME -W						
	MILLIN	IETERS	INC	HES			
DIM	MIN	MAX	MIN	MAX			
Α	6.40	6.60	0.252	0.260			
В	4.30	4.50	0.169	0.177			
С		1.20		0.047			
D	0.05	0.15	0.002	0.006			
F	0.50	0.75	0.020	0.030			
G	0.65	BSC	0.026 BSC				
Н	0.27	0.37	0.011	0.015			
J	0.09	0.20	0.004	0.008			
J1	0.09	0.16	0.004	0.006			
K	0.19	0.30	0.007	0.012			
K1	0.19	0.25	0.007	0.010			
L	6.40		0.252 BSC				
M	n٥	gο	n٥	g٥			

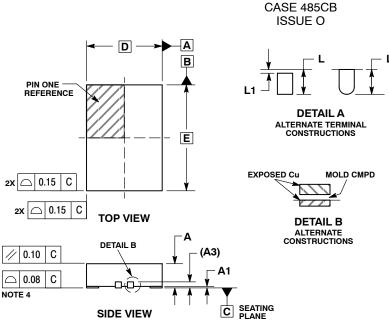
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

QFN20, 2.5x3.5, 0.4P



0.10 C A B

E2

 Φ

0.10 C A B

20X b

0.10 C A B

0.05 C NOTE 3

Ф

D2

BOTTOM VIEW

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20X I

DETAIL A

е

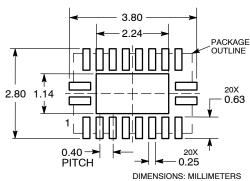
e/2

NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
 COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS.

	MILLIMETERS				
DIM	MIN	MAX			
Α	0.80	1.00			
A1	0.00	0.05			
A3	0.20	REF			
b	0.15 0.2				
D	2.50	BSC			
D2	0.90	1.10			
Е	3.50	BSC			
E2	2.00	2.20			
е	0.40	BSC			
L	L 0.35 0.4				
14		0.15			

SOLDERING FOOTPRINT*



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