

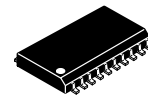
Octal D-Type Flip-Flop with 3-State Outputs

The MC74LVX574 is an advanced high speed CMOS octal flip-flop with 3-state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8-bit D-type flip-flop is controlled by a clock pulse input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

- High Speed: $t_{PD} = 8.5\text{ns}$ (Typ) at $V_{CC} = 3.3\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8\text{V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

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MC74LVX574
LVX
LOW-VOLTAGE CMOS


DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-04



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

PIN NAMES

Pins	Function
\overline{OE}	Output Enable Input
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	3-State Latch Outputs

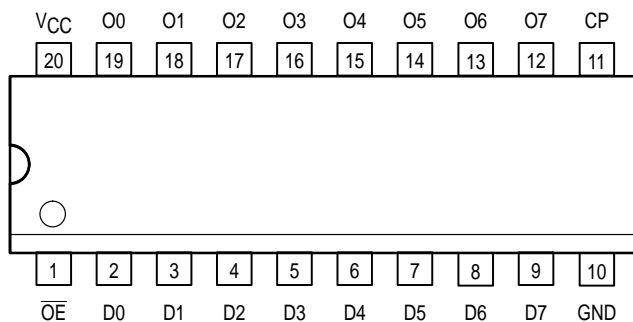


Figure 1. 20-Lead Pinout (Top View)

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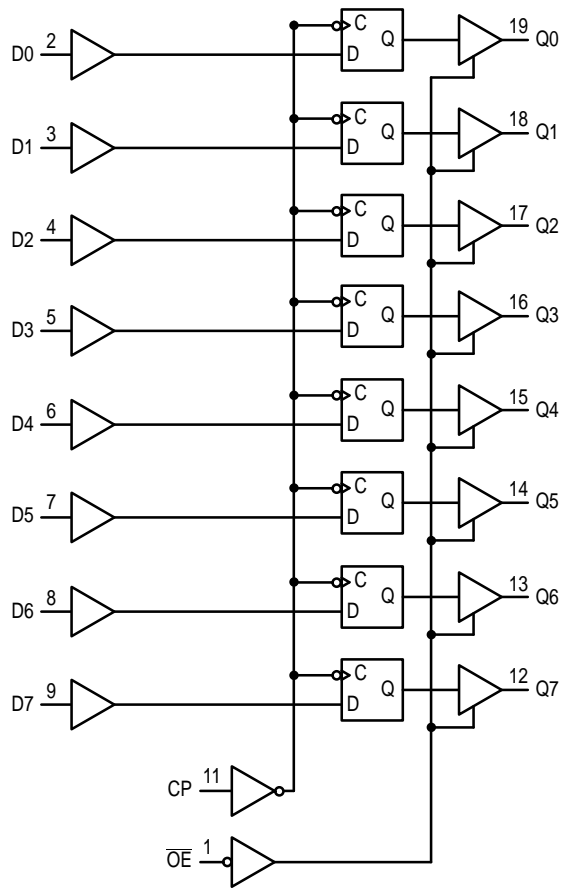


Figure 2. Logic Diagram

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}	CP	D	Q
L	\nearrow	H	H
L	\searrow	L	L
L	L, H, \nearrow , \searrow	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage	-0.5 to +7.0	V
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IJK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V _{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50μA I _{OH} = -50μA I _{OH} = -4mA	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I _{in}	Input Leakage Current	V _{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I _{oZ}	Maximum Three-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.25		±2.5	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{\text{CC}} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	60 45	115 60		50 40		ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	80 50	125 75		65 45		
t_{PLH} , t_{PHL}	Propagation Delay CP to O	$V_{\text{CC}} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		9.2 11.5	14.5 18.0	1.0 1.0	17.5 21.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.5 11.0	13.2 16.7	1.0 1.0	15.5 19.0	
t_{PZL} , t_{PZH}	Output Enable Time OE to O	$V_{\text{CC}} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		9.8 11.4	15.0 18.5	1.0 1.0	18.5 22.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.2 10.7	12.8 16.3	1.0 1.0	15.0 18.5	
t_{PLZ} , t_{PHZ}	Output Disable Time OE to O	$V_{\text{CC}} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		12.1	19.1	1.0	22.0	ns
		$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		11.0	15.0	1.0	17.0	
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note NO TAG)	$V_{\text{CC}} = 2.7\text{V}$ $V_{\text{CC}} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		28				pF

- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{\text{CC(OPR)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{in}} + I_{\text{CC}}/8$ (per latch). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{\text{PD}} \cdot V_{\text{CC}}^2 \cdot f_{\text{in}} + I_{\text{CC}} \cdot V_{\text{CC}}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{\text{CC}} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	T _A = 25°C		T _A = -40 to 85°C	Unit
			Typ	Limit	Limit	
t _{w(h)}	Minimum Pulse Width, CP	V _{CC} = 2.7V V _{CC} = 3.3 ±0.3V		6.5 5.0	7.5 5.0	ns
t _{su}	Minimum Setup Time, D to CP	V _{CC} = 2.7V V _{CC} = 3.3 ±0.3V		5.0 3.5	5.0 3.5	ns
t _h	Minimum Hold Time, D to CP	V _{CC} = 2.7V V _{CC} = 3.3 ±0.3V		1.5 1.5	1.5 1.5	ns

SWITCHING WAVEFORMS

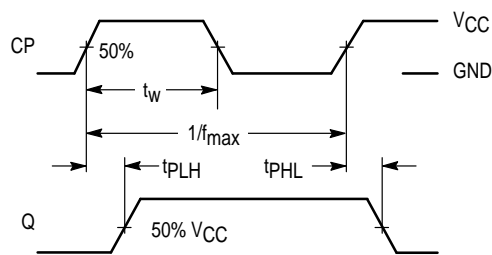


Figure 3.

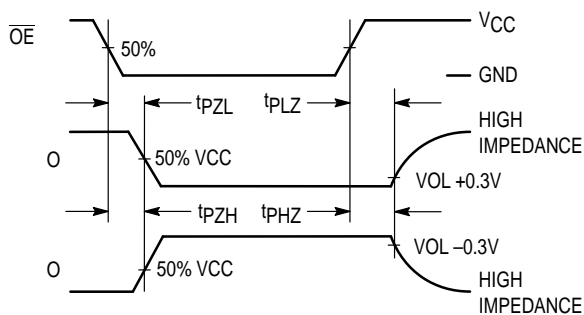


Figure 4.

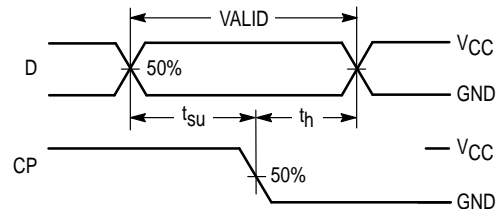
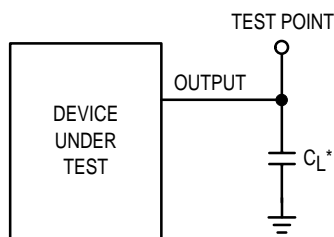


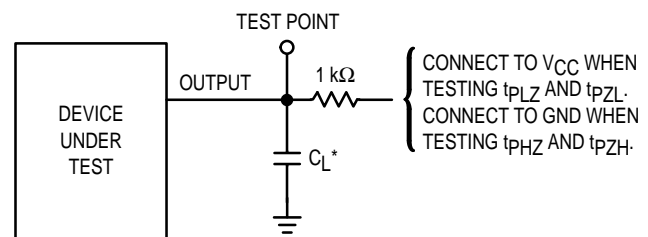
Figure 5.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 6. Propagation Delay Test Circuit



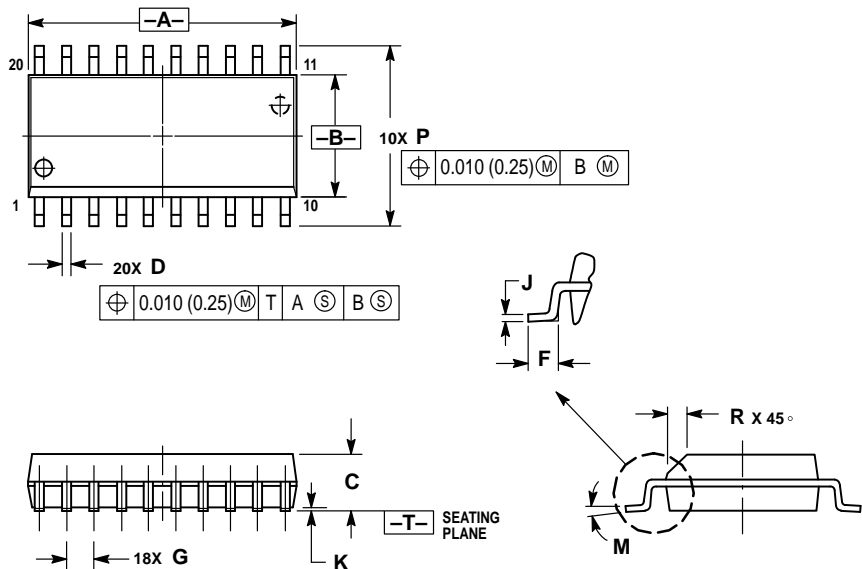
* Includes all probe and jig capacitance

Figure 7. Three-State Test Circuit

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OUTLINE DIMENSIONS

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 PLASTIC SOIC PACKAGE
 CASE 751D-04
 ISSUE E

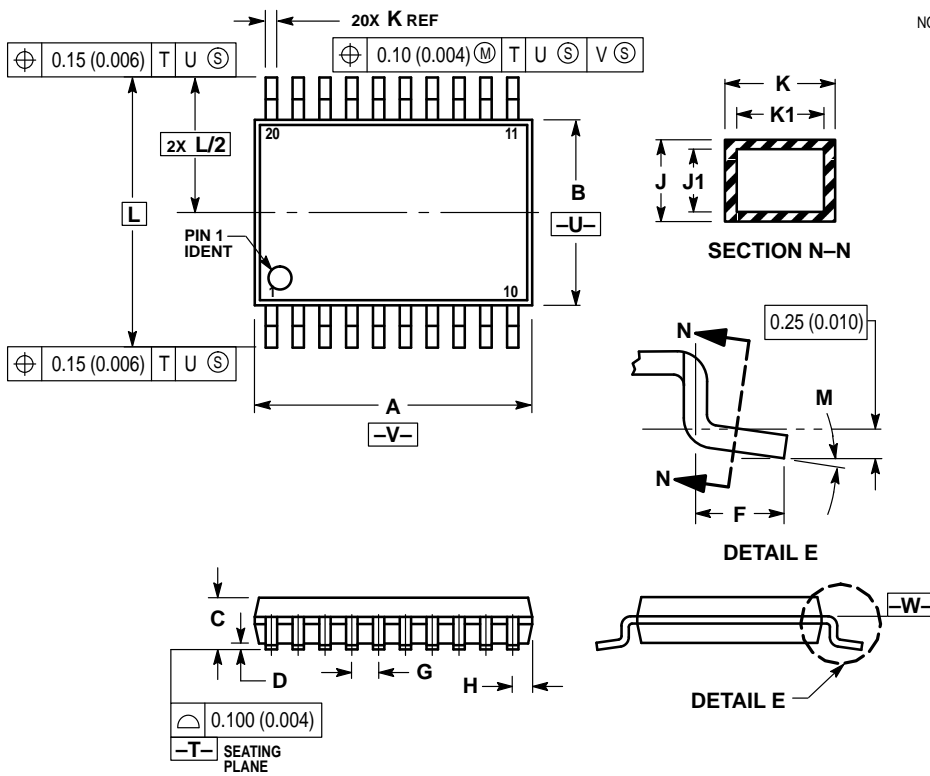


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS


DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948E-02
 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74LVX574

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