

# MC74VHC541

## Octal Bus Buffer

The MC74VHC541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC541 is a noninverting type. When either  $\overline{OE1}$  or  $\overline{OE2}$  are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 3.7\text{ns}$  (Typ) at  $V_{CC} = 5.0\text{ V}$
- Low Power Dissipation:  $I_{CC} = 4\ \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.2\text{ V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

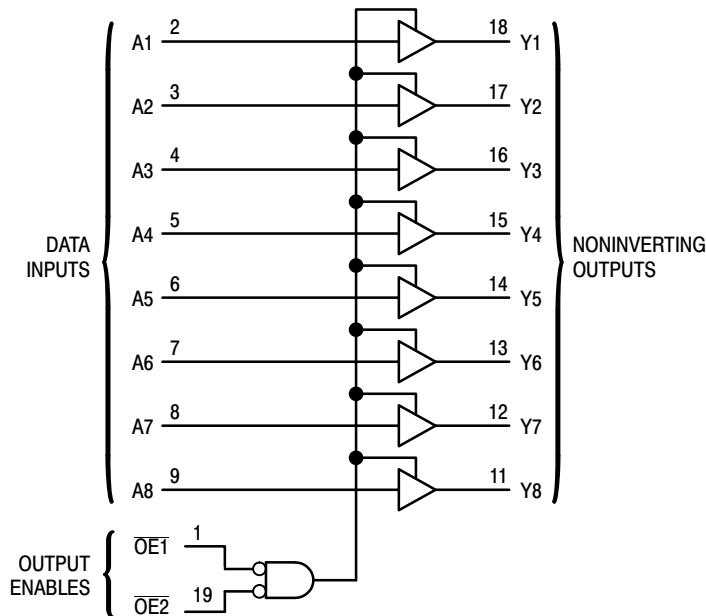
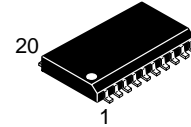


Figure 1. Logic Diagram

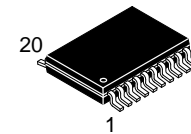


ON Semiconductor®

<http://onsemi.com>



SOIC-20WB  
SUFFIX DW  
CASE 751D



TSSOP-20  
SUFFIX DT  
CASE 948E

### PIN ASSIGNMENT

$\overline{OE1}$	1	20	$V_{CC}$
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

### FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

# MC74VHC541

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage	- 0.5 to + 7.0	V
$V_{out}$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	- 20	mA
$I_{OK}$	Output Diode Current	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	5.5	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$T_A = 25^\circ\text{C}$			$T_A = -55 \text{ to } 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$			1.50 $V_{CC} \times 0.7$		V
$V_{IL}$	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 $V_{CC} \times 0.3$		0.50 $V_{CC} \times 0.3$	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4\text{mA}$ $I_{OH} = -8\text{mA}$	3.0 4.5	2.58 3.94			2.48 3.80		
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 4\text{mA}$ $I_{OL} = 8\text{mA}$	3.0 4.5			0.36 0.36	0.44 0.44		
$I_{in}$	Maximum Input Leakage Current	$V_{in} = 5.5V$ or GND	0 to 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	Maximum 3-State Leakage Current	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	5.5			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74VHC541

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -55 \text{ to } 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.0	7.0	1.0	8.5	ns
		$C_L = 50\text{pF}$		7.5	10.5	1.0	12.0	
$t_{PZL}$ , $t_{PZH}$	Output Enable Time, $\overline{\text{OE}}$ to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.8	10.5	1.0	12.5	ns
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		9.3	14.0	1.0	16.0	
$t_{PLZ}$ , $t_{PHZ}$	Output Disable Time, $\overline{\text{OE}}$ to Y	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$		4.7	7.2	1.0	8.5	ns
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		6.2	9.2	1.0	10.5	
$t_{OSLH}$ , $t_{OSHL}$	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	ns
		(Note 1)						
$t_{OSLH}$ , $t_{OSHL}$	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 50\text{pF}$			1.0		1.0	ns
		(Note 1)						
$C_{in}$	Maximum Input Capacitance			4	10		10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High Impedance State)			6				pF

Symbol	Parameter	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$		Unit
		Min	Max	
$C_{PD}$	Power Dissipation Capacitance (Note 2)		18	pF

- Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ .
- $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$  (per bit).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ , $C_L = 50\text{pF}$ , $V_{CC} = 5.0\text{V}$ )

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.9	1.2	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.9	-1.2	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		3.5	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		1.5	V

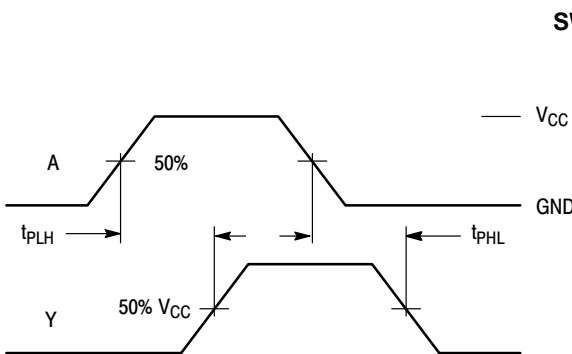


Figure 2.

## SWITCHING WAVEFORMS

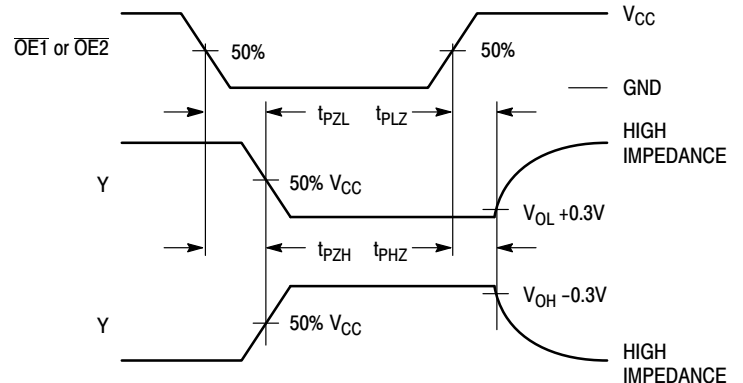
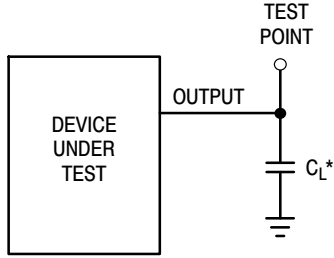


Figure 3.

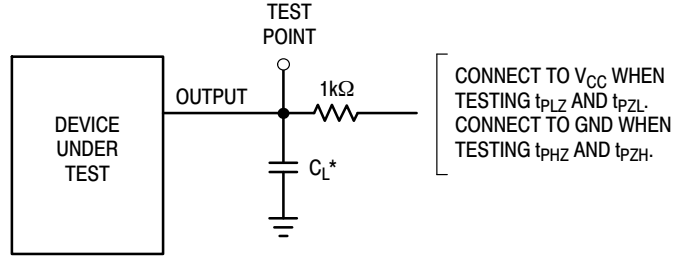
# MC74VHC541

## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 4.



\*Includes all probe and jig capacitance

Figure 5.

CONNECT TO  $V_{CC}$  WHEN TESTING  $t_{PLZ}$  AND  $t_{PZL}$ .  
CONNECT TO GND WHEN TESTING  $t_{PHZ}$  AND  $t_{PZH}$ .

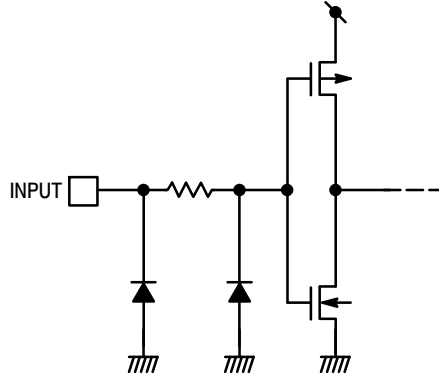


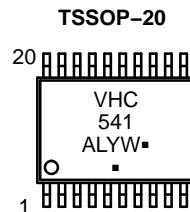
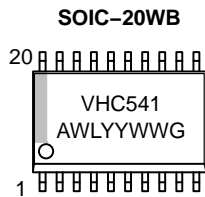
Figure 6. Input Equivalent Circuit

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC541DWR2G	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHC541DTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74VHC541DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

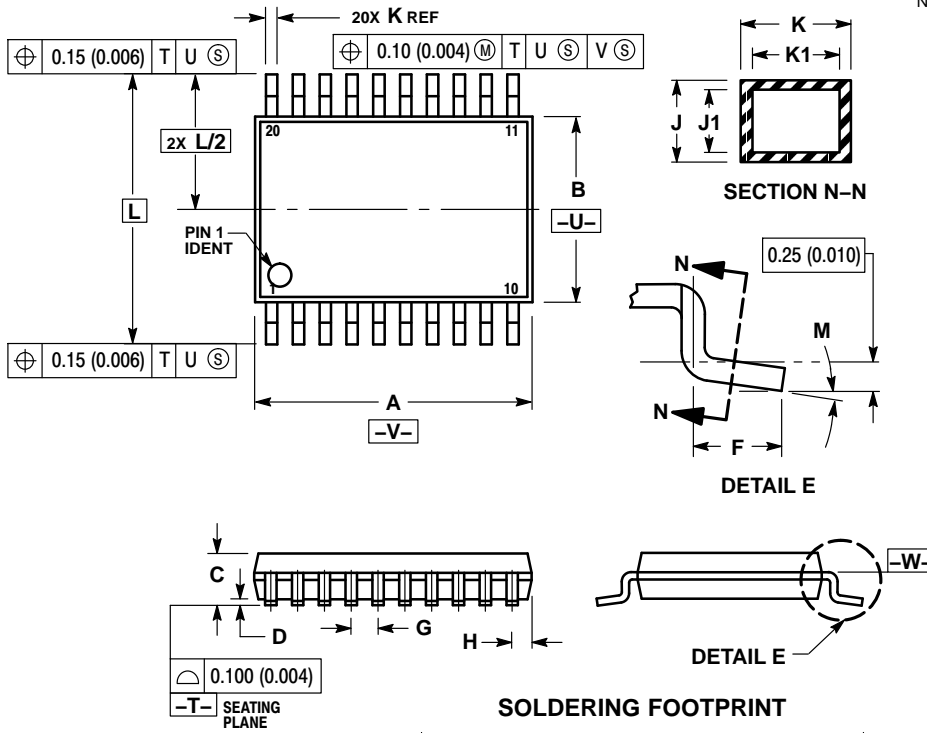


A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

# MC74VHC541

## PACKAGE DIMENSIONS

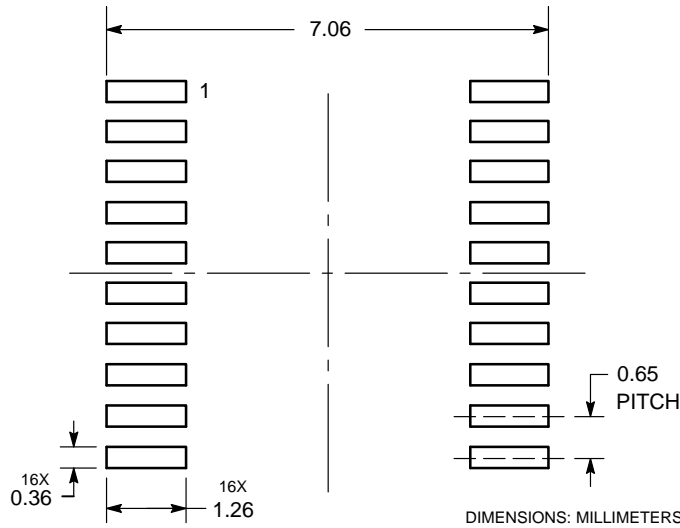
TSSOP-20  
CASE 948E-02  
ISSUE C



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

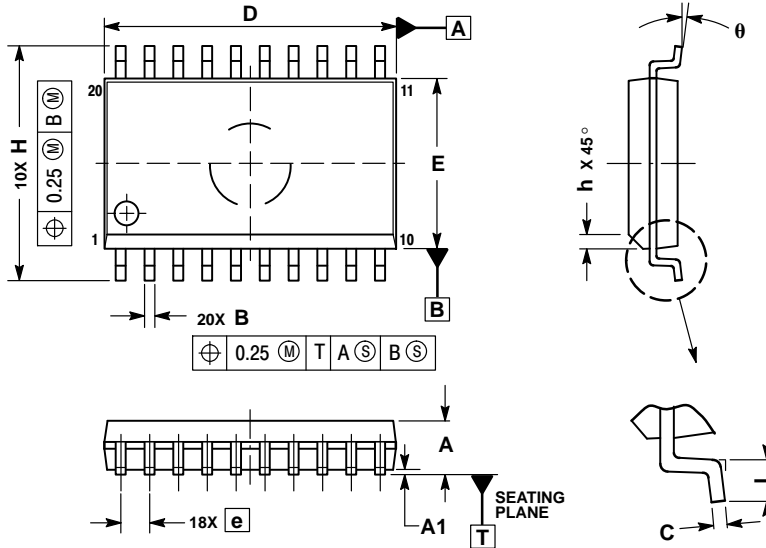
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



# MC74VHC541

## PACKAGE DIMENSIONS

SOIC-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE G



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative