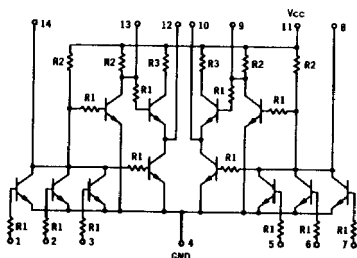


DUAL 3-INPUT BUFFERS NON-INVERTING

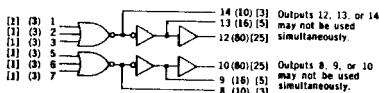
PLASTIC mW MRTL MC700P/800P series

MC788P • MC888P



TYPICAL RESISTANCE
VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.

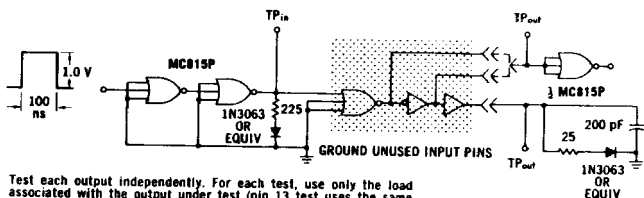


$$14 = 1 + 2 + 3 \quad 13 = 1 + 2 + 3 \quad 12 = 1 + 2 + 3$$

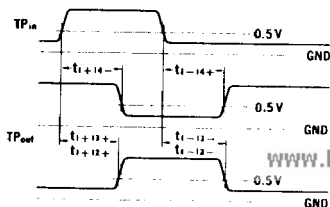
NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

$t_{pd} = 24 \text{ ns}$
 $P_o = 145 \text{ mW (Input Low)}$
 $56 \text{ mW (Inputs Low)}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.



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ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC888P Test Limits	Unit	MC788P Test Limits	Unit	TEST VOLTAGE	End												
			0°C	Min	+25°C	Min	+75°C	Max	Max	Max	Max	+15°C	Min	+25°C	Min	+55°C	Max	Max	Max	Max
			Max	Min	Max	Min	Max	Min	Max	Max	Max	Max	Min	Max	Min	Max	Min	Max	Max	Max
			Min	Max	Min	Max	Min	Max	Max	Max	Max	Min	Max	Min	Max	Min	Max	Max	Max	Max
			1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
			μA	μA	μA	mAdc	mAdc	mAdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
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			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
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			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc	mVdc
			mVdc																	

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}