ABOV SEMICONDUCTOR Co., Ltd.
LIGHT-TO-DIGITAL CONVERTER

MC8121

Data Sheet (REV.1.61)

REVISION HISTORY

REVISION 0.0 (June 7, 2012)

- Initial Version

REVISION 0.1 (July 4, 2012)

- Combine MC8111 & MC8121
- Correct register description

REVISION 0.2 (August 6, 2012)

- Add Optical characteristics

REVISION 1.0 (September 24, 2012)

- Change I2C slave address
- Change default values of registers

REVISION 1.1 (October 11, 2012)

- Add characteristics of CH1 PD

REVISION 1.2 (October 18, 2012)

- Add Pinout & Package Dimension

REVISION 1.3 (November 06, 2012)

- Fix ODFN Package Dimension
- Correct device name for MC8121FN

REVISION 1.4 (January 15, 2013)

- Remove MC8111 related contents

REVISION 1.5 (January 22, 2013)

- Fix ID register description

REVISION 1.6 (March 08, 2013)

- Fix electrical characteristics

REVISION 1.61 (May 24, 2013)

- Correct unit notation

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MC8121

Digital Ambient Light Sensor

1. OVERVIEW

1.1 DESCRIPTION

The MC8121 is an advanced digital ambient light sensor (ALS) IC that transforms illuminance (light intensity) to a digital signal output. For ambient light sensing, MC8121 has two opened photodiodes(CH0/CH1). One is an whole ray responding photodiode and the other is a visible ray responding photodiode. The visible ray responding photodiode is coated with Infra Red cut off filter on a CMOS integrated circuit. The photovoltaic responses are converted into digital counter values by two internal ALS ADCs of 16-bit resolution. It closely approximates the human eye spectral response of visible wavelength. The operation voltage ranges from 2.4 to 3.6 volt.

The ALS features are ideal for reducing power consumption and adjusting brightness of display equipments like LCD, PDP, LED, virtual keyboard and portable projector, etc.

1.2 FEATURES

- CMOS technology
- Independently programmable exposure time for ALS CH0 and CH1 ADCs

Ambient Light Sensing

- Convert incident light intensity to digital data
- 16-bit ALS ADC resolution
- Automatic light flickering cancellation supporting
- Block off IR(Infrared) by IR cut off filter coating(CH0)
- Spectral response close to human eye
- Linear ALS response for easy design
- Low dark noise

Additional Features

- I^2C protocol interface
- Low stand-by current, 1uA typical
- Operating range 2.4 ~ 3.6V

1.3 ORDERING INFORMATION

DEVICE NAME	PACKAGE−LEADS	CH0	CH1
MC8121	chip sale	IR cut off filter on wafer	Visible + IR ray
MC8121FN	ODFN 6L	IR cut off filter on wafer	Visible + IR ray

Table 1-1 Ordering Information

1.4 APPLICATIONS

- Cell phone
- Display-equipped portable devices,etc..

1.5 BLOCK DIAGRAM

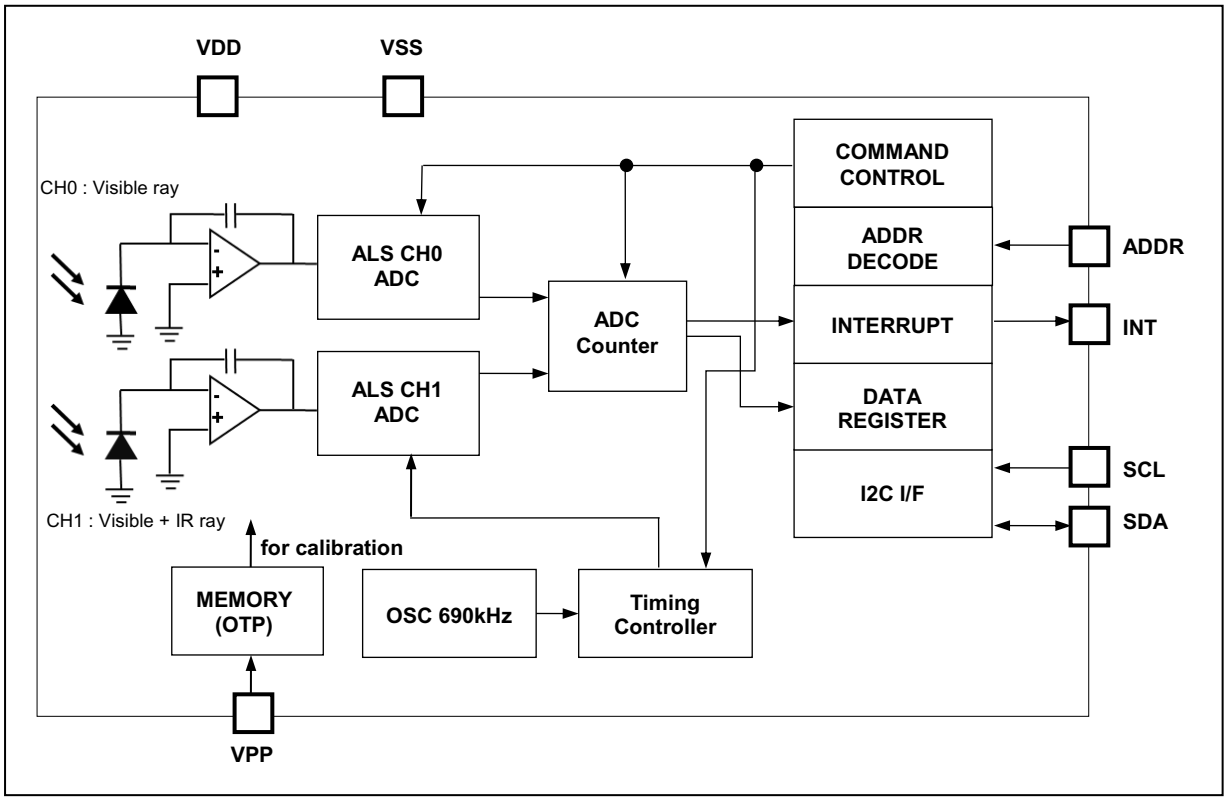


Figure 1-1 Block Diagram of MC8121

1.6 PIN CONFIGURATIONS

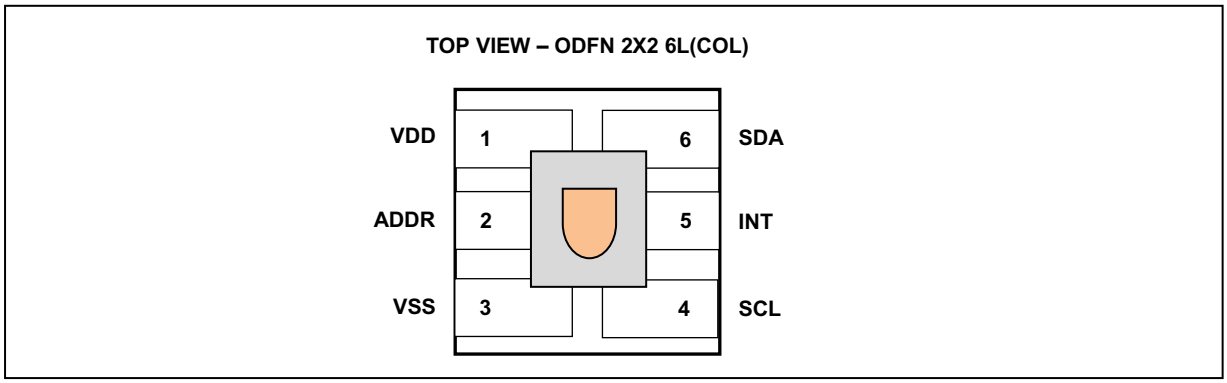
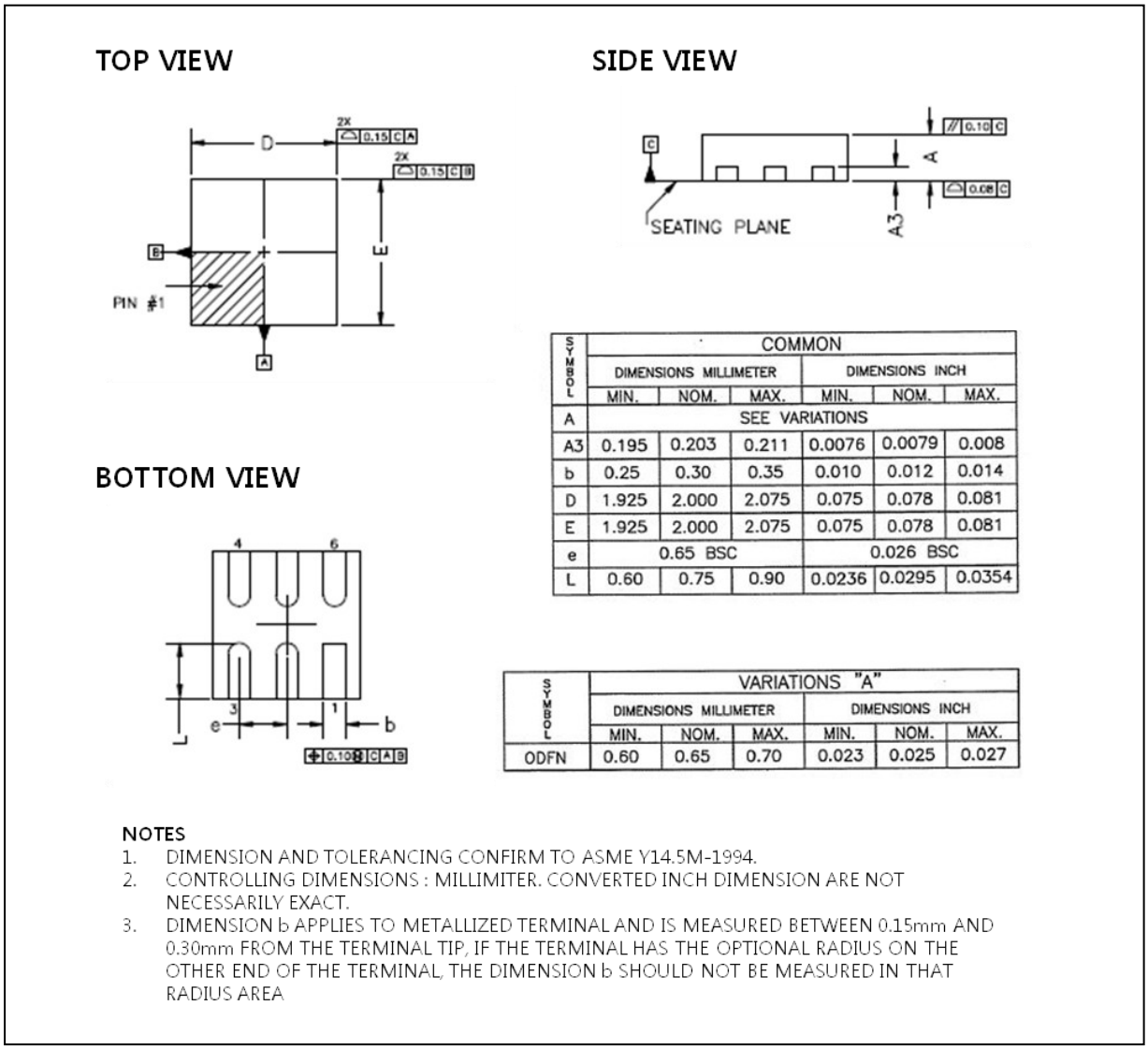


Figure 1-2 Pinout – ODFN 2X2 6L(COL)

1.7 PKG DIMENSION



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATIONS					
A3	0.195	0.203	0.211	0.0076	0.0079	0.008
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.925	2.000	2.075	0.075	0.078	0.081
E	1.925	2.000	2.075	0.075	0.078	0.081
e	0.65 BSC			0.026 BSC		
L	0.60	0.75	0.90	0.0236	0.0295	0.0354

SYMBOL	VARIATIONS "A"					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
ODFN	0.60	0.65	0.70	0.023	0.025	0.027

NOTES
1. DIMENSION AND TOLERANCING CONFIRM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMITER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 1-3 Package Dimension – ODFN 2X2 6L(COL)

1.8 PIN DESCRIPTION

PIN Number	PIN Name	Description	I/O
1	VDD	Power supply : 2.4 to 3.6V	Power
2	ADDR	Address Select	Input
3	VSS	Ground	Power
4	SCL	I^2C Serial Clock Line	Input
5	INT	ALS Interrupt	O(Open Drain)
6	SDA	I^2C Serial Data Line	O(Open Drain)

Table 1-2 Pin Description – ODFN 2X2 6L(COL)

1.9 SLAVE ADDRESS

ADDR	SLAVE ADDRESS
LOW / OPEN	0101_001
HIGH	1010_110

Table 1-3 Slave Address Selection

1.10 ELELCTRICAL CHARACTERISTICS

1.10.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit.	Remark
VDD	Supply voltage	0	4.0	V	
Tstg	Storage temperature range	-40	85	˚C	
VO	Digital ouput voltage range	-0.5	4.0	V	
IO	Digital output current	-1	20	mA	
VHBM	ESD tolerance, Human Body Model		8,000	V	

Table 1-4 Absolute Maximum Ratings

NOTE Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablility.

1.10.2 RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
VDD	Supply voltage	2.4	3.0	3.6	V	
TA	Operating temperature	-40		85	˚C	
VIL	SCL,SDA input low voltage			600	mV	
VIH	SCL,SDA input low voltage	1.4			V	

Table 1-5 Recommended Operating Condition

1.10.3 ELECTRICAL SPECIFICATIONS

(VDD =3.0V, VSS =0V, TA=+25℃±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
V_{DD}	Power Supply	2.4	-	3.6	V	
I_{SLEEP}	Stand-by Current		1	3	uA	I^2C interface enable
I_{DDALS0}	Active Current for ALS CH0		80		uA	
I_{DDALS1}	Active Current for ALS CH1		80		uA	
$I_{DDALS01}$	Active Current for ALS CH0 and CH1			120	uA	
λ_{PCH0}	Peak Sensitivity wavelength of ALS CH0		550		nm	
λ_{PCH1}	Peak Sensitivity wavelength of ALS CH1		850		nm	
f_{OSC}	Internal Oscillator Frequency	552	690	828	kHz	
t_{INT}	ADC Integration/Conversion Time		100	500	ms	16-bit ADC data
V_{OL}	INT,SDA ouput low voltage	0		0.4	V	6mA sink current
$A0_{000L}$	ADC Count Value of CH0 PD (ATIME0 = 06_H, INTR[7]=1)	-	0	2	counts	@0Lux, white color LED
$A0_{001L}$			5		counts	@1Lux, white color LED
$A0_{200L}$		980	1090	1200	counts	@200Lux, white color LED
$A1_{000L}$	ADC Count Value of CH1 PD (ATIME0 = 06_H, INTR[7]=1)	-	0	4	counts	@0Lux, white color LED
$A1_{001L}$			8		counts	@1Lux, white color LED
$A1_{200L}$		1334	1640	1975	counts	@200Lux, white color LED
DF_{ALS0}	Full Scale ALS CH0 ADC Count			65535	counts	
DF_{ALS1}	Full Scale ALS CH1 ADC Count			65535	counts	

Table 1-6 Electrical Specifications

1.10.4 I²C CHARACTERISTICS

The following table and figure show the timing codition of SDA and SCL bus lines for fast mode I²C bus devices. NOTE1.

(VDD =3.0V, VSS =0V, TA=+25℃±10%)

Parameter	Symbol NOTE2	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	us
LOW period of the SCL clock	t_{LOW}	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	0.6	-	us
Setup time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	0.9	us
Data setup time	$t_{SU;DAT}$	100	-	ns
Clock/data fall time	t_F	0	300	ns
Clock/data rise time	t_R	0	300	ns
Setup time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condtion	t_{BUF}	1.3	-	us

Table 1-7 Timing characteristics of I²C

NOTE1 All timing is shown with respect to 30% VDD and 70% VDD.

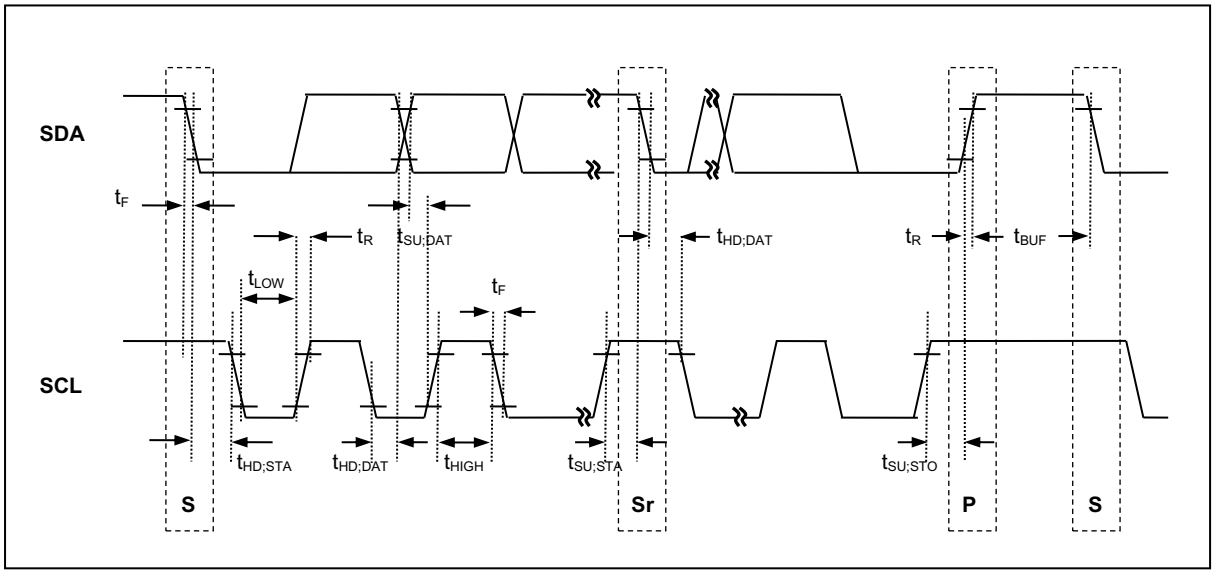


Figure 1-4 Definition of ti rity ming for fast mode devices on the I2C bus

1.10.5 OPTICAL CHARACTERISTICS

A. Spectral response

Spectrum of MC8121 is the below curve by using monochrometer and integrated sphere.

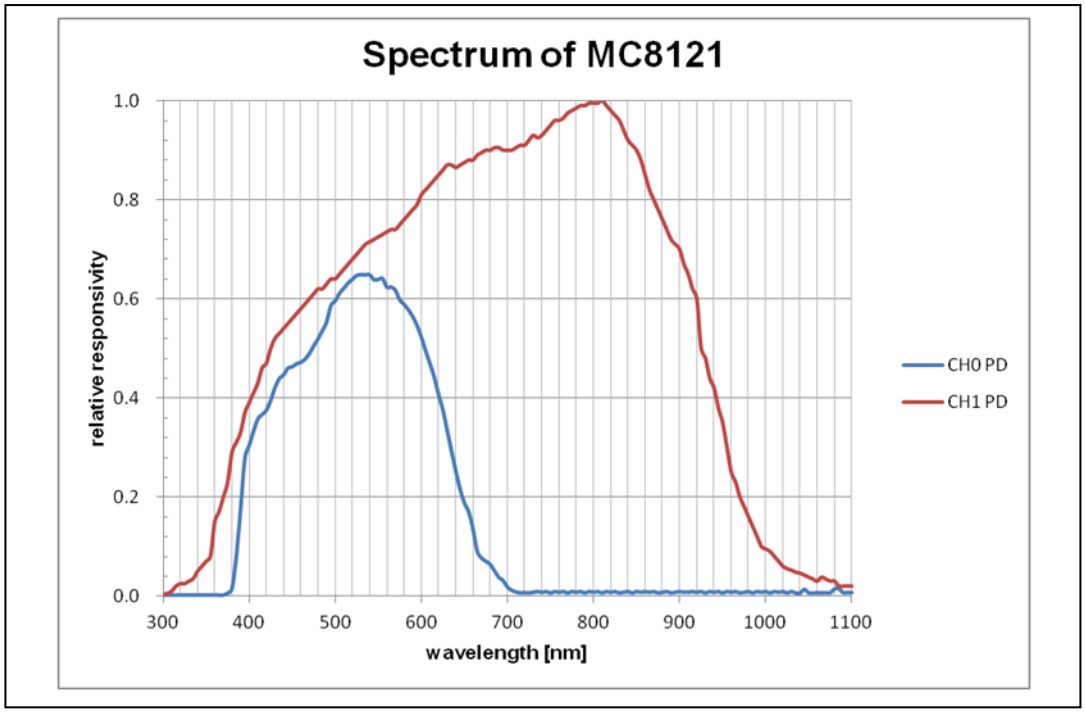


Figure 1-5 Spectral response of MC8121

2. OPERATION

2.1 I²C

2.1.1 OVERVIEW

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I²C interface
- Up to 400kHz data transfer speed
- Support two 7-bit slave address
- Slave operation only

2.1.2 I²C BIT TRANSFER

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

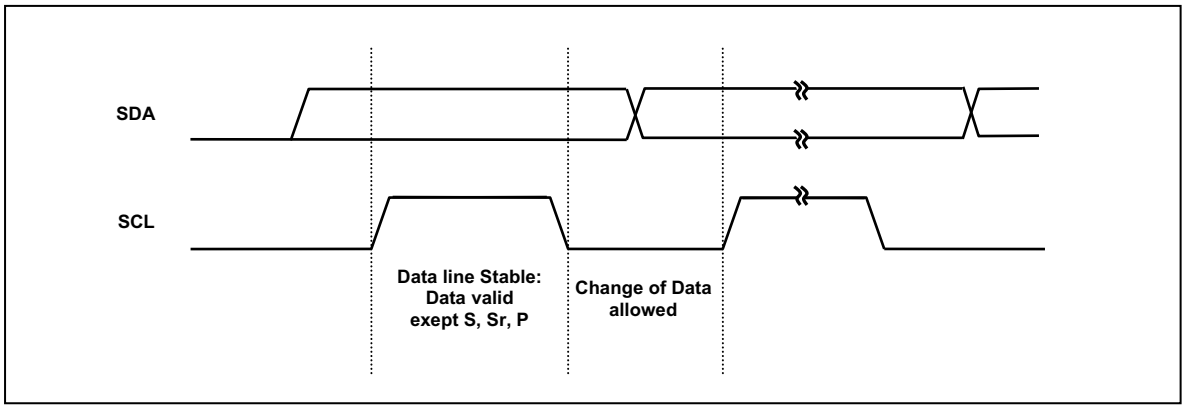


Figure 2-1 Bit Transfer on the I²C-Bus

2.1.3 START / REPEATED START / STOP

One master can issue a START (S) condition to notice other devices connected to the SCL, SDA lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

A high to low transition on the SDA line while SCL is high defines a START (S) condition.

A low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

START and STOP conditions are always generated by a master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

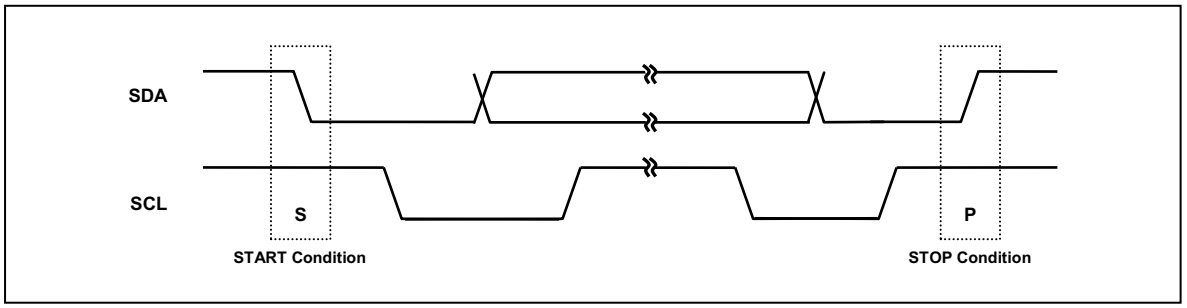


Figure 2-2 START and STOP Condition

2.1.4 DATA TRANSFER

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

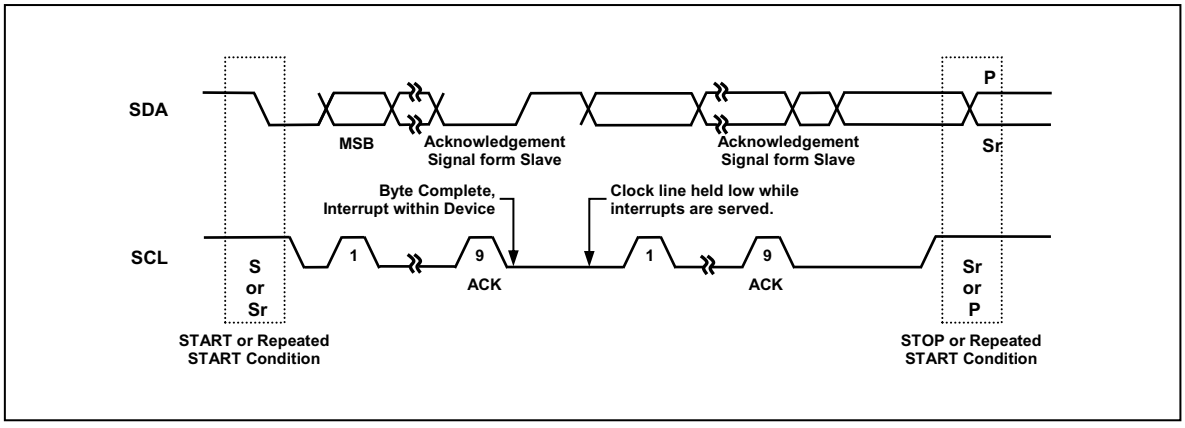


Figure 2-3 STOP or Repeated START Condition

2.1.5 ACKNOWLEDGE

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

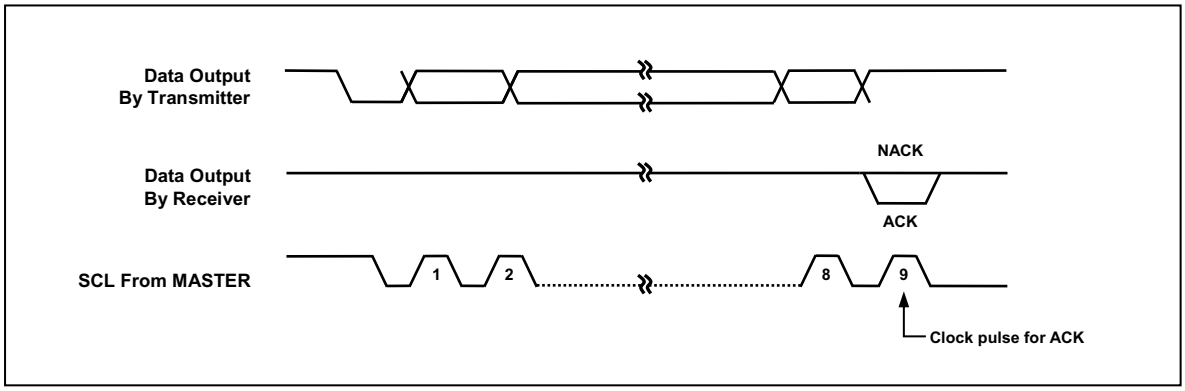


Figure 2-4 Acknowledge on the I²C-Bus

2.1.6 OPERATION

The I²C is byte-oriented serial protocol and data transfer between master and this slave device is initiated by a start condition(S) from master. After start condition, the master sends 7-bit slave address and 1-bit read-write control bit. We call these 8-bit data address packet. The next bytes followed by address packet are all data packet unless another start condition is detected before a stop condition.

The 2nd byte sent from master after address packet with write direction is interpreted as base register or memory address byte. And this base address is incremented only when master transmits more than 2 bytes after start condition because the 2nd byte is register address field.

The MC8121's I²C slave address is configured as "0101001_B" or "1010110_B" according to the input condition of ADDR pin.

2.1.6.1 WRITE PROTOCOL (MASTER TRANSMITTER)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the MC8121 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. The master transmits a number of data to be written and the slave always acknowledges for every data received. To finish transfer the master sends a stop condition regardless of the acknowledgement.

The destination address for incoming data byte increments automatically by one data packet. For example, if master transmits 5 data bytes including a base address(=register address in the following figure) byte and the base address is configured as 00_H, the internal address is defined as 00_H for 1st data byte, 01_H for 2nd data byte, 02_H for 3rd data byte and 03_H for 4th data byte. This applies to Read Protocol also.

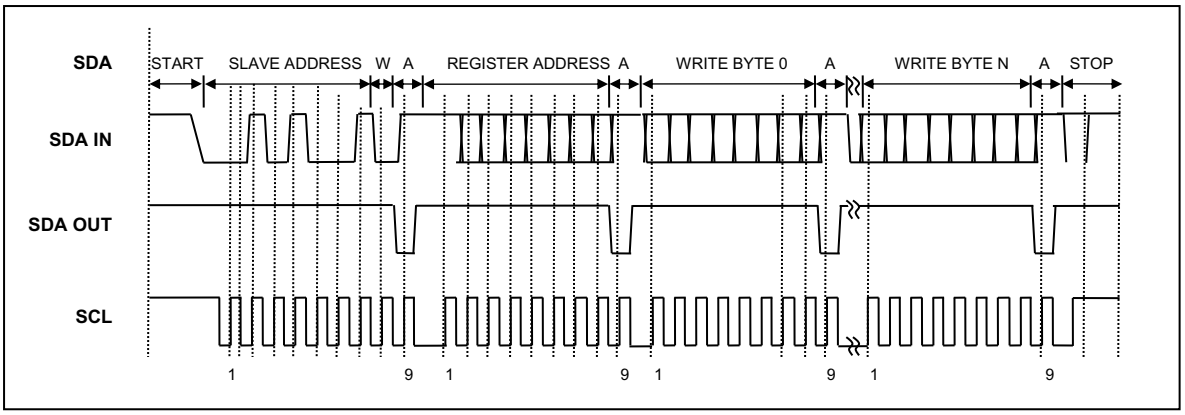


Figure 2-5 I2C Write Protocol

2.1.6.2 READ PROTOCOL (MASTER RECEIVER)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the MC8121 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. To initiate read operations, the master sends repeated start condition and slave address with Read bit. After this address packet, the master reads data bytes until it does not acknowledges. Note that to send a stop condition after receiving last data byte, the master must generate a NACK(not acknowledging) on the last data byte received. Like Write Protocol, the read address increases by 1 after every read byte.

Note that the transfer direction changes in this protocol.

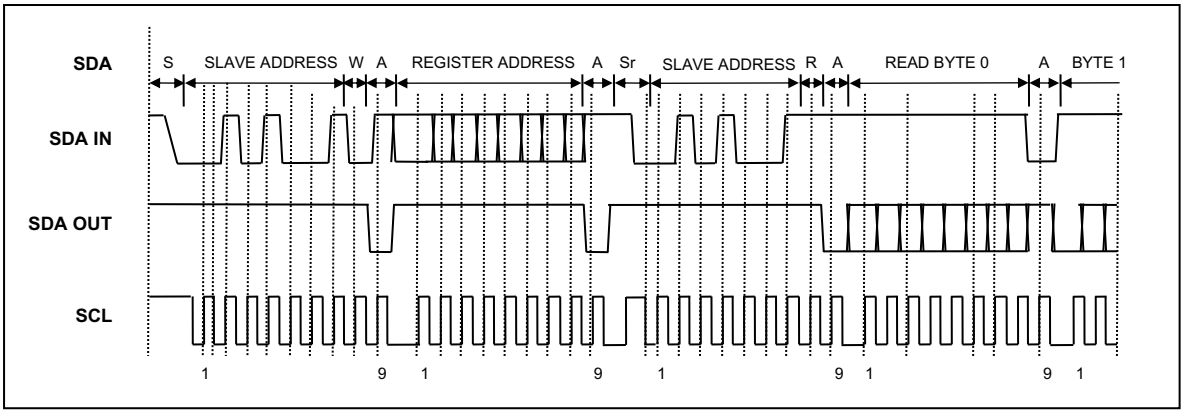


Figure 2-6 I2C Read Protocol

2.2 REGISTERS

2.2.1 OVERVIEW

The MC8121 is controlled and monitored by 17 registers. These registers provide a variety of control functions and can be read to determine results of the ADC conversions.

2.2.2 REGISTER MAP

Name	Address	Dir	Default	Description
ADDRSET	-	W	-	Address Set Register
CONTROL	00_H	R/W	00_H	Control Register
INTR	01_H	R/W	80_H	Interrupt Control Register
ATIME0	02_H	R/W	FF_H	ALS CH0 Integration Time Register
ATIME1	03_H	R/W	FF_H	ALS CH1 Integration Time Register
WTIME	04_H	R/W	01_H	Wait Time Register
AILTL	05_H	R/W	FF_H	ALS CH0 Interrupt Low Threshold Low Register
AILTH	06_H	R/W	03_H	ALS CH0 Interrupt Low Threshold High Register
AIHTL	07_H	R/W	FF_H	ALS CH0 Interrupt High Threshold Low Register
AIHTH	08_H	R/W	BF_H	ALS CH0 Interrupt High Threshold High Register
PERSIST	$0D_H$	R/W	00_H	ALS Interrupt Persistence Register
ADATA0L	$0E_H$	R	FF_H	ALS CH0 ADC Data Low Register
ADATA0H	$0F_H$	R	FF_H	ALS CH0 ADC Data High Register
ADATA1L	10_H	R	FF_H	ALS CH1 ADC Data Low Register
ADATA1H	11_H	R	BF_H	ALS CH1 ADC Data High Register
ID	12_H	R	$A1_H$	ID Register NOTE
AGC0	14_H	R/W	01_H	ADC Gain control 0 Register
AGC1	15_H	R/W	99_H	ADC Gain control 1 Register

Table 2-1 Registers of MC8121

Caution : Do not alter registers addressed $1D_H$ to $1F_H$. Writing to these registers may result in unexpected function.

NOTE Default value is $A1_H$ for MC8121.

2.2.3 REGISTER DESCRIPTION

ADDRSET (Address Set Register) **$--_H$**

7	6	5	4	3	2	1	0
-	-	-	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
-	-	-	W	W	W	W	W

Initial value : 00_H

ADDR[4:0] Base address for subsequent register access. When the I2C master initiates a write protocol with start bit and slave address transfer, the second byte is used to configure register address.

CONTROL (Control Register) **00_H**

7	6	5	4	3	2	1	0
ONESHOT	SOFTRST	-NOTE1	-NOTE1	MODE2	MODE1	MODE0	POWER
R/W	R/W	-	-	R/W	R/W	R/W	R/W

Initial value : 00_H

ONESHOT Stops ADC integration on completion of one integration cycle.

0 Continuous operation.

1 Once an integration cycle is over, ALS ADC will automatically

stop and also the MODE[1:0] bits in CONTROL register is to be cleared. To resume operation, re-assert MODE[2:0] bits.

SOFTRST Soft reset. This bit is auto-cleared.

0 No operation

1 Reset internal registers

MODE[2:0] Select operating mode. These 3 bits determine the operating mode of the device. Note that bit 1 and bit 0 are effective only when POWER bit is set to '1'. NOTE2

000 Disable ALS CH0/CH1 ADCs.

001 Enable ALS CH0/CH1 ADCs. CH0 and CH1 ADCs operate concurrently.

010 Reserved (Do not use)

011 Reserved (Do not use)

100 Reserved (Do not use)

101 Enable CH0 ADC only.

110 Enable CH1 ADC only.

111 Enable ALS CH0/CH1 ADCs. CH0 and CH1 ADCs operate sequentially(CH1 first).

POWER Power On. Enables internal RC oscillator(Typically 690KHz)

0 Turns off the MC8121.

1 Turns on the MC8121.

NOTE1 This bit should be written to '0'.

NOTE 2 The real MODE[1] and MODE[0] bits are updated after internal oscillator is enabled. So reading CONTROL register will return "---- --00_B" right after writing '1' to these bits while POWER bit is disabled or after setting MODE[2:0] bits and POWER bit simultaneously.

INTR (Interrupt Control Register) 01_H

7	6	5	4	3	2	1	0
PSX4EN	-	-	-	AINTF	INTEDGE	-	AINTEN
R/W	-	-	-	R	R/W	-	R/W

Initial value : 80_H

PSX4EN Make ALS integration time and Wait time step 4 times longer. It is recommended to change this bit before enabling POWER bit or changing MODE[2:0] bits.

0 ALS integration time and Wait time step are about 4.5ms

1 ALS integration time and Wait time step are about 18ms

AINTF ALS Interrupt Flag. Indicates that the device is asserting an interrupt. Writing 0 to this bit clears AINTF.

0 No Interrupt or interrupt cleared.

1 ALS interrupt requested.

INTEDGE Interrupt signal is triggered as pulse type at rising edge of internal clock,typically 1.45us period. The host needs not to clear interrupt.

0 Level interrupt

1 Edge interrupt

AINTEN Enables ALS Interrupt generation.

0 ALS Interrupt output is disabled.

1 ALS Interrupt occurs on INT pin.

ATIME0 (ALS CH 0 Integration Time Register) 02_H

7	6	5	4	3	2	1	0

ATIME07	ATIME06	ATIME05	ATIME04	ATIME03	ATIME02	ATIME01	ATIME00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

ATIME0[7:0] ALS CH0 Integration Time. Specifies the integration time in 4.5ms intervals. When MODE[2] bit is '0', the CH1 integration time is also decided by this register.

ALS CH0 Integration time = 4.5ms x ATIME0[7:0] (when PSX4EN=0)

ALS CH0 Integration time = 18ms x ATIME0[7:0] (when PSX4EN=1)

	PSX4EN=0	PSX4EN=1
00000000	Prohibited. Writing "00_H" has no effect.	
00000001	4.5ms	18ms
00000010	9.0ms	36ms
00001010	45.0ms	180ms
00010100	90.0ms	360ms
00101000	180.0ms	720ms
01010000	360.0ms	1440ms
11111111	1147.5ms	4608ms

ATIME1 (ALS CH1 Integration Time Register) 03_H

7	6	5	4	3	2	1	0
ATIME17	ATIME16	ATIME15	ATIME14	ATIME13	ATIME12	ATIME11	ATIME10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

ATIME1[7:0] ALS CH1 Integration Time. Specifies the integration time in 4.5ms intervals. This register value is effective only when MODE[2] bit is '1'.

ALS CH1 Integration time = 4.5ms x ATIME0[7:0] (when PSX4EN=0)

ALS CH1 Integration time = 18ms x ATIME0[7:0] (when PSX4EN=1)

	PSX4EN=0	PSX4EN=1
00000000	Prohibited. Writing "00_H" has no effect.	
00000001	4.5ms	18ms
00000010	9.0ms	36ms
00001010	45.0ms	180ms
00010100	90.0ms	360ms
00101000	180.0ms	720ms
01010000	360.0ms	1440ms
11111111	1147.5ms	4608ms

WTIME (Wait Time Register) 04_H

7	6	5	4	3	2	1	0
WTIME7	WTIME6	WTIME5	WTIME4	WTIME3	WTIME2	WTIME1	WTIME0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 01_H

WTIME[7:0] Wait Time. Specifies the wait time between continuous ALS operations in 4.5ms intervals.

Wait time = 4.5ms x WTIME[7:0] (when PSX4=0)

Wait time = 18ms x WTIME[7:0] (when PSX4=1)

	PSX4EN=0	PSX4EN=1
00000000	No wait	No wait

00000001	4.5ms	18ms
00000010	9.0ms	36ms
00001010	45ms	180ms
00010100	90ms	360ms
00101000	180ms	720ms
01111000	360ms	1440ms
11111111	1147.5ms	4608ms

The WTIME is used to reduce average power consumption, because both ALS CH0 and CH1 ADCs stop integrating during wait time period.

NOTE Although setting a larger wait time contributes to reduce average consumption current, it makes update period and response time longer.

AILTL (ALS CH0 Interrupt Low Threshold Low Register) **05_H**

7	6	5	4	3	2	1	0
AILTL7	AILTL6	AILTL5	AILTL4	AILTL3	AILTL2	AILTL1	AILTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

AILTL[7:0] ALS CH0 ADC channel interrupt low threshold low register.

AILTH (ALS CH0 Interrupt Low Threshold High Register) **06_H**

7	6	5	4	3	2	1	0
AILTH7	AILTH6	AILTH5	AILTH4	AILTH3	AILTH2	AILTH1	AILTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 03_H

AILTH[7:0] ALS CH0 ADC channel interrupt low threshold high register.

AIHTL (ALS CH0 Interrupt High Threshold Low Register) **07_H**

7	6	5	4	3	2	1	0
AIHTL7	AIHTL6	AIHTL5	AIHTL4	AIHTL3	AIHTL2	AIHTL1	AIHTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

AIHTL[7:0] ALS CH0 ADC channel interrupt high threshold low register.

AIHTH (ALS CH0 Interrupt High Threshold High Register) **08_H**

7	6	5	4	3	2	1	0
AIHTH7	AIHTH6	AIHTH5	AIHTH4	AIHTH3	AIHTH2	AIHTH1	AIHTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : BF_H

AIHTH[7:0] ALS CH0 ADC channel interrupt high threshold high register.

The interrupt threshold registers store the values to be used as the high and low trigger points for the adc data registers. If the value of adc data register crosses below or equal to the low threshold specified, an interrupt can be asserted on the interrupt pin. Likewise, if the result from ADC

conversion crosses above the high threshold specified, an interrupt can be asserted on the interrupt pin. The concatenated AILTH and AILTL is used as interrupt low threshold(=AILT) and the concatenated AIHTH and AIHTL is used as interrupt high threshold(=AIHT).

PERSIST (Interrupt Persistence Register) **$0D_H$**

7	6	5	4	3	2	1	0
-	-	-	-	APER3	APER2	APER1	APER0
-	-	-	-	R/W	R/W	R/W	R/W

Initial value : 00_H

APER[3:0] ALS CH0 Interrupt persistence. These bit field control the rate of ALS interrupt request to host chip.

0000	Every ALS CH0 cycle generates an interrupt.
0001	1 consecutive ALS CH0 ADC value out of range.
0010	2 consecutive ALS CH0 ADC value out of range.
...	…
1111	15 consecutive ALS CH0 ADC value out of range.

ADATA0L (ALS CH0 ADC Data Low Register) **$0E_H$**

7	6	5	4	3	2	1	0
ADATA0L7	ADATA0L6	ADATA0L5	ADATA0L4	ADATA0L3	ADATA0L2	ADATA0L1	ADATA0L0
R	R	R	R	R	R	R	R

Initial value : FF_H

ADATA0L[7:0] ALS CH0 ADC data low register.

The ALS ADCs included in MC8121 are of 16-bit resolution, and the integrated values appear on two registers ADATA0L/ADATA0H and ADATA1L/ADATA1H respectively. All ALS ADC data registers are read-only.

ADATA0H (ALS CH0 ADC Data High Register) **$0F_H$**

7	6	5	4	3	2	1	0
ADATA0H7	ADATA0H6	ADATA0H5	ADATA0H4	ADATA0H3	ADATA0H2	ADATA0H1	ADATA0H0
R	R	R	R	R	R	R	R

Initial value : FF_H

ADATA0H[7:0] ALS CH0 ADC data high register.

ADATA1L (ALS CH1 ADC Data Low Register) **10_H**

7	6	5	4	3	2	1	0
ADATA1L7	ADATA1L6	ADATA1L5	ADATA1L4	ADATA1L3	ADATA1L2	ADATA1L1	ADATA1L0
R	R	R	R	R	R	R	R

Initial value : 00_H

ADATA1L[7:0] ALS CH1 ADC data low register.

ADATA1H (ALS CH1 ADC Data High Register) 11_H

7	6	5	4	3	2	1	0
ADATA1H7	ADATA1H6	ADATA1H5	ADATA1H4	ADATA1H3	ADATA1H2	ADATA1H1	ADATA1H0
R	R	R	R	R	R	R	R

Initial value : 00_H

PDATA0H[7:0] ALS CH1 ADC data high register

ID (ID Register) 12_H

7	6	5	4	3	2	1	0
ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
R	R	R	R	R	R	R	R

Initial value : $A1_H$

ID[4:0] Device ID

10100 MC8121

REV[2:0] Revision number

AGC0 (ADC Gain Control 0 Register) 14_H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	VGAIN0
-	-	-	-	-	-	-	R/W

Initial value : 01_H

VGAIN0 ADC Voltage Gain Control NOTE

0	x3.0 (not recommended)
1	x2.5 (recommended)

Caution : Do not alter AGC0[7:1]. Writing non-zero value to these bits may result in mal-function.

NOTE Grayed voltage gain is not recommended.

AGC1 (ADC Gain Control 1 Register) 15_H

7	6	5	4	3	2	1	0
AGAIN13	AGAIN12	AGAIN11	AGAIN10	AGAIN03	AGAIN02	AGAIN01	AGAIN00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 99_H

AGAIN1[3:0] CH1 ADC gain control NOTE

1001 x1.8

AGAIN0[3:0] CH0 ADC gain control NOTE

1001 x1.8

NOTE For ADC CH0 and CH1, gains are fixed to x1.8 after factory calibration. Other gains are not recommended.

2.3 OPERATION

2.3.1 ALS CONCURRENT OPERATION

ALS concurrent operation is enabled by setting MODE[2:0] bits to 001_B, and after pre-defined ALS period the ALS CH0 ADC counter value is transferred to ADATA0H/ADATA0L registers and the CH1 ADC counter valude is transferred to ADATA1H/ADATA1L registers which can be read via I2C read transaction.

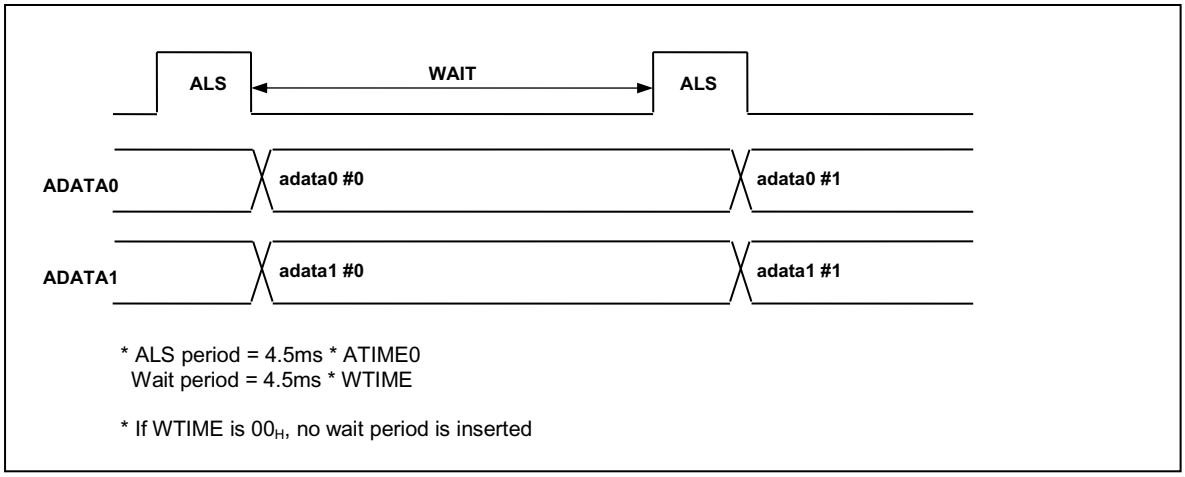


Figure 2-7 ALS Operation

2.3.2 ALS CH0 / CH1 SEQUENTIAL OPERATION

ALS CH0 / CH1 sequential operation mode is enabled by setting MODE[2] bit to 1. In this mode of operation, ALS CH1 operation is done followed by ALS CH0 operation and optional WAIT cycle. ALS CH0 and CH1 integration time is decided by each timing control registers ATIME0 and ATIME1. In sequential operation mode, only CH0 or CH1 ADC can be enabled by setting MODE bits properly, and this can reduce operating power consumption.

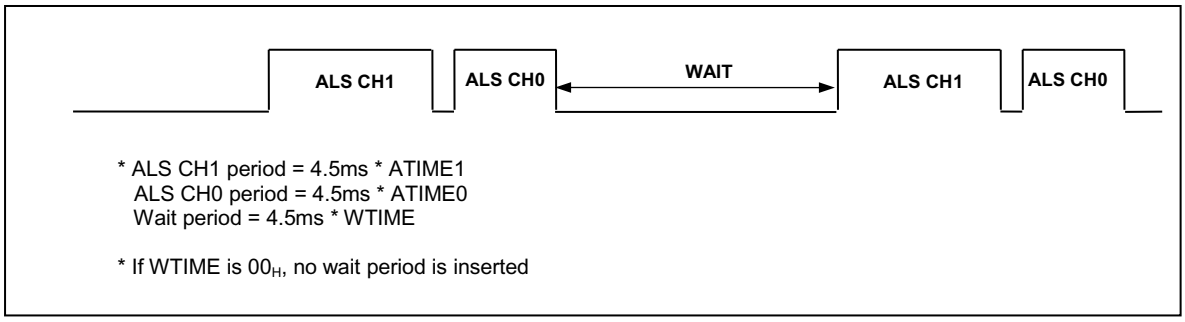


Figure 2-8 ALS CH0 / CH1 Sequential Operation

2.3.3 INTERRUPT

2.3.3.1 INTERRUPT OUTPUT MODE

INT pin operates as interrupt output mode by setting AINTEN bit.

ALS Interrupt

An ALS interrupt can be requested when ALS CH0 ADC result is greater than or equal to AITH or less than AILT after one ALS cycle. If APER(ALS Persistence) value is non-zero, it is needed the ALS CH0 ADC results are out of range APER consecutive times. The result of interrupt judgement for ALS is stored into AINTF bit in INTR register.

There are two kinds of output mode, level or pulse interrupt. Below is the description of the level interrupt type.

Transition from H to L in INT pin means that an interrupt condition is generated, and the INT pin remains L level until the interrupt flag(AINTF) is cleared. ALS interrupt is cleared by writing 0 to it's flag bit in INTR register.

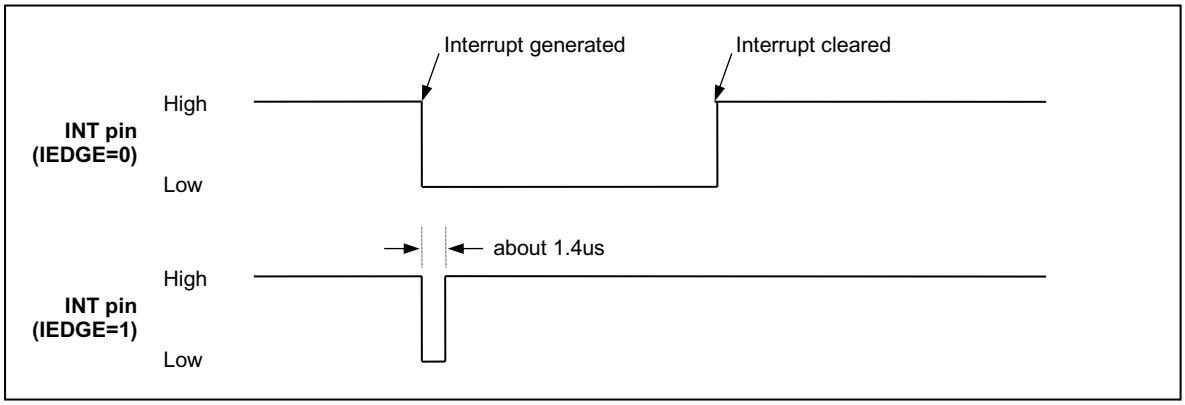


Figure 2-9 ALS CH0 Interrupt output (level or pulse interrupt)

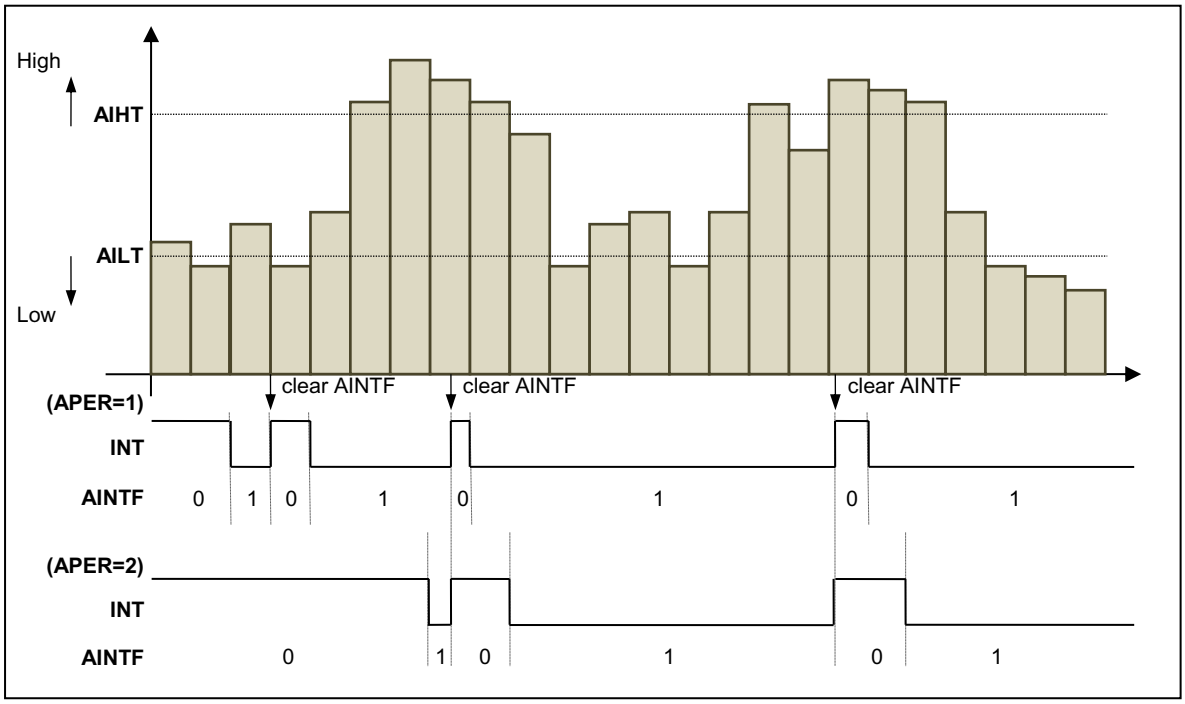


Figure 2-10 ALS Interrupt Output (APER=1 or 2 & INTEDGE=0)

2.3.4 POWER CONSUMPTION

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 60uA of power.

2.4 APPLICATION INFORMATION : SOFTWARE

2.4.1 OVERVIEW

After applying VDD, the device will initially be in the power down mode. To start ALS sensing operation, set the POWER bit in CONTROL register to enable internal RC oscillator. The ATIME0, ATIME1 or WTIME registers should be configured for the preferred integration and wait time, and then the MODE[2:0] bits in CONTROL register should be set to enable each ADC channel.

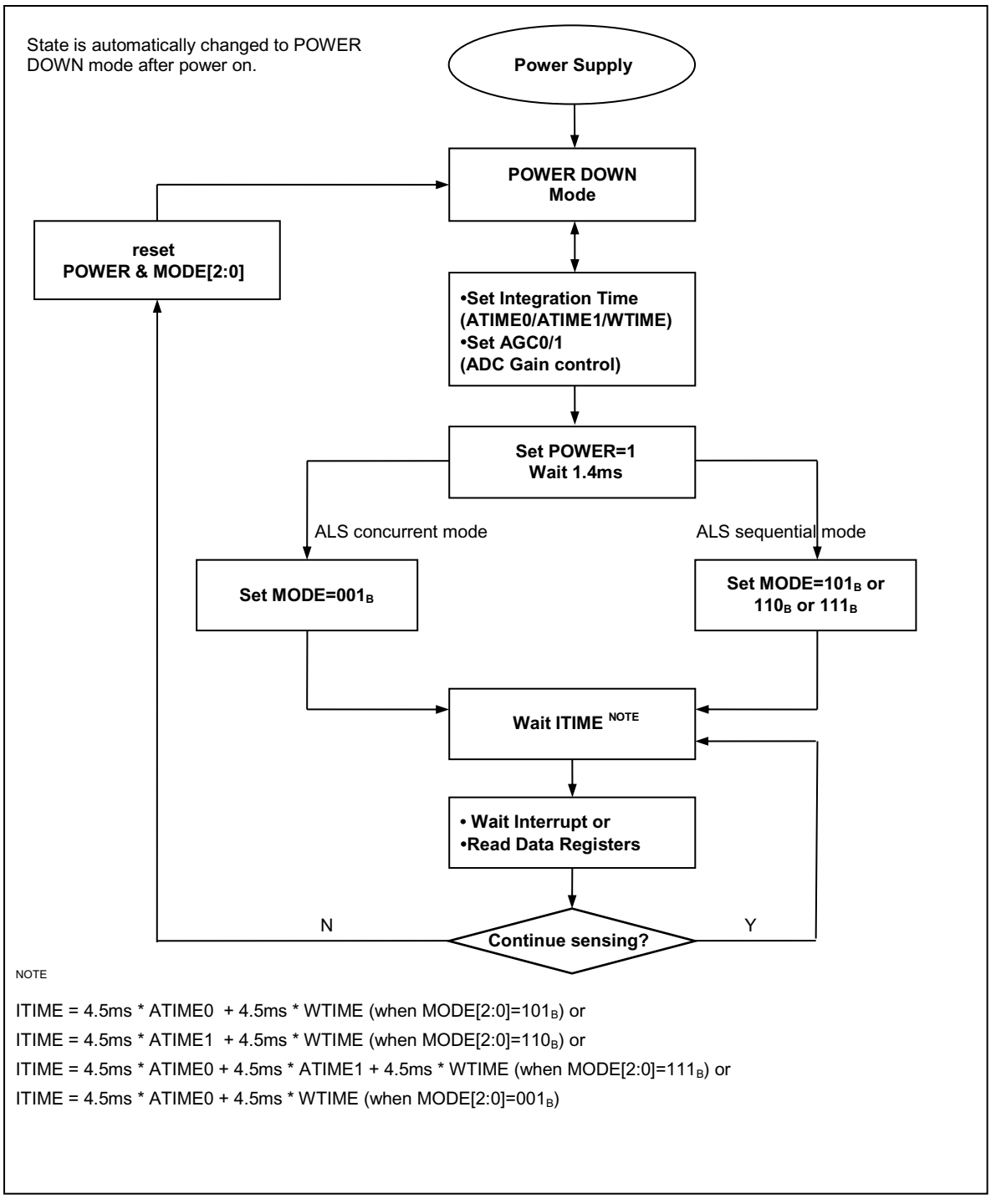


Figure 2-11 Operating Modes

3. APPENDIX

A. Brief Application Note

A capacitor should be located close to VDD pin of MC8121 to reduce power noise. The pull up resistors of two line serial bus are recommended to be around 10kΩ, especially a pull up registor for INT connected to host controller must be 100kΩ.

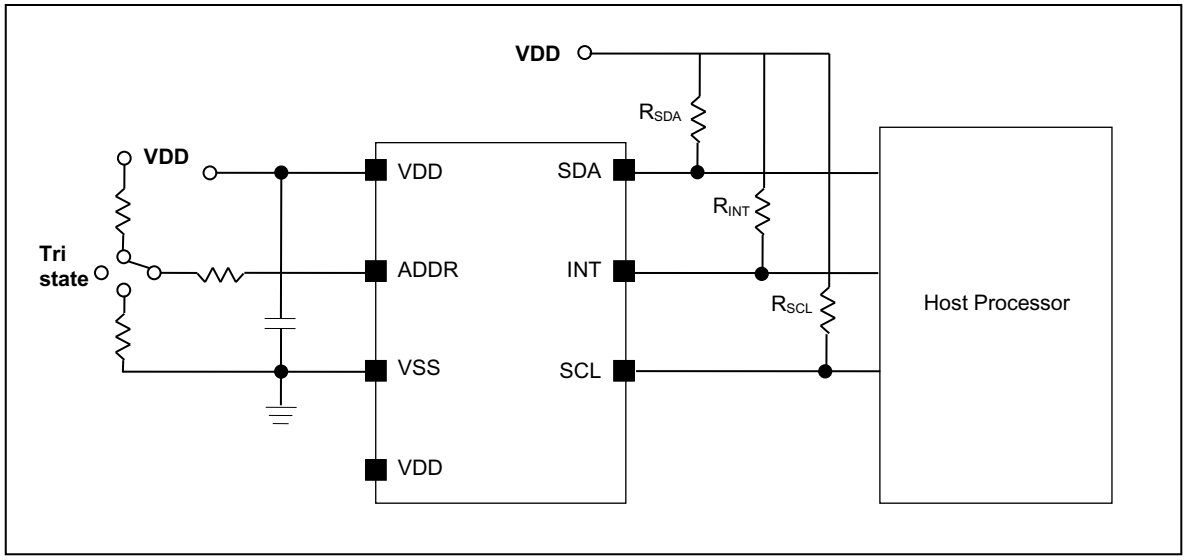


Figure 3-1 Hardware pin connection diagram

B. Notice

The below explains matters to be attended to when customer develops a program for MC8121.

1) Operation voltage 2.4 to 3.6V

2) Set SLAVE address (Determined by ADDR pin condition during power-up)

Input Low : 0x29(0101001) => In Master IIC situation when writing and its value is 0x 52 and when reading , its value is 0x53
Input High : 0x56(1010110) => In Master IIC situation when writing, value is 0xAC and when reading, value is 0xAD
Floating : 0x29(0101001) => In Master IIC situation when writing, value is 0x52 and when reaing, value is 0x53

3) IIC speed is the standard, about 100kHz.

When writing IIC Multi bytes (Single byte read and write rarely is used)

- Multi bytes Writing :
START(M)+SlaveAddress_W(0x52,M)+ACK(S)+REG_ADDR(0xxx,M)+ACK(S)+WRITE_BYTE0+ACK(S)…+STOP(M)

For example) When ADDR pin is low, you want to write 0x33 in CONTROL (address 00_H) Register. You should follow the below sequence.

START+0x52+ACK+0x00+ACK+0x33+ACK+STOP

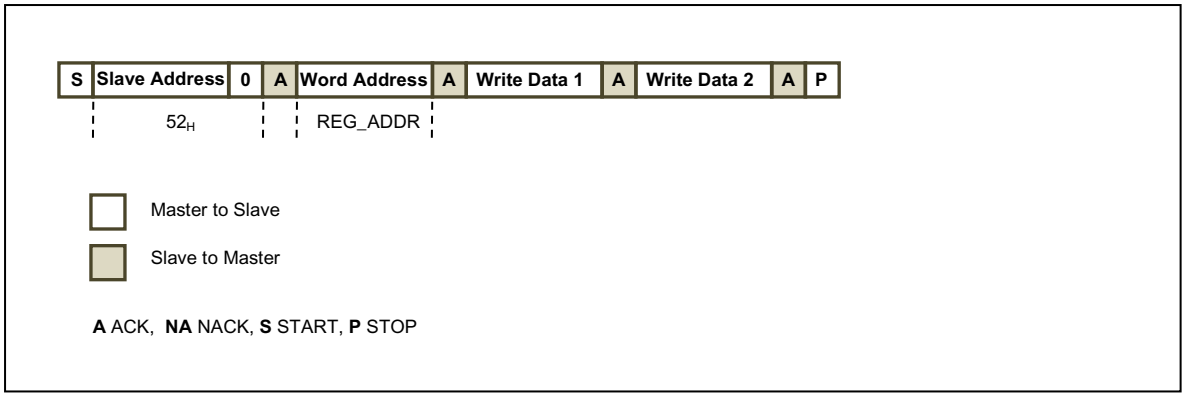


Figure 3-2 I2C write example

When reading IIC Multi bytes

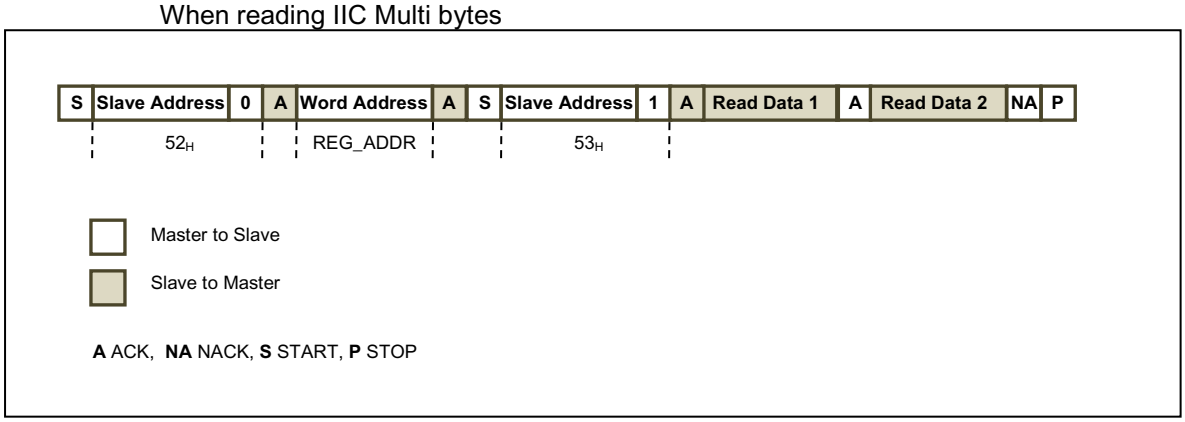


Figure 3-3 I2C read example

- Multi bytes reading:

  START(M)+SlaveAddress_W(0x52,M)+ACK(S)+REG_ADDR(0xxx,M)+ACK(S)+START +

  SlaveAddress_R(0x53,M)+ACK(S)+READ_BYTE0(S)+ACK(M)…+NACK+STOP(M)

  For example) When ADDR pin is low, you want to read values of ADATA0L and ADATA0H (address $0E_H$~$0F_H$) register. You should follow the below sequence.

  START+0x52+ACK+0x0E+ACK+START+0x53+ACK+??+ACK+…??+NACK+STOP

- After sending IIC Read/Write Command, delay time needs about 2msec for protocol transferring and MC8121 writing time)