ABOV SEMICONDUCTOR Co., Ltd.
8-BIT SINGLE-CHIP MICROCONTROLLERS

MC81F6104
MC81F6204

User's Manual (Ver. 1.0)

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REVISION HISTORY

VERSION 1.0 (November 2, 2011)

Package diagram is added.

VERSION 0.03 (December 23, 2009)

Some errata is fixed.

"Figure 1.27 8MHz Int.ISC" is added.

VERSION 0.02 (March 31, 2009)

Some errata is fixed.

VERSION 0.00 (January 08, 2009)

A draft manual.

Table of Contents

MC81F6204 / MC81F6104

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH PROGRAMMABLE PULSE GENERATOR

1. OVERVIEW

1.1 Description

MC81F6204 is a general purpose microcontroller based on G800 Core which contains 4K internal flash memory, 192byte SRAM, 3-channel Timer, 8bit ADC, Watch Dog Timer, Buzzer, PWM, Auto Triggering PWM with Analog Comparators, On-chip OP-Amp.

PKG Type	Memory Size	RAM Size	Device Name	
24 SKDIP/SOP	4K Bytes	192 Bytes	General	MC81F6204K (24SKDIP) MC81F6204D (24SOP)
			PPG	MC81F6104K (24SKDIP) MC81F6104D (24SOP)
20 PDIP/SOP	4K Bytes	192 Bytes	General	MC81F6204M (20SOP) MC81F6204B (20PDIP)
			PPG	MC81F6104M (20SOP) MC81F6104B (20PDIP)

1.2 Features

▶8Bit CPU (G800 Core)
▶4K bytes Code Flash
▶192 Bytes On-Chip Data RAM
(Including STACK Area)
▶Minimum Instruction Execution time
: 250ns at 8MHz (2-cycle NOP Instruction)
▶One 8-bit Basic Interval Timer
▶One 7-bit Watch Dog Timer
▶Timer
▷ Timer/Counter/Capture: 8-bit × 2 ch. (16-bit × 1ch.)
▷ Compare: 8-bit × 2 ch
▶10-bit High Speed PWM 2 ch
▷ Duty & Period Programmable PWM: 2ch
▷ Duty Programmable PWM with auto triggering mod: 1ch
▶5 Internal Comparator (CMP0, 1, 2, 3, 4)
▶OP-Amp for Current Protection (1/2 stage)
: Condition - 4.5V ~ 5.5V, offset < 5mV
▶4 External Interrupt Source Ports
▶One Programmable 6-bit Buzzer Driving Port
▶8(7) Ch. 8-bit On-Chip Analog to Digital Converter (Total Accuracy : **±1.5 LSB**)
▶16 Interrupt Sources (including RESET)
▷4 External Sources (INT0, 1, 2, 3)
▷5 Comparator Interrupts Sources
▷3 Timer/Counter Sources (Timer0,1,3)
▷3 Functional Sources (ADC,WDT,BIT)
▶Operating Voltage & Frequency
▷ 2.2V ~ 5.5V (at 1~4MHz)
▷ 2.7V ~ 5.5V (at 1~8MHZ)
▷ 4.5V ~ 5.5V (at 1~12MHz)
▷ 5.0V ~ 5.5V (at 1~12MHz) (Op-Amp, Comparator-0, Auto Triggered PWM enabled)
▶Oscillator:
▷Crystal
▷Ceramic Resonator
▷External RC/R Oscillator
▷ Internal 1MHz/2MHz/4MHz/8MHz Oscillator
▶Low Power Saving Modes
▷ STOP mode

▷ SLEEP mode
▷ RC-WDT mode
▶ Noise Immunity Circuit
▷ Low Voltage Reset (2.2V/ 2.7V/3V/4.0V)
▷ Power On Reset (2.4V)
▶ Package Type
: 24SKDIP/SOP, 20 PDIP/SOP
▶ All I/O: programmable Pull-up, Open drain

Device	PIN #	R0	R1	R2	I/O #
MC81F6104	20	6	2	8	16
	24	6	5	8	19
MC81F6204	20	8	2	8	18
	24	8	5	8	21

1.3 Block Diagram

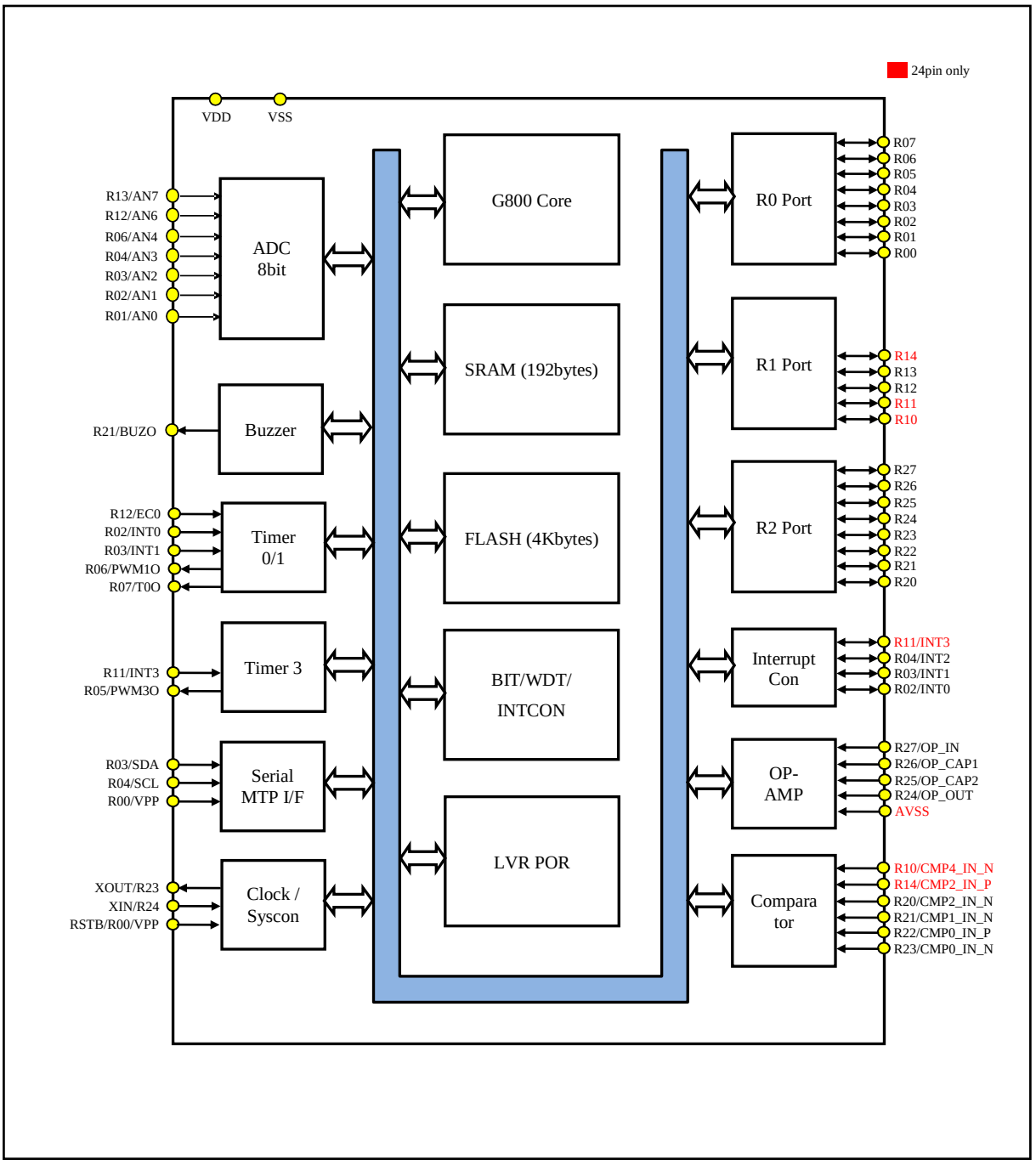


Figure 1.1 Top Abstract Block Diagram

1.4 PIN Assignment

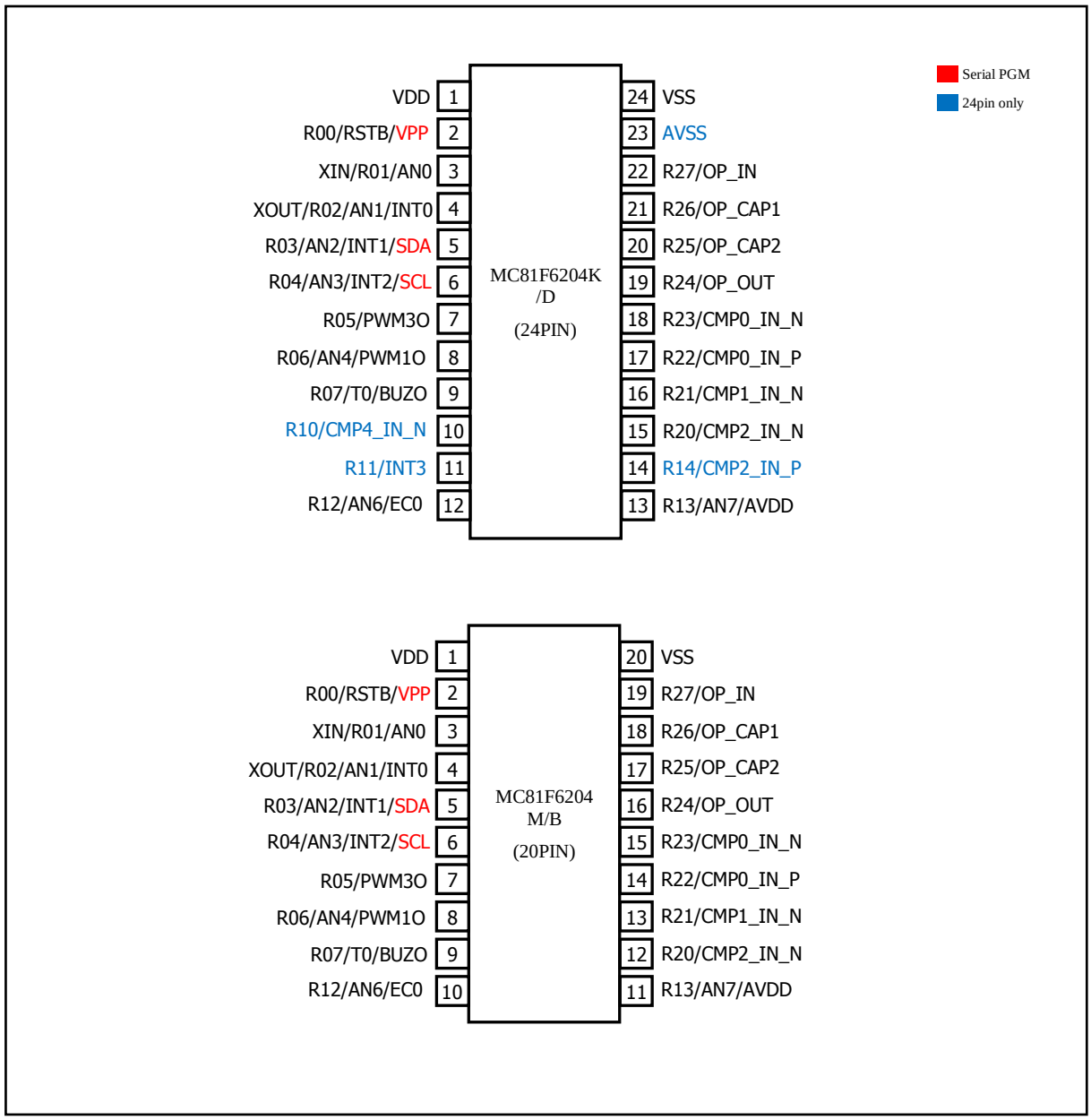


Figure 1.2 PIN Assignment Diagram of MC81F6204 (with non protection pin)

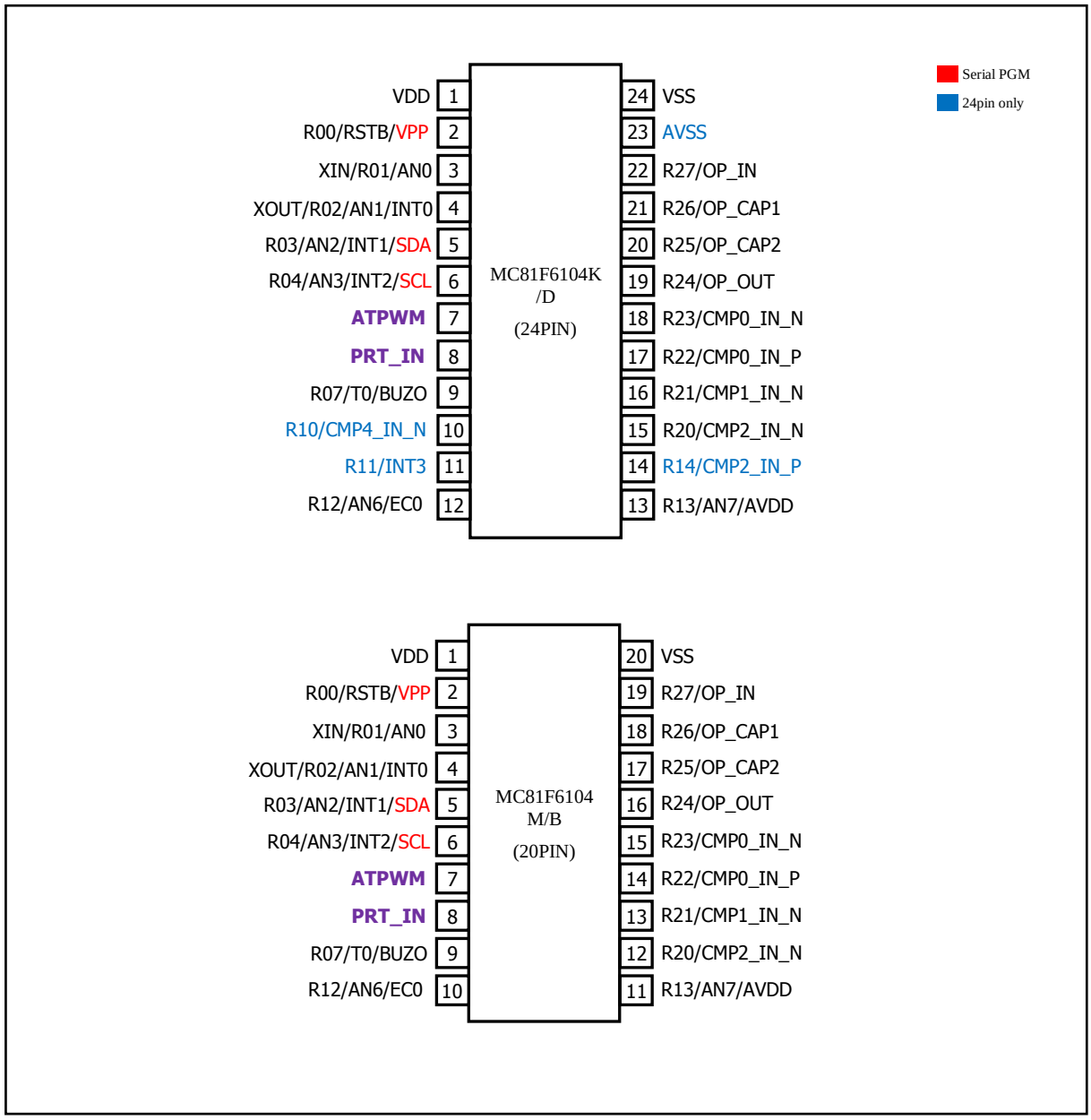
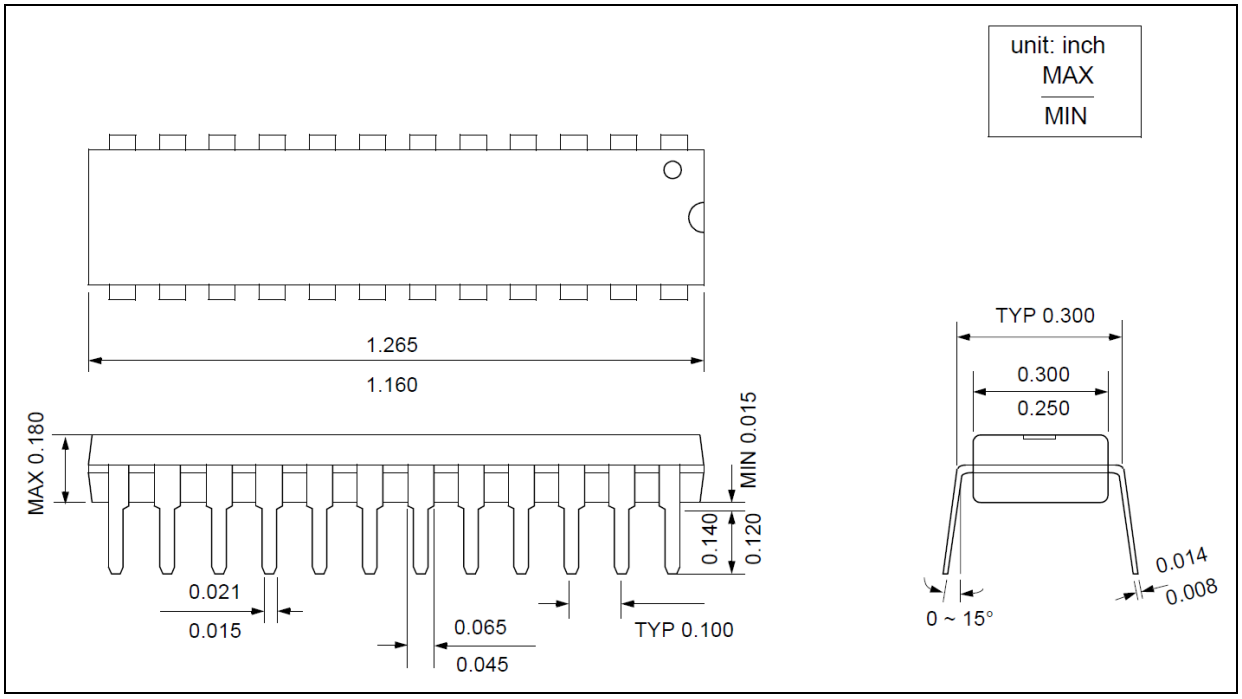


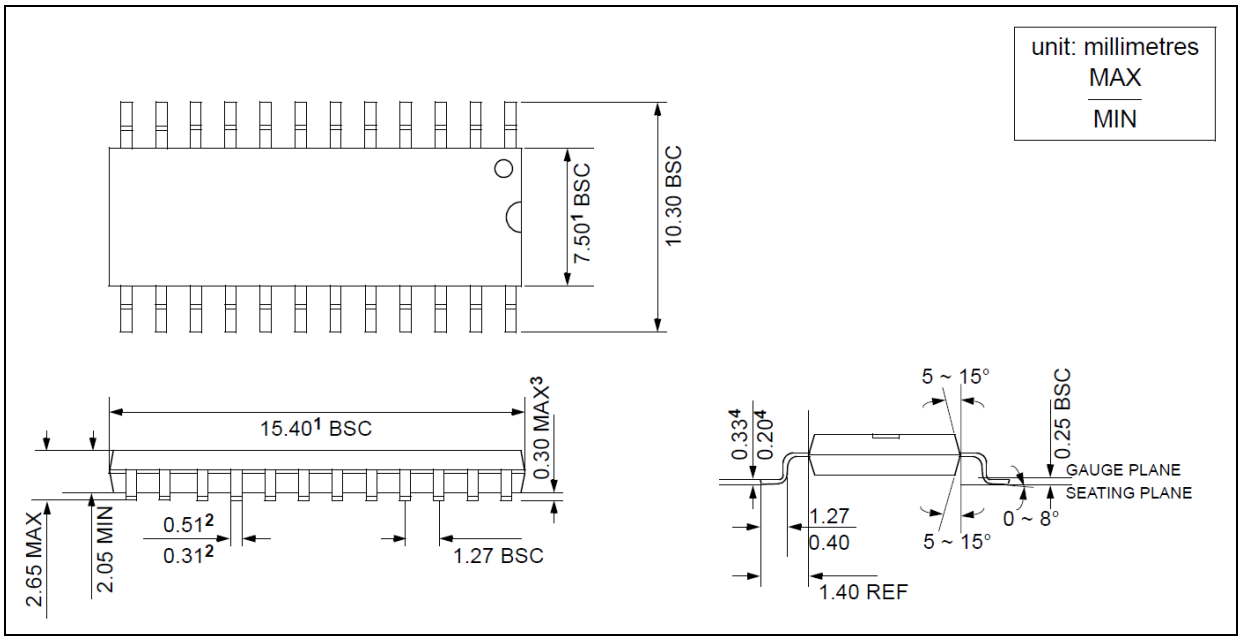
Figure 1.3 PIN Assignment Diagram of MC81F6104 (with protection pin)

1.5 PACKAGE DIAGRAM

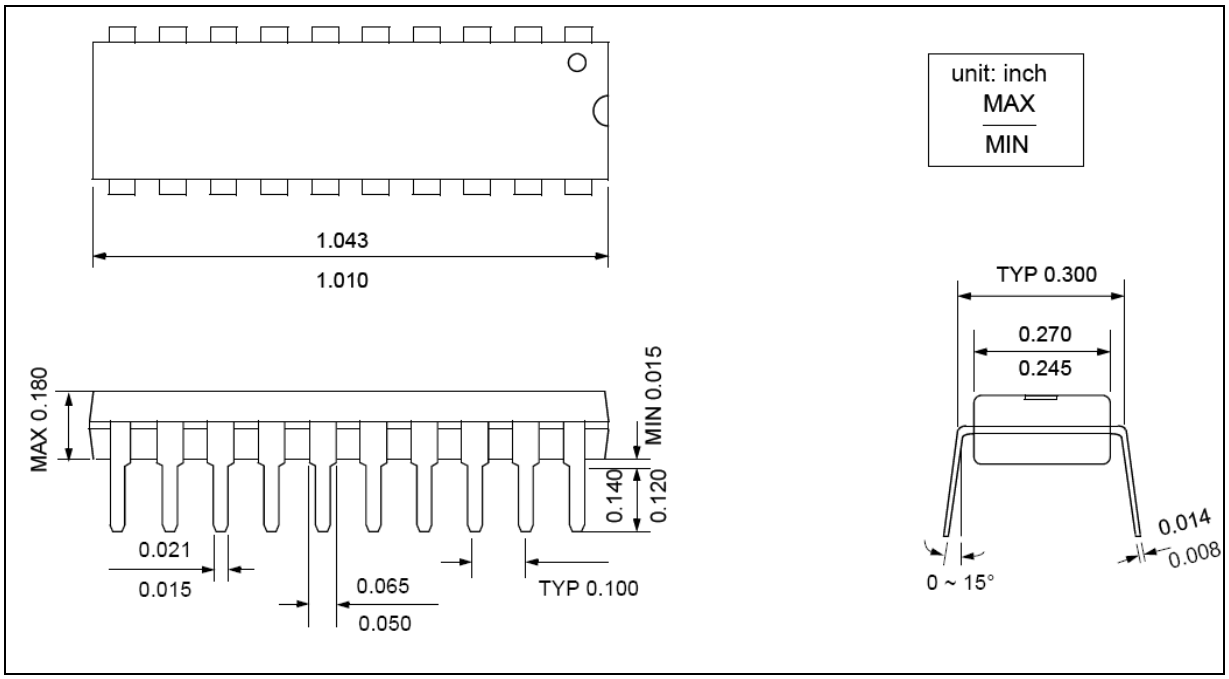
1.5.1 24 SKDIP



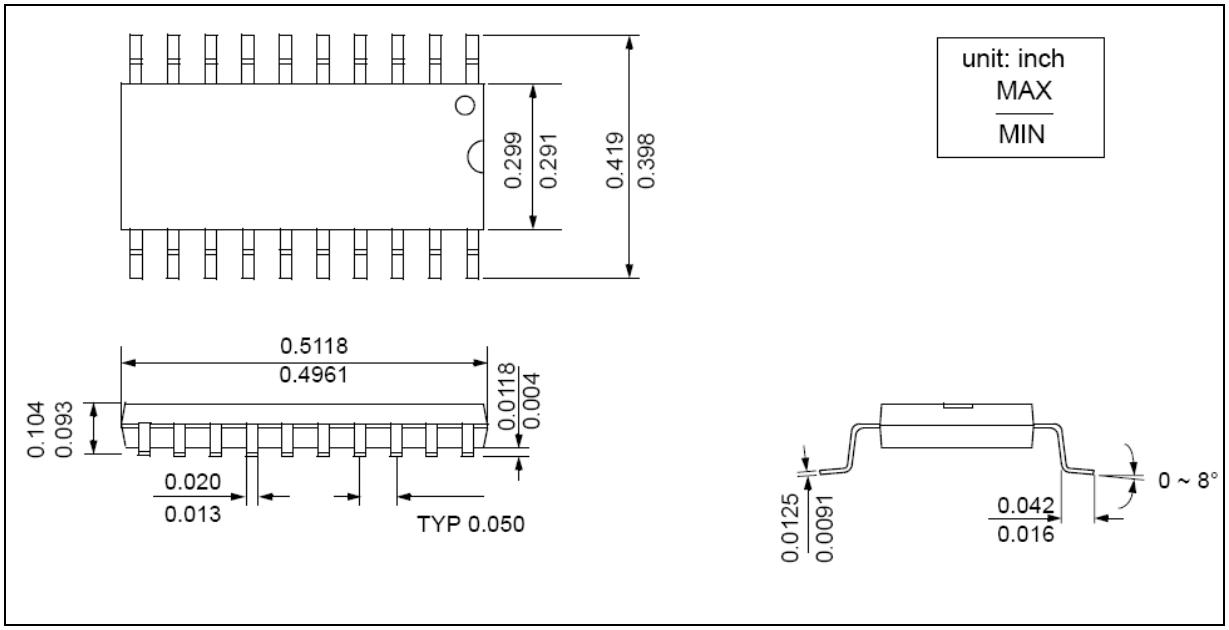
1.5.2 24 SOP



1.5.3 20 PDIP



1.5.4 20 SOP



1.6 PIN Description

PIN	I/O	Function	@Reset	Shared With
R00	I/O	▶ Port R0. ▶ 8-bit I/O port. (7-bit I/O port at 24pin) ▶ Can be set in input or output mode in 1-bit units. ▶ Internal pull-up register can be used via software when this port is used as input port. ▶ Open Drain enable register can be used via software when this port is used as output port. ▶ Secondary Function can be controlled by PSR0, PSR1, and PSR2 Register.	Input	RSTB,VPP
R01				XIN,AN0
R02				XOUT,AN1,INT0
R03				AN2,INT1,SDA
R04				AN3,INT2,SCL
R05				PWM3O,IGBT_PWM3O
R06				AN4,PW1O,PRT_IN
R07				T0O,BUZO
R10	I/O	▶ Port R1. ▶ 5-bit I/O port. (2-bit I/O port at 20pin) ▶ Can be set in input or output mode in 1-bit units. ▶ Internal pull-up register can be used via software when this port is used as input port. ▶ Open Drain enable register can be used via software when this port is used as output port. ▶ Secondary Function can be controlled by R1FUNC Register	Input	CMP4_IN_N
R11				INT3
R12				AN6,EC0
R13				AN7,AVDD
R14				CMP2_IN_P
-				-
-				-
-				-
R20	I/O	▶ Port R2. ▶ 8-bit I/O port. ▶ Can be set in input or output mode in 1-bit units. ▶ Internal pull-up register can be used via software when this port is used as input port. ▶ Open Drain enable register can be used via software when this port is used as output port. ▶ Secondary Function can be controlled by R2FUNC Register.	Input	CMP2_IN_N
R21				CMP1_IN_N
R22				CMP0_IN_P
R23				CMP0_IN_N
R24				OP_OUT
R25				OP_CAP2
R26				OP_CAP1
R27				OP_IN

Table 1.1 Pin Description

PIN	Power	I/O	ADC	INT	CLK/RST	TIMER	PGM	PPG
1	VDD							
2		R00			RSTB		VPP	
3		R01	AN0		XIN			
4		R02	AN1	INT0	XOUT			
5		R03	AN2	INT1			SDA	
6		R04	AN3	INT2			SCL	
7		R05				PWM3O		**ATPWM**

PIN	Power	I/O	ADC	INT	CLK/RST	TIMER	PGM	PPG
8		R06	AN4			PWM1O		**PRT_IN**
9		R07				T0O/BUZO		
10*		R10						CMP4_IN_N
11*		R11		INT3				
12		R12	AN6			EC0		
13	AVDD	R13	AN7					AVDD
14*		R14						CMP2_IN_P
15		R20						CMP2_IN_N
16		R21						CMP1_IN_N
17		R22						CMP0_IN_P
18		R23						CMP0_IN_N
19		R24						OP_OUT
20		R25						OP_CAP2
21		R26						OP_CAP1
22		R27						OP_IN
23	AVSS							AVSS
24	VSS							

Table 1.2 Second Function Category Map

* 24pin package only.

1.7 Port Structure

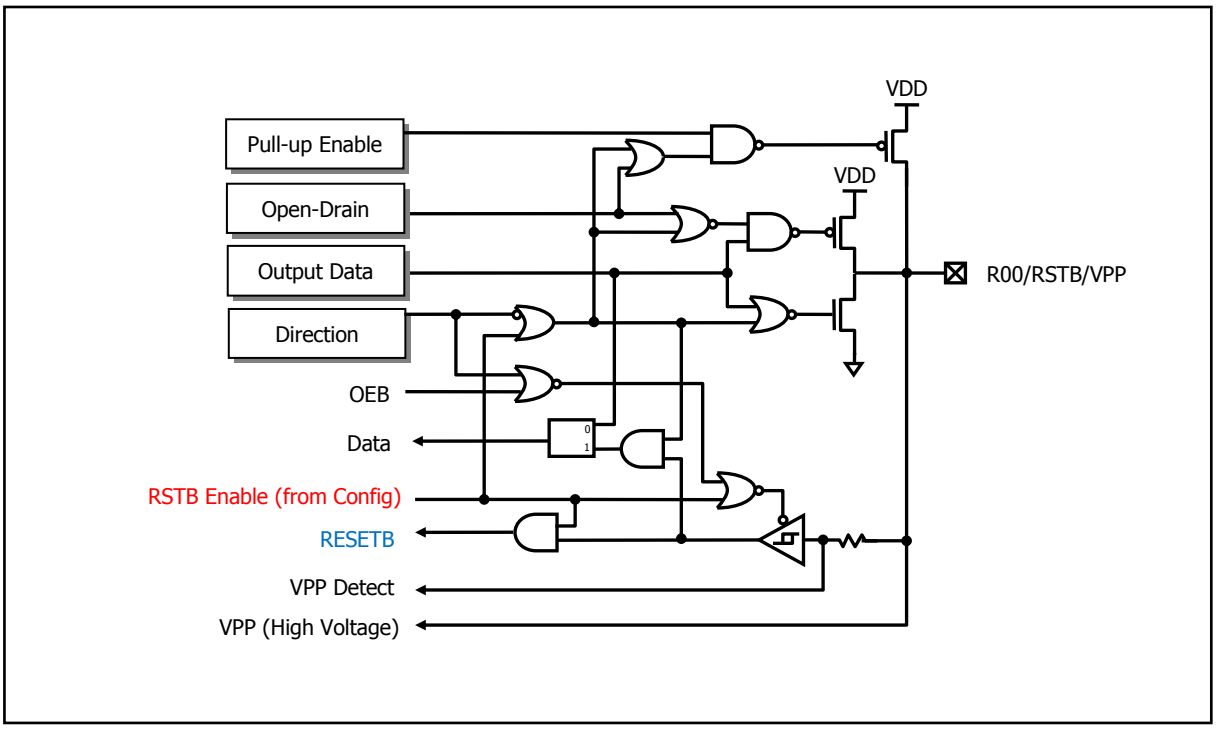


Figure 1.4 R00/RSTB/VPP Port Structure

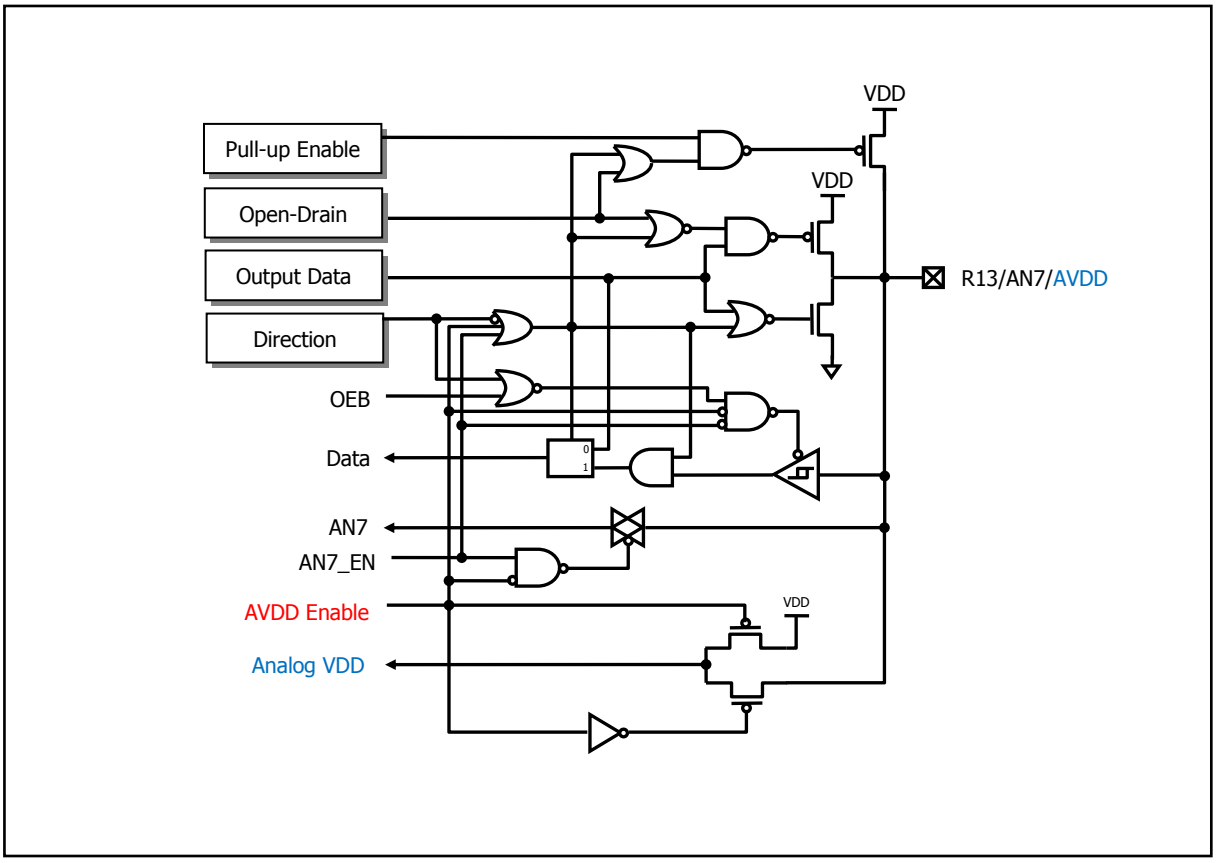


Figure 1.5 R13/AN7/AVDD Port Structure

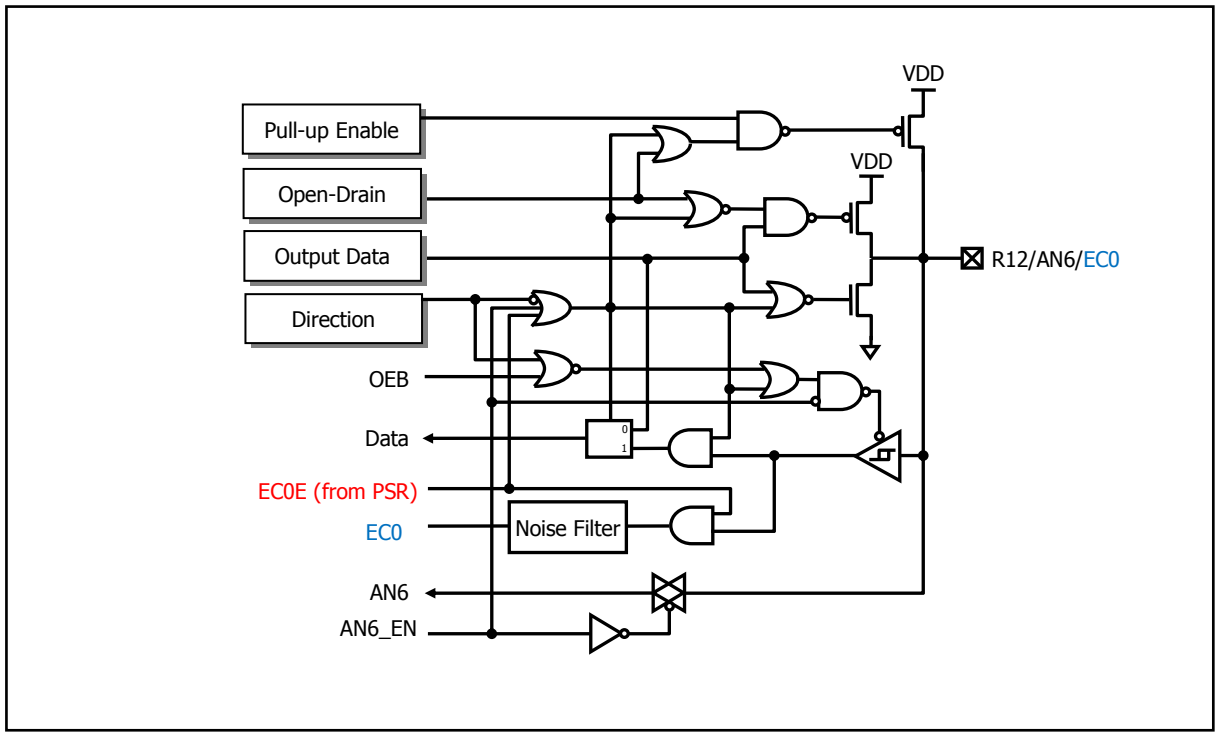


Figure 1.6 R12/AN6/EC0 Port Structure

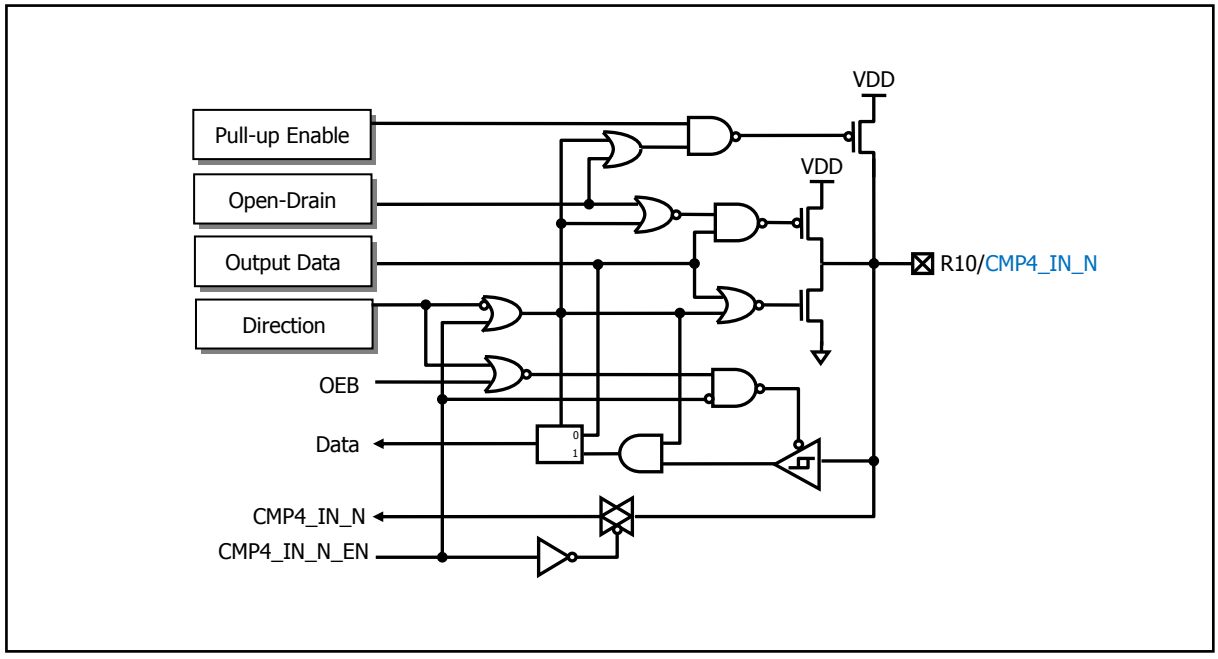


Figure 1.7 R10/CMP4_IN_N Port Structure

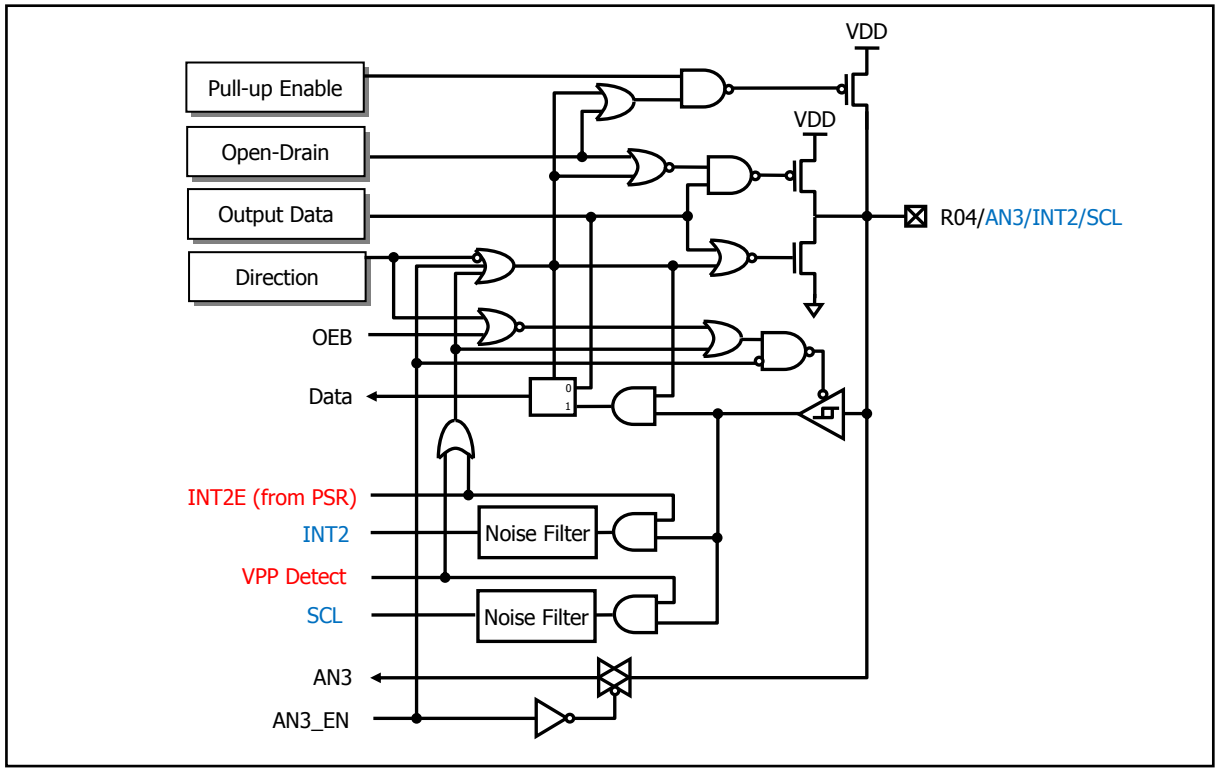


Figure 1.8 R04/AN3/INT2/SCL Port Structure

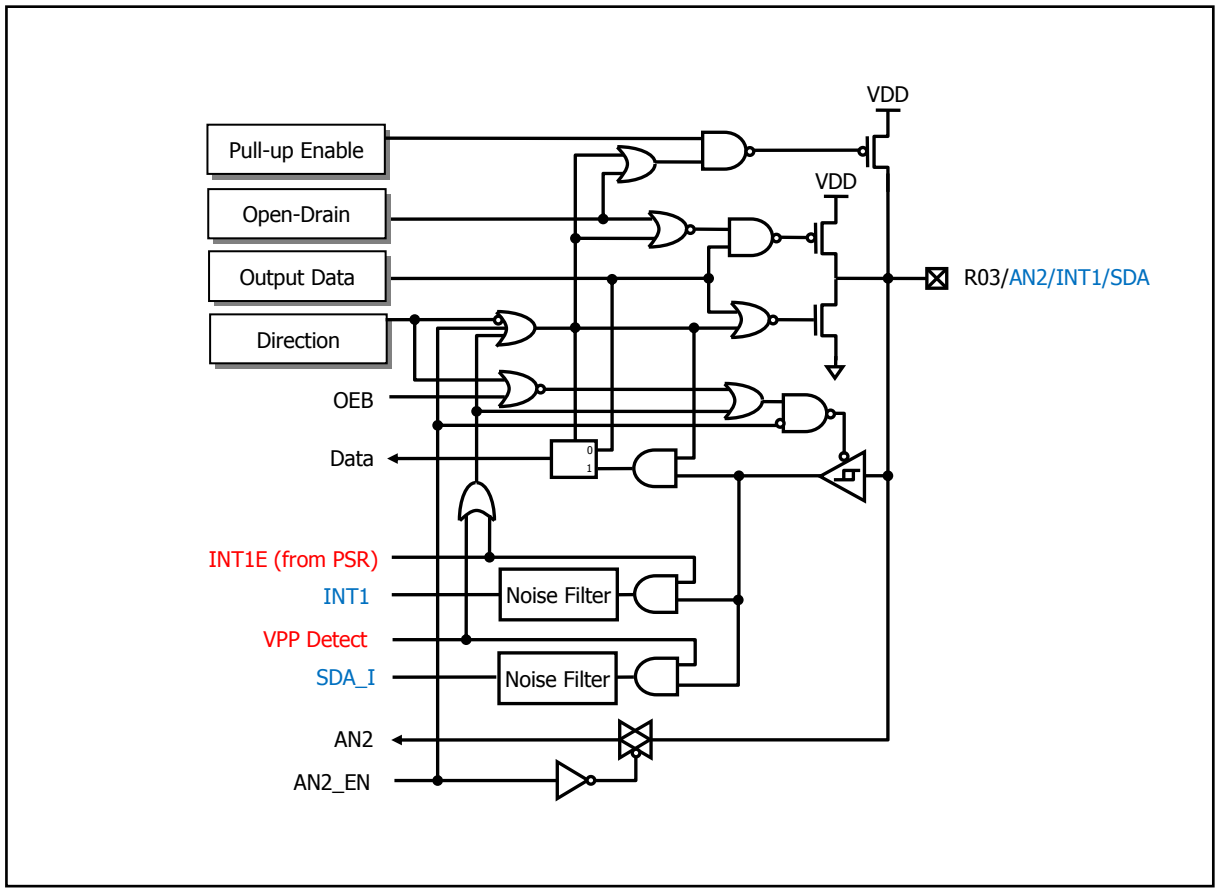


Figure 1.9 R03/AN2/INT1/SDA

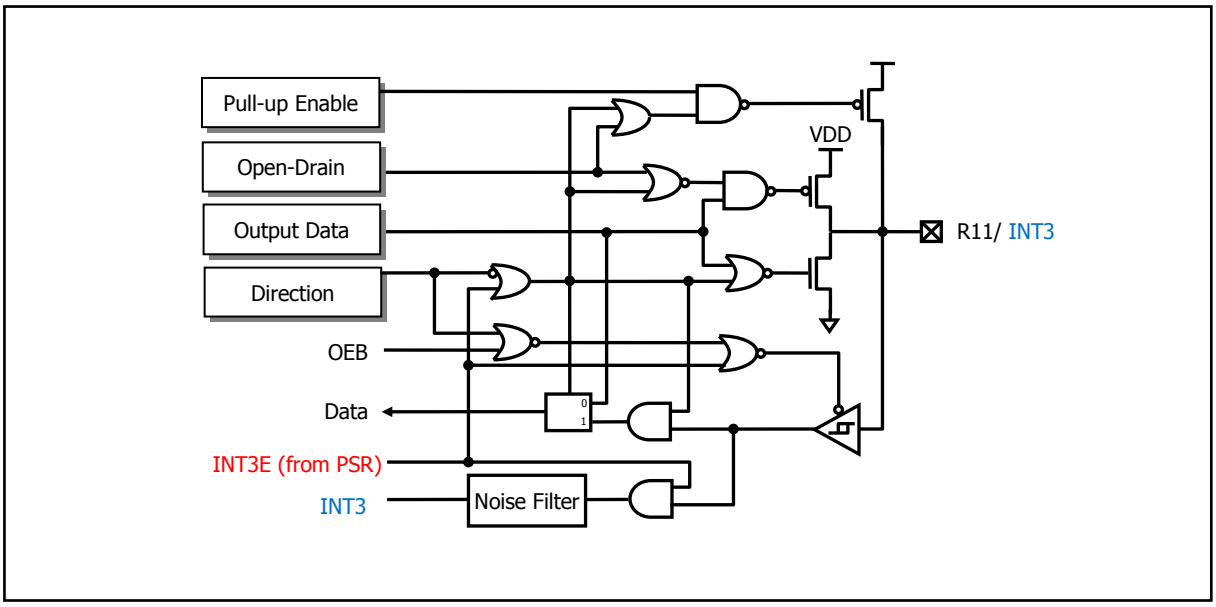


Figure 1.10 R11/INT3 Port Structure

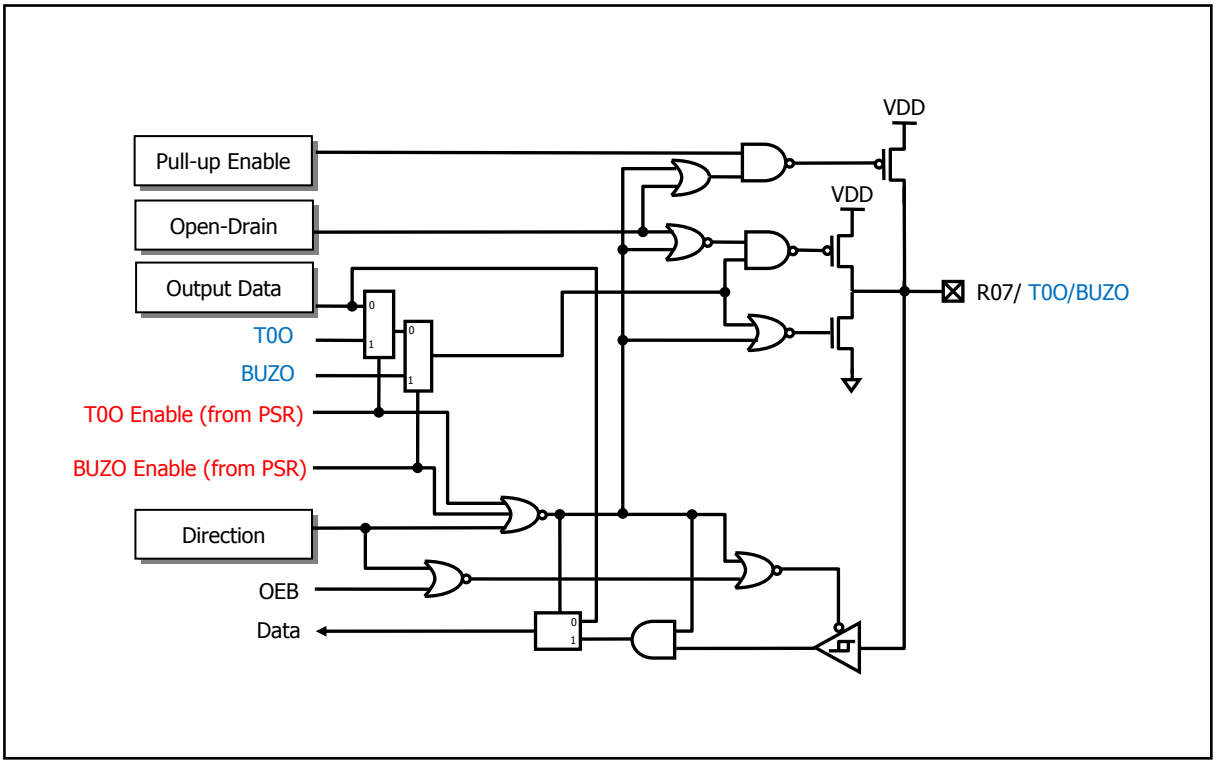


Figure 1.11 R07/T0O/BUZO Port Structure

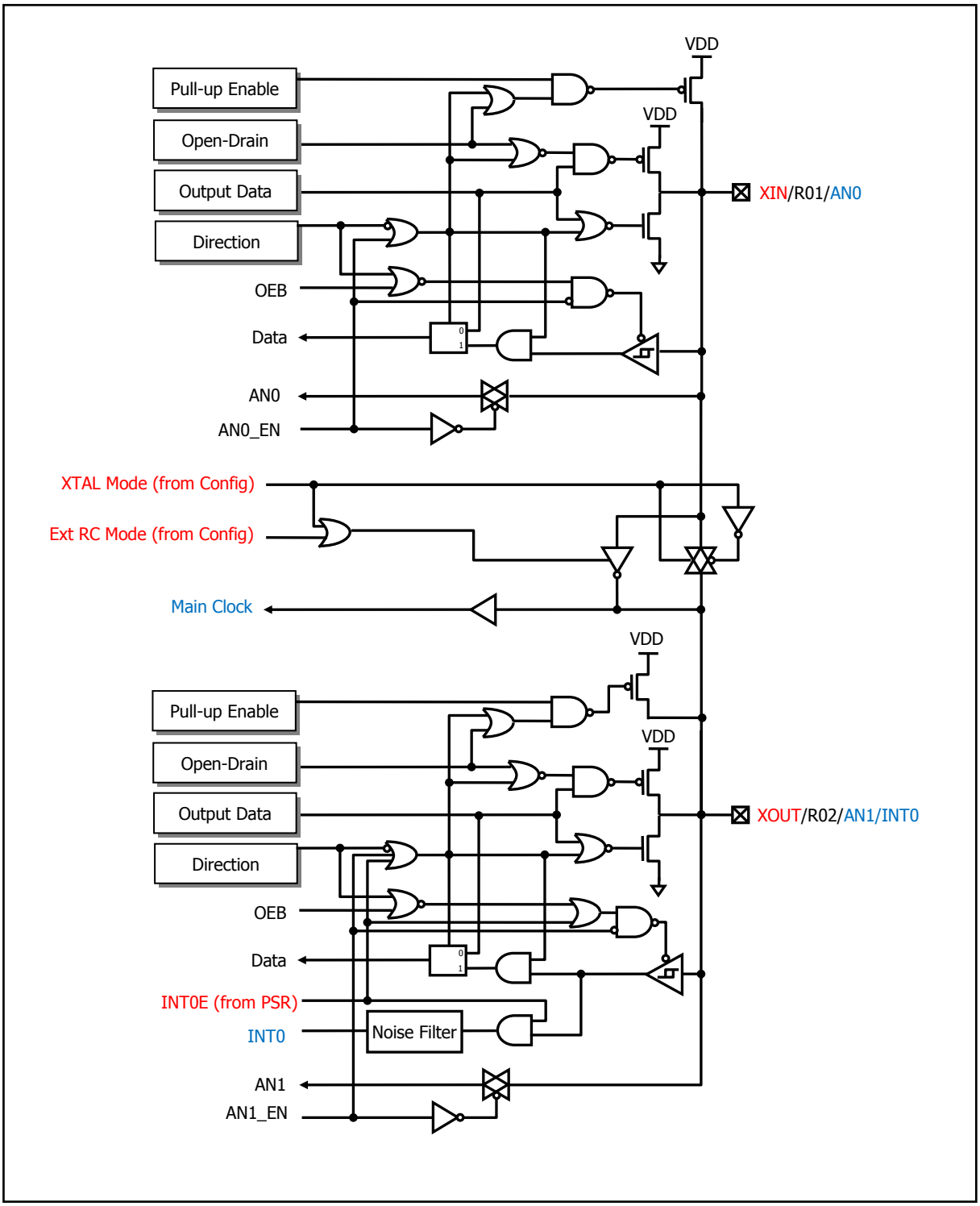


Figure 1.12 XIN, XOUT Port Structure

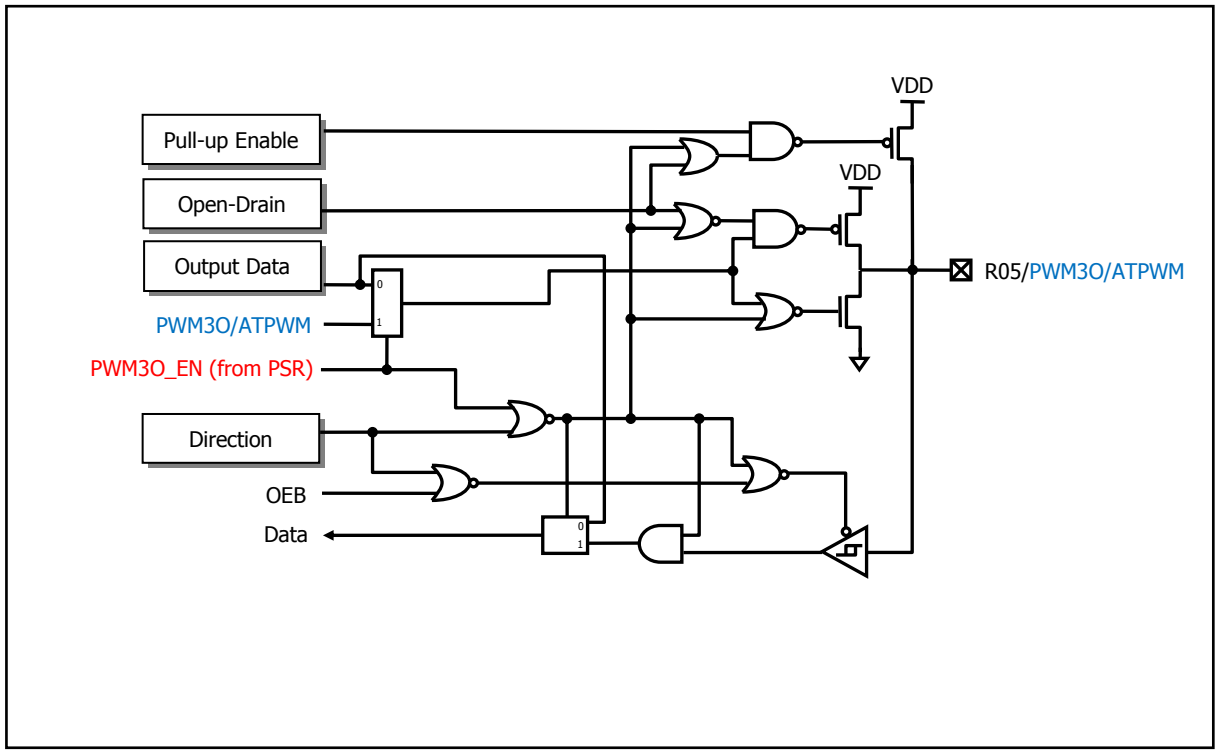


Figure 1.13 R05/PWM3O/ATPWMO Port Structure

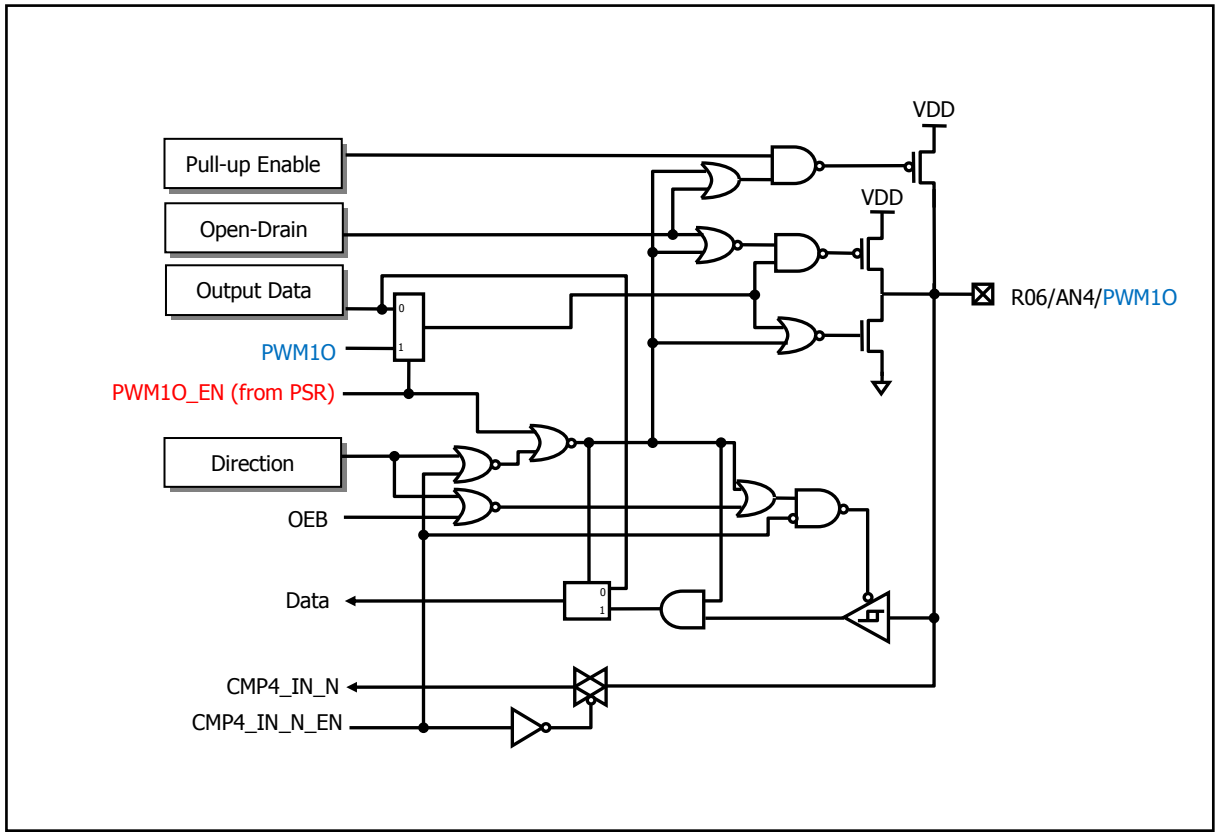


Figure 1.14 R06/AN4/PWM1O Port Structure

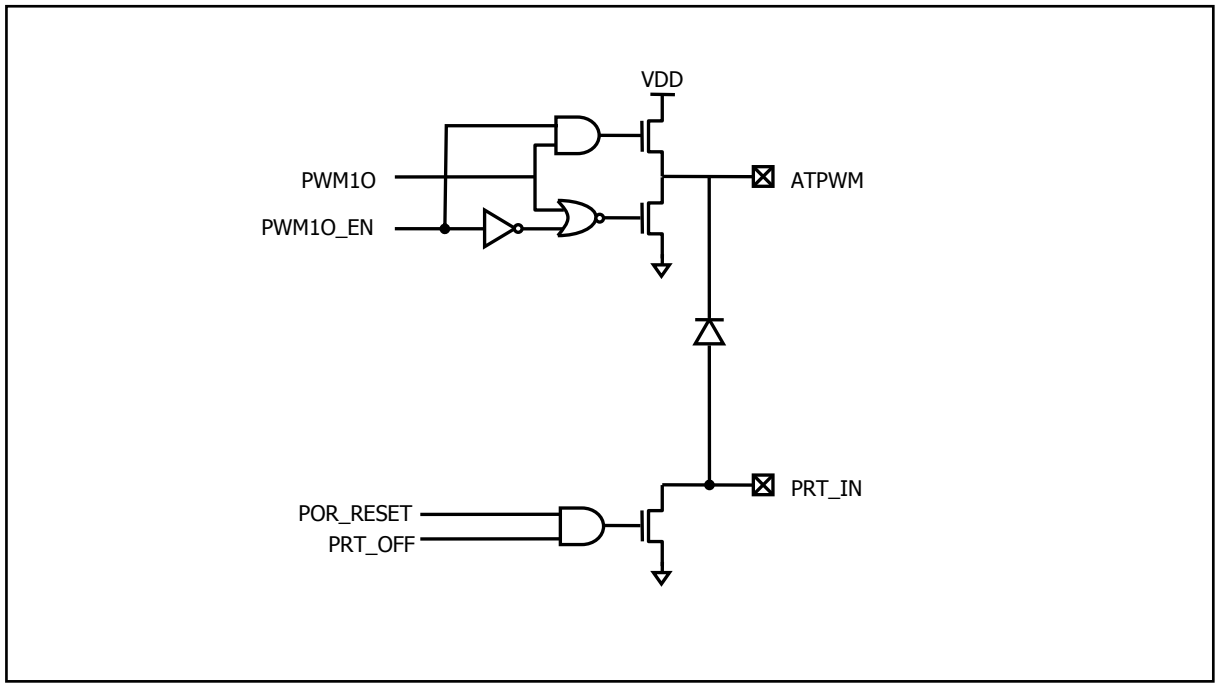


Figure 1.15 ATPWM/PRT_IN Port Structure

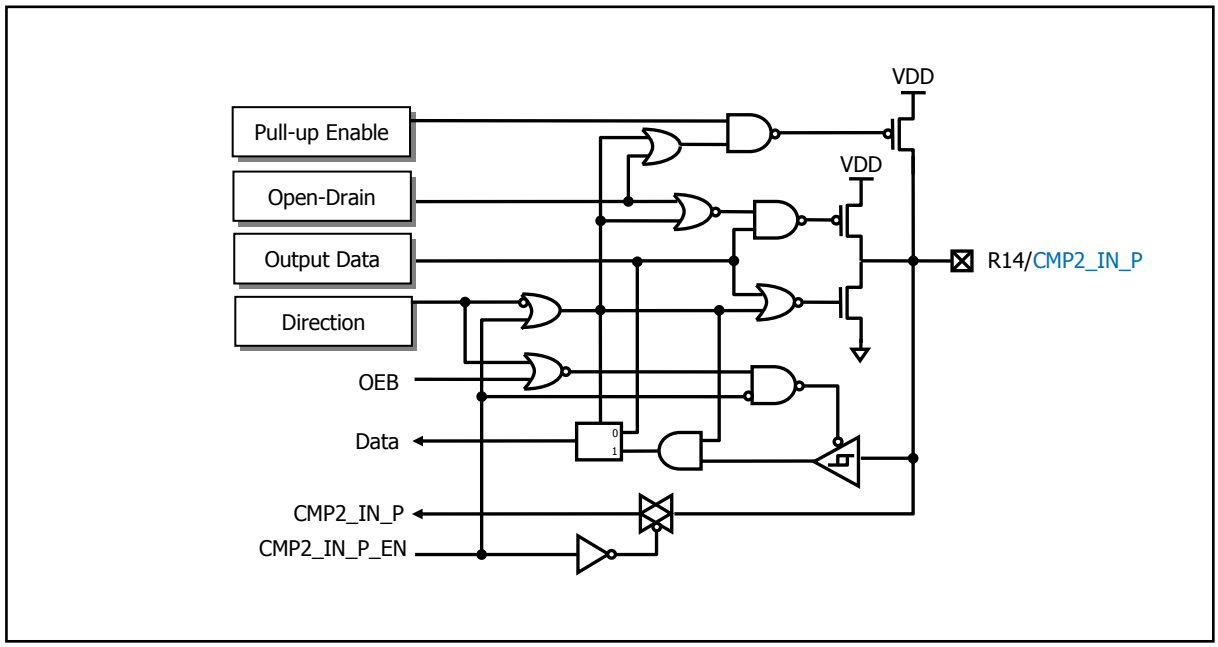


Figure 1.16 R14/CMP2_IN_P Port Structure

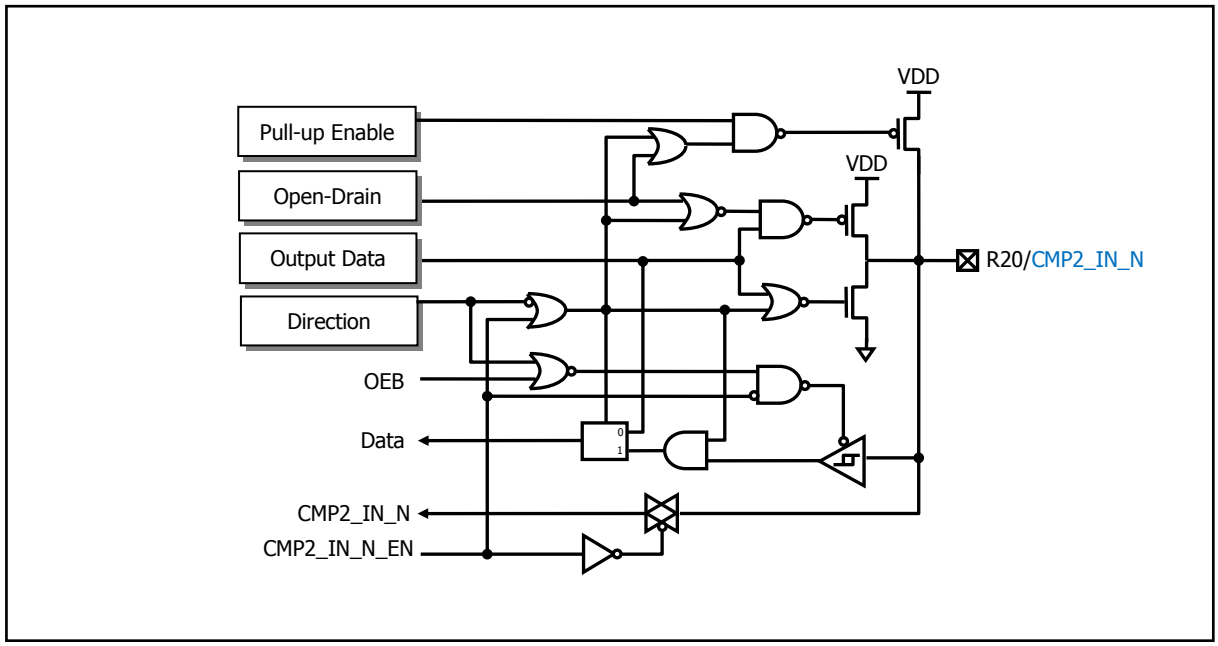


Figure 1.17 R20/CMP2_IN_N Port Structure

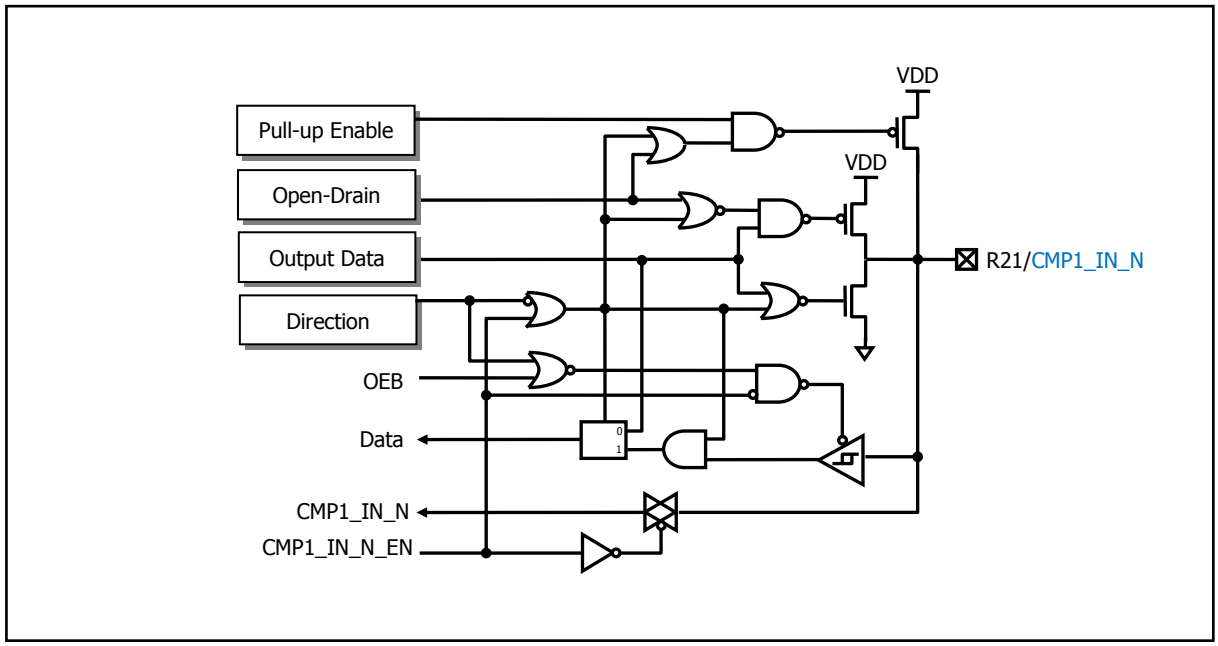


Figure 1.18 R21/CMP1_IN_N Port Structure

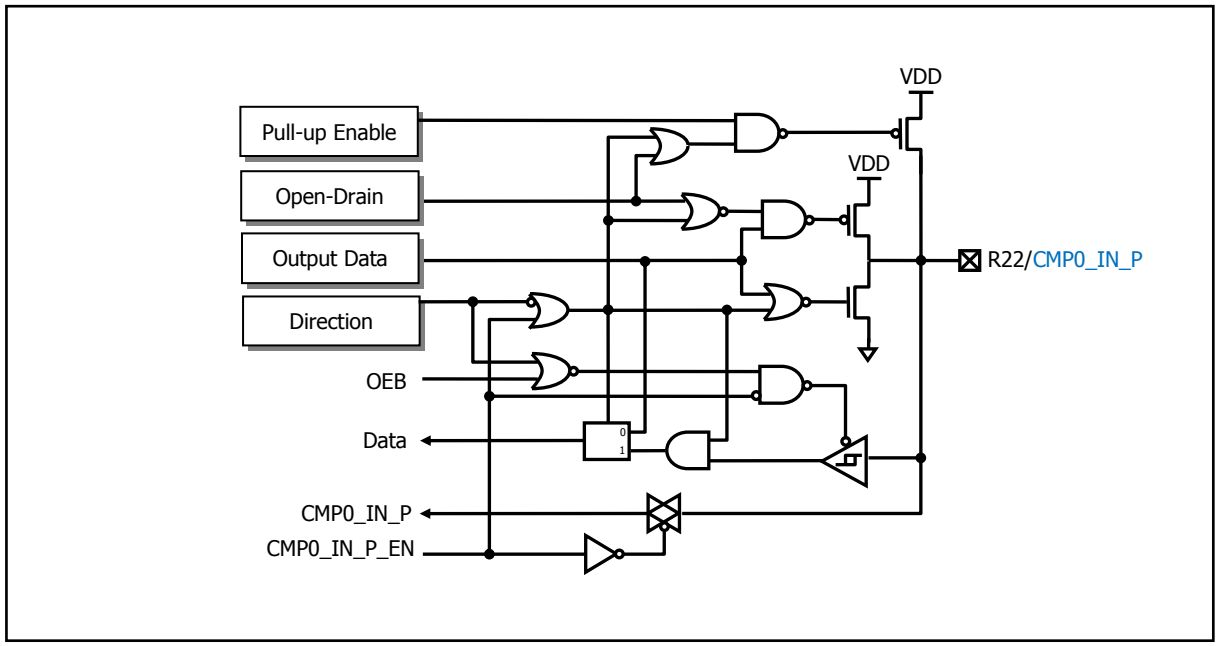


Figure 1.19 R22/CMP0_IN_P Port Structure

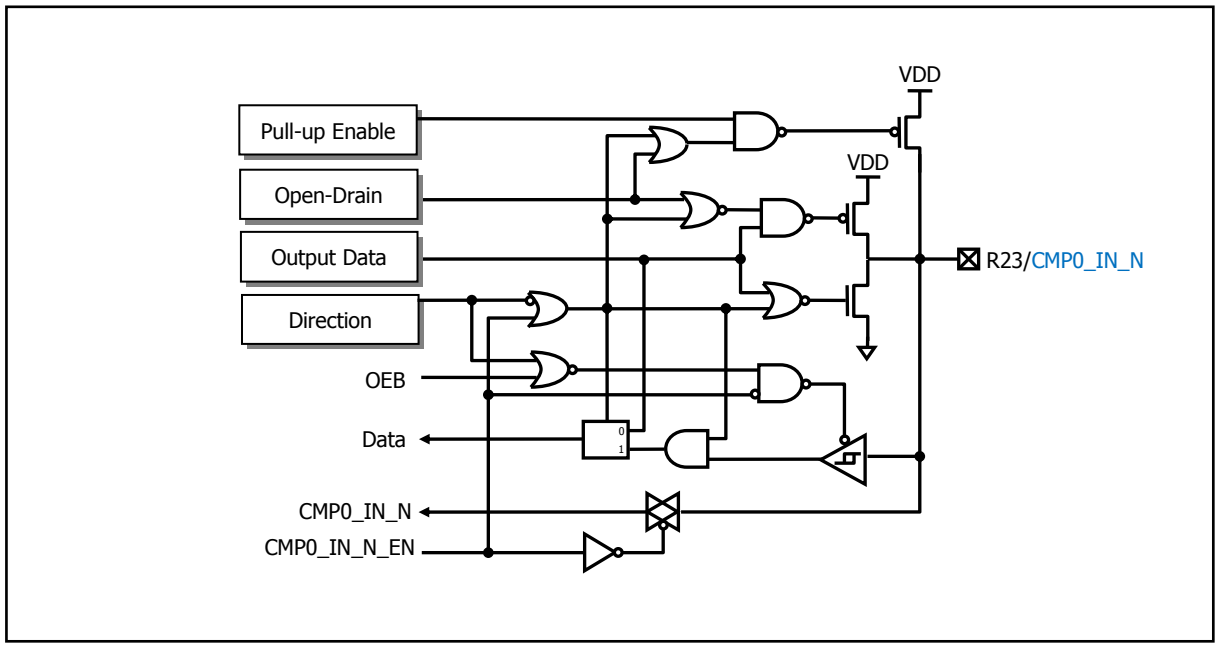


Figure 1.20 R23/CMP0_IN_N Port Structure

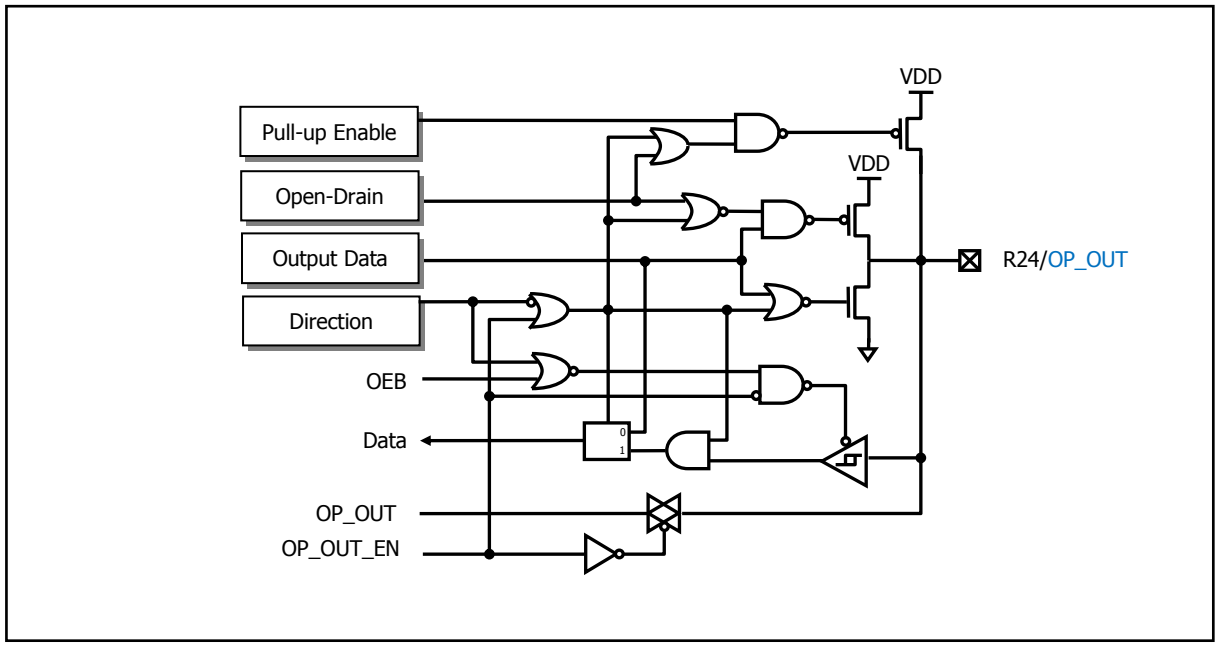


Figure 1.21 R24/OP_OUT Port Structure

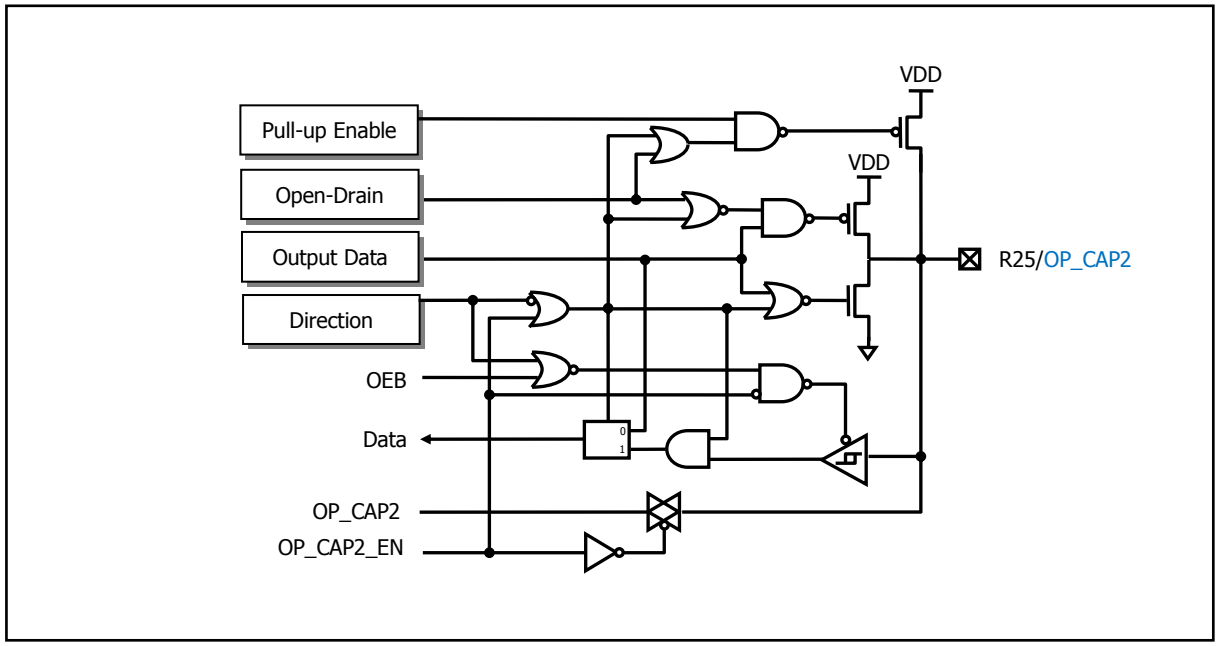


Figure 1.22 R25/OP_OUT Port Structure

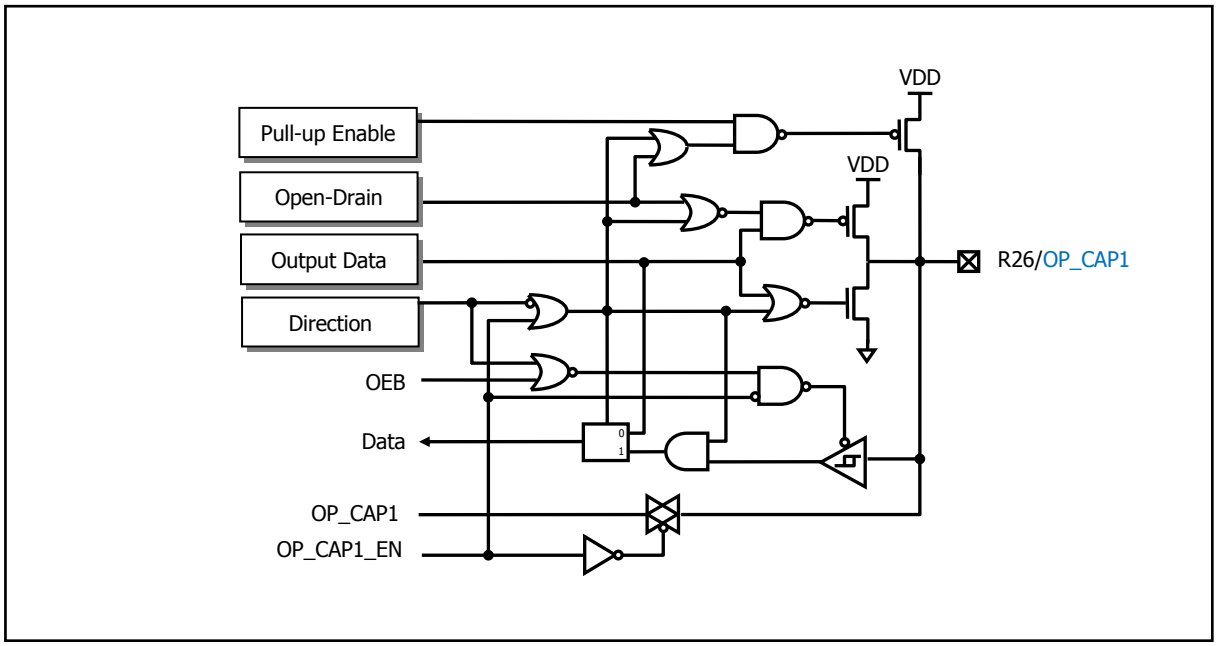


Figure 1.23 R26/OP_CAP1 Port Structure

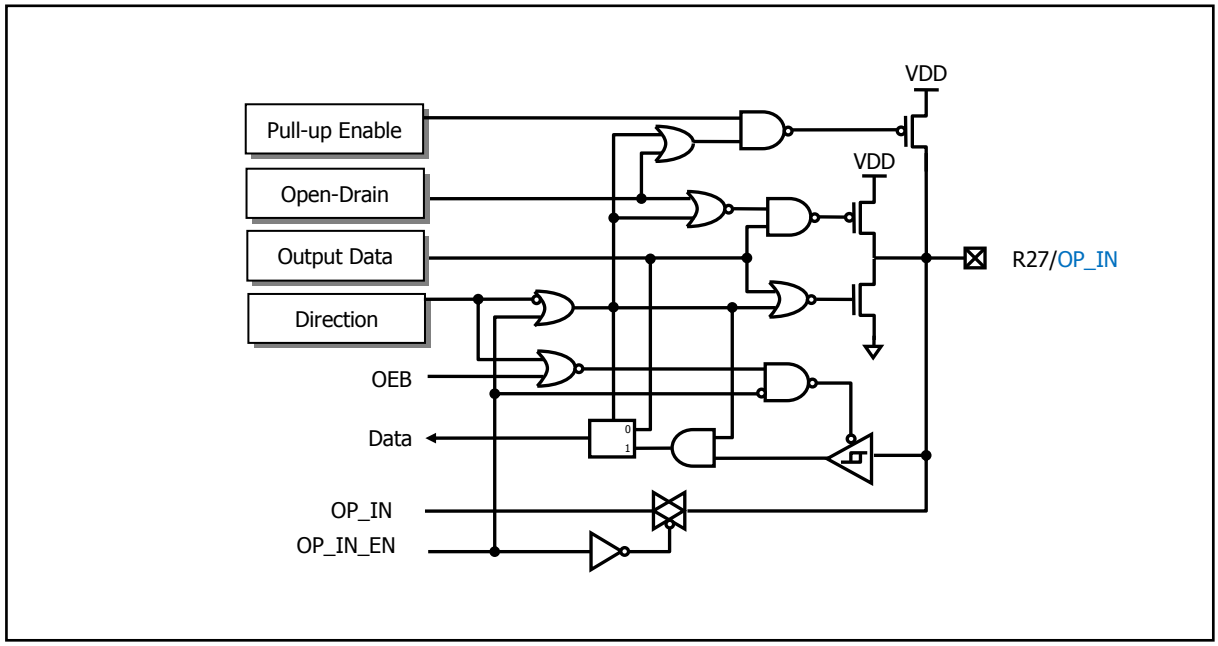


Figure 1.24 R27/OP_IN Port Structure

1.8 Electrical Characteristics

1.8.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3 ~ +6.0	V
	AVDD	VDD - 0.3 ~ VDD + 0.3	V
	AVSS	-0.3 ~ 0.3	V
Normal Voltage Pin	VI	-0.3 ~ VDD + 0.3	V
	VO	-0.3 ~ VDD+0.3	V
	IOH	10	mA
	∑IOH	80	mA
	IOL	20	mA
	IOL	160	mA
Total Power Dissipation	PT	600	mW
Storage Temperature	TSTG	-45 ~ +125	℃

Table 1.3 Absolute Maximum Ratings

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.8.2 Recommended Operating Condition

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VDD	fXIN = 12MHz	4.5		5.5	V
		fXIN = 4.0MHz *	2.7		5.5	V
Operating Temperature	TOPR	VDD=4.5 ~ 5.5V	-40		85	℃
		VDD=2.7 ~ 5.5V *	-40		85	℃
Operating Frequency	fXIN	VDD=4.5 ~ 5.5V	1		12	MHz
		VDD=2.7 ~ 5.5V	1		4.2	MHz

Table 1.4 Recommended Operating Condition

* This condition will be confirmed from the final test result.

1.8.3 A/D Converter Characteristics

(TA=-40~85℃, AVDD=VDD=5.12V, AIN=3.072V, VSS=VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Analog Power Supply Input Voltage Range	AVDD	-	VSS	-	VDD	V
Analog Input Voltage Range	VAN	-	VSS-0.3	-	AVDD+0.3	V
Conversion Current	ICON	VDD=3.072V fXIN = 4MHz	-	80	200	uA
Overall Accuracy	CAIN	-	-	±1.0	±2.0	LSB
Non Linearity Error	NNLE	fXIN = 4MHZ	-	±1.0	±2.0	LSB
Differential Non Linearity Error	NDNLE		-	±1.0	±2.0	LSB
Zero Offset Error	NZOE		-	±0.5	±1.5	LSB
Full Scale Error	NFSE		-	±0.25	±0.5	LSB
Gain Error	NGE		-	±1.0	±1.5	LSB
Conversion clock	TCONV	fMAIN = 4MHz	-	-	30	uS
Resolution	RES	-	-	8	-	bit

Table 1.5 A/D Converter Characteristics

1.8.4 DC Characteristics

Parameter	Symbol	PIN	Condition	Unit	Specification		
					Min	Typ	Max
'H' Input Voltage	V_{IH1}	X_{IN} , RESET	VDD = 4.5V – 5.5V	V	$0.8V_{DD}$	-	V_{DD}
	V_{IH2}	Normal Port (Schmitt Pin)			$0.8V_{DD}$	-	V_{DD}
'L' Input Voltage	V_{IL1}	X_{IN} , RESET	VDD = 4.5V – 5.5V	V	0	-	$0.2V_{DD}$
	V_{IL2}	Normal Port (Schmitt Pin)			0	-	$0.2V_{DD}$
Input Pull-up Current	I_P	R0,R1,R2	VI=0V, TA=25℃, V_{DD} = 5.0V	kΩ	25	50	100
			VI=0V, TA=25℃, V_{DD} = 3.0V		50	100	200
'H' Input Leakage Current	I_{IH}	All Pins (except Xin)	V_{DD} = 5.0V	uA	-	-	1
'L' Input Leakage Current	I_{IL}	All Pins (except Xin)	V_{DD} = 5.0V	uA	-1	-	-
'H' Output Voltage	V_{OH1}	R0,R1,R2	V_{DD} = 5.0V/I_{OH}=-	V	V_{DD}-1	-	-

Parameter		Symbol	PIN	Condition	Unit	Specification		
						Min	Typ	Max
				2mA				
		V_{OH2}	R05	V_{DD} = 5.0V/I_{OH}=-5mA	V	V_{DD}-1.5	-	-
'L' Output Voltage		V_{OL}	R0,R1,R2	V_{DD} = 5.0V/I_{OL}=15mA	V	-	-	2.0
Hysteresis		V_T	Schmitt Pin	V_{DD} = 5.0V	V	0.5	-	-
Power Current	Operating Current	I_{DD}	V_{DD}	f_{XIN}=12Mhz/ V_{DD}=5.5V	mA	-	6	12
	Idle Timer Current	$I_{idle-Timer}$	V_{DD}	f_{XIN}=12Mhz/ V_{DD}=5.5V	mA	-	1	2
	Stop Mode Current	I_{STOP1}	V_{DD}	f_{XIN}=12Mhz/ V_{DD}=5.5V CMP disable, OP amp disable, LVR off	uA	-	1	5
		I_{STOP2}	V_{DD}	f_{XIN}=12Mhz/ V_{DD}=5.5V CMP enable, OP amp enable, LVR	mA	-	-	1.5
	RCWDT Mode Current	I_{RCWDT}	V_{DD}	f_{XIN}=12Mhz/ V_{DD}=5.5V	uA	-	20	55
Internal RCWDT Period		T_{RCWDT}	X_{OUT}	V_{DD}=5.0V	us	25	-	90
Power On RESET		V_{POR}	V_{DD}	-	V	-	1.83	-
		V_{START}	V_{DD}	-	V	0	-	V_{POR}
		T_{RISE}	V_{DD}	-	V/ms	-	-	0.02
RESETB Input Noise Cancel Time		T_{RSTB_NC}	RESETB	V_{DD}=5.0V	us	1.5u		1.8u

Table 1.6 DC Characteristics

1.8.5 LVR (Low Voltage Reset) Electrical Characteristics

(TA = - 40 ℃ to + 85℃, VDD = 2.2 V to 5.5 V)

Parameter	Symbol	Condition	Unit	Specification		
				Min	Typ	Max
LVR Voltage	V_{LVR}	-	V	2.2	2.4	2.6
				2.5	2.7	2.9
				2.7	3.0	3.3
				3.6	4.0	4.4
VDD voltage rising time	t_R	-	uS	10	-	(note2)
VDD voltage off time	t_{OFF}	-	S	0.5	-	-
Hysteresis voltage of	Δ V	-	mV	-	10	100

Parameter	Symbol	Condition	Unit	Specification		
				Min	Typ	Max
LVR						
Current consumption	I_{LVR}	VDD = 3V	uA	-	45	80

Table 1.7LVR (Low Voltage Reset) Electrical Characteristics

NOTES:

1. The current of LVR circuit is consumed when LVR is enabled by "ROM Option".
2. 2^{16}/fx (= 6.55 ms at fx = 10 MHz)

1.8.6 Main Clock Oscillator Characteristics

(TA = - 10 ℃ to + 70℃, VDD = 2.2 V to 5.5 V)

Oscillator	Parameter	Condition	Specification			Unit
			Min	Typ	Max	
Crystal	Main oscillation frequency	2.2 V – 5.5 V	1.0	-	4.2	MHz
		2.7 V – 5.5 V	1.0	-	8.0	
		4.0 V – 5.5 V	1.0	-	12.0	
Ceramic Oscillator	Main oscillation frequency	2.2 V – 5.5 V	1.0	-	4.2	MHz
		2.7 V – 5.5 V	1.0	-	8.0	
		4.0 V – 5.5 V	1.0	-	12.0	
External Clock	X_{IN} input frequency	2.2 V – 5.5 V	1.0	-	4.2	MHz
		2.7 V – 5.5 V	1.0	-	8.0	
		4.0 V – 5.5 V	1.0	-	12.0	

Table 1.8 Main Clock Oscillator Characteristics

1.8.7 External RC Oscillation Characteristics

(TA = - 10 ℃ to + 70℃, VDD = 2.2 V to 5.5 V)

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
RC oscillator frequency range(Note 1)	fERC	TA = 25℃	1	-	8	MHz
Accuracy of RC oscillation(Note 2)	ACCERC	VDD =3.3V, TA = 25℃	-6	-	+6	%
		VDD =3.3V, TA = – 10 C to + 70℃	-12	-	+12	
RC oscillator setup time(Note 3)	tSUERC	TA = 25℃	-	-	10	mS

Table 1.9 External RC Oscillation Characteristics

NOTES:

1. The external resistor is connected between VDD and XIN pin and the 270pF capacitor is connected between XIN and VSS pin. (XOUT pin can be used as a normal port). The frequency is adjusted by external resistor.
2. The min/max frequencies are within the range of RC OSC frequency (1MHz to 8MHz)
3. Data based on characterization results, not tested in production

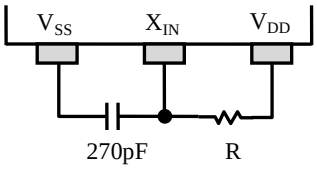


Figure 1.25 External Clock

1.8.8 Internal RC Oscillation Characteristics

(TA = - 40 ℃ to + 85℃, VDD = 2.2 V to 5.5 V)

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
RC oscillator frequency range(Note 1)	fIRC	VDD =3.3V, TA = 25℃	7.2	8.0	8.88	MHz
		VDD =3.3V, TA = – 10°C to + 70°C	6.4	8.0	9.6	
Clock duty ratio	TOD	-	40	50	60	%
RC oscillator setup time(Note 2)	tSUIRC	TA = 25℃	-	-	10	mS

Table 1.10 Internal RC Oscillation Characteristics

NOTES:

1. Data based on characterization results, not tested in production
2. XIN and XOUT pins can be used as I/O ports.

1.8.9 AC Characteristics

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Operating Frequency	fMCP	XIN	0.4		12	㎒
System Clock Cycle Time	tSYS		1 ÷ fMCP			ns
Oscillation Stabilization Time(4MHz)	tMST1	XIN,XOUT	20			㎳
External Clock “H” or “L” Pulse Width	tCPW	XIN	35			ns
External Clock Transition Time	tRCP,tFCP	XIN			20	ns
Interrupt Input Pulse Width	tIW	INT0 ~ INT3	2			tSYS
RESETB Input Pulse “L” Width	tRST	RESETB	8			tSYS
Event Counter Input “H” or “L” Pulse Width	tECW	EC0,EC1	2			tSYS
Event Counter Transition Time	tREC,tFEC	EC0,EC1			20	ns

Table 1.11 AC Characteristics

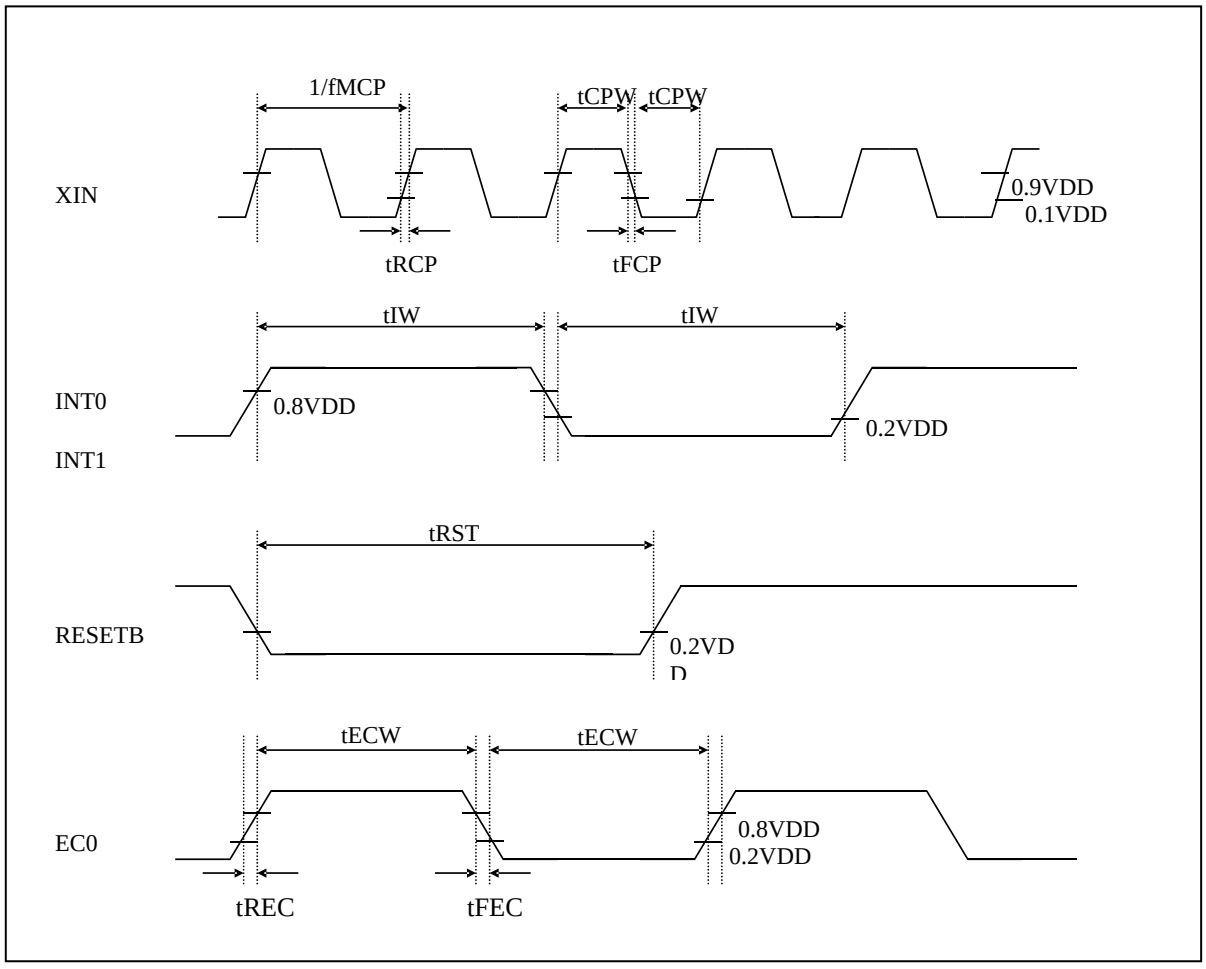


Figure 1.26 AC Characteristics Timing Diagram

1.8.10 Typical Characteristics

This graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range. The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean. 3σ) respectively where σ is standard deviation.

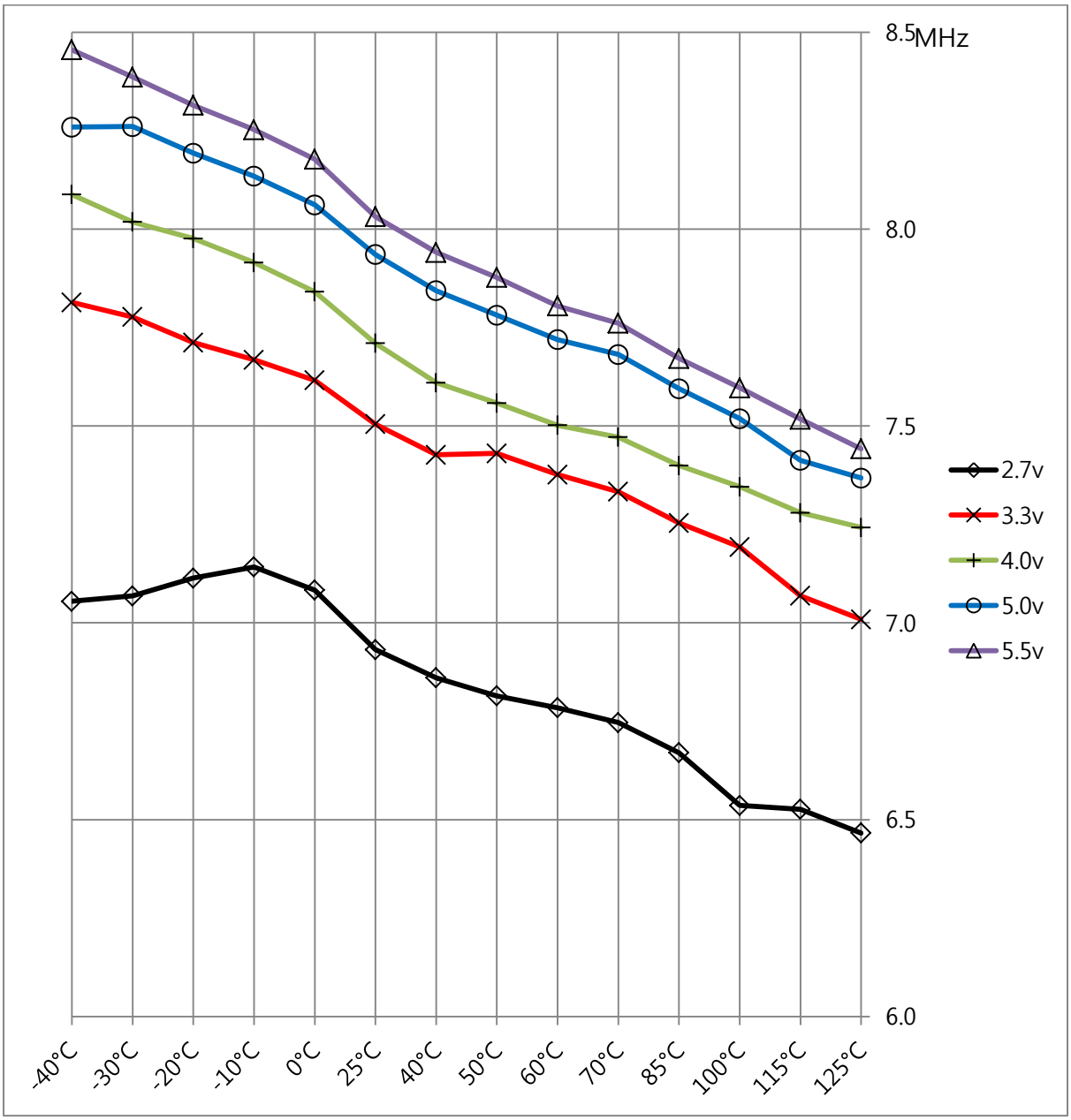


Figure 1-27 8MHz Int.OSC

2. Functional Description

2.1 Registers

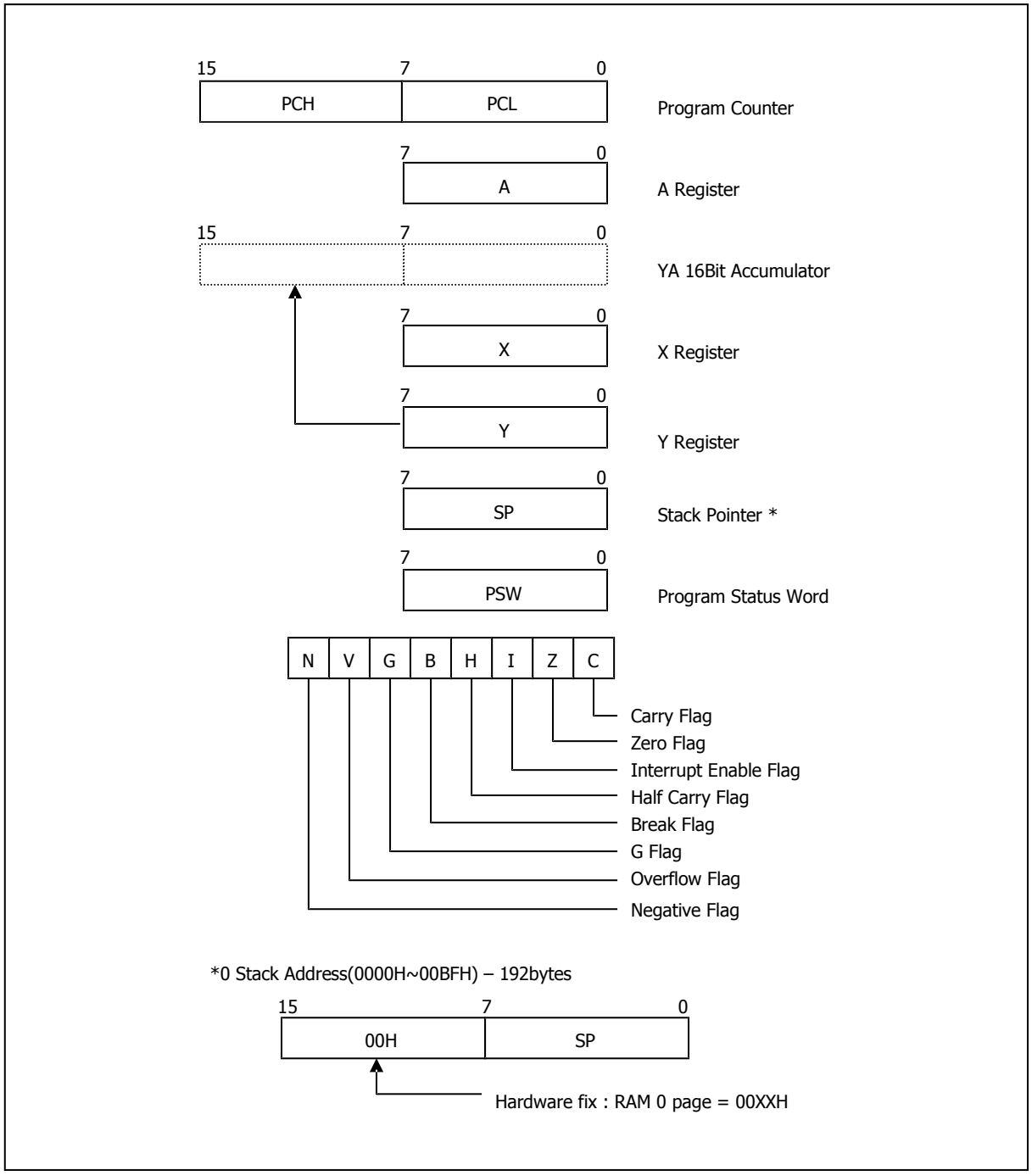


Figure 2.1 Registers

The MC81F6204 device is based on G800-Core which contains special internal registers, ALU buffers like A, X, Y, stack pointer SP, and program counter PC. The core's ALU operation results in program status word register (PSW).

The following figure describes the stack operation using stack pointer (SP) for each operation case-by-case.

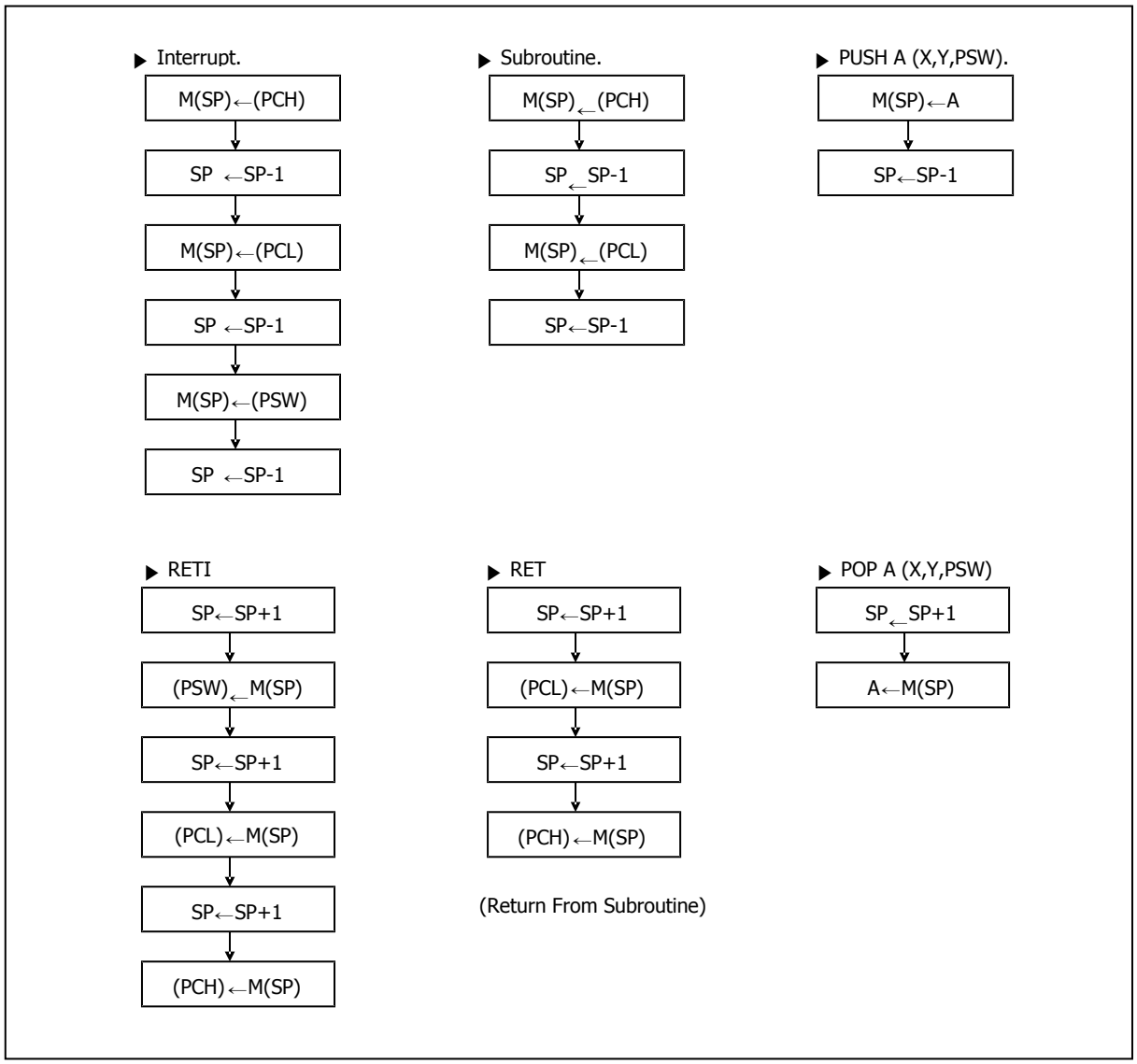


Figure 2.2 Stack Operation

2.2 Memory Map

The G800 Core contains 16bit program counter (PC) which can access the maximum 64k address space. The MC81F6204 has specific address space containing SRAM, registers, and FLASH ROM in 64K memory space.

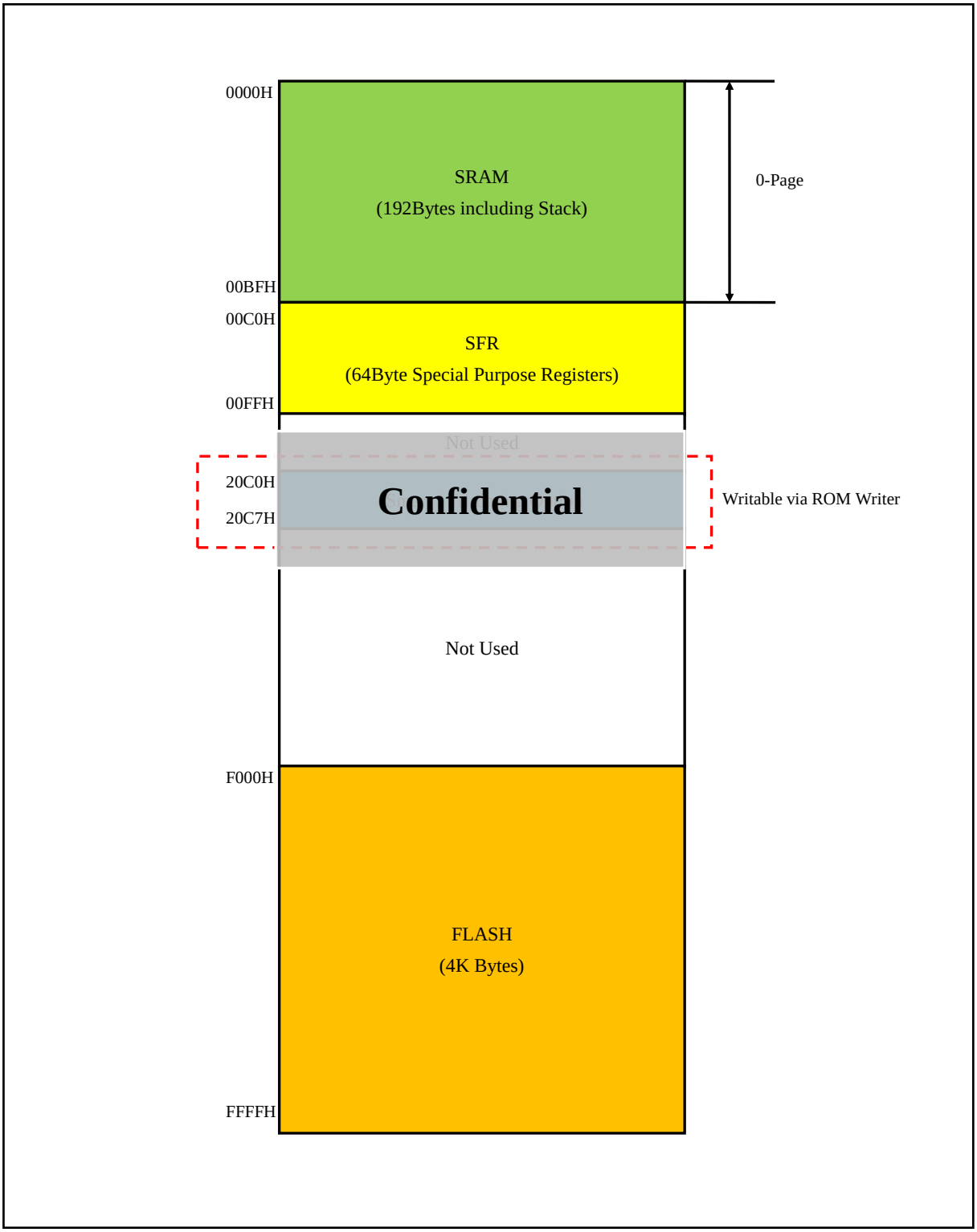


Figure 2.3 Memory Map

2.3 SMART Option

	SMART Option Address	Register Name								Test Register (Mirror)
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
Confidential										
System Mode	0x20C7	LVR ENB	LVR LEVEL SEL		FCLK DIV	LOCK	OSC Mode Selection			0x00CF

Table 2.1 Smart Option Bit Table

Confidential

(7) System Mode (@20C7)

20C5H	SM_20C5 (SMART Option 20C5 Area)							
SM_20C5[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SM_20C5					COM0 CLK		PPG PAD	PKG 20PIN

20C5H	SM_20C5 (SMART Option 20C5 Area)							
					DLY EN			
R/W	Can be only written by ROM Writer							
RESET	-	-	-	-	0	-	0	0

Table 2.2 Smart 20C5h Option

Address	[0]	Remark
20C5H	PKG 20PIN	20 Pin Package Selection
	0	24 Pin Package
	1	20 Pin Package -> R1[0], R1[1], R1[4] is input mode and pull up enabled

Address	[1]	Remark
20C5H	PPG PAD	PPG, PRT PIN Pad Selection
	0	R05 /PWM3O, R06/AN4/PWM1O
	1	ATPWMO, PRT_IN

Address	[3]	Remark
20C5H	COM0 CLK DLY EN	Comparator0 Low Pass Filter Clock Delay Enable 16T and PWM1O's Period is selected with CMPLPF0[1:0]. CMPLPF0[1:0] & 20C5H[3] : 110(16T), 111(PWM1O's Period)
	0	16T – In case Comparator0 LPF Clock Source (CMPLPF0[1:0]) is 11.
	1	PWM1O's Period - In case Comparator0 LPF Clock Source (CMPLPF0[1:0]) is 11.

20C7H	SM_20C7 (SMART Option 20C7 Area)							
SM_20C7[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SM_20C7	LVRENB	LVRLS[1:0]		FCLK_DIV	LOCK	OSCS[2:0]		
R/W	Can be only written by ROM writer							
RESET	0	0	0	0	0	0	0	0

Table 2.3 Smart 20C7h Option

Address	[7]	Remark
20C7H	LVRENB	Low-Voltage-Reset Enable (active low)
	0	LVR Enabled (default) - RSTB Pin can be used as normal I/O
	1	LVR Disabled (using External RSTB)

Address	[6]	[5]	Remark
20C7H	LVRLS[2:0]		LVR Level Selection

	0	0	2.2V
	0	1	2.7V
	1	0	3.0V
	1	1	4.0V

Address	[4]	Remark
20C7H	FCLK DIV	FCLK 1/2 Selection
	0	Default FCLK is System Clock
	1	System Clock SCLK is FCLK/2

FCLK is main clock (external XTAL or internal osc clock source)

Address	[3]	Remark
20C7H	LOCK	Flash Access Lock
	0	Code Protection Disabled
	1	Code Protection Enabled (can't read or PGM by Writer before entirely erased)

Address	[2]	[1]	[0]	Remark	
20C7H	OSCS[2:0]			System Clock Selection	
	0	0	0	External RC (8Mhz @ R=30K) – XOUT pin can be used as normal I/O	
	0	0	1	Internal Oscillator (4Mhz)	XIN/XOUT pin can be used as normal I/O
	0	1	0	Internal Oscillator (2Mhz)	
	0	1	1	Internal Oscillator (1Mhz)	
	1	0	0	Internal Oscillator (8Mhz)	
	1	0	1	Not Available	
	1	1	0	Not Available	
	1	1	1	Crystal / Ceramic Resonator	

Table 2.4 Oscillator Mode Selection on Normal Mode

2.4 TCALL & Interrupt Vector

2.4.1 PCALL and TCALL Area

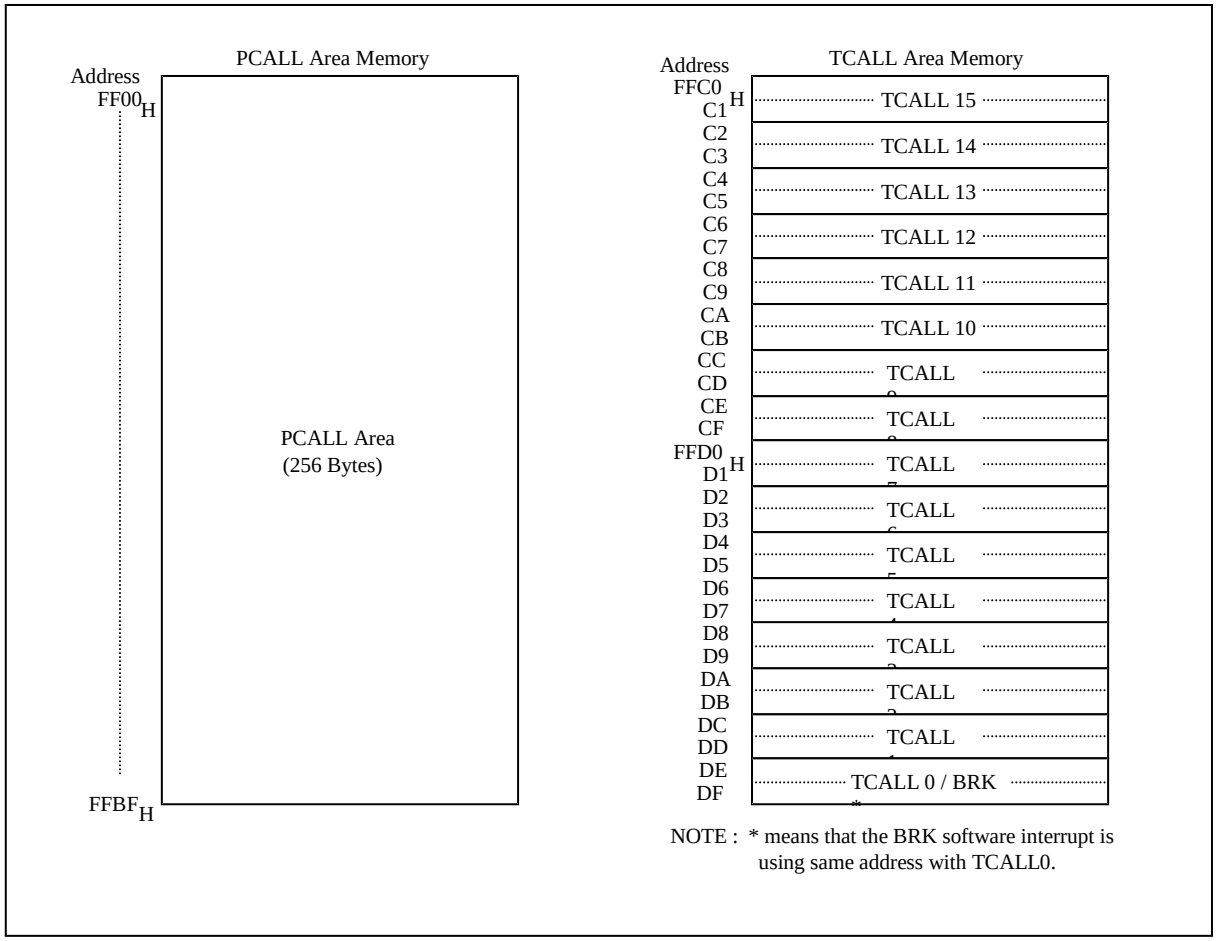


Figure 2.4 PCALL and TCALL Area Map

2.4.2 Interrupt Vector Area

Request Source	Symbol	Priority	MASK	Vector High	Vector Low
Hardware Reset	RESETB	0	Non Maskable	FFFFh	FFFEh
External Interrupt 0	INT0	1	Maskable	FFFDh	FFFCh
External Interrupt 1	INT1	2		FFFBh	FFFAh
External Interrupt 2	INT2	3		FFF9h	FFF8h
External Interrupt 3	INT3	4		FFF7h	FFF6h
Analog Comparator 0	CMP0	5		FFF5h	FFF4h
Analog Comparator 1	CMP1	6		FFF3h	FFF2h
Analog Comparator 2	CMP2	7		FFF1h	FFF0h
Analog Comparator 3	CMP3	8		FFEFh	FFEEh

Request Source	Symbol	Priority	MASK	Vector High	Vector Low
Analog Comparator 4	CMP4	9		FFEDh	FFECh
Timer 0 Interrupt	T0	10		FFEBh	FFEAh
Timer 1 Interrupt	T1	11		FFE9h	FFE8h
Timer 3 Interrupt	T3	12		FFE7h	FFE6h
ADC Interrupt	ADC	13		FFE5h	FFE4h
WDT Interrupt	WDT	14		FFE3h	FFE2h
BIT Interrupt	BIT	15		FFE1h	FFE0h

Table 2.5 Interrupt Vector Area

2.5 Peripheral Registers

Address	Function	Symbol	R/W	Reset Value							
				7	6	5	4	3	2	1	0
00C0H	Port R0 Data Register	R0	R/W	0	0	0	0	0	0	0	0
00C1H	Port R0 Direction Register	R0IO	W	0	0	0	0	0	0	0	0
00C2H	Port R1 Data Register	R1	R/W	0	0	0	0	0	0	0	0
00C3H	Port R1 Direction Register	R1IO	W	0	0	0	0	0	0	0	0
00C4H	Port R2 Data Register	R2	R/W	0	0	0	0	0	0	0	0
00C5H	Port R2 Direction Register	R2IO	W	0	0	0	0	0	0	0	0
00C6H	R0 Pull Up Register	R0PU	W	0	0	0	0	0	0	0	0
00C7H	R1 Pull Up Register	R1PU	W	0	0	0	0	0	0	0	0
00C8H	R2 Pull Up Register	R2PU	W	0	0	0	0	0	0	0	0
00C9H	R0 Open Drain Register	R0OD	W	0	0	0	0	0	0	0	0
00CAH	R1 Open Drain Register	R1OD	W	0	0	0	0	0	0	0	0
00CBH	R2 Open Drain Register	R2OD	W	0	0	0	0	0	0	0	0
00CCH	Reserved										
00CDH	Reserved										
00CEH	Buzzer Driver Register	BUZR	W	1	1	1	1	1	1	1	1
00CFH	Reserved										
00D0H	Timer 0 Mode Control Register	T0CR	R/W			0	0	0	0	0	0
00D1H	Timer 0 Register	T0	R	0	0	0	0	0	0	0	0
	Timer 0 Data Register	T0DR	W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	CDR0	R	0	0	0	0	0	0	0	0
00D2H	Timer 1 Mode Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
00D3H	Timer 1 Data Register	T1DR	W	1	1	1	1	1	1	1	1
	Timer 1 PWM Period Register	T1PPR	W	1	1	1	1	1	1	1	1

Address	Function	Symbol	R/W	Reset Value							
				7	6	5	4	3	2	1	0
00D4H	Timer 1 Register	T1	R	0	0	0	0	0	0	0	0
	Timer 1 PWM Duty Register	T1PDR	R/W	0	0	0	0	0	0	0	0
	Timer 1 Capture Data Register	CDR1	R	0	0	0	0	0	0	0	0
00D5H	Timer 1 PWM High Register	T1PWHR	W					0	0	0	0
00D6H	Reserved										
00D7H	Reserved										
00D8H	Timer 3 Mode Control Register	T3CR	R/W	0	0	0	0	0	0	0	0
00D9H	Timer 3 Data Register	T3DR	W	1	1	1	1	1	1	1	1
	Timer 3 PWM Period Register	T3PPR	W	1	1	1	1	1	1	1	1
	Timer3 Auto Triggering PWM Maximum Period Register	ATMPR	R/W	1	1	1	1	1	1	1	1
00DAH	Timer 3 Register	T3	R	0	0	0	0	0	0	0	0
	Timer 3 PWM Duty Register	T3PDR	R/W	0	0	0	0	0	0	0	0
	Timer 3 Auto Triggering PWM Duty Register	ATDR	R/W	0	0	0	0	0	0	0	0
	Timer 3 Capture Data Register	CDR3	R	0	0	0	0	0	0	0	0
00DBH	Timer 3 PWM High Register	T3PWHR	W					0	0	0	0
	Timer 3 Auto Triggering PWM High Register	ATPWHR	W			0	0			0	0
			R			0	0	0	0	0	0
00DCH	Timer 3 Auto Triggering PWM Control Register	ATCR	R/W	0	0	0	0	0	0	0	0
00DDH	Timer 3 Auto Triggering PWM Duty Buffer Register	ATDBR	R	0	0	0	0	0	0	0	0
00DEH	Timer 3 Auto Triggering PWM Flag Register	ATPWFR	R/W					0	0	0	0
00DFH	Timer 3 Auto Triggering PWM Step Register	ATSTEP	R/W	0	0	0	0	0	0	0	0
00E0H	8bit A/D Converter Control Register	ADCM	R/W		0		0	0	0	0	1
00E1H	8bit A/D Converter Result Register	ADCR	R	-	-	-	-	-	-	-	-
00E2H	Reserved										
00E3H	Reserved										
00E4H	Reserved										
00E5H	LVR Control Register for POR on/off	PORC	W	0	0	0	0	0	0	0	0
00E6H	Clock Control Register	CKCTLR	W	0		0	1	0	1	1	1
	BIT Counter Value Register	BITR	R	0	0	0	0	0	0	0	0
00E7H	Reserved										
00E8H	Watch Dog Timer Register	WDTR	W	0	1	1	1	1	1	1	1
00E9H	Sleep and Stop Mode Control Register	SSCR	W	0	0	0	0	0	0	0	0
00EAH	Comparator Control Register	CMPCR	R/W	0	0	0	0	0	-	0	1
00EBH	Comparator Emergency Channel Selection Register	CMPEMCR	R/W	0	0	1	1	1	0	0	1

Address	Function	Symbol	R/W	Reset Value							
				7	6	5	4	3	2	1	0
00ECH	Comparator Positive Input Selection Register0	CMPPIN0	R/W	0	0	0	0	0	0	1	0
00EDH	Comparator Positive Input Selection Register1	CMPPIN1	R/W							0	1
00EEH	Comparator Edge Selection Register0	CMPEDS0	R/W	1	0	1	0	1	0	1	0
00EFH	Comparator Edge Selection Register1	CMPEDS1	R/W							1	0
00F0H	Comparator Low Pass Filter Control Register0	CMPLPF0	R/W	0	1	0	1	0	1	0	1
00F1H	Comparator Low Pass Filter Control Register1	CMPLPF1	R/W							0	1
00F2H	Operational Amplifier Control Register	AMPCR	R/W	0	-	-	-	-	0	0	0
00F3H	Port Selection Register 0	PSR0	W	0	0	0	0	0	0	0	0
00F4H	Port Selection Register 1	PSR1	W	0	0	0	0	0	0	0	0
00F5H	Port Selection Register 2	PSR2	W					0	0	0	0
00F6H	Interrupt Enable Register High	IENH	R/W	0	0	0	0	0	0	0	0
00F7H	Interrupt Enable Register Low	IENL	R/W	0	0	0	0	0	0	0	
00F8H	Interrupt Request Register High	IRQH	R/W	0	0	0	0	0	0	0	0
00F9H	Interrupt Request Register Low	IRQL	R/W	0	0	0	0	0	0	0	
00FAH	Reserved										
00FBH	Reserved										
00FCH	Interrupt Edge Selection Register	IEDS	R/W	0	0	0	0	0	0	0	0
00FDH	Interrupt Vector Test Register	INTV	R	0	0	0	0	0	0	0	0
00FEH	Reserved										
00FFH	Reserved										

Table 2.6 Peripheral Registers

2.6 I/O Port

2.6.1 R0 Port Group

00C0H	**R0 (R0 Data Register)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R0	R07	R06	R05	R04	R03	R02	R01	R00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

R0[7:0] – Port R0 Group Read or Output Data, Bit Handling Available

Table 2.7 R0 Data Register

00C1H	R0IO (R0 Direction Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R0IO	R0IO7	R0IO6	R0IO5	R0IO4	R0IO3	R0IO2	R0IO1	R0IO0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.8 R0IO - R0 Direction Register

0: Input Mode, 1: Output Mode

00C6H	R0PU (R0 Pull-up Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R0PU	R0PU7	R0PU6	R0PU5	R0PU4	R0PU3	R0PU2	R0PU1	R0PU0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.9 R0PU - R0 Pull Up Register

0: Internal Pull-up Register Off, 1: Internal Pull-up On

00C9H	R0OD (R0 Open-Drain Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R0OD	R0OD7	R0OD6	R0OD5	R0OD4	R0OD3	R0OD2	R0OD1	R0OD0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.10 R0OD - R0 Open-Drain Register

0: Push-Pull, 1: Open-Drain

2.6.2 R1 Port

00C2H	R1 (R1 Data Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R1	-	-	-	R14	R13	R12	R11	R10
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
RESET	-	-	-	0	0	0	0	0

Table 2.11 R1 - R1 Data Register

R1[7:0] – Port R1 Group Read or Output Data, Bit Handling Available

00C3H	R1IO (R1 Direction Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]

R1IO	-	-	-	R1IO4	R1IO3	R1IO2	R1IO1	R1IO0
R/W	-	-	-	W	W	W	W	W
RESET	-	-	-	0	0	0	0	0

Table 2.12 R1IO – R1 Direction Register

0: Input Mode, 1: Output Mode

00C7H	R1PU (R1 Pull-up Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R1PU	R1PU7	R1PU6	R1PU5	R1PU4	R1PU3	R1PU2	R1PU1	R1PU0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.13 R1PU – R1 Pull Up Register

0: Internal Pull-up Off, 1: Internal Pull-up On

00CAH	R1OD (R1 Open-Drain Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R1OD	R1OD7	R1OD6	R1OD5	R1OD4	R1OD3	R1OD2	R1OD1	R1OD0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.14 R1OD – R1 Open-Drain Register

0: Push-Pull, 1: Open-Drain

2.6.3 R2 Port

00C4H	R2 (R2 Data Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R2	R27	R26	R25	R24	R23	R22	R21	R20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 2.15 R2 – R2 Data Register

R2[7:0] – Port R2 Group Read or Output Data, Bit Handling Available

00C5H	R2IO (R1 Direction Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R2IO	R2IO7	R2IO6	R2IO5	R2IO4	R2IO3	R2IO2	R2IO1	R2IO0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.16 R2IO – R2 Direction Register

0: Input Mode, 1: Output Mode

00C8H	R2PU (R2 Pull-up Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R2PU	R2PU7	R2PU6	R2PU5	R2PU4	R2PU3	R2PU2	R2PU1	R2PU0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.17 R2PU – R2 Pull Up Register

0: Internal Pull-up Register Off, 1: Internal Pull-up On

00CBH	R2OD (R2 Open-Drain Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R2OD	R2OD7	R2OD6	R2OD5	R2OD4	R2OD3	R2OD2	R2OD1	R2OD0
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.18 R2OD – R2 Open-Drain Register

0: Push-Pull, 1: Open-Drain

2.6.4 Port Selection Registers

00F3H	PSR0 (Port Selection Register 0)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PSR0	INT3E	INT2E	INT1E	INT0E	BUZOE	EC0E	T0OE	PWM1OE
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 2.19 PSR0 - Port Selection Register 0

INT3E is only available for 24pin package.

Address	[7]	Remark
00F3H	INT3E	INT3 Input Selection
	0	R11 Port
	1	INT3 Input Port

Address	[6]	Remark
00F3H	INT2E	INT2 Input Selection
	0	R04 Port

	1	INT2 Input Port

Address	[5]	Remark
00F3H	INT1E	INT1 Input Selection
	0	R03 Port
	1	INT1 Input Port

Address	[4]	Remark
00F3H	INT0E	INT0 Input Selection
	0	R02 Port
	1	INT0 Input Port

Address	[3]	Remark
00F3H	BUZOE	Buzzer Output Selection
	0	R07 Port
	1	Buzzer Output Port

Address	[2]	Remark
00F3H	EC0E	Event Counter Input Selection
	0	R12 Port
	1	EC0 Input Port

Address	[1]	Remark
00F3H	T0OE	Timer0 Output Selection
	0	R07
	1	Timer0 Output Port

Address	[0]	Remark
00F3H	PWM1OE	PWM1 Output Selection
	0	R06 Port
	1	PWM1O Output Port

00F4H	**PSR1 (Port Selection Register 1)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PSR1	CMP0_P	CMP0_N	OP_OUT	OP_CAP2	OP_CAP1	OP_IN	AVDD	PWM3OE
R/W	W	W	W	W	W	W	W	W

RESET	0	0	0	0	0	0	0	0

Table 2.20 PSR1 - Port Selection Register 1

Address	[7]	Remark
00F4H	CMP0_P	Comparator0 Input Selection
	0	R22 Port
	1	Comparator0 Positive Input Selection

Address	[6]	Remark
00F4H	CMP0_N	Comparator0 Input Selection
	0	R23 Port
	1	Comparator0 Negative Input Selection

Address	[5]	Remark
00F4H	OP_OUT	Op-Amp Output Selection
	0	R24 Port
	1	Op-Amp Output Port

Address	[4]	Remark
00F4H	OP_CAP2	Op-Amp External Capacitor Selection
	0	R25 Port
	1	Op-Amp External Capacitor Pin

Address	[3]	Remark
00F4H	OP_CAP1	Op-Amp External Capacitor Selection
	0	R26 Port
	1	Op-Amp External Capacitor Pin

Address	[2]	Remark
00F4H	OP_IN	Op-Amp Input Selection
	0	R27
	1	Op-Amp Input Port

Address	[1]	Remark
00F4H	AVDD	AVDD Analog Voltage Selection
	0	R13
	1	AVDD Voltage Used

Address	[0]	Remark
00F4H	PWM3OE	PWM3 Output Selection
	0	R05
	1	PWM3O Output Port

00F5H	**PSR2 (Port Selection Register 2)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PSR2	-	-	-	-	CMP4_N	CMP2_P	CMP2_N	CMP1_N
R/W	-	-	-	-	W	W	W	W
RESET	-	-	-	-	0	0	0	0

Table 2.21 PSR2 - Port Selection Register 2

CMP4_N is only available for 24pin package.

CMP2_P is only available for 24pin package.

Address	[3]	Remark
00F5H	CMP4_N	Comparator 4 Input Selection
	0	R10
	1	Comparator 4 Negative Input Port

Address	[2]	Remark
00F5H	CMP2_P	Comparator 2 Input Selection
	0	R14
	1	Comparator 2 Positive Input Port

Address	[1]	Remark
00F5H	CMP2_N	Comparator 2 Input Selection
	0	R20
	1	Comparator 2 Negative Input Port

Address	[0]	Remark
00F5H	CMP1_N	Comparator 1 Input Selection
	0	R21
	1	Comparator 1 Negative Input Port

3. Peripheral Hardware

3.1 System Configuration (ROM Option)

The system configuration is loaded into register buffer from FLASH special region on Power-on-Reset (POR), External PAD Reset, or Low-Voltage-Reset (LVR) release. The configuration area can only be accessed by ROM writer. The default value is 00h. The following table describes the details of the system configuration value.

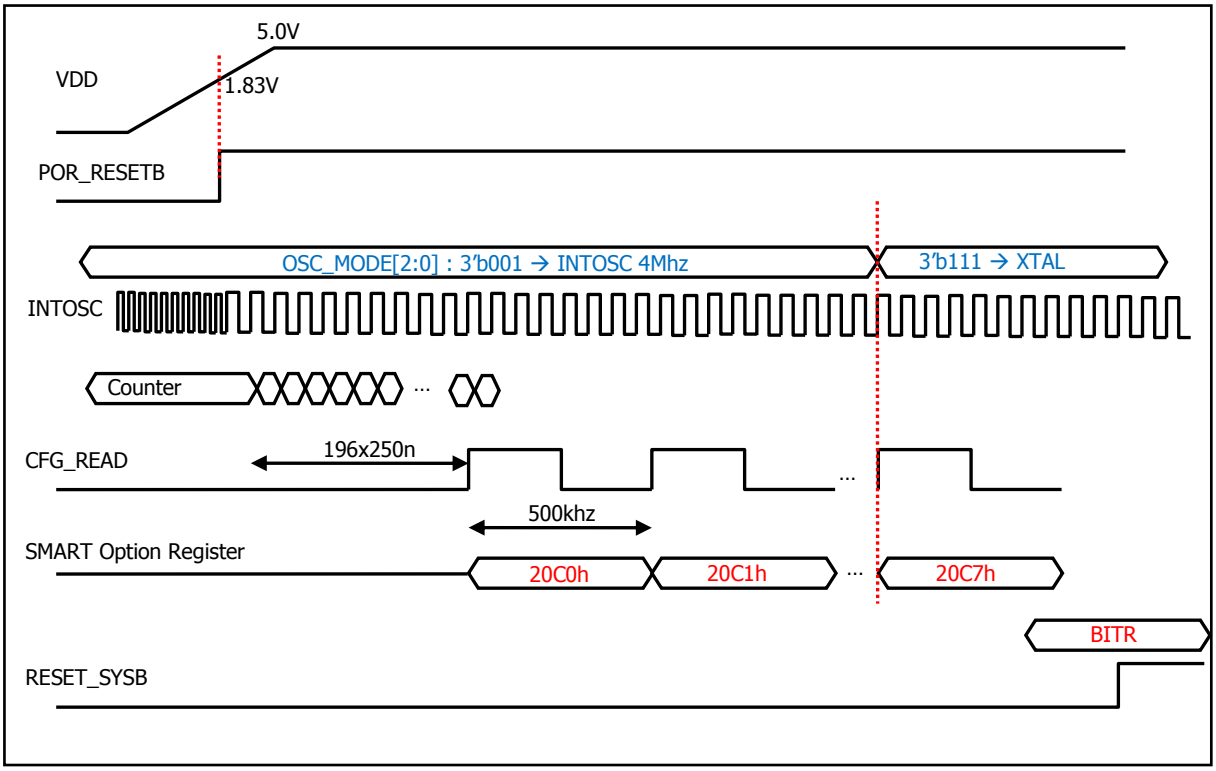


Figure 3.1 Smart Option Read Timing

20C7H	SYSCFG (System Configuration)							
SYSCFG[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SYSCFG	LVRENB	LVRLS[1:0]		FCLK DIV	LOCK	OSCS[2:0]		
R/W	Can be only written by ROM writer							
RESET	0	0	0	-	0	0	0	0

Table 3.1 System Configuration Option

Address	[7]	Remark
20C7H	LVRENB	Low-Voltage-Reset Enable (active low)
	0	LVR Enabled (default) - RSTB Pin can be used as normal I/O
	1	LVR Disabled (using External RSTB)

Address	[6]	[5]	Remark
20C7H	LVRLS[2:0]		LVR Level Selection
	0	0	2.2V
	0	1	2.7V
	1	0	3.0V
	1	1	4.0V

Address	[4]	Remark
20C7H	LOCK	Flash Access Lock
	0	Code Protection Disabled
	1	Code Protection Enabled (can't read or PGM by Writer before entirely erased)

Address	[2]	[1]	[0]	Remark	
20C7H	OSCS[2:0]			System Clock Selection	
	0	0	0	External RC (8Mhz @ R=30K) – XOUT pin can be used as normal I/O	
	0	0	1	Internal Oscillator (4Mhz)	XIN/XOUT pin can be used as normal I/O
	0	1	0	Internal Oscillator (2Mhz)	
	0	1	1	Internal Oscillator (1Mhz)	
	1	0	0	Internal Oscillator (8Mhz)	
	1	0	1	Not Available	
	1	1	0	Not Available	
	1	1	1	Crystal / Ceramic Resonator	

00E5H	**PORC (POR Control Register)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SSCR	PORC[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 3.2 Power-On-Reset Control Register (PORC)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Remark
00E5H	PORC[7:0]								POR Control Register
	0	1	0	1	1	0	1	0	POR Disable (prevent static current of LVR circuit)
	0	0	0	0	0	0	0	0	Default POR Enabled (1.83V)

3.2 SLEEP and STOP

The entire hardware including G800 Core and Peripherals has STOP or SLEEP mode for low power feature. The SLEEP/STOP can be enabled via register access by writing 5Ah/0Fh. The following is a table describing Sleep Stop Control Register (SSCR).

00E9H	SSCR (Stop & Sleep Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SSCR	SSCR[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0

Table 3.3 Stop & Sleep Mode Control Register

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Remark
00E9H	SSCR[7:0]								Stop & Sleep Control Register
	0	1	0	1	1	0	1	0	Stop Mode Enabled
	0	0	0	0	1	1	1	1	Sleep Mode Enabled

To enter the STOP mode, SSCR must be configured before STOP instruction. To enter the SLEEP mode, just write 0Fh to SSCR.

In the Sleep/Stop mode, the core and peripherals has each states summarized in the following table.

Peripherals	STOP Mode	SLEEP Mode
CPU	All CPU operation are disabled	All CPU operations are disabled
RAM	Retain	Retain
BIT	Halted	Operates Continuously
WDT	Stop (except RCWDT mode)	Operates Continuously
TIMER0/1	Halted (except Event Counter Mode)	Operates Continuously
BUZZER	Stop	Operates Continuously
ADC	Stop	Stop
MAIN OSC	Stop (Xin=L, Xout=H)	Oscillation
I/O Port	Retain	Retain
Control Registers	Retain	Retain
Comparator	Disabled, (or can be enabled)	Disabled, (or can be enabled)
OP AMP	Disabled	Disabled
Release Method	RESET, or All Interrupts	RESET or All Interrupts

Table 3.4 Peripheral Operation in Sleep/Stop Mode

3.3 PPG & Protection PAD

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Remark
00E7H	**PRT_IN_DIS[7:0]**								**Protection In Pin Disable**
	0	1	0	1	1	0	1	0	PRT_IN Disabled (Write 5AH)
	0	0	0	0	0	0	0	0	PRT_IN Enabled

Table 3.5 Protection Pin Disable Register

3.4 Clock Generator

The Clock Generator provide the features of XTAL, External RC, and INTOSC (1/2/4/8 MHz). The XIN/XOUT port is dedicated to XTAL mode. The external RC mode needs only XIN port. The INTOSC mode doesn't need any dedicated ports. The selected main clock is directly used as the internal system clock. The prescaler generates the divided clocks for peripherals. The STOP mode disables the main clock. The SLEEP mode only disables system clock, so the peripheral clocks are alive.

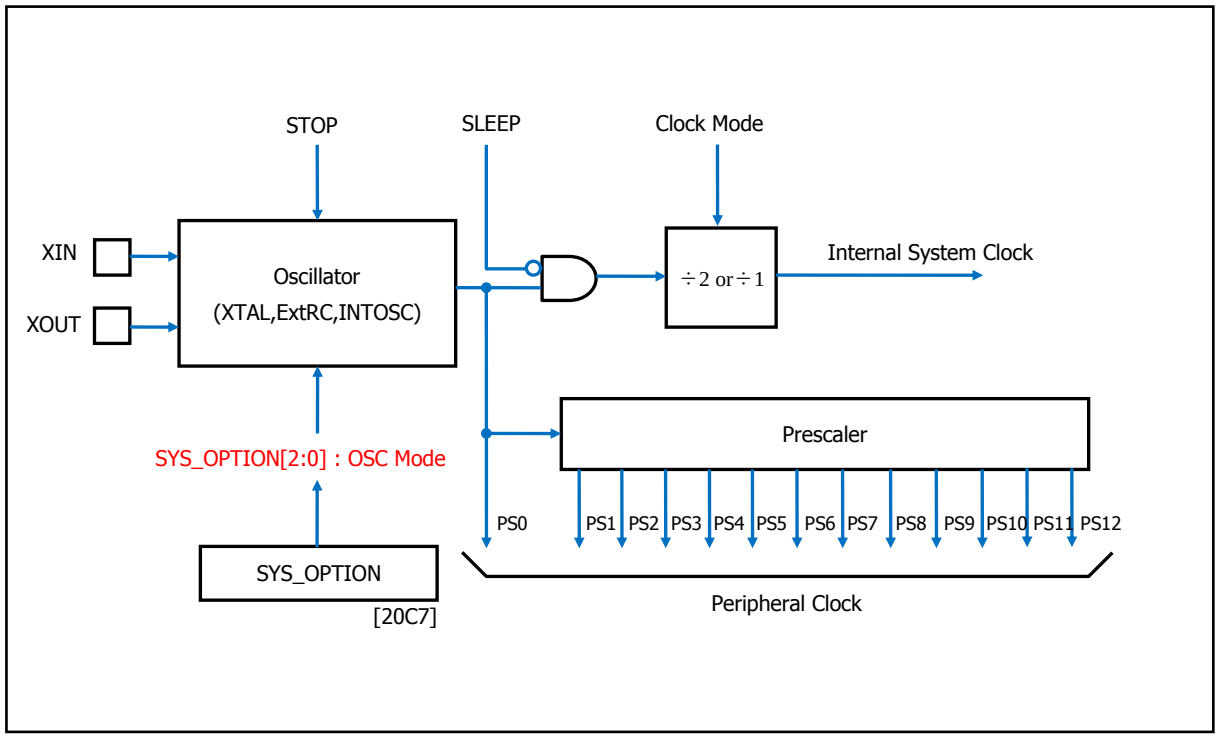


Figure 3.2 Clock Generator Block Diagram

3.5 Basic Interval Timer (BIT)

The Basic Interval Timer (BIT) is an 8-bit binary counter containing the following three features.

1. Timer for Oscillation stabilization time on Power-up
2. Timer for Oscillation stabilization time on Stop release
3. Interrupt Request for Timer

The BIT is controlled by BIT Clock Control Register (CKCTLR). 8-bit BIT counter is operated by the clock selected from PS3~PS10, or RCWDT Clock by CKCTLR[2:0]. The BIT counter is cleared by BCL bit of

CKCTLR which is automatically cleared after 1 machine cycle. If the RCWDT bit is enabled, the BIT is counted by RCWDT ring clock and the overflow is directly connected to WDT clock.

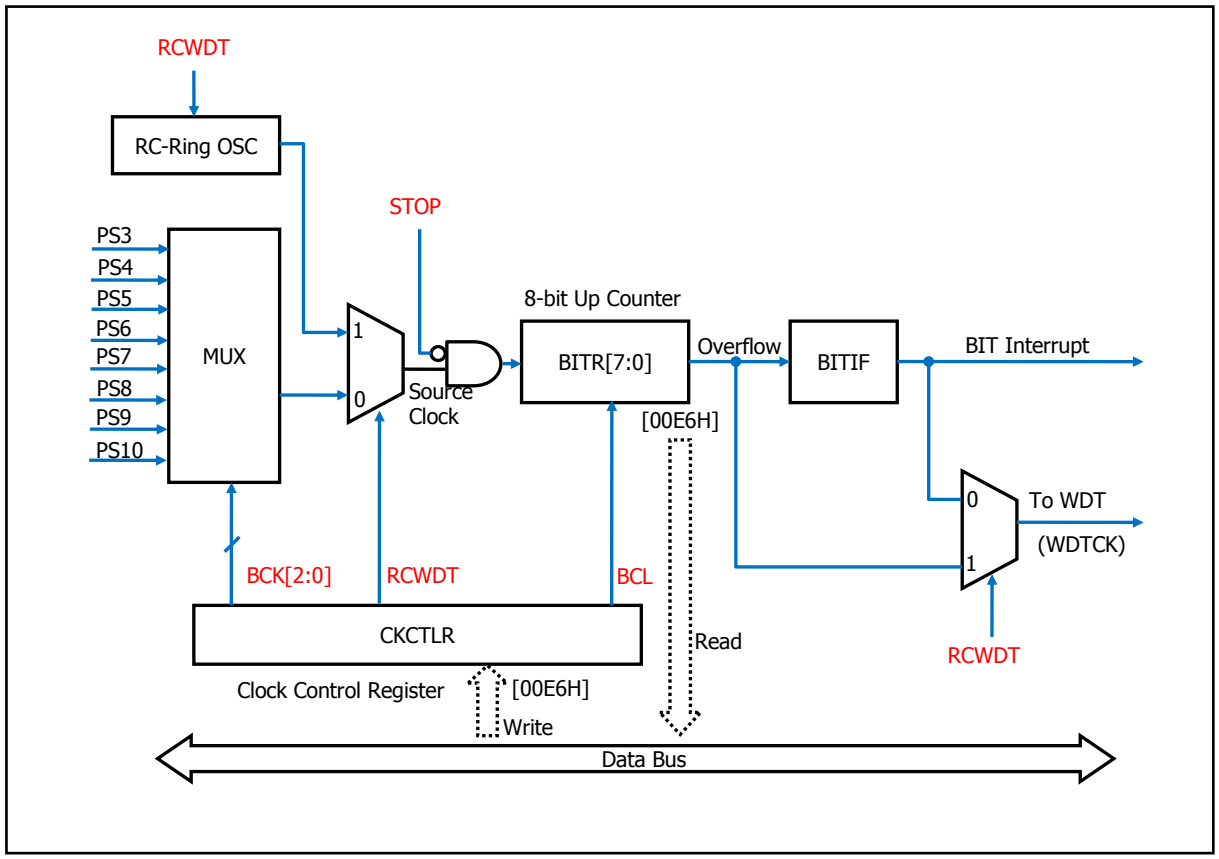


Figure 3.3 BIT Block Diagram

The CKCTLR register is write-only register accessed via [00F2H]. The BITR counter register uses same address which is read-only register via [00F2H].

00E6H	**CKCTLR (Clock Control Register)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CKCTLR	ADRST	-	RCWDT	WDTON	BCL	BCK[2:0]		
R/W	W	-	W	W	W	W	W	W
RESET	0	-	0	1	0	1	1	1

Table 3.6 CKCTLR - Clock Control Register (Write-Only)

Address	**[2]**	**[1]**	**[0]**	**Remark**
00E6H	BCK[2:0]			Basic Interval Timer Clock Selection
	0	0	0	$fx/2^3$
	0	0	1	$fx/2^4$
	0	1	0	$fx/2^5$
	0	1	1	$fx/2^6$
	1	0	0	$fx/2^7$

	1	0	1	$fx/2^8$
	1	1	0	$fx/2^9$
	1	1	1	$fx/2^{10}$

Address	[3]	Remark
00E6H	BCL	Basic Interval Timer Counter Clear
	0	Free Running
	1	Counter Clear (Auto clear after 1 Machine Cycle)

Address	[4]	Remark
00E6H	WDTON	Watch Dog Timer Enable
	0	7bit Timer
	1	Watch Dog Timer

Address	[5]	Remark
00E6H	RCWDT	RC WDT Selection
	0	Disable Internal RC-WDT
	1	Enable Internal RC-WDT

Address	[7]	Remark
00E6H	ADRST	Address Trap Reset
	0	Enable Address Trap Reset
	1	Disable Address Trap Reset

00E6H	**BITR[7:0] – Basic Interval Timer Register**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BITR	BIT[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	X	X	X	X	X	X	X	X

Table 3.7 BITR - Basic Interval Timer Register (Read-Only)

3.6 Watch Dog Timer (WDT)

The Watch Dog Timer (WDT) contains 7-bit binary counter, 7-bit comparator, and Watch Dog Timer Register(WDTR[7:0]). The WDT reset feature is enabled by WDTON bit (CKCTLR[4]), or used as 7-bit Timer. The WDT counter can be cleared by WDTCL (WDTR[7]).

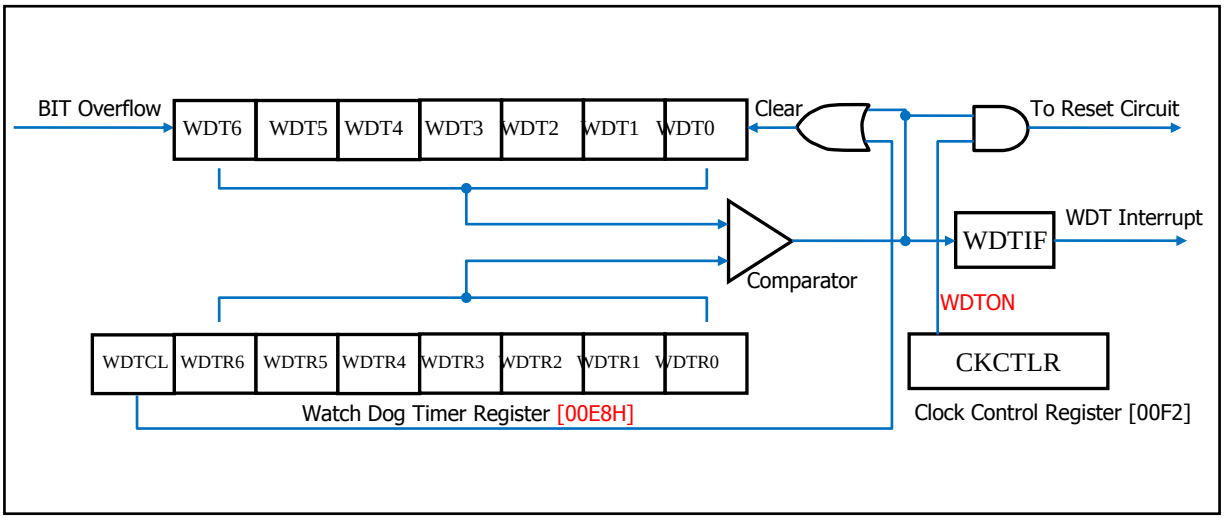


Figure 3.4 Block Diagram of Watch Dog Timer

00E8H	WDTR (Watch Dog Timer Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
WDTR	WDTCL	WDT[6:0]						
R/W	W	W	W	W	W	W	W	W
RESET	0	1	1	1	1	1	1	1

Address	Bit 7	Remark
00E8H	WDTCL	WDT Clear
	0	Free Run
	1	WDT Clear (Auto Clear after 1 cycle)

Address	Bit[6:0]	Remark
00E8H	WDT[6:0]	WDT Interrupt Interval Value
	XXXXXX	WDT Interrupt Interval = (BIT Interrupt Interval) * (WDT + 1)

3.7 Reset Generator

The Reset is used to initialize all hardware including logic, analog circuit. The reset sources are listed in the following list.

- External RESETB Pin
- Power-On-Reset (PORC 00h)
- Low-Voltage-Reset (LVRENB low)
- WDT overflow reset
- Address Trap Reset

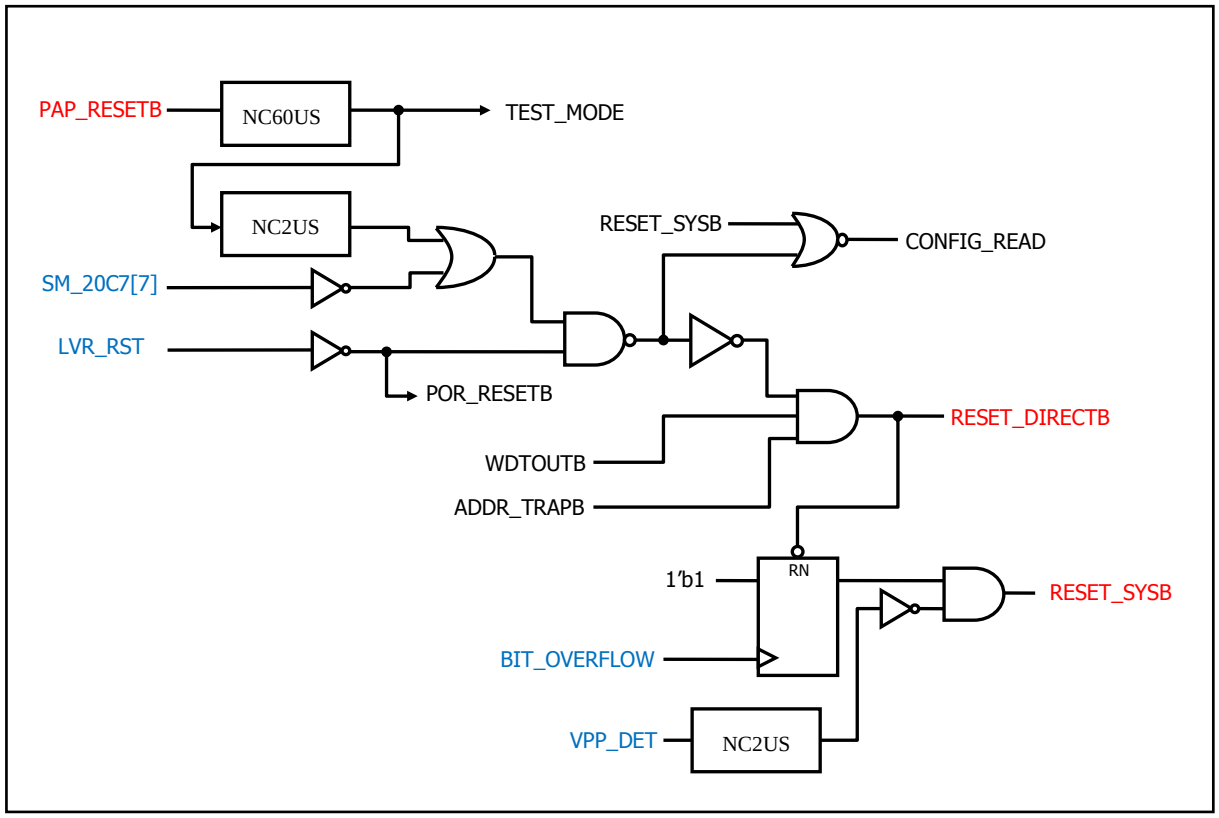


Figure 3.5 Reset Generator

The following figure describes the RESET tree of MC81F6204. The RSTB PAD is directly used in TEST Mode regardless of any other control signals. The first reset is controlled by LVR reset and Smart option. If SM_20C7[0] is 0, the RESET_DIRECTB is controlled by LVR_RST only. Otherwise, the system waits for External PAD_RESETB release. The RESET_SYSB is released on BIT overflow after RESET_DIRECTB is released. If VPP is detected, the system is all disabled by RESET_SYSB.

3.8 Timer/Counter/PWM (Timer 0/1)

The timer consists of two 8-bit timer (0,1) which can be used as 16-bit timer mode. The timer has 7 different operating mode.

- 8 Bit Timer/Counter Mode
- 8 Bit Capture Mode
- 8 Bit Compare Output Mode
- 16 Bit Timer/Counter Mode
- 16 Bit Capture Mode
- 16 Bit Compare Output Mode
- PWM Mode

Timer 0 uses prescaler output and external EC0 as clock source. Timer 1 does timer 0 clock and prescaler output. The capture mode captures the timer result by INT0 or INT1. Timer 0 compare result outputs into T0O. Timer 1 compares outputs into PWM1O. In PWM mode, PWM waveform is assigned into PWM1O.

00D0H	T0CR (Timer0 Mode Control Register)

00D0H	T0CR (Timer0 Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0CR	-	-	CAP0	T0CK[2:0]			T0CN	T0ST
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
RESET	-	-	0	0	0	0	0	0

Table 3.8 T0CR - Timer0 Mode Control Register

Address	[5]	Remark
00D0H	CAP0	Counter Mode Selection
	0	Timer / Counter Mode
	1	Capture Mode

Address	[1]	Remark
00D0H	T0CN	Timer0 Continue Start
	0	Pause Counting
	1	Continue Counting

Address	[0]	Remark
00D0H	T0ST	Timer0 Start Count
	0	Counter Stop
	1	Counter Cleared and Start Again

Address	[4]	[3]	[2]	Remark
00D0H	T0CK2	T0CK1	T0CK0	Timer 0 Clock Selection
	0	0	0	fx/2
	0	0	1	$fx/2^2$
	0	1	0	$fx/2^3$
	0	1	1	$fx/2^5$
	1	0	0	$fx/2^7$
	1	0	1	$fx/2^9$
	1	1	0	$fx/2^{11}$
	1	1	1	External Clock(EC0)

00D1H	T0 (Timer0 Register) – Counter Value							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0	T0[7:0]							

00D1H	T0 (Timer0 Register) – Counter Value							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.9 T0 - Timer0 Counter Register

T0 register can be read on Timer/Counter Mode.

00D1H	T0DR (Timer0 Data Register) – T0 Compare Data							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0DR	T0D[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.10 T0DR - Timer0 Data Register

00D1H	CDR0 (Capture 0 Data Register) – T0 Capture Data (Capture Mode)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CDR0	CDR0[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.11 CDR0 - Capture 0 Data Register

CDR0 register is readable on Capture mode

00D2H	T1CR (Timer1 Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.12 Timer 1 Mode Control Register

Address	[7]	Remark
00D2H	POL	PWM Polarity Selection
	0	Negative
	1	Positive

Address	[6]	Remark
00D2H	16BIT	16BIT Mode Selection
	0	8-BIT Mode
	1	16-BIT Mode

Address	[5]	Remark
00D2H	PWM1E	PWM1 Enable
	0	Disable PWM1
	1	PWM1 Enabled

Address	[4]	Remark
00D2H	CAP1	Counter Mode Selection
	0	Timer / Counter Mode
	1	Capture Mode

Address	[3]	[2]	Remark
00D2H	T1CK[1:0]		Timer 1 Clock Selection
	0	0	fx
	0	1	fx/2
	1	0	$fx/2^3$
	1	1	Timer 0 Selected Clock

Address	[1]	Remark
00D2H	T1CN	Timer1 Continue Start
	0	Pause Counting
	1	Continue Counting

Address	[0]	Remark
00D2H	T1ST	Timer1 Start Count
	0	Counter Stop
	1	Counter Cleared and Start Again

00D3H	**T1DR (Timer1 Data Register) – T1 Compare Data**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1DR	T1DR[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.13 Timer 1 Data Register

T1DR can be written in Timer/Capture mode

00D3H	**T1PPR (Timer1 PWM Period Register) – T1 PWM Period**

00D3H	T1PPR (Timer1 PWM Period Register) – T1 PWM Period							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1PPR	T1PPR[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.14 Timer 1 PWM Period Register

T1PPR can be written in PWM Mode

00D4H	T1 (Timer1 Register) – Counter Value							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1	T1[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.15 Timer 1 Counter Register

T1 register can be read on Timer/Counter Mode.

00D4H	CDR1 (Capture 1 Data Register) – T1 Capture Data (Capture Mode)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CDR1	CDR1[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.16 Timer1 Capture Data

CDR1 register can be read on Capture mode

00D4H	T1PDR (Timer1 PWM Duty Register) – T1 PWM Duty							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1PDR	T1PDR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.17 Timer 1 PWM Duty Register

T1PDR can be written or read in PWM Mode

00D5H	T1PWHR (Timer1 PWM High Register) – T1 PWM Period / Duty High Register							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1PWHR					T1PWHR[3:0]			
R/W					W	W	W	W

00D5H	T1PWHR (Timer1 PWM High Register) – T1 PWM Period / Duty High Register							
RESET					0	0	0	0

Table 3.18 Timer 1 PWM High Register

T1PWHR[3:2],T1PPR[7:0] -> 10bit Period

T1PWHR[1:0],T1PDR[7:0] -> 10bit Duty

16BIT	CAP0	CAP1	PWM1E	T0CK	T1CK	T0O_EN	PWM1O_EN	TIMER0	TIMER1`
0	0	0	0	XXX	XX	0	0	8-bit timer	8-bit timer
0	0	0	0	XXX	XX	1	0	8-bit compare output	8-bit timer
0	0	1	0	111	XX	0	0	8-bit event counter	8-bit capture
0	1	0	0	XXX	XX	0	1	8-bit capture	8-bit compare output
0	0	0	1	XXX	XX	0	1	8-bit timer	10bit PWM
1	0	0	0	XXX	11	0	0	16-bit timer	
1	0	0	0	111	11	0	0	16-bit event counter	
1	1	1	0	XXX	11	0	0	16-bit capture	
1	0	0	0	XXX	11	0	1	16bit compare output	

Table 3.19 Operating Mode of Timer 0/1

The operating mode of timer is defined by the control register and port selection register value.

3.8.1 8Bit Timer/Counter Mode of Timer 0/1

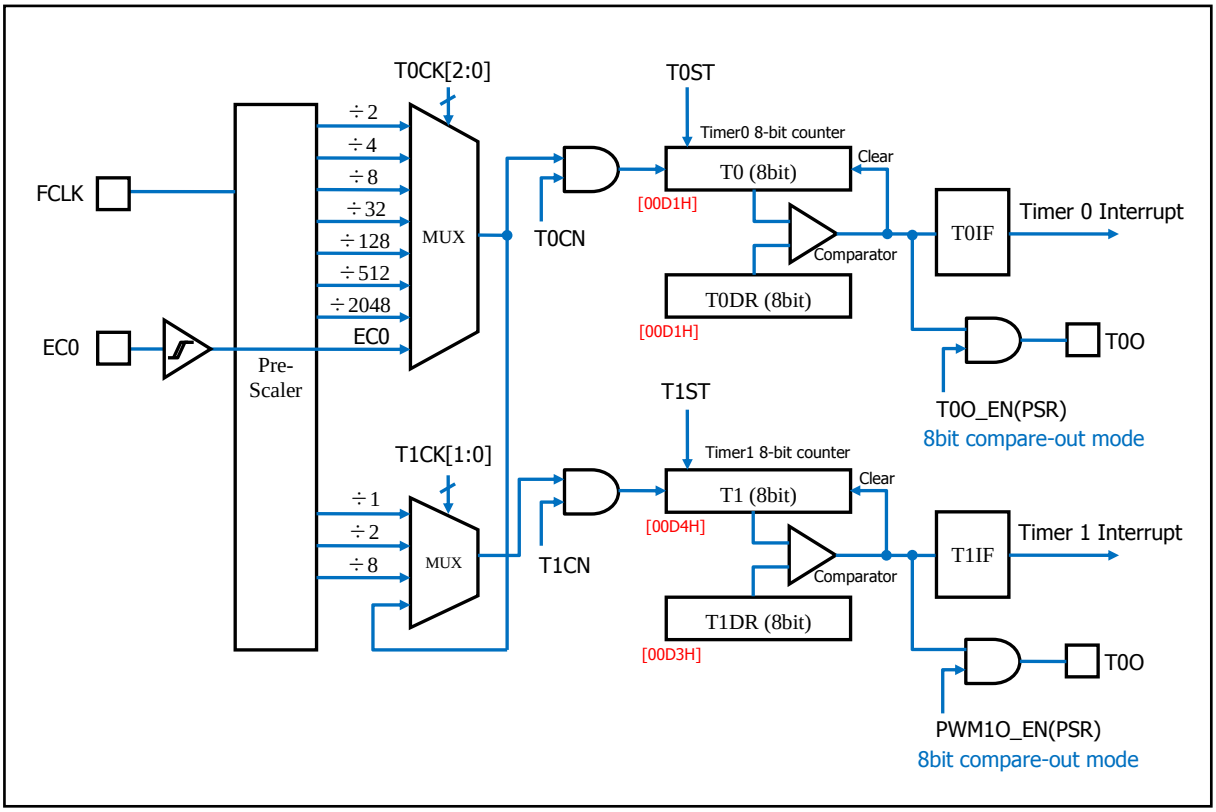


Figure 3.6 Block Diagram of 8 Bit Timer/Event Counter Mode of Timer 0/1

00D0H	T0CR (Timer0 Mode Control Register) – 8bit Timer / Counter Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0CR	-	-	CAP0	T0CK[2:0]			T0CN	T0ST
Value	-	-	0	X	X	X	X	X

00D2H	T1CR (Timer1 Mode Control Register) – 8bit Timer / Counter Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
Value	X	0	0	0	X	X	X	X

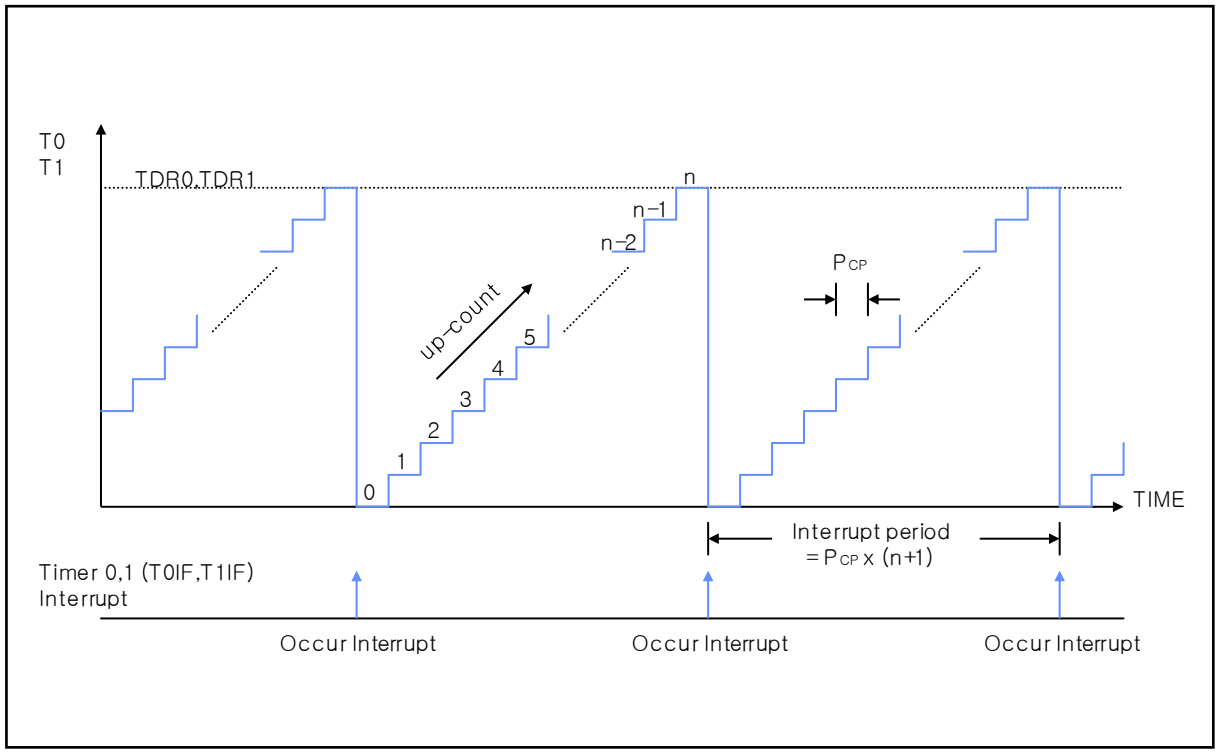


Figure 3.7 Counting Example of Timer Data Registers

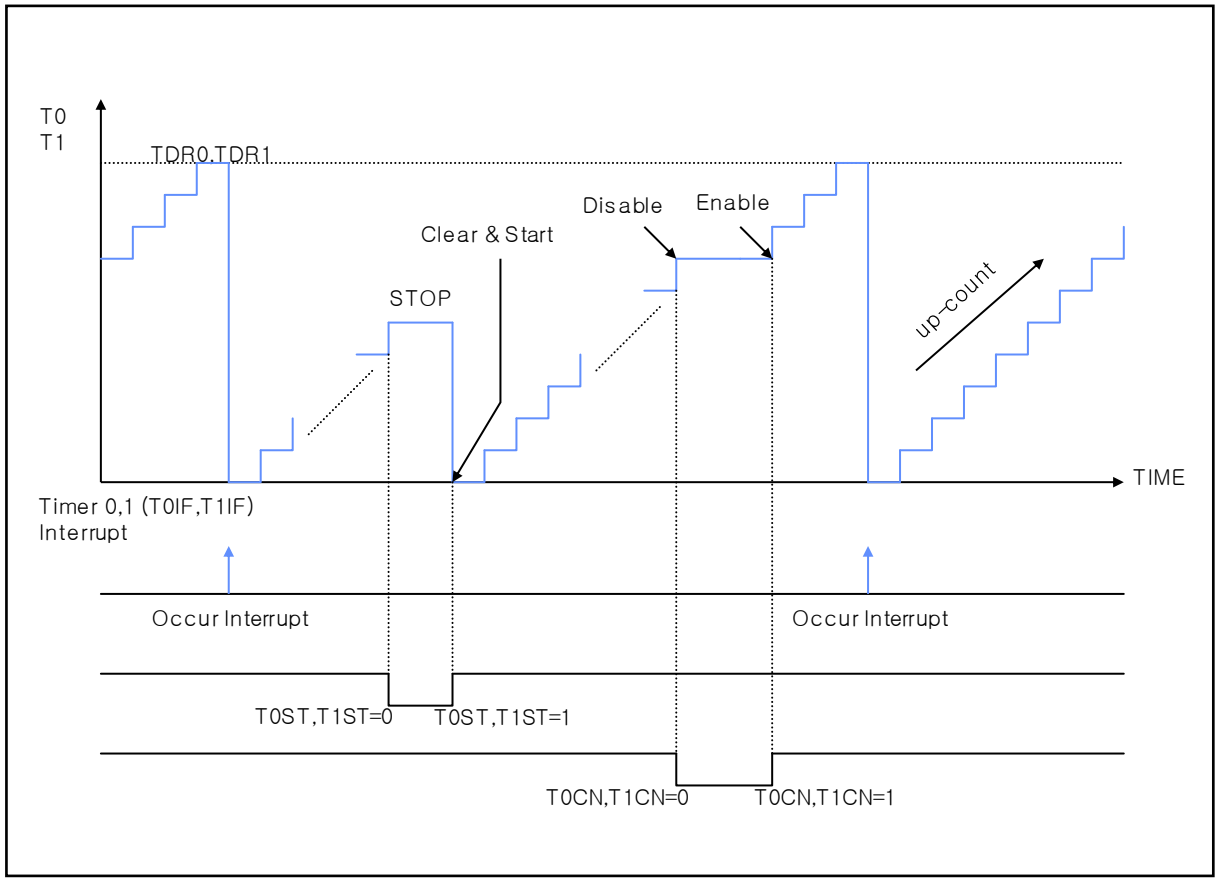


Figure 3.8 Timer Count Operation

3.8.2 16bit Timer / Counter Mode of Timer 0/1

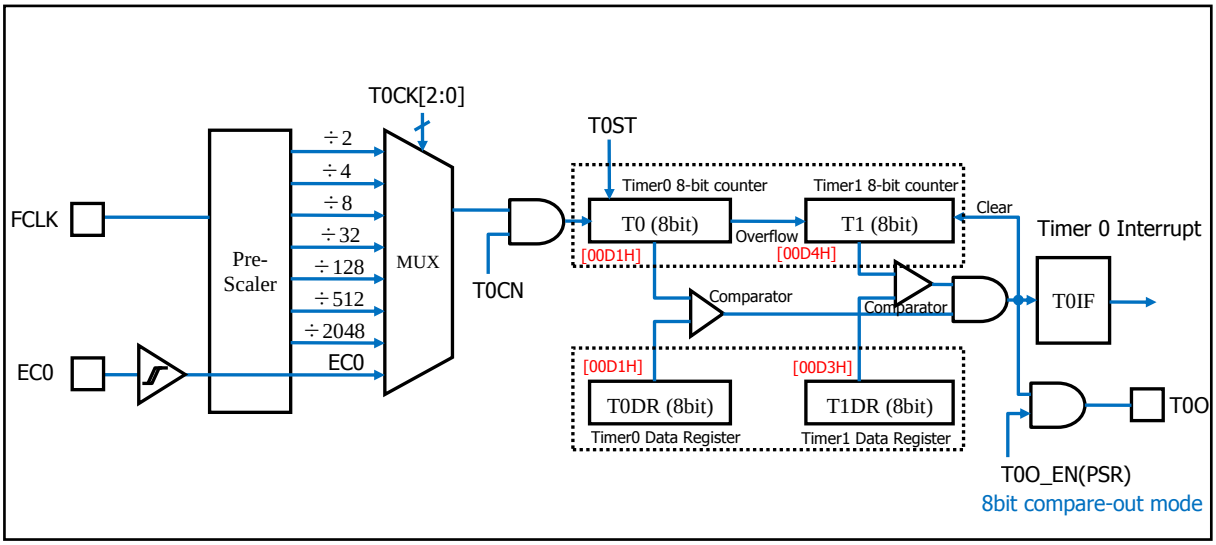


Figure 3.9 Block Diagram of 16 Bit Timer/Event Counter Mode of Timer 0/1

00D0H	T0CR (Timer0 Mode Control Register) – 16bit Timer / Counter Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0CR	-	-	CAP0	T0CK[2:0]			T0CN	T0ST
Value	-	-	0	X	X	X	X	X

00D2H	T1CR (Timer1 Mode Control Register) – 16bit Timer / Counter Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
Value	X	1	0	0	1	1	X	X

3.8.3 8 Bit Capture Mode of Timer 0/1

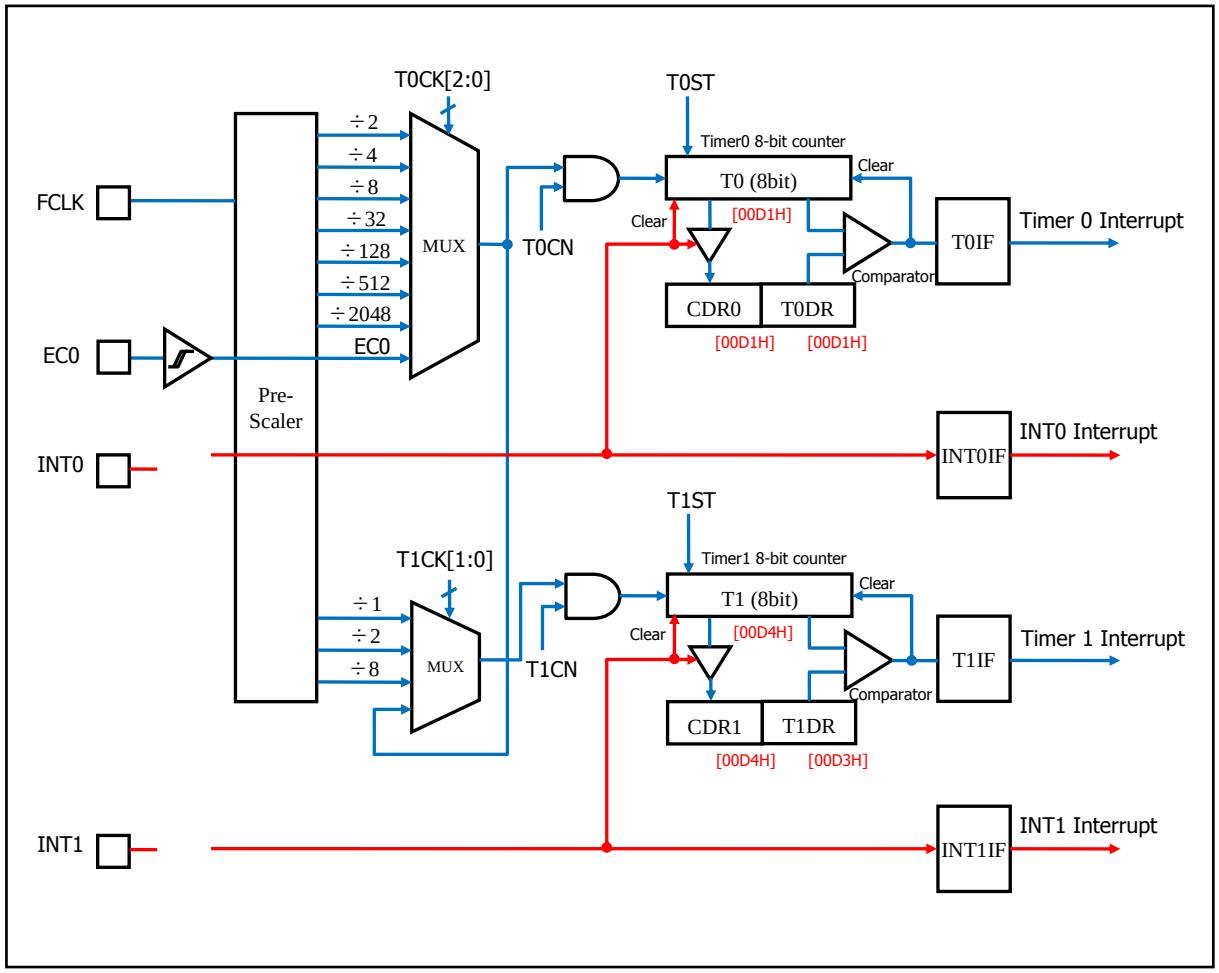


Figure 3.10 Block Diagram of 8bit Capture Mode of Timer 0/1

00D0H	T0CR (Timer0 Mode Control Register) – 8bit Capture Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0CR	-	-	CAP0	T0CK[2:0]			T0CN	T0ST
Value	-	-	1	X	X	X	X	X

00D2H	T1CR (Timer1 Mode Control Register) – 8bit Capture Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
Value	X	0	0	1	X	X	X	X

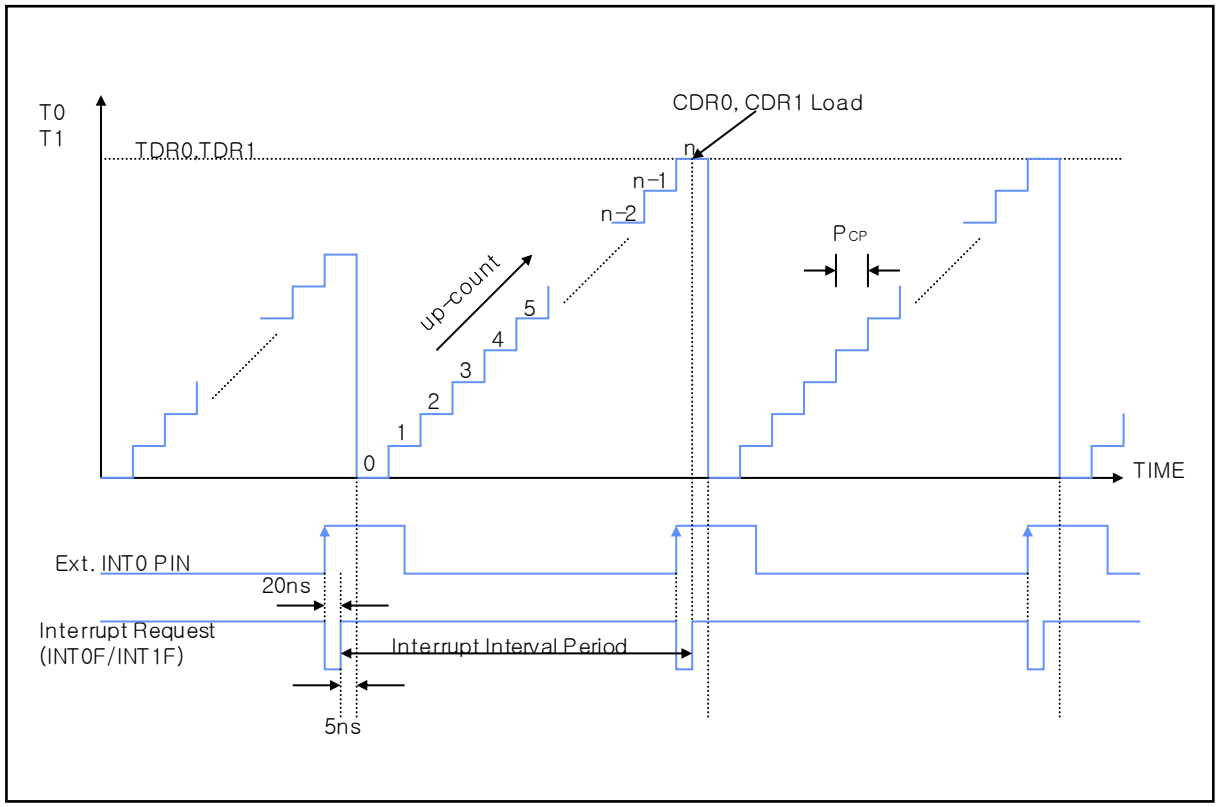


Figure 3.11 Example of 8Bit Capture Mode

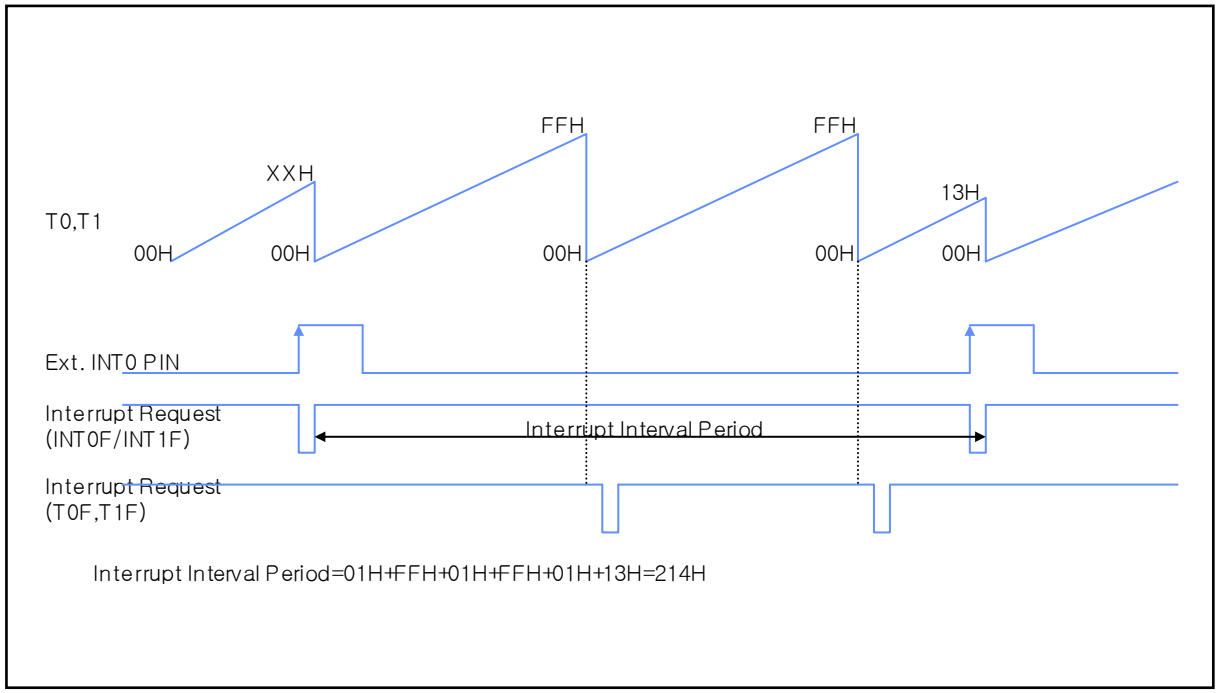


Figure 3.12 Excess Timer Overflow in Capture Mode

3.8.4 16-Bit Capture Mode of Timer 0/1

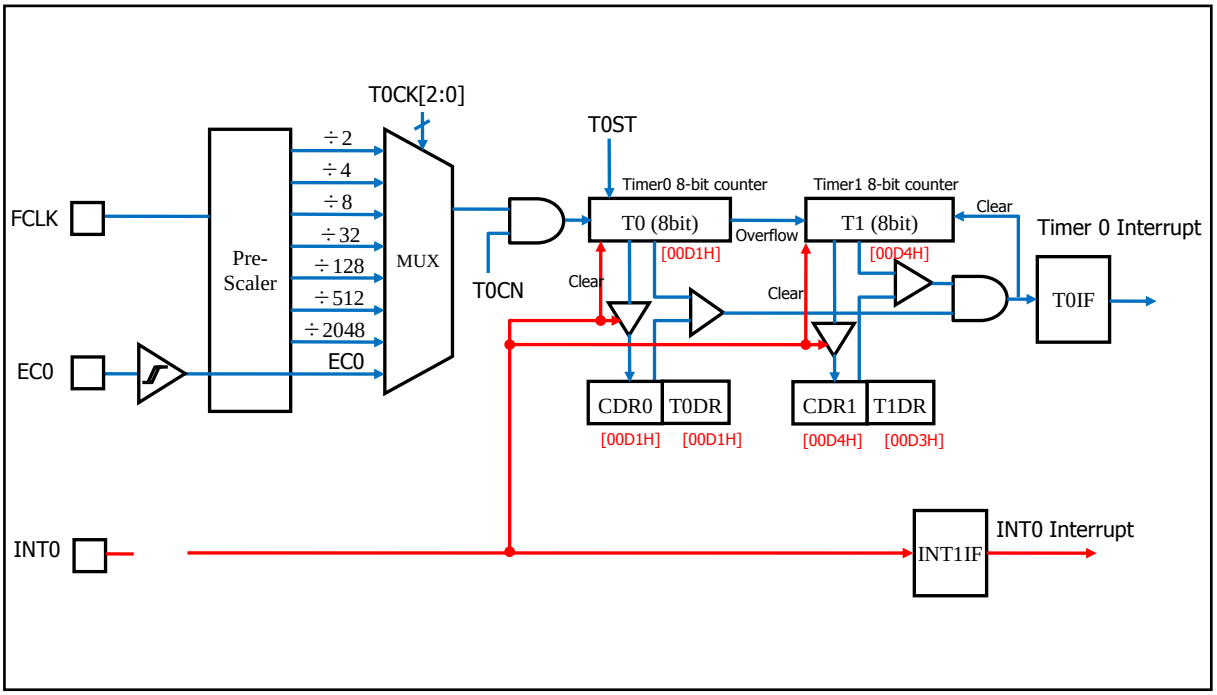


Figure 3.13 Block Diagram of 16bit Capture Mode of Timer 0/1

00D0H	T0CR (Timer0 Mode Control Register) – 16bit Capture Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T0CR	-	-	CAP0	T0CK[2:0]			T0CN	T0ST
Value	-	-	1	X	X	X	X	X

00D2H	T1CR (Timer1 Mode Control Register) – 16bit Capture Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
Value	X	1	0	1	1	1	X	X

3.8.5 PWM Mode of Timer 0/1

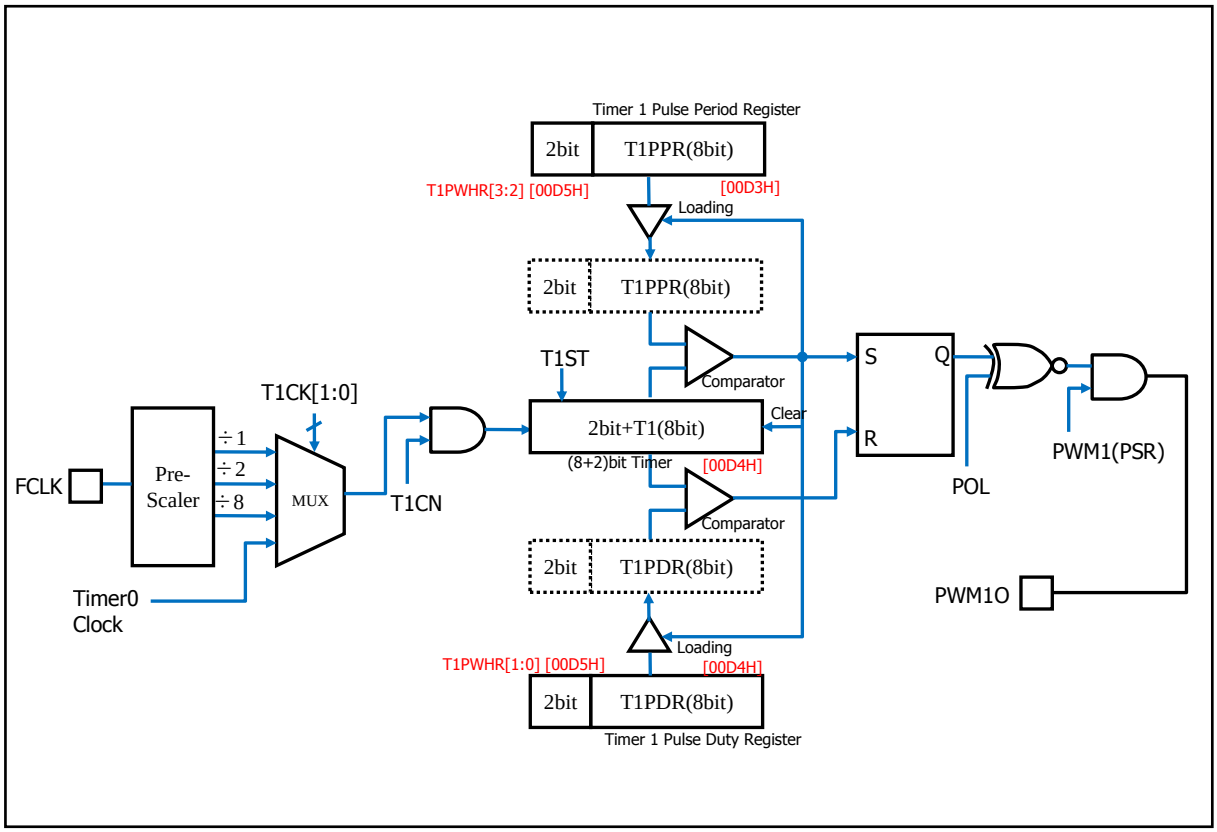


Figure 3.14 Block Diagram of PWM Mode of Timer 0/1

00D2H	T1CR (Timer1 Mode Control Register) – PWM Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1CR	POL1	16BIT	PWM1E	CAP1	T1CK[1:0]		T1CN	T1ST
Value	X	0	1	0	X	X	X	X

00D5H	T1PWHR (Timer1 PWM High Register) – PWM Pulse High Register							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T1PWHR	-	-	-	-	T1PWHR[3:2]		T1PWHR[1:0]	
Value	-	-	-	-	X	X	X	X
Remark	-	-	-	-	Period High		Duty High	

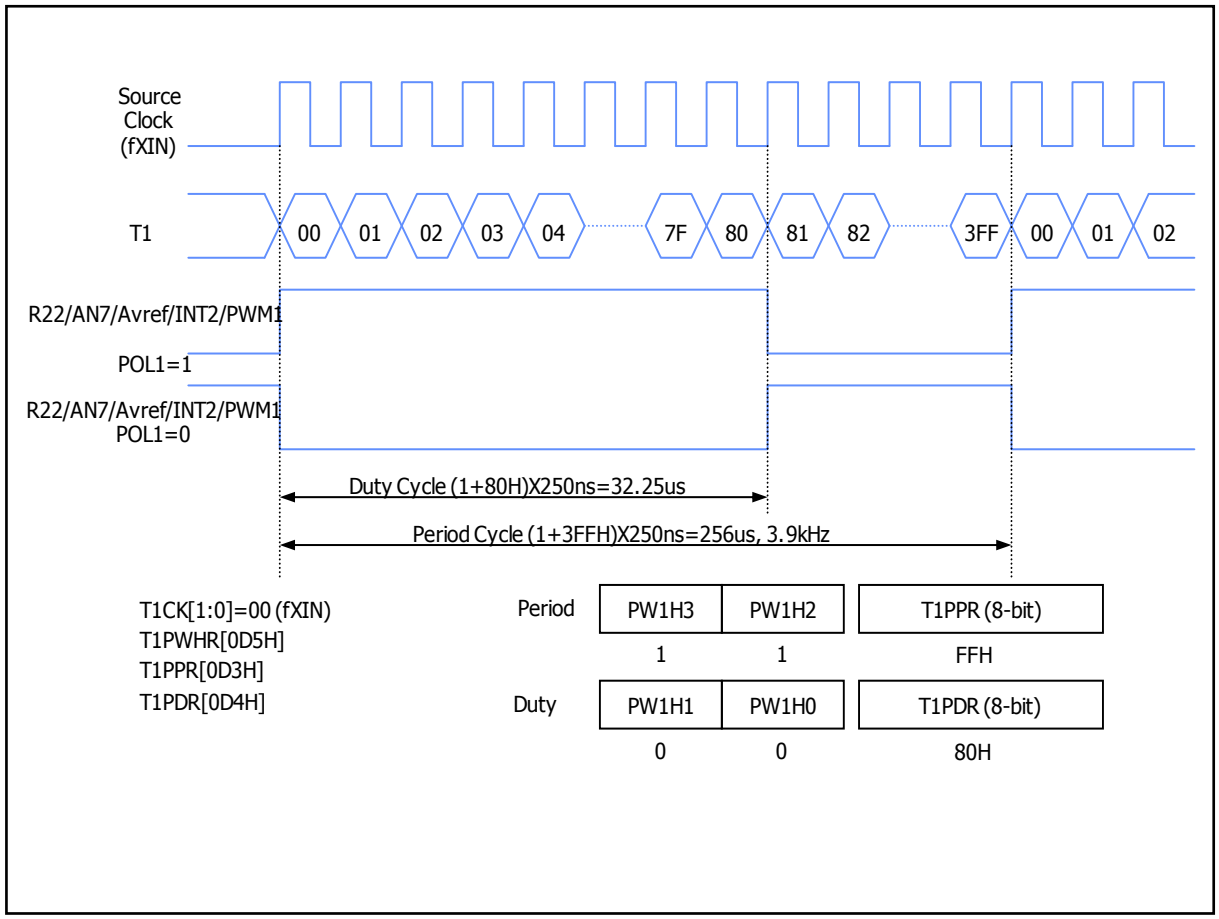


Figure 3.15 Example of PWM at 4Mhz

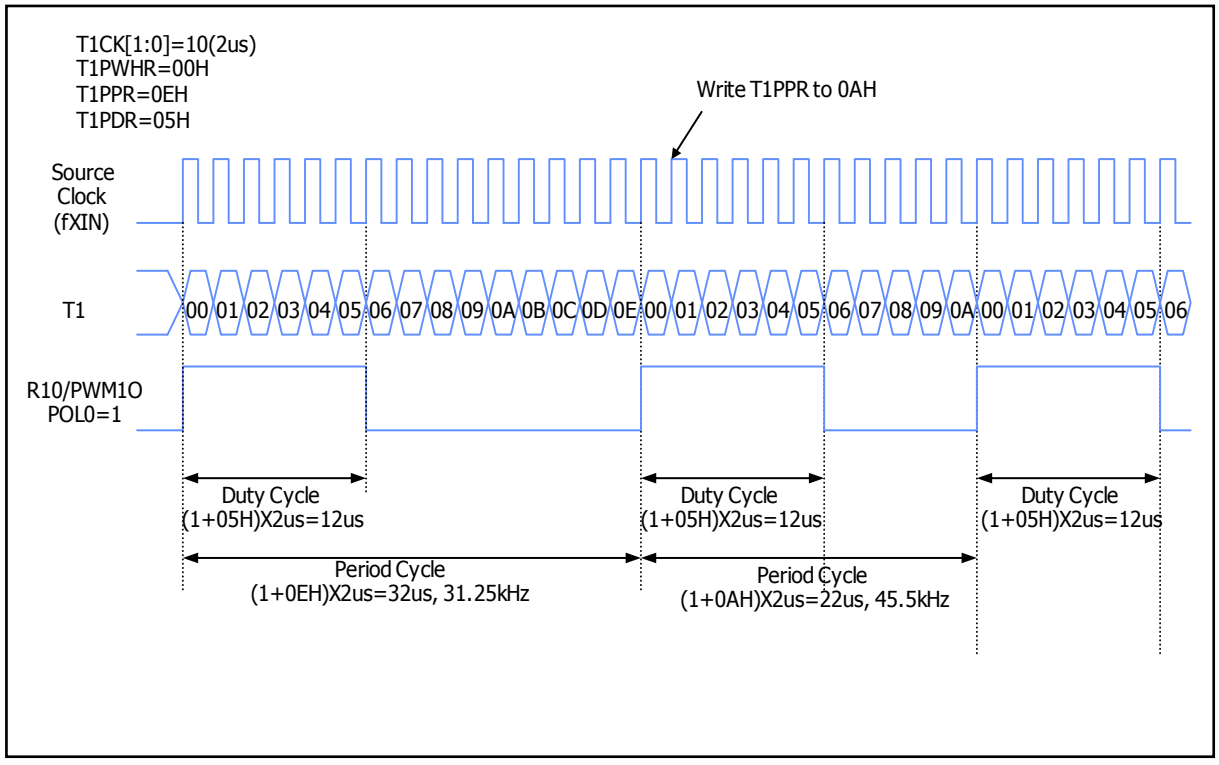


Figure 3.16 Example of Changing Period in Absolute Duty Cycle (4Mhz)

3.9 Analog Comparator

The MC81F6204 contains 5 analog comparators which can be easily used to compare the external input voltage with internally selected voltage like VDD. The each comparator has its comparator interrupt controlled by interrupt controller. The interrupt vector address is described in interrupt controller section. The comparator input port can be also used as normal I/O port.

The comparator0 is a special comparator featured with low offset characteristics which can be used as a trigger source of ATPWM block.

The comparator4 output is used as a sync signal to write the duty in specific time into ATDBR.

The comparator3's input pin is connected with the internal node of on-chip OP-Amp's 1st stage.

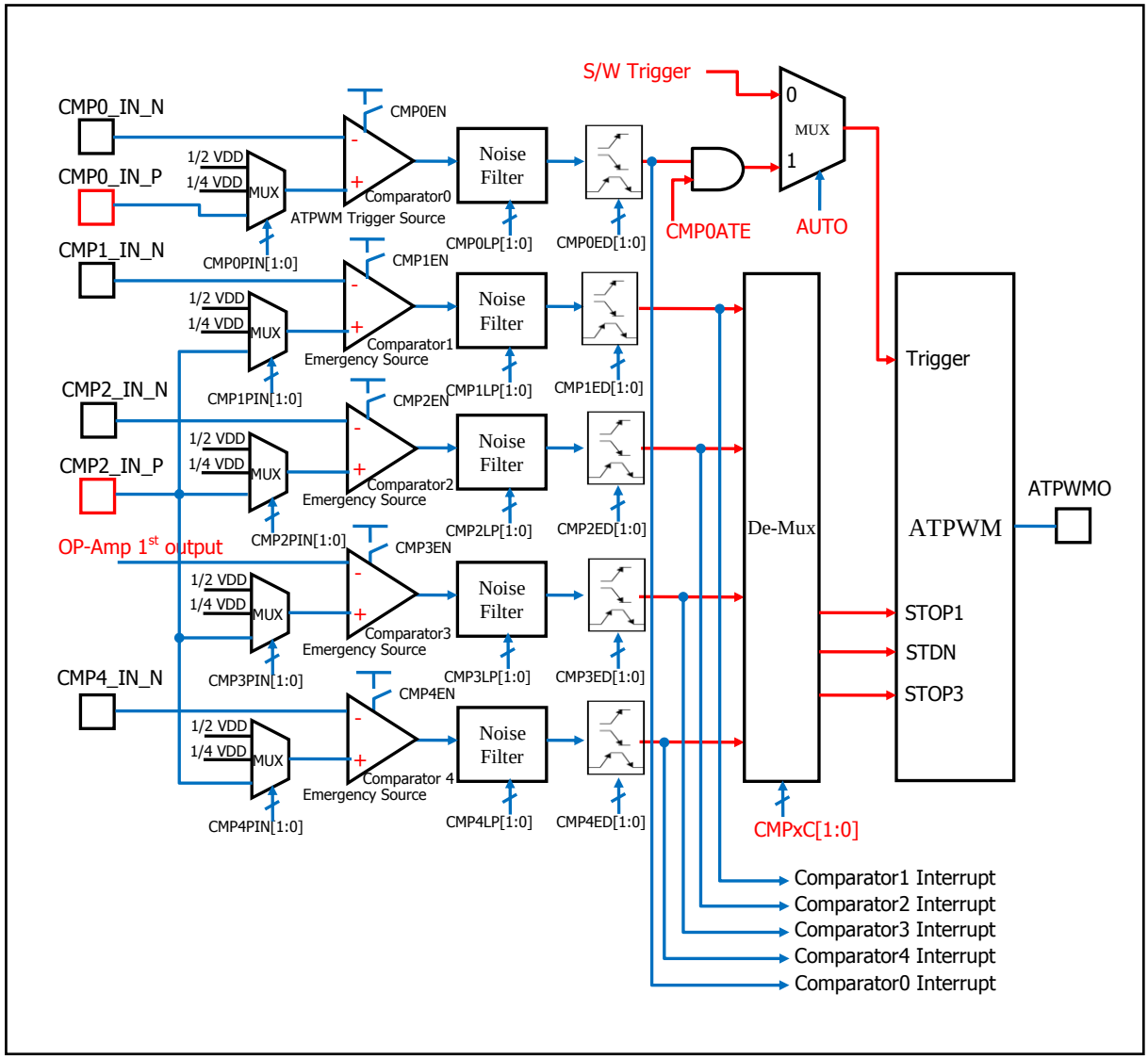


Figure 3.17 Block Diagram of Comparator and ATPWM

00EAH	CMPCR (Analog Comparator Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPCR	CMP4EN	CMP3EN	CMP2EN	CMP1EN	CMP0EN	-	CMP4DWT	CMP0ATE
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
RESET	0	0	0	0	0	-	0	1

Table 3.20 CMPCR - Analog Comparator Control Register

Address	[7]	Remark
00EAH	CMP4EN	Analog Comparator4 Enable
	0	Disabled
	1	Enabled

Address	[6]	Remark
00EAH	CMP3EN	Analog Comparator3 Enable
	0	Disabled
	1	Enabled

Address	[5]	Remark
00EAH	CMP2EN	Analog Comparator2 Enable
	0	Disabled
	1	Enabled

Address	[4]	Remark
00EAH	CMP1EN	Analog Comparator1 Enable
	0	Disabled
	1	Enabled

Address	[3]	Remark
00EAH	CMP0EN	Analog Comparator0 Enable
	0	Disabled
	1	Enabled

Address	[1]	Remark
00EAH	CMP4DWT	Comparator4 Duty Write Trigger Enable
	0	Disabled
	1	Enabled (use as duty writing sync signal)

Address	[0]	Remark
00EAH	CMP0ATE	Analog Comparator0 ATPWM Use as Trigger Source
	0	Disabled
	1	Enabled (use as a trigger source)

00EBH	CMPEMCR (Analog Comparator Emergency Channel Selection Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPEMCR	CMP4C[1:0]		CMP3C[1:0]		CMP2C[1:0]		CMP1C[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	1	1	1	0	0	1

Table 3.21 CMPEMCR - Analog Comparator Emergency Channel Selection Register

Address	[7]	[6]	Remark
00EBH	CMP4C[1:0]		Comparator4 Emergency Channel Selection
	0	0	Disabled
	0	1	STOP1 (Stop until STOP1F cleared to 0 by S/W)
	1	0	STDN (ATDBR decrease with STEP value)
	1	1	STOP3 (Stop until comparator0 trigger signal occurred)

Address	[5]	[4]	Remark
00EBH	CMP3C[1:0]		Comparator3 Emergency Channel Selection
	0	0	Disabled
	0	1	STOP1 (Stop until STOP1F cleared to 0 by S/W)
	1	0	STDN (ATDBR decrease with STEP value)
	1	1	STOP3 (Stop until comparator0 trigger signal occurred)

Address	[3]	[2]	Remark
00EBH	CMP2C[1:0]		Comparator2 Emergency Channel Selection
	0	0	Disabled
	0	1	STOP1 (Stop until STOP1F cleared to 0 by S/W)
	1	0	STDN (ATDBR decrease with STEP value)
	1	1	STOP3 (Stop until comparator0 trigger signal occurred)

Address	[1]	[0]	Remark
00EBH	CMP1C[1:0]		Comparator1 Emergency Channel Selection
	0	0	Disabled

	0	1	STOP1 (Stop until STOP1F cleared to 0 by S/W)
	1	0	STDN (ATDBR decrease with STEP value)
	1	1	STOP3 (Stop until comparator0 trigger signal occurred)

00ECH	CMPPIN0 (Analog Comparator Positive Input Selection Register0)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPPIN0	CMP3PIN[1:0]		CMP2PIN[1:0]		CMP1PIN[1:0]		CMP0PIN[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	1	0

Table 3.22 CMPPIN0 - Analog Comparator Positive Input Source Selection Register 0

Address	[7]	[6]	Remark
00ECH	CMP3PIN[1:0]		Comparator3 Positive Input Selection
	0	0	1/2 VDD
	0	1	1/4 VDD
	1	0	R11/CMP2_IN_P (24pin package only)
	1	1	Prohibited

Address	[5]	[4]	Remark
00ECH	CMP2PIN[1:0]		Comparator2 Positive Input Selection
	0	0	1/2 VDD
	0	1	1/4 VDD
	1	0	R11/CMP2_IN_P (24pin package only)
	1	1	Prohibited

Address	[3]	[2]	Remark
00ECH	CMP1PIN[1:0]		Comparator1 Positive Input Selection
	0	0	1/2 VDD
	0	1	1/4 VDD
	1	0	R11/CMP2_IN_P (24pin package only)
	1	1	Prohibited

Address	[1]	[0]	Remark
00ECH	CMP0PIN[1:0]		Comparator0 Positive Input Selection
	0	0	1/2 VDD
	0	1	1/4 VDD
	1	0	R14/CMP0_IN_P

	1	1	Prohibited

00EDH	CMPPIN1 (Analog Comparator Positive Input Selection Register0)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPPIN1							CMP4PIN[1:0]	
R/W							R/W	R/W
RESET							0	1

Table 3.23 CMPPIN1 - Analog Comparator Positive Input Source Selection Register 1

Address	[1]	[0]	Remark
00D0H	CMP4PIN[1:0]		Comparator4 Positive Input Selection
	0	0	1/2 VDD
	0	1	1/4 VDD
	1	0	R11/CMP2_IN_P (24pin package only)
	1	1	Prohibited

00EEH	CMPEDS0 (Analog Comparator Edge Selection Register 0)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPEDS0	CMP3ED[1:0]		CMP2ED[1:0]		CMP1ED[1:0]		CMP0ED[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	1	0	1	0	1	0

Table 3.24 CMPEDS0 - Analog Comparator Edge Selection Register 0

Address	[7]	[6]	Remark
00EEH	CMP3ED[1:0]		Comparator3 Edge Selection
	0	0	Prohibited
	0	1	Rising Edge
	1	0	Falling Edge
	1	1	Both Edge

Address	[5]	[4]	Remark
00EEH	CMP2ED[1:0]		Comparator2 Edge Selection
	0	0	Prohibited
	0	1	Rising Edge
	1	0	Falling Edge
	1	1	Both Edge

Address	[3]	[2]	Remark
00EEH	CMP1ED[1:0]		Comparator1 Edge Selection
	0	0	Prohibited
	0	1	Rising Edge
	1	0	Falling Edge
	1	1	Both Edge

Address	[1]	[0]	Remark
00EEH	CMP0ED[1:0]		Comparator0 Edge Selection
	0	0	Prohibited
	0	1	Rising Edge
	1	0	Falling Edge
	1	1	Both Edge

00EFH	CMPEDS1 (Analog Comparator Edge Selection Register 1)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPEDS1							CMP4ED[1:0]	
R/W							R/W	R/W
RESET							1	0

Table 3.25 CMPEDS1 - Analog Comparator Edge Selection Register 0

Address	[1]	[0]	Remark
00EFH	CMP4ED[1:0]		Comparator4 Edge Selection
	0	0	Prohibited
	0	1	Rising Edge
	1	0	Falling Edge
	1	1	Both Edge

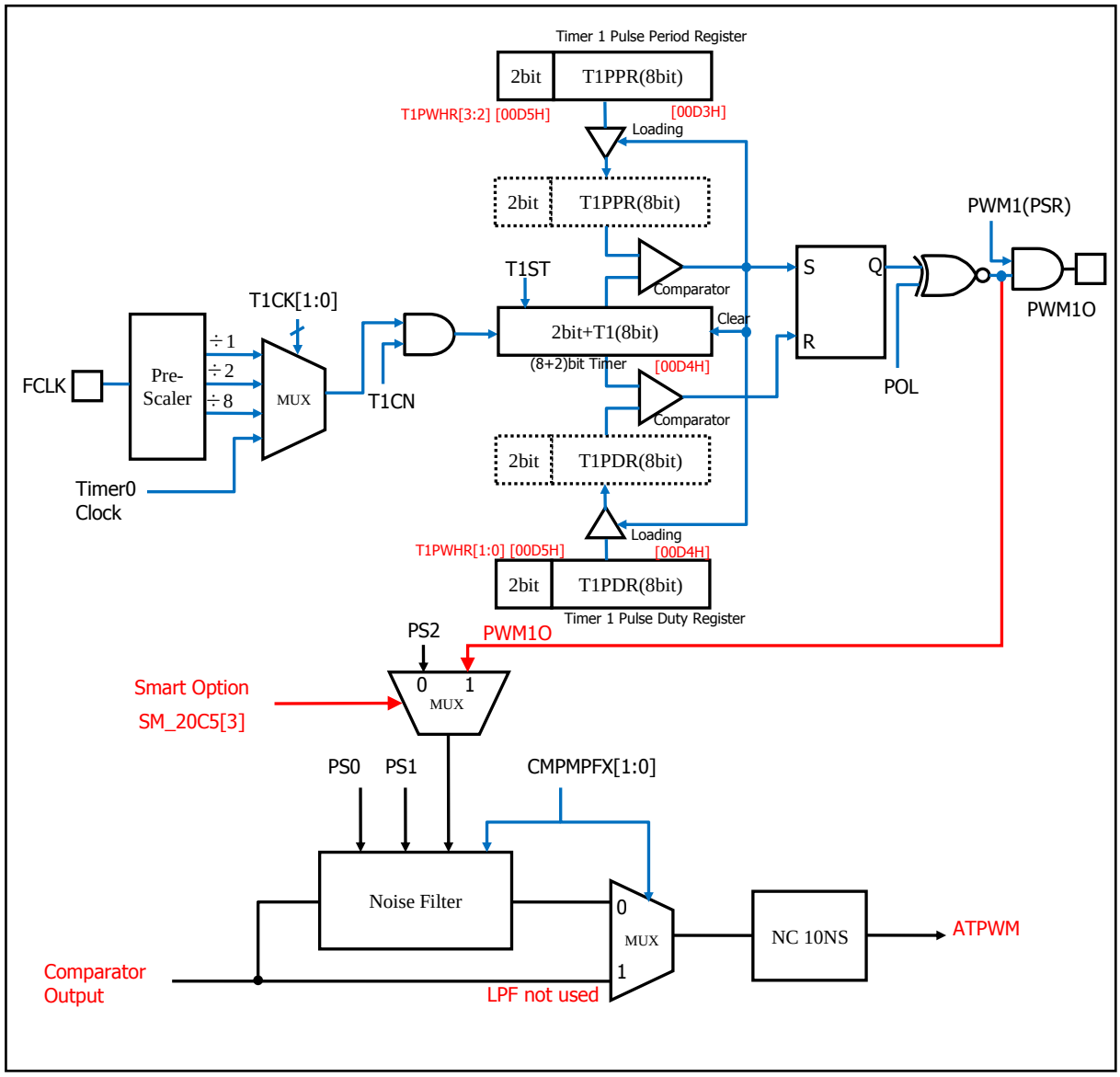


Figure 3.18 Low Pass Filter Block Diagram(Comparator0)

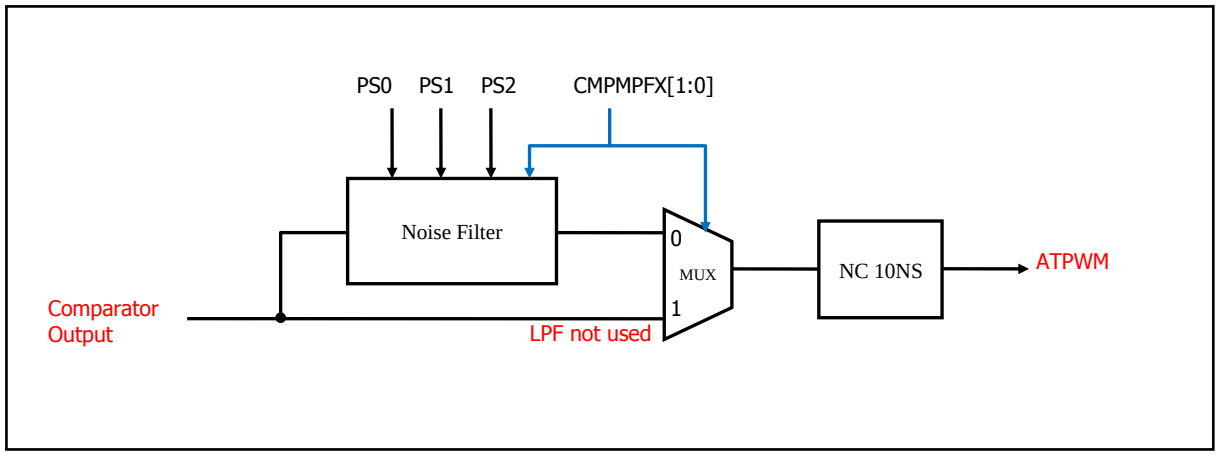


Figure 3.19 Low Pass Filter Block Diagram(Comparator1,2,3,4 except Comparator0)

Remarks)

Noise Filter is a noise canceler based on the clock edge type to cancel the signal of the specific duty. Therefore if you use thie noise filter as the delay effect, the amount of the delay varies from 0 to filtering duty .

00F0H	CMPLPF0 (Analog Comparator Output Low Pass Filter Selection Register 0)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPLPF0	CMP3LP[1:0]		CMP2LP[1:0]		CMP1LP[1:0]		CMP0LP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	1	0	1	0	1	0	1

Table 3.26 CMPLPF0- Analog Comparator Output Low Pass Filter Selection Register 0

Address	[7]	[6]	Remark
00F0H	CMP3LP[1:0]		Comparator3 Low Pass Filter Selection
	0	0	LPF is not used
	0	1	(1/2)T
	1	0	T
	1	1	16T

Address	[5]	[4]	Remark
00F0H	CMP2LP[1:0]		Comparator2 Low Pass Filter Selection
	0	0	LPF is not used
	0	1	(1/2)T
	1	0	T
	1	1	16T

Address	[3]	[2]	Remark
00F0H	CMP1LP[1:0]		Comparator1 Low Pass Filter Selection
	0	0	LPF is not used
	0	1	(1/2)T
	1	0	T
	1	1	16T

Address	[1]	[0]	Remark
00F0H	CMP0LP[1:0]		Comparator0 Low Pass Filter Selection
	0	0	LPF is not used
	0	1	(1/2)T

	1	0	T
	1	1	16T
			PWM1O's Period (if SM_20C5[3] is 1)

00F1H	CMPLPF1 (Analog Comparator Output Low Pass Filter Selection Register 1)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPLPF1							CMP4LP[1:0]	
R/W							R/W	R/W
RESET							0	1

Table 3.27 CMPLPF1 - Analog Comparator Output Low Pass Filter Selection Register 1

Address	[1]	[0]	Remark
00F1H	CMP4LP[1:0]		Comparator4 Low Pass Filter Selection
	0	0	LPF is not used
	0	1	(1/2)T
	1	0	T
	1	1	16T

3.10 Operational Amplifier

The MC81F6204 contains the on-chip two-stage operation amplifier which can provide the find-grained current measurement. The output of Op-Amp 1st stage is connected with comparator3. The output of Op-Amp 2nd stage is connected with ADC channel. The 1st stage has fixed gain (x20) and the 2nd stage gain is variably controlled by S/W register (8 steps) defined in the following table.

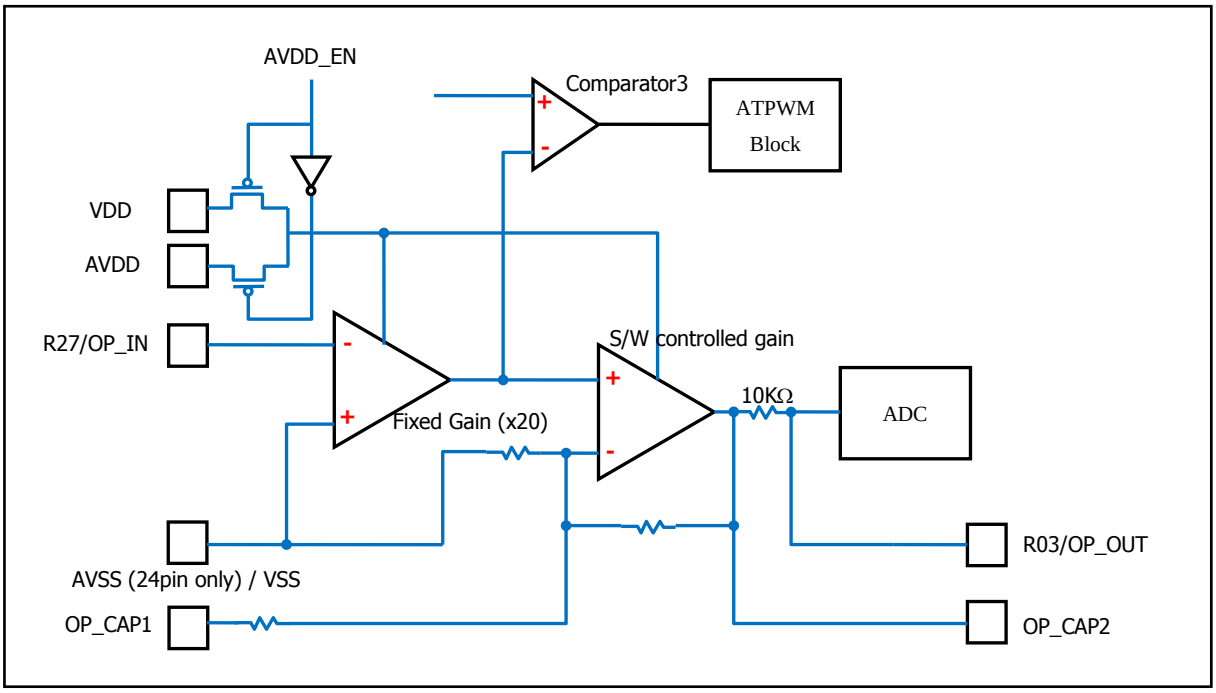


Figure 3.20 Block Diagram of Operational Amplifier

00F2H	AMPCR (Operational Amplifier Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
AMPCR	AMP_EN	-	-	-	-	GAIN[2:0]		
R/W	R/W	-	-	-	-	R/W	R/W	R/W
RESET	0	-	-	-	-	0	0	0

Table 3.28 AMPCR - Operational Amplifier Control Register

Address	[7]	Remark
00F2H	AMP_EN	Operational Amplifier Enable
	0	Disabled
	1	Enabled

Address	[2]	[1]	[0]	Remark
00F2H	GAIN[2:0]			2nd Stage Operational Amplifier Gain
	0	0	0	x 1.0
	0	0	1	x 2.0
	0	1	0	x (9/4)
	0	1	1	x (18/7)
	1	0	0	x 3.0
	1	0	1	x 3.6
	1	1	0	x 4.5

1	1	1	x 6.0

3.11 Auto Triggering PWM Mode (Timer 3)

The timer3 contains auto triggering PWM output feature in addition to the basic timer/counter/capture integrated with timer 0/1. The timer 3 can be normal PWM mode or Auto-Triggering PWM mode. Timer3 don't support 16bit timer/counter/capture/compare-out mode and 8bit compare-out mode.

- 8 Bit Timer/Counter/Capture Mode
- PWM Mode (Timer 3)
- Auto-Triggering PWM Mode (Timer 3)

Timer 3 uses clock used in timer0 and prescaler output as the clock source. The capture mode captures the timer result by INT3. In PWM mode, PWM waveform is also assigned into PWM3O. In Auto-triggering PWM mode, the PWM waveform derived by Analog comparator output is redirected into PWM3O.

00D8H	**T3CR (Timer3 Mode Control Register)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3CR	POL3	ATPWM	PWM3E	CAP3	T3CK[1:0]		T3CN	T3ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.29 Timer 3 Mode Control Register

Address	**[7]**	**Remark**
00D8H	POL3	PWM Polarity Selection
	0	Negative
	1	Positive

Address	**[6]**	**Remark**
00D8H	ATPWM	Auto-Triggering PWM Mode
	0	ATPWM Disabled
	1	ATPEM Enabled

Address	**[5]**	**Remark**
00D8H	PWM3E	PWM3 Enable
	0	Disable PWM3
	1	PWM3 Enabled

Address	**[4]**	**Remark**
00D8H	CAP3	Counter Mode Selection
	0	Timer / Counter Mode

	1	Capture Mode

Address	[3]	[2]	Remark
00D8H	T3CK[1:0]		Timer 3 Clock Selection
	0	0	fx
	0	1	fx/2
	1	0	$fx/2^3$
	1	1	Using Timer0 Clock

Address	[1]	Remark
00D8H	T3CN	Timer3 Continue Start
	0	Pause Counting
	1	Continue Counting

Address	[0]	Remark
00D8H	T3ST	Timer3 Start Count
	0	Counter Stop
	1	Counter Cleared and Start Again

00D9H	**T3DR (Timer1 Data Register) – T3 Compare Data**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3DR	T3DR[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.30 Timer 3 Data Register

T3DR can be written in Timer/Capture mode

00D9H	**T3PPR (Timer3 PWM Period Register) – T3 PWM Period**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3PPR	T3PPR[7:0]							
R/W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.31 Timer 3 PWM Period Register

T3PPR can be written in PWM Mode

00DAH	**T3 (Timer3 Register) – Counter Value**

Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3	T3[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.32 Timer 3 Counter Register

T3 register can be read on Timer/Counter Mode.

00DAH	CDR3 (Capture 1 Data Register) – T3 Capture Data (Capture Mode)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CDR3	CDR3[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.33 Timer3 Capture Data

CDR3 register can be read on Capture mode

00DAH	T3PDR (Timer3 PWM Duty Register) – T3 PWM Duty							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3PDR	T3PDR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.34 Timer 3 PWM Duty Register

T3PDR can be written or read in PWM Mode

00DBH	T3PWHR (Timer3 PWM High Register) – T3 PWM Period / Duty High Register							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3PWHR					T3PWHR[3:0]			
R/W					W	W	W	W
RESET					0	0	0	0

Table 3.35 Timer 3 PWM High Register

T3PWHR[3:2],T3PPR[7:0] -> 10bit Period

T3PWHR[1:0],T3PDR[7:0] -> 10bit Duty

00DCH	ATCR (Auto Triggering PWM Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RESET	0	0	0	0	0	0	0	0

Table 3.36 ATCR - Auto Triggering PWM Mode Control Register

Address	[7]	Remark
00DCH	AT_EN	ATPWM Enable
	0	Disabled
	1	ATPWM Enabled

Output Status (Disabled) : POL:0 -> output low, POL:1 -> output high

Address	[6]	Remark
00DCH	AUTO	Triggering Source Selection
	0	Manual (S/W) Trigger
	1	Auto (H/W) Trigger

Manual Trigger Mode: generates manually high pulse (POL:1) or low pulse (POL:0) by writing 1 into M_ST

Auto Trigger Mode: generates automatically high pulse (POL:1) or low pulse (POL:0) according to comparator 0 output trigger signal.

Address	[5]	Remark
00DCH	M_ST	Manual Trigger to Start
	0	No effect
	1	Start PWM (one pulse)

On manual trigger mode, writing 1 on M_ST generates one pulse (auto cleared)

Address	[4]	Remark
00DCH	STDNE	Decrease ATDBR by Comparator2
	0	Disabled
	1	Enabled of ATBR-decrease mode

On STDNE enabled, ATDBR will be decreased with ATSTEP value when the comparator2 trigger happens during comparator0 triggered.

If there is no comparator2 trigger during previous comparator0 triggered, the ATDBR is immediately reset to ATDR (RS Mode 1), or will be increased with ATSTEP.

Address	[3]	Remark
00DCH	STOP1E	STOP PWM by Comparator1
	0	Disabled
	1	Enable of PWM-STOP mode by Comparator1

If STOP1E is enabled, the ATPWM output is immediately disabled on comparator1 trigger until STOP1 bit of ATCR is cleared by S/W.

Address	[2]	Remark
00DCH	STOP3E	STOP PWM by Comparator3
	0	Disabled

	1	Enable of PWM-STOP mode by Comparator3

If STOP3E is enabled, the ATPWM output is immediately disabled on comparator3 trigger until comparator 0 trigger happens. The STOP3 bit of ATFR is also cleared on comparator0 trigger.

Address	[1]	Remark
00DCH	MAX_E	Maximum Period Enable
	0	Disabled
	1	Enabled

On MAX_E enabled, the pulse will be generated on the maximum period after comparator0 trigger happens..

Address	[0]	Remark
00DCH	MAX_CN	Maximum Period Auto Start Mode
	0	One pulse
	1	Continuous Mode

In one pulse mode, one pulse is generated on the maximum period after comparator0 trigger happens and waits until comparator0 trigger happens.

In continuous mode, one pulse is continuously generated on the maximum period until comparator0 trigger happens.

00DAH	ATDR (Auto Triggering Mode PWM Duty Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATDR	ATDR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.37 ATDR - Auto Triggering Mode PWM Duty Register

ATDR value means auto triggering PWM duty which can be writable when PWM3E is 0 and ATPWM is 1

ATDR is accessible on ATPWM mode

00DDH	ATDBR (Auto Triggering Mode PWM Duty Buffer Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATDBR	ATDBR[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.38 ATDBR - Auto Triggering Mode PWM Duty Buffer Register

The ATDBR value will be updated with ATDR value on PWM pulse start. The ATDBR is used to compare with the PWM counter value to generate PWM pulse.

On STDNE enabled (Decrease mode on comparator2 trigger), ATDBR will be decreased with ATSTEP value when the comparator2 trigger happens during comparator0 triggered.

If there is no comparator2 trigger during previous comparator0 triggered, the ATDBR is immediately reset to ATDR (RS Mode 1), or will be increased with ATSTEP. But ATDBR can' be greater than ATDR value.

00D9H	ATMPR (Auto Triggering Mode PWM Maximum Period Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATMPR	ATMPR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

Table 3.39 ATMPR - Auto Triggering Mode PWM Maximum Period Register

On MAX_E of ATCR register enabled, the pulse will be generated on the maximum period after comparator0 trigger happens. The maximum period check mode is divided into two modes by MAX_CN bit of ATCR register.

In one pulse mode, one pulse is generated on the maximum period after comparator0 trigger happens and waits until comparator0 trigger happens.

In continuous mode, one pulse is continuously generated on the maximum period until comparator0 trigger happens.

ATMPR is accessible on ATPWM mode.

00DBH	ATPWHR (Auto-Triggering PWM High Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATPWHR			ATPWPH[1:0]		ATPWBH[1:0]		ATPWDH[1:0]	
R/W			R/W	R/W	R	R	R/W	R/W
RESET			0	0	0	0	0	0
Remark			Max Period High		Buffer High		Duty High	

Table 3.40 ATPWHR - Auto-Triggering PWM High Register

ATPWPH[1:0]+ATMPR[7:0] : Auto Triggering Mode PWM Maximum Period Value (10bit)

ATPWBH[1:0]+ATDBR[7:0] : Auto Triggering Mode PWM Duty Buffer Value (10bit)

ATPWDH[1:0]+ATDR[7:0] : Auto Triggering Mode PWM Duty Value (10bit)

ATPWBH[1:0] is read-only.

ATPWBH is accessible on ATPWM mode

00DEH	ATPWFR (Auto-Triggering PWM Flag Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATPWFR				CMP4F	MAXF	STOP3F	STNDF	STOP1F
R/W				R/W	R/W	R/W	R/W	R/W
RESET				0	0	0	0	0

Table 3.41 ATPWFR - Auto Triggering Mode PWM Flag Register

Address	[4]	Remark
00DEH	CMP4F	Comparator4 Trigger
	0	Idle
	1	Comparator4 Trigger happened

Address	[3]	Remark
00DEH	MAX_F	Maximum Period Flag
	0	Idle
	1	Maximum Period Expired

The MAX_F is set when comparator0 trigger didn't happen during maximum period time defined in ATPWP[1:0]H+ATMPR[7:0]. The MAX_F is automatically cleared on comparator0 trigger.

Address	[2]	Remark
00DEH	STOP3F	Emergency Stop Flag (type 3)
	0	Idle
	1	Emergency stop happened (type 3)

The emergency stop 3 trigger (default by comparator3) will disable PWM output and set the STOP3F flag value until comparator0 trigger happens. The STOP3F will be automatically cleared on comparator0 trigger. The emergency stop 3 trigger source can be selected from comparator1,2,3

Address	[1]	Remark
00DEH	STDNF	Emergency Standby Flag
	0	Idle
	1	Emergency Standby happened

The emergency standby flag STNDE flag will be set by comparator2 trigger. The STDNF will be automatically cleared on comparator0 trigger. The emergency standby 1 trigger source can be selected from comparator1,2,3

Address	[0]	Remark
00DEH	STOP1F	Emergency Stop Flag (type 1)
	0	Idle
	1	Emergency Stop happened (type 1)

The emergency stop 1 trigger (default by comparator1) will disable PWM output and set the STOP1F flag value until the STOP1F is cleared by software. The STOP3F will be **not** automatically cleared on comparator0 trigger. The emergency stop 1 trigger source can be selected from comparator1,2,3

00DFH	**ATSTEP (Auto-Triggering PWM Duty Adjust Step Register)**							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATSTEP	RS_MODE	STEP[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.42 ATSTEP - Auto Triggering Mode PWM Duty Adjust Step Register

Address	[0]	Remark
00DFH	RS_MODE	ATDR Restore Mode
	0	ATDBR will be directly restored to ATDR
	1	ATDBR will be increased with STEP[6:0]

When RS_MODE is 0, the ATDBR value will be directly restored to ATDR value after the comparator2 trigger not happened, Otherwise, the ATDBR value will be increased with STEP[6:0] value.

ATDBR = ATDBR + ATSTEP[6:0] (maximum ATDBR)

On comparator2 trigger during comparator0 trigger, the ATDR will be decreased with STEP[6:0].

ATDBR = ATDBR – ATSTEP[6:0]

ATPWM	CAP3	PWM3E	T3CK[1:0]	PWM3O_EN	TIMER3`
0	0	0	XX	0	8-bit timer
0	1	0	XX	0	8-bit capture
0	0	0	XX	1	8-bit compare output
0	0	1	XX	1	10bit PWM
1	0	0	XX	1	10-bit Auto Triggering PWM Mode

Table 3.43 Operating Mode of Timer3

The operating mode of timer is defined by the control register and port selection register value.

3.11.1 8Bit Timer/Counter Mode of Timer3

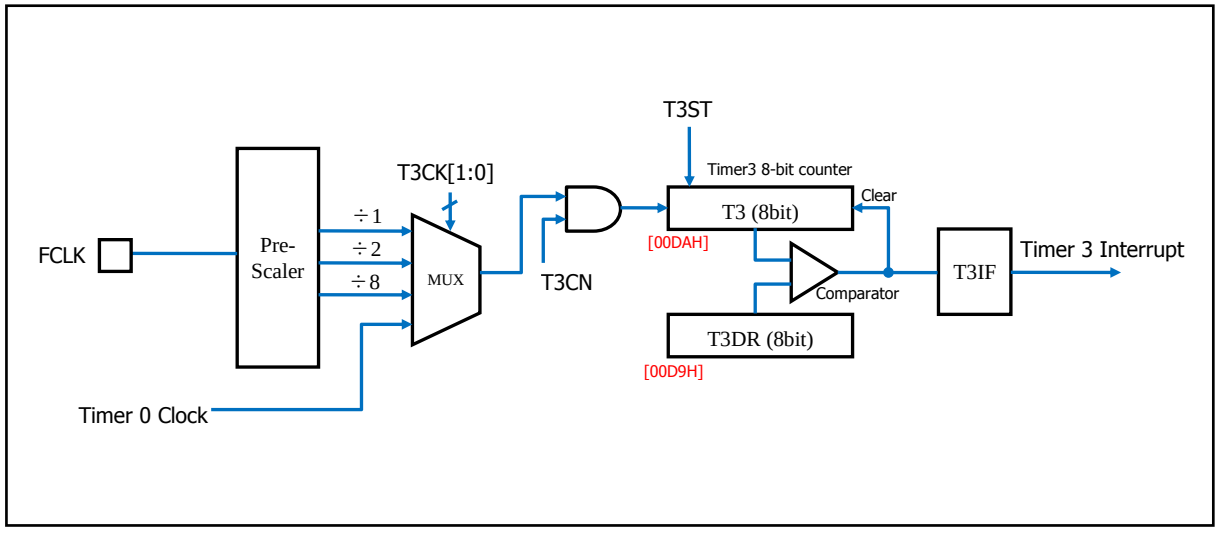


Figure 3.21 Block Diagram of 8 Bit Timer/Counter Mode of Timer 3

00D8H	T3CR (Timer3 Mode Control Register) – 8bit Timer / Counter Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3CR	POL3	ATPWM	PWM3E	CAP3	T3CK[1:0]		T3CN	T3ST
Value	X	0	0	0	X	X	X	X

3.11.2 8 Bit Capture Mode of Timer3

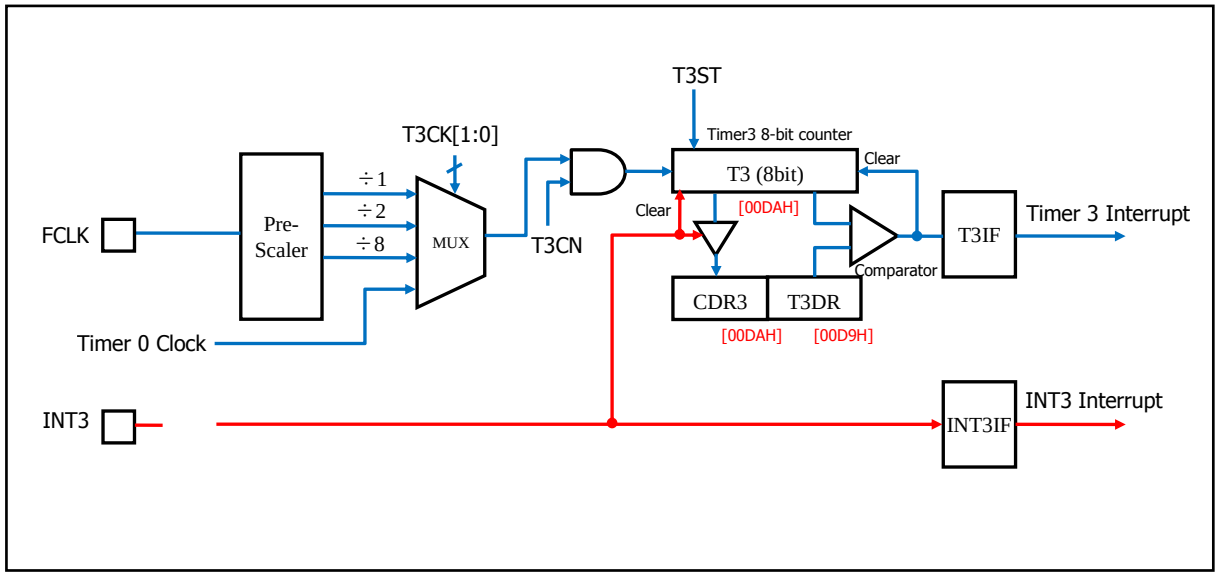


Figure 3.22 Block Diagram of 8bit Capture Mode of Timer 3

00D8H	T3CR (Timer3 Mode Control Register) – 8bit Capture Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3CR	POL3	ATPWM	PWM3E	CAP3	T3CK[1:0]		T3CN	T3ST
Value	X	0	0	1	X	X	X	X

3.11.3 PWM Mode of Timer3

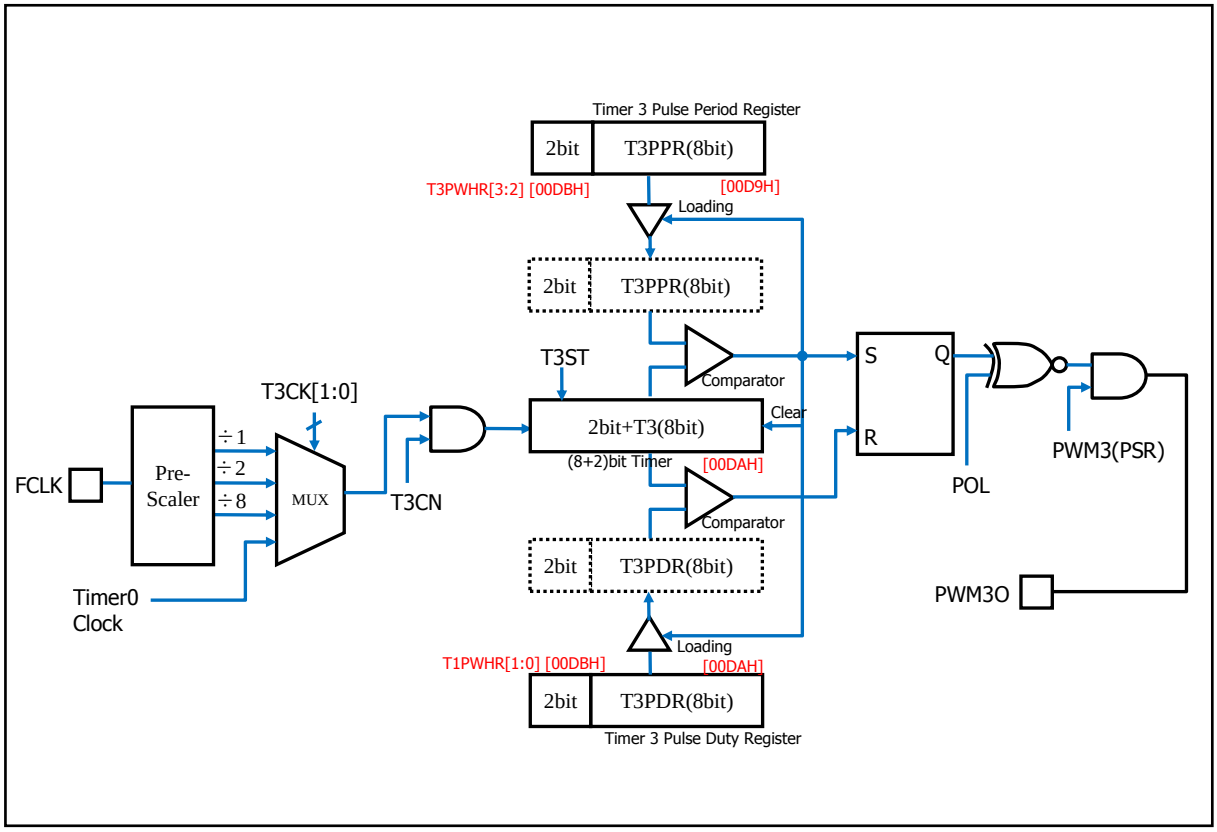


Figure 3.23 Block Diagram of PWM Mode of Timer 3

00D8H	T3CR (Timer3 Mode Control Register) – PWM Mode Configuration							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3CR	POL3	ATPWM	PWM3E	CAP3	T3CK[1:0]		T3CN	T3ST
Value	X	0	1	0	X	X	X	X

00DBH	T3PWHR (Timer3 PWM High Register) – PWM Pulse High Register							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
T3PWHR	-	-	-	-	T3PWHR[3:2]		T3PWHR[1:0]	
Value	-	-	-	-	X	X	X	X
Remark	-	-	-	-	Period High		Duty High	

3.11.4 Auto Triggering PWM Mode of Timer3

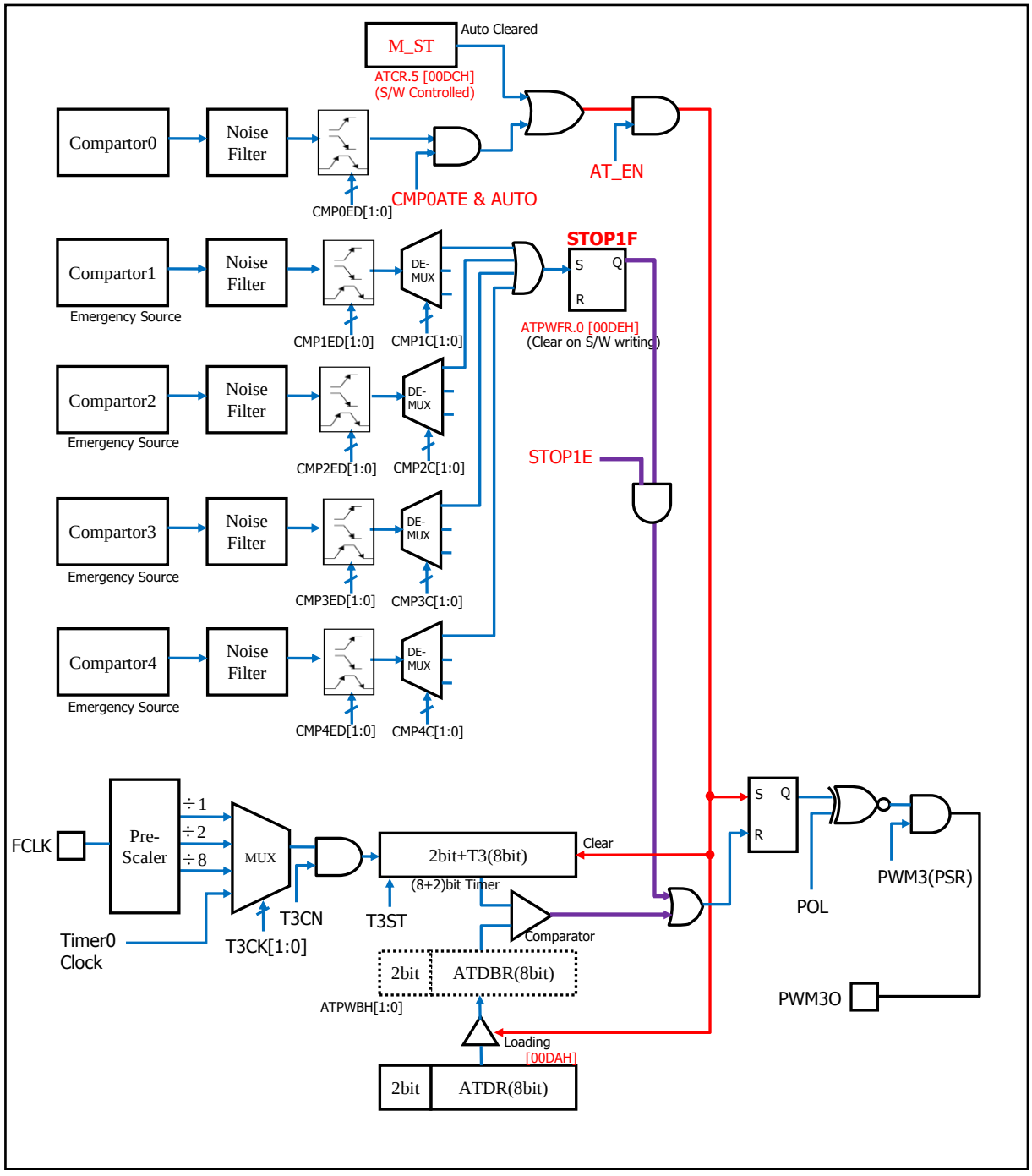


Figure 3.24 Auto Triggering PWM Mode by Emergency STOP1 Type

00DCH	ATCR (Auto Triggering PWM Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
Value	1	X	X	X	1	X	0	X

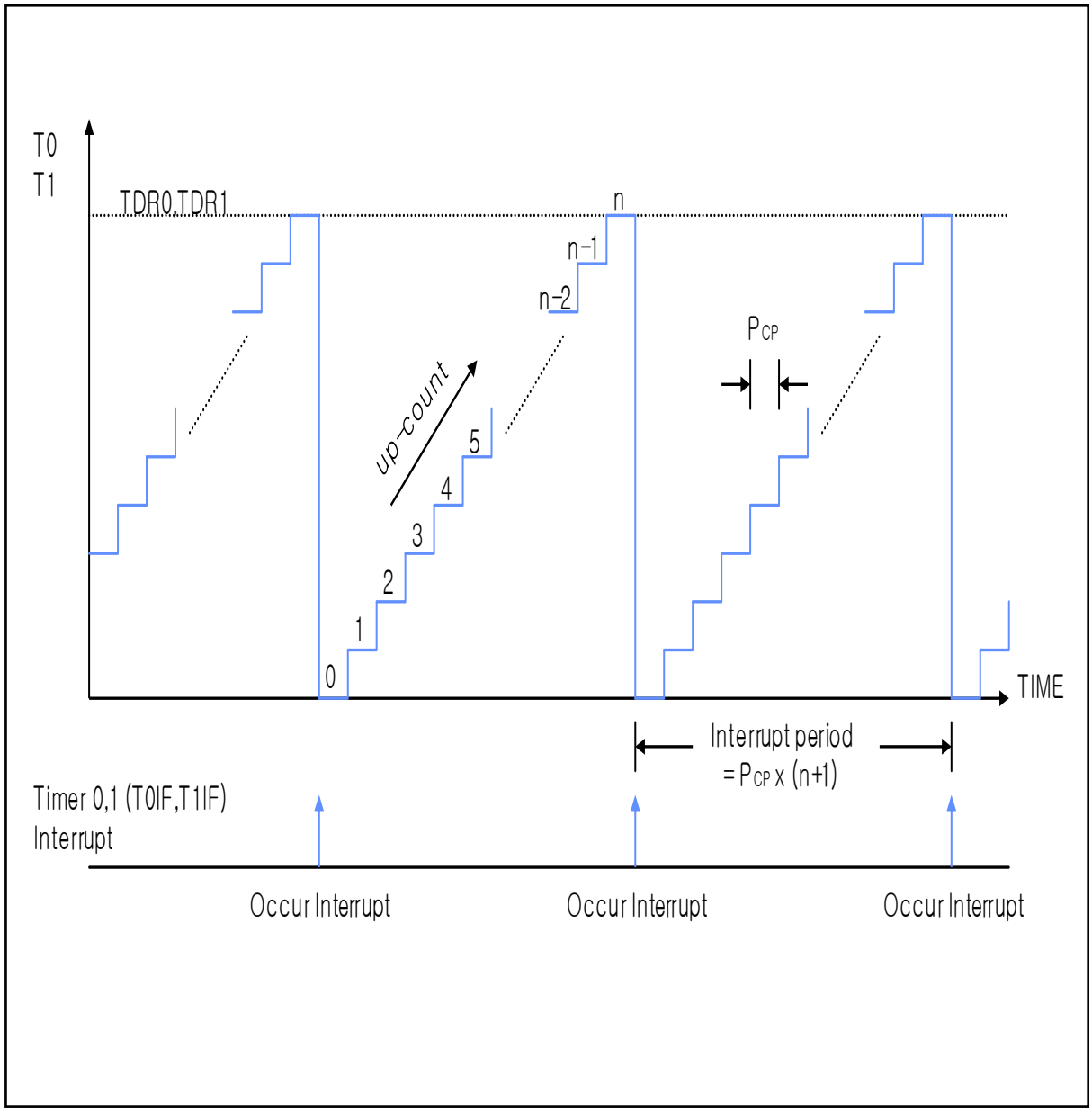


Figure 3.25 Example of ATPWM

CMP0ED selection bit (falling edge, rising edge, both edge). The PWM out is set to 1 on the edge detection of comparator output after the counter value is reset and continues to count. When the counter value matches the duty register value (ATDR). The glitch of comparator output is ignored by low pass filter.

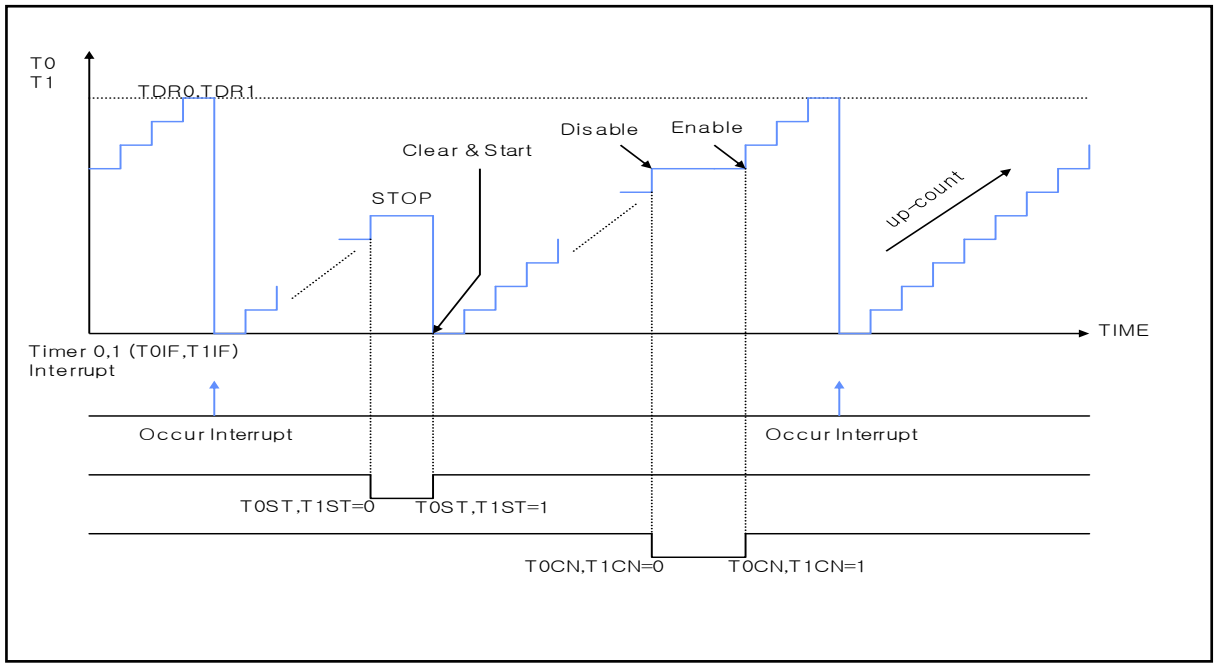


Figure 3.26 Example of STOP1 Mode by Comparator1

The comparator-0 output immediately disables the PWM output. Then the PWM output is disabled until the ATFR STOP1F bit is cleared in spite of comparator-0 trigger.

```
# CMP0 Trigger (or Manual Start) and STOP1 Emergency by CMP1 Trigger
    LDM    ATCR,   #8AH    ; ATPWM Enabled, STOP1E Enabled, Maximum period One Pulse
    LDM    PSR2,   #05H    ; CMP2_P, CMP1_N secondary selection (comparator1 source)
    LDM    CMPEMCR,#01H    ; Using comp1 for STOP1
    LDM    CMPPIN0,#08H    ; Comp1 positive input -> CMP2_P
    LDM    CMPEDS0,#08H    ; Comp1 output falling edge detect
    LDM    CMPLPF0,#00H    ; Comp1 output LPF Disable
    LDM    CMPCR,  #10H    ; CMP1 Enable
    LDM    ATDR,   #0FH    ; Duty Register
    LDM    ATMPR,  #2FH    ; Maximum Period
    LDM    ATPWFR, #00H    ; clear flag
    SET1   ATCR.5          ; Manual Start (M_ST) or wait CMP0 Trigger
```

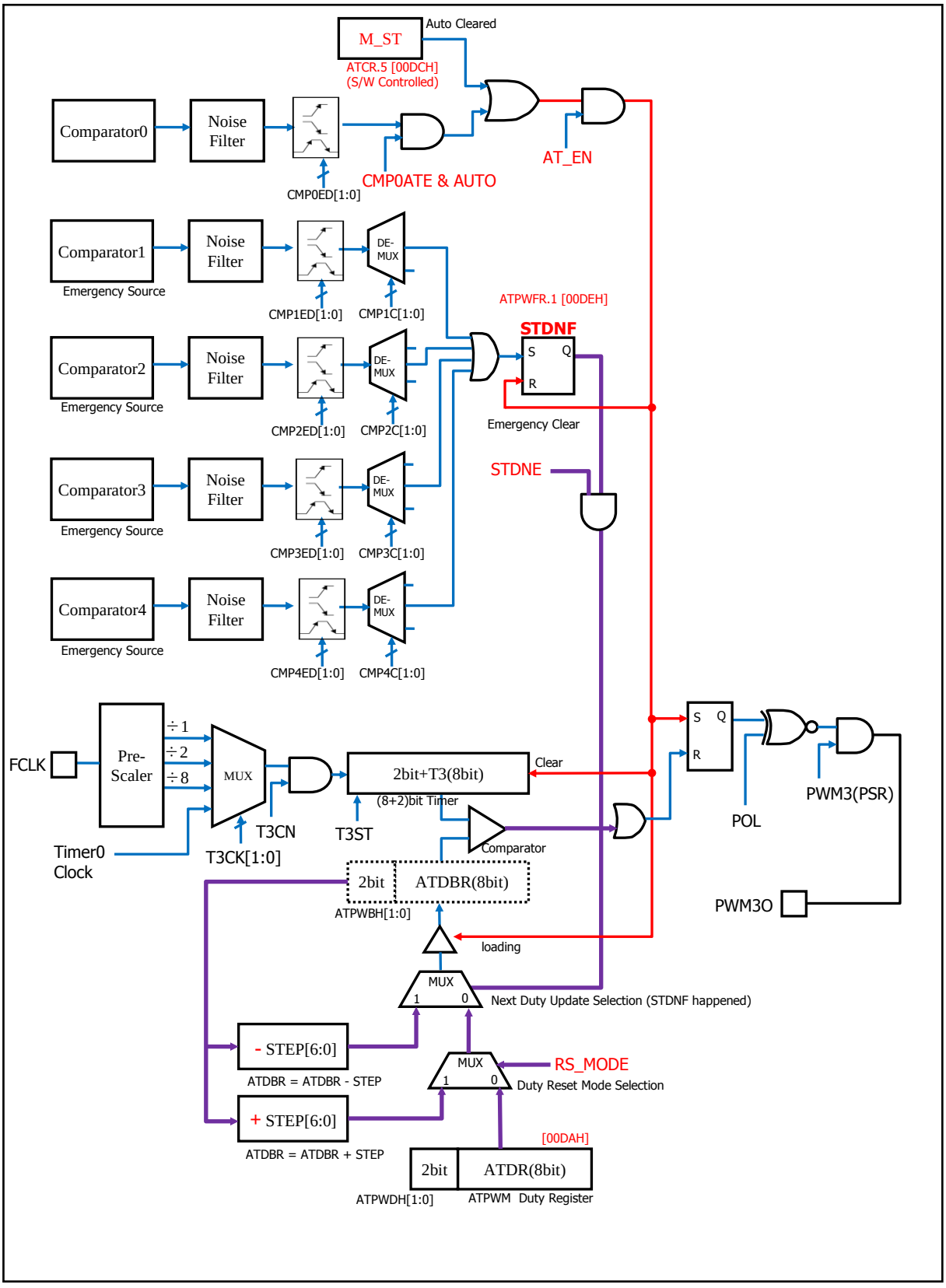


Figure 3.27 Auto Triggering PWM Mode by Emergency STDN Type

00DCH	ATCR (Auto Triggering PWM Mode Control Register)

Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
Value	1	X	X	1	X	X	0	X

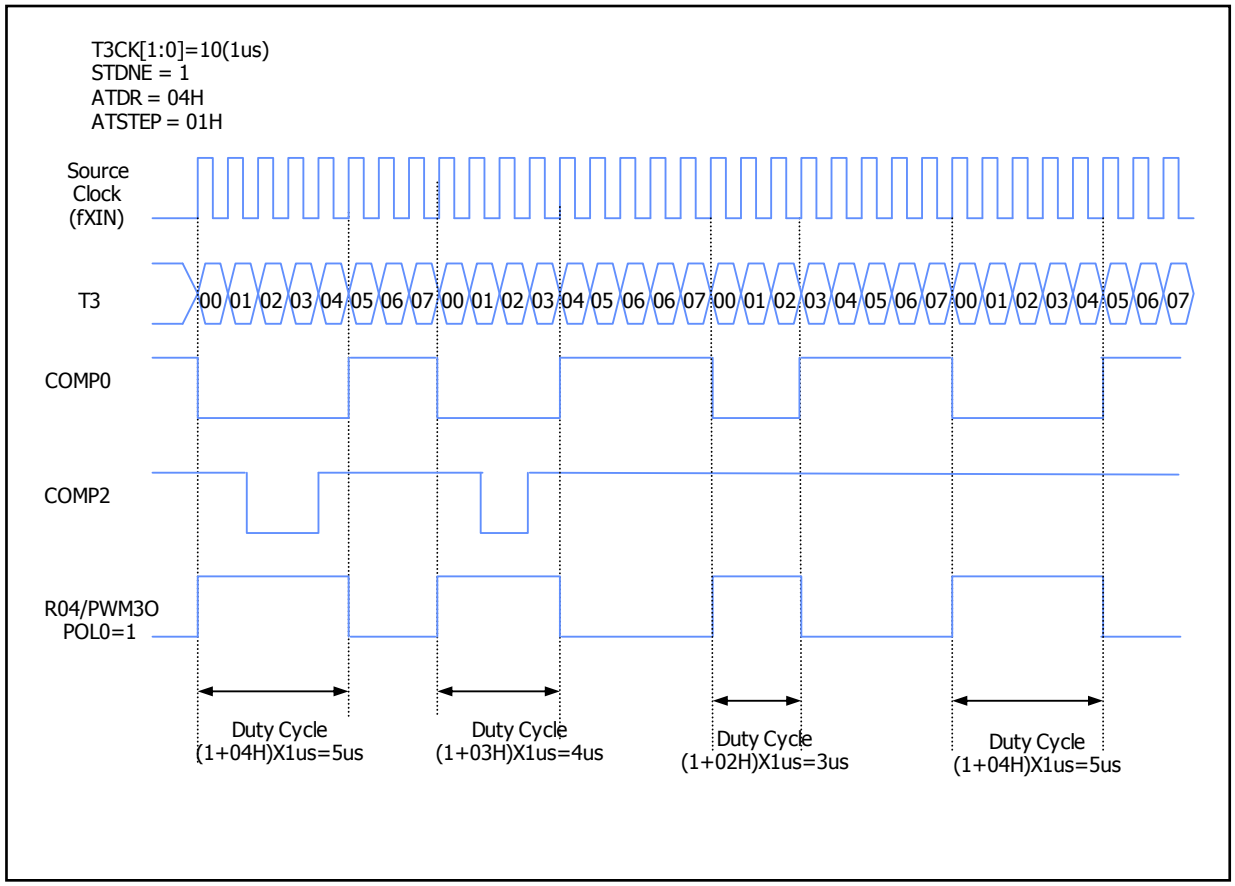


Figure 3.28 Example of STDN Mode (Duty Reset Mode)

If the STDN is enabled for comparator-2 output, the next ATDBR is decreased on compactor-2 trigger. If there is no trigger of comparator-2, the ATDBR is immediately restored to ATDR (RS_MODE 0). If RS_MODE is 1, the ATDBR will be increased with ATSTEP.

```
# CMP0 Trigger (or Manual Start) and Auto Decrement STDN Mode by CMP1 Trigger
    LDM    ATCR,   #90H    ; ATPWM Enabled, STDN Enabled, Maximum period Disabled
    LDM    PSR2,   #05H    ; CMP2_P, CMP1_N secondary selection (comparator1 source)
    LDM    CMPEMCR,#02H    ; Using comp1 for STDN
    LDM    CMPPIN0,#08H    ; Comp1 positive input -> CMP2_P
    LDM    CMPEDS0,#08H    ; Comp1 output falling edge detect
    LDM    CMPLPF0,#00H    ; Comp1 output LPF Disable
    LDM    CMPCR,  #10H    ; CMP1 Enable
    LDM    ATDR,   #0FH    ; Duty Register
    LDM    ATMPR,  #2FH    ; Maximum Period
    LDM    ATSTEP, #06H    ; Auto Decrement Step -> 06H, Direct Restore Mode
    LDM    ATPWFR, #00H    ; clear flag
    SET1   ATCR.5          ; Manual Start (M_ST) or wait CMP0 Trigger
```

CMP0 Trigger (or Manual Start) and Auto Increment STDN Mode by CMP1 Trigger

LDM ATSTEP, #86H ; Auto Decrement Step -> 06H, Increment Restore Mode

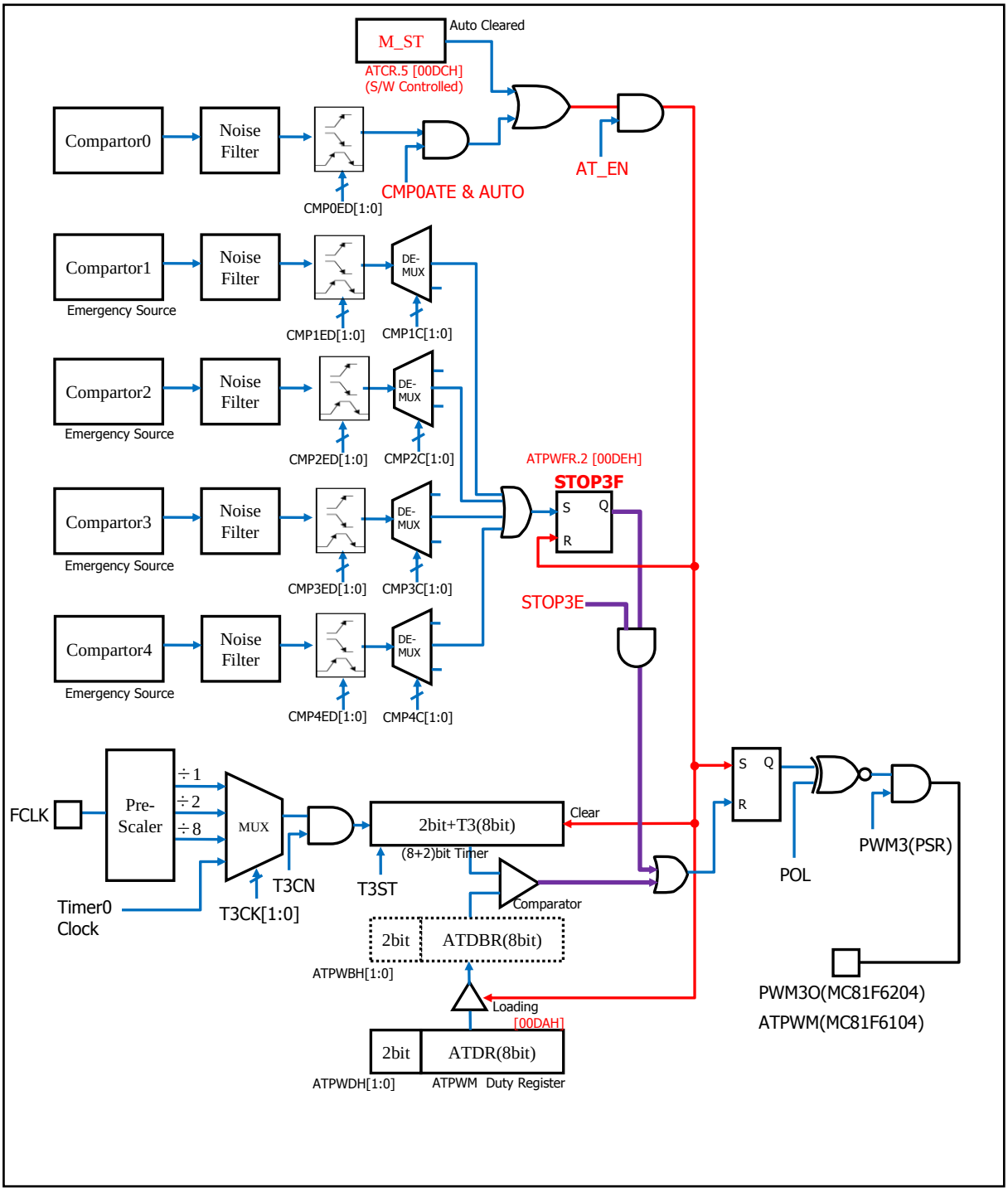


Figure 3.29 Auto Triggering PWM Mode by Emergency STOP3 Type

00DCH	ATCR (Auto Triggering PWM Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
Value	1	X	X	X	X	1	0	X

```
# CMP0 Trigger (or Manual Start) and STOP3 Emergency by CMP1 Trigger
    LDM    ATCR,  #8AH   ; ATPWM Enabled, STOP3E Enabled, Maximum period One Pulse
    LDM    PSR2,  #05H   ; CMP2_P, CMP1_N secondary selection (comparator1 source)
    LDM    CMPEMCR,#03H   ; Using comp1 for STOP3
    LDM    CMPPIN0,#08H   ; Comp1 positive input -> CMP2_P
    LDM    CMPEDS0,#08H   ; Comp1 output falling edge detect
    LDM    CMPLPF0,#00H   ; Comp1 output LPF Disable
    LDM    CMPCR, #10H   ; CMP1 Enable
    LDM    ATDR,  #0FH   ; Duty Register
    LDM    ATMPR, #2FH   ; Maximum Period
    LDM    ATPWFR, #00H   ; clear flag
    SET1   ATCR.5        ; Manual Start (M_ST) or wait CMP0 Trigger
```

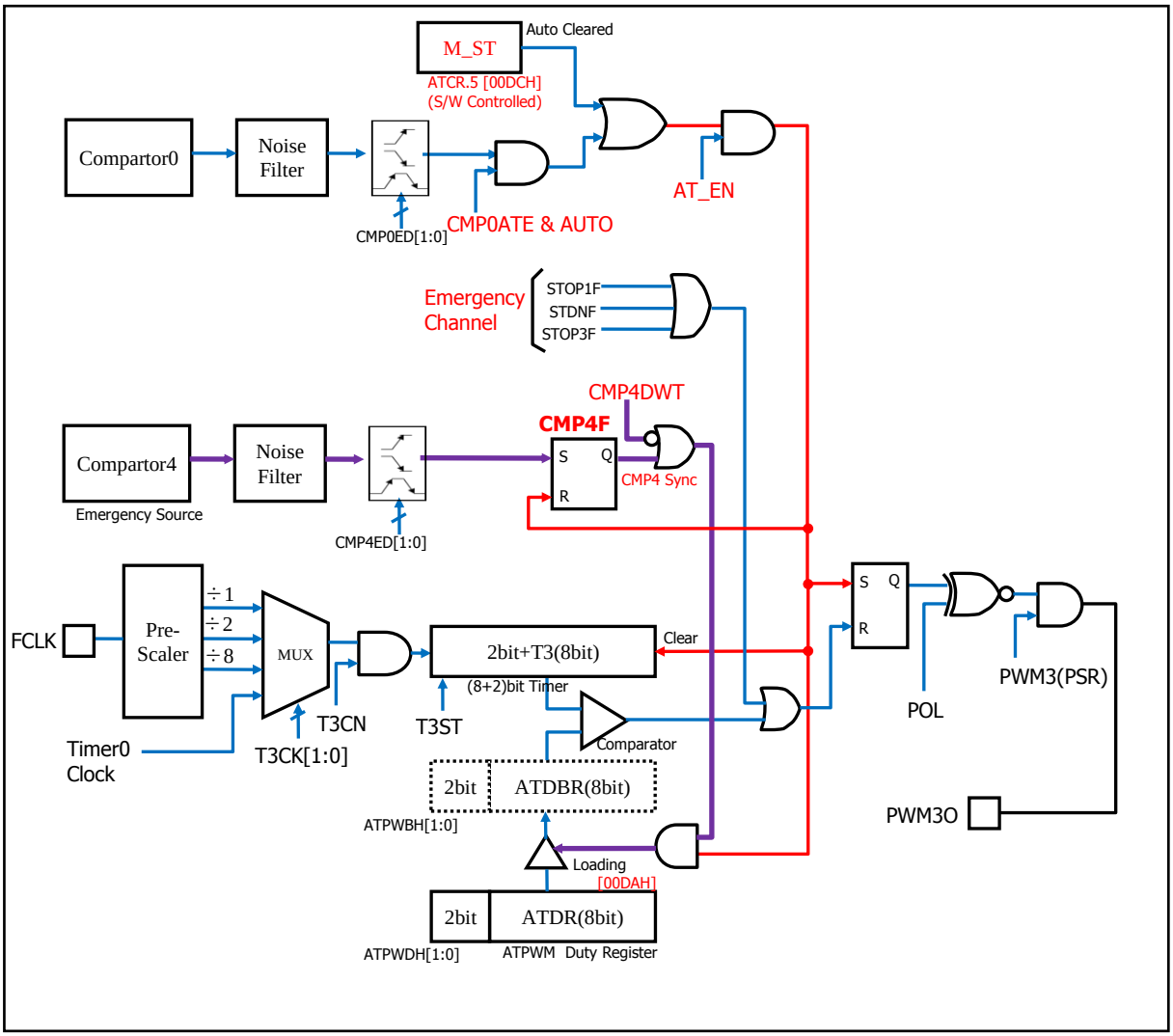


Figure 3.30 Duty Change Mode Synced by Compartor4 Trigger

00DCH	ATCR (Auto Triggering PWM Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
Value	1	X	X	X	X	X	0	X

00EAH	CMPCR (Analog Comparator Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CMPCR	CMP4EN	CMP3EN	CMP2EN	CMP1EN	CMP0EN	-	CMP4DWT	CMP0ATE
Value	1	X	X	X	1	-	1	1

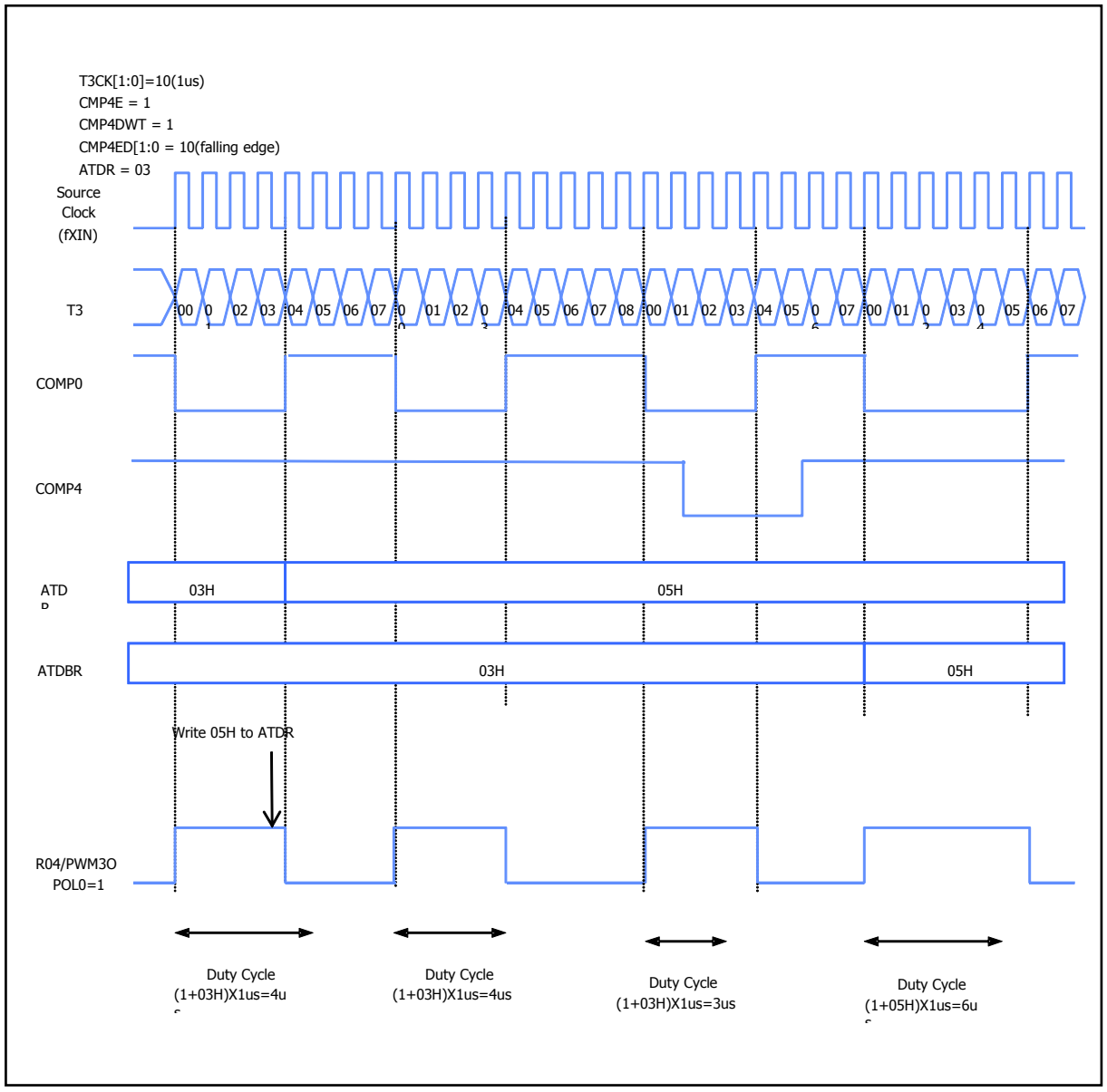


Figure 3.31 Example of Duty Change Synced by Comparator4

The ATDBR is basically updated with ATDR on comparator0 trigger (CMP4DWT is 0). If CMP4DWDT is 1, the ATDBR is not updated with ATDR until the comparator4 trigger happens. The ATDBR is updated with ATDR on first comparator0 trigger after the comparator4 trigger happens.

```
# CMP0 Trigger (or Manual Start) and ATDBR Update Mode Synced by CMP4 Trigger
    LDM    ATCR,   #80H    ; ATPWM Enabled, Maximum period Disabled
    LDM    PSR2,   #0CH    ; CMP2_P, CMP$_N secondary selection (comparator4 source)
    LDM    CMPEMCR,#00H    ; Emergency Channel Disabled
    LDM    CMPPIN1,#02H    ; Comp4 positive input -> CMP2_P
    LDM    CMPEDS1,#02H    ; Comp4 output falling edge detect
    LDM    CMPLPF1,#00H    ; Comp4 output LPF Disable
    LDM    CMPCR,  #82H    ; CMP4 Enabled, CPW4DWT Enabled (ATDBR sync mode by CMP4)
    LDM    ATDR,   #1FH    ; Duty Register
    LDM    ATMPR,  #2FH    ; Maximum Period
```

```
LDM     ATPWFR, #00H    ; clear flag
SET1    ATCR.5          ; Manual Start (M_ST) or wait CMP0 Trigger
```

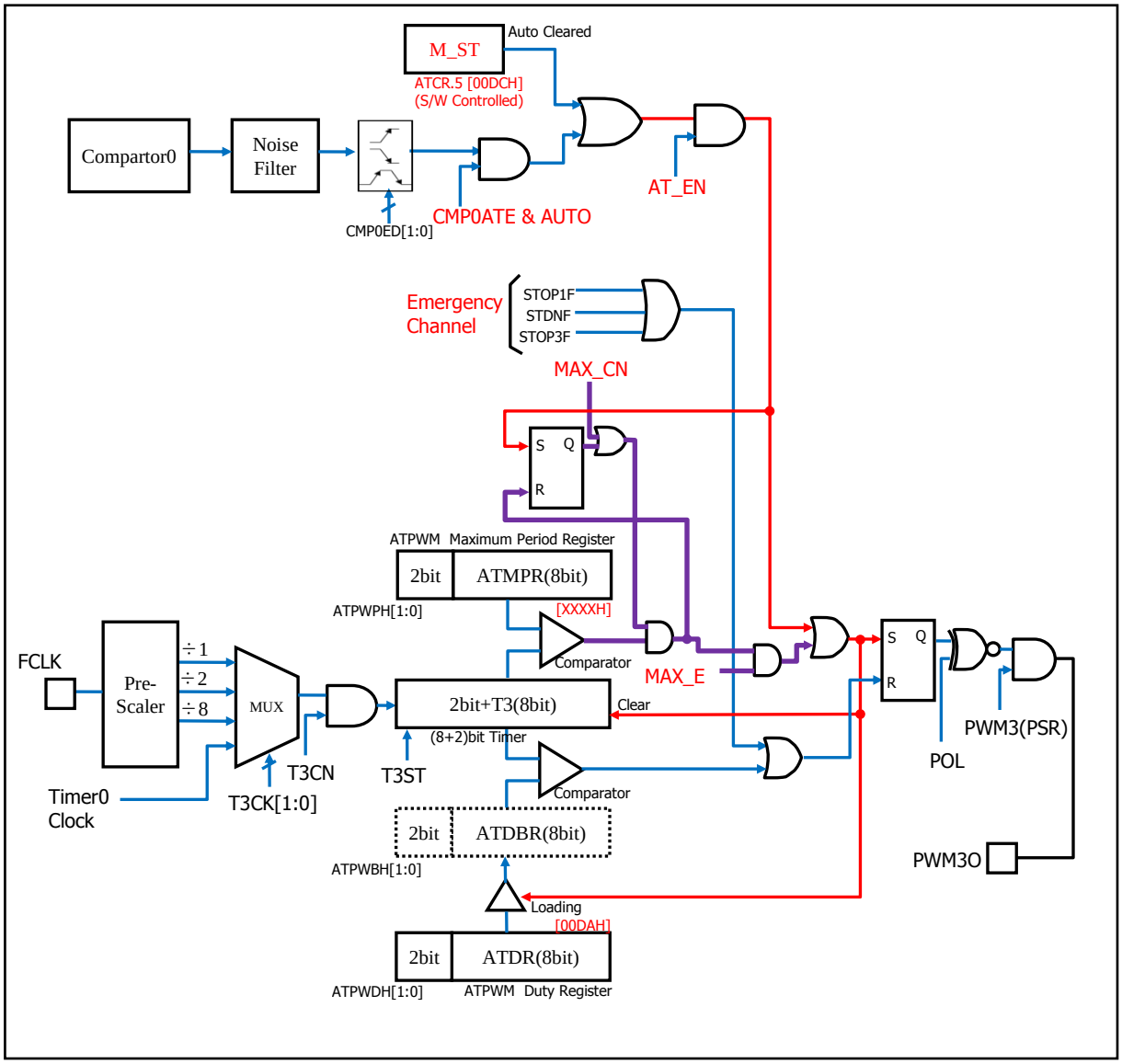


Figure 3.32 Auto Triggering PWM Maximum Period Auto Start Mode

00DCH	ATCR (Auto Triggering PWM Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ATCR	AT_EN	AUTO	M_ST	STDNE	STOP1E	STOP3E	MAX_E	MAX_CN
Value	1	X	X	X	X	X	1	X

```
# CMP0 Trigger (or Manual Start) and Maximum Period Restart (one pulse)
    LDM     ATCR,   #8AH    ; ATPWM Enabled, STOP1E Enabled, Maximum period One Pulse
```

```
    LDM     T3CR,   #C6H    ; ATPWM Mode, Fx/2, T3CN, POL1
    LDM     PSR1,   #01H    ; select PWM3
    LDM     ATDR,   #0FH    ; Duty -> 0FH
    LDM     ATMPR,  #2FH    ; Maximum Period -> 2FH
    SET1    T3ST            ; Start T3 Counter
    SET1    ATCR.5          ; Manual Start (M_ST) or wait CMP0 Trigger
```

```
# CMP0 Trigger (or Manual Start) and Maximum Period Restart (Continuous pulse)
    LDM     ATCR,   #83H    ; ATPWM Enabled, Maximum period Continuous Pulse
    LDM     T3CR,   #C6H    ; ATPWM Mode, Fx/2, T3CN, POL1
    LDM     PSR1,   #01H    ; select PWM3
    LDM     ATDR,   #0FH    ; Duty -> 0FH
    LDM     ATMPR,  #2FH    ; Maximum Period -> 2FH
    SET1    T3ST            ; Start T3 Counter
    SET1    ATCR.5          ; Manual Start (M_ST) or wait CMP0 Trigger
```

3.12 Interrupt Controller

3.12.1 Overview

The Interrupt Controller contains interrupt enable register (IENH,IENL), interrupt request register (IRQH,IRQL), interrupt edge selection register (IEDS), interrupt flag register (IFR), priority circuit, master enable flag (I flag from PSW).

- External Interrupt INT0,INT1,INT2,INT3
- Comparator Interrupt CMP0,CMP1,CMP2,CMP3, CMP4
- Peripheral Interrupt (BIT,T0,T2,T3,ADC,BIT,WDT)
- Multiple Interrupt Supported
- Software Interrupt by IRQH,IRQL setting
- Interrupt Masking Support by IENH,IENL except RESET

The interrupt request operating is globally controlled by I flag bit of PSW register of CPU. The I flag have to be set before interrupt service routine started. On interrupt requested, its interrupt request flag maintains until the CPU accepts the interrupt (auto cleared).

The BRK command is used to request the software interrupt. The BRK command set the B-bit of PSW, reset the I-bit of PSW after the current PC(program counter), PSW(program status word) has been saved into stack. The BRK vector tables shares the TCALL0 routine. The B-bit of PSW can be used to determine whether BRK vector happens or TCALL0 is requested.

Because interrupt request clears the interrupt enable bit, any other interrupts is ignored during a interrupt service routine is performed. The EI command activates the multiple interrupt service features based on interrupt

priority. Although any interrupt service routine is being performed, an interrupt having higher priority interrupt is immediately accepted. The paused interrupt service is immediately performed after the prior interrupt returned.

3.12.2 Block Diagram

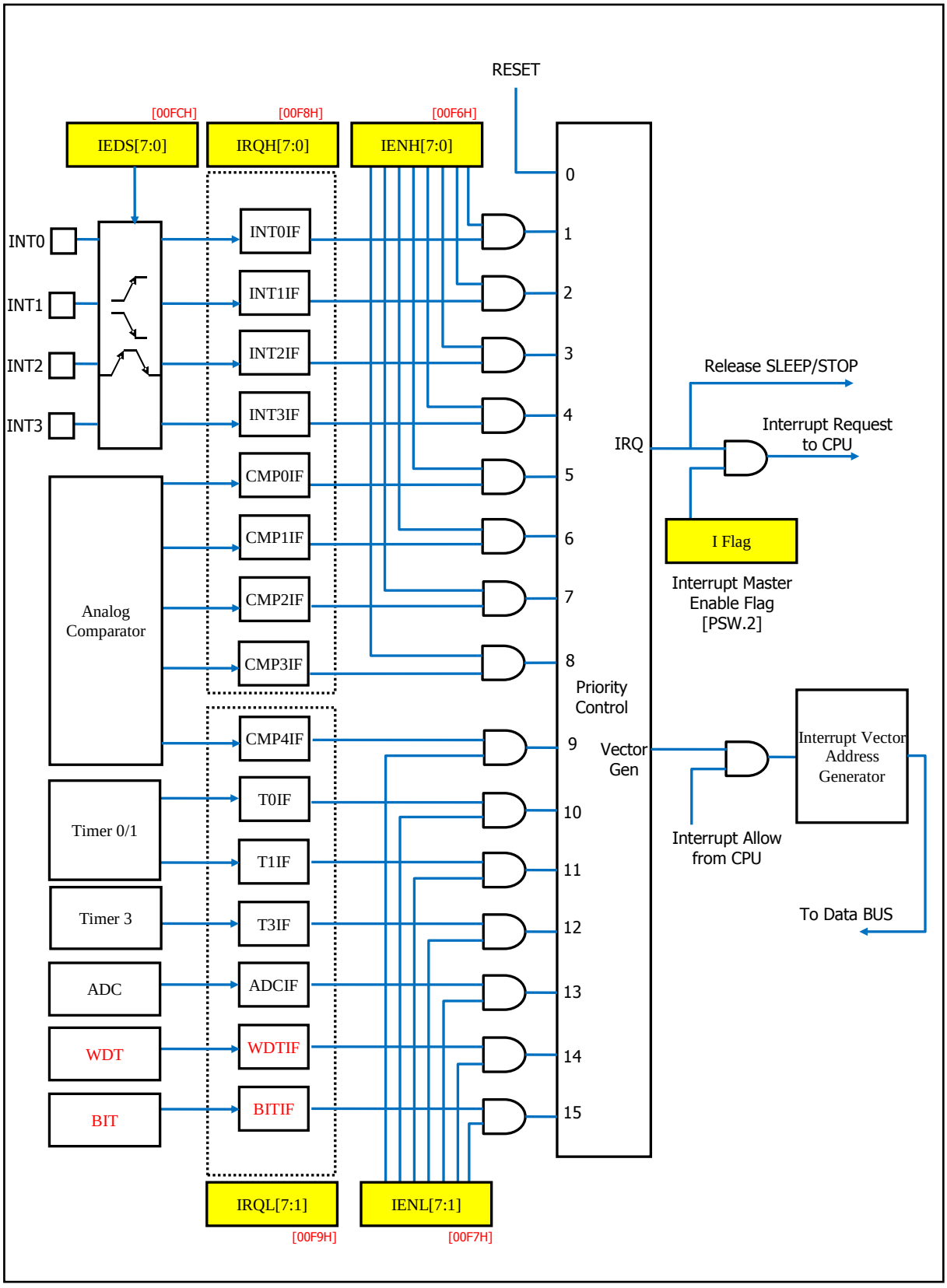


Figure 3.33 Block Diagram of Interrupt Controller

00F6H	IENH (Interrupt Enable Register High)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IENH	INT0IE	INT1IE	INT2IE	INT3IE	CMP0IE	CMP1IE	CMP2IE	CMP3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.44 IENH - Interrupt Enable Register High

0: Interrupt Disabled, 1: Interrupt Enabled

00F7H	IENL (Interrupt Enable Register Low)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IENL	CMP4IE	T0IE	T1IE	T3IE	ADCIE	WDTIE	BITIE	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
RESET	0	0	0	0	0	0	0	-

Table 3.45 IENL - Interrupt Enable Register Low

0: Interrupt Disabled, 1: Interrupt Enabled

00F8H	IRQH (Interrupt Request Flag High Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IRQH	INT0IF	INT1IF	INT2IF	INT3IF	CMP0IF	CMP1IF	CMP2IF	CMP3IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.46 IRQH - Interrupt Request Flag High Register

0: Interrupt not occurred, 1: Interrupt Requested

00F9H	IRQL (Interrupt Request Flag Low Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IRQL	CMP4IF	T0IF	T1IF	T3IF	ADCIF	WDTIF	BITIF	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
RESET	0	0	0	0	0	0	0	-

Table 3.47 IRQL - Interrupt Request Flag Low Register

0: Interrupt not occurred, 1: Interrupt Requested

00FCH	IEDS (Interrupt Edge Selection Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IEDS	IED3H	IED3L	IED2H	IED2L	IED1H	IED1L	IED0H	IED0L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Table 3.48 IEDS - Interrupt Edge Selection Register

Address	[1]	[0]	Remark
00FCH	IED0H	IED0L	INT0 Edge Selection Register
	0	0	Reserved
	0	1	Falling Edge
	1	0	Rising Edge
	1	1	Both (Falling & Rising Edge)

Address	[3]	[2]	Remark
00FCH	IED1H	IED1L	INT1 Edge Selection Register
	0	0	Reserved
	0	1	Falling Edge
	1	0	Rising Edge
	1	1	Both (Falling & Rising Edge)

Address	[5]	[4]	Remark
00FCH	IED2H	IED2L	INT2 Edge Selection Register
	0	0	Reserved
	0	1	Falling Edge
	1	0	Rising Edge
	1	1	Both (Falling & Rising Edge)

Address	[7]	[6]	Remark
00FCH	IED3H	IED3L	INT3 Edge Selection Register
	0	0	Reserved
	0	1	Falling Edge
	1	0	Rising Edge
	1	1	Both (Falling & Rising Edge)

3.12.3 Interrupt Category

The interrupts have three categories of maskable interrupt request, unmaskable reset interrupt, and software interrupt (BRK). The interrupts are controlled by interrupt priority handler with priority level(0~15). The each interrupt has its target address to jump into service routine. The following tables describe all summary of interrupt priority, maskable option, and target address for each interrupt.

Request Source	Symbol	Priority	MASK	Vector High	Vector Low
Hardware Reset	RESETB	0	Non Maskable	FFFFh	FFFEh
External Interrupt 0	INT0	1	Maskable	FFFDh	FFFCh
External Interrupt 1	INT1	2		FFFBh	FFFAh

External Interrupt 2	INT2	3		FFF9h	FFF8h
External Interrupt 3	INT3	4		FFF7h	FFF6h
Analog Comparator 0	CMP0	5		FFF5h	FFF4h
Analog Comparator 1	CMP1	6		FFF3h	FFF2h
Analog Comparator 2	CMP2	7		FFF1h	FFF0h
Analog Comparator 3	CMP3	8		FFEFh	FFEEh
Analog Comparator 4	CMP4	9		FFEDh	FFECh
Timer 0 Interrupt	T0	10		FFEBh	FFEAh
Timer 1 Interrupt	T1	11		FFE9h	FFE8h
Timer 3 Interrupt	T3	12		FFE7h	FFE6h
ADC Interrupt	ADC	13		FFE5h	FFE4h
WDT Interrupt	WDT	14		FFE3h	FFE2h
BIT Interrupt	BIT	15		FFE1h	FFE0h

Table 3.49 Interrupt Vector Address

3.13 A/D Converter

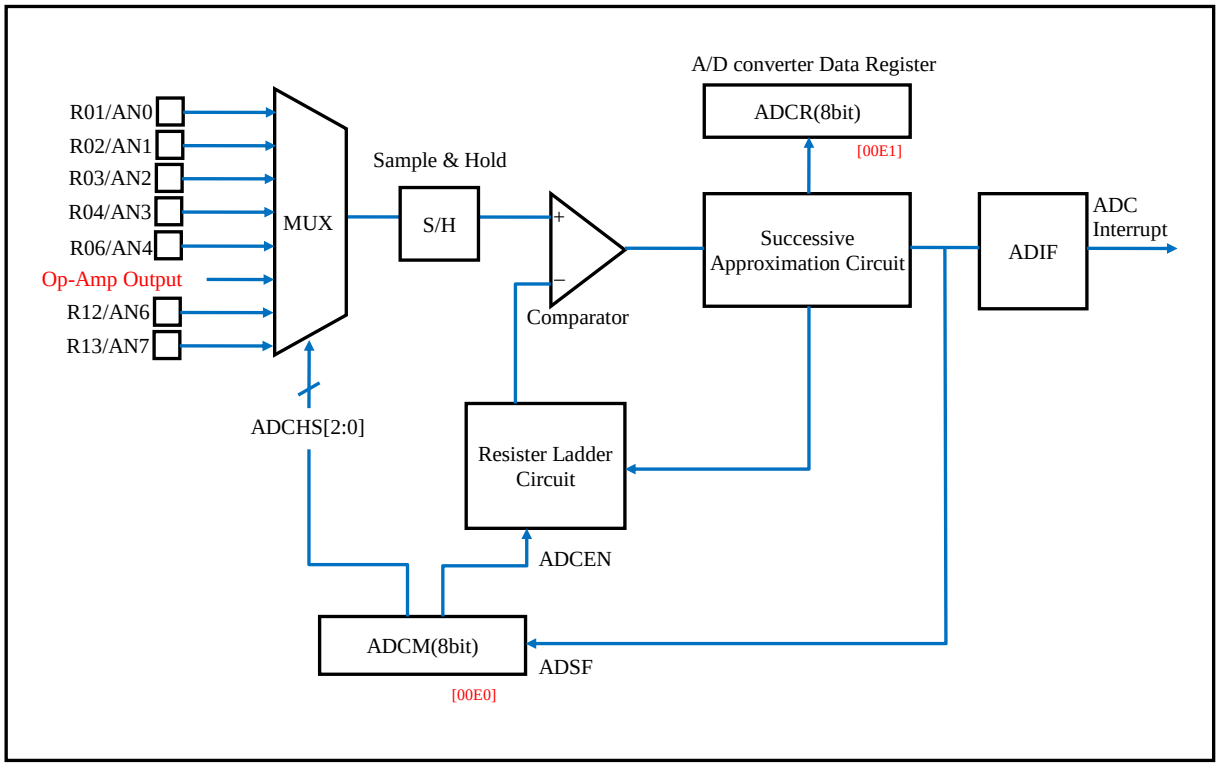


Figure 3.34 8-bit A/D Converter Block Diagram

Figure 3.34 is an abstract block diagram of our A/D converter. The analog input can be selected with ADCHS[3:0]. The A/D converter processing result is saved in ADCR[7:0] The following table describes registers related in A/D converter. To start A/D conversion, the ADCST bit must be set. After the A/D conversion finished, the ADSF is set to 1. The ADC On/Off is globally controlled by ADCEN bit.

00E0H	ADCM (A/D Converter Mode Control Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ADCM	-	ADCEN	-	ADCHS[3:0]			ADCST	ADSF
R/W	-	R/W	-	R/W	R/W	R/W	R/W	R
RESET	0	0	-	0	0	0	0	0

Table 3.50 ADCM - A/D Converter Mode Control Register

Address	[6]	Remark
00E0H	ADCEN	A/D Converter Enable
	0	ADC Disabled
	1	ADC Enabled

Address	[4]	[3]	[2]	Remark
00E0H	ADCHS[2:0]			A/D Converter Channel Selection
	0	0	0	Channel 0 (AN0)
	0	0	1	Channel 1 (AN1)
	0	1	0	Channel 2 (AN2)
	0	1	1	Channel 3 (AN3)
	1	0	0	Channel 4 (AN4)
	1	0	1	Op-Amp Output
	1	1	0	Channel 6 (AN6)
	1	1	1	Channel 7 (AN7)

Address	[1]	Remark
00E0H	ADCST	A/D Converter Start Control
	0	Stopped
	1	A/D Conversion start

Address	[0]	Remark
00E0H	ADSF	A/D Converter Status Bit
	0	During A/D Conversion (clear on ADC Started)
	1	A/D Conversion Finished

00E1H	ADCR (A/D Converter Data Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ADCR	ADCR[7:0]							
R/W	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

Table 3.51 A/D Converter Data Register

3.14 Buzzer Driver

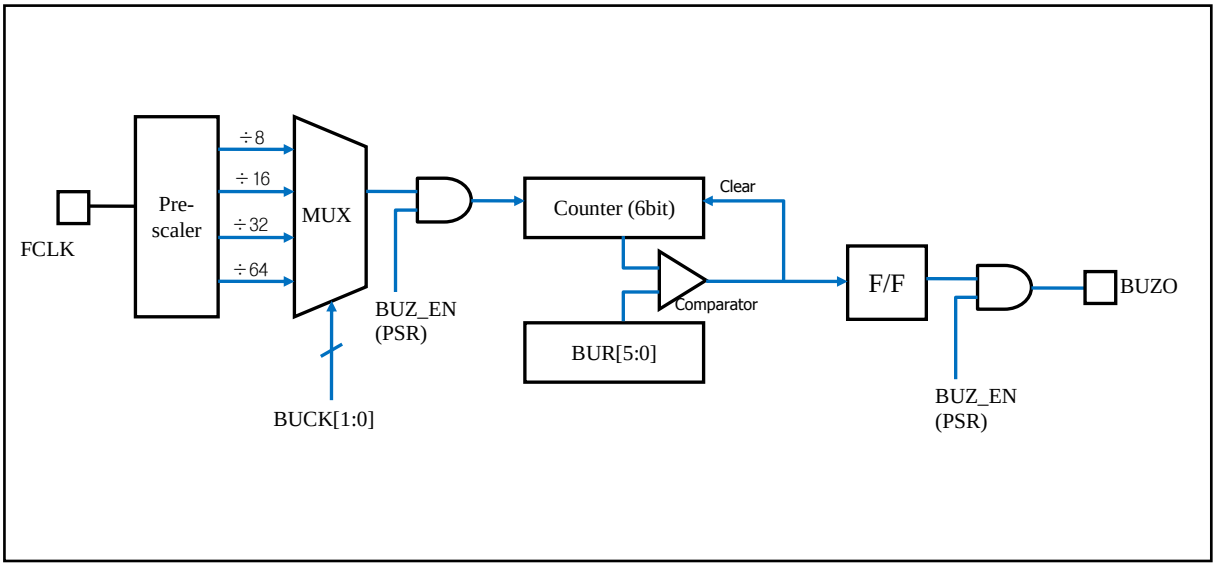


Figure 3.35 Block Diagram of BUZZER Driver

00CEH	BUZR (Buzzer Driver Register)							
Bit[7:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BUZR	BUCK[1:0]		BUR[5:0]					
W	W	W	W	W	W	W	W	W
RESET	1	1	1	1	1	1	1	1

Table 3.52 Buzzer Driver Control Register

Address	[7]	[6]	Remark
00CEH	BUCK[1:0]		Buzzer Clock Selection
	0	0	$fx/2^3$
	0	1	$fx/2^4$
	1	0	$fx/2^5$
	1	1	$fx/2^6$

Address	Bit 5~0	Remark
00CEH	BUR[5:0]	Buzzer Period Data
	00_0000	00h
	11_1111	3Fh

3.14.1 Minimizing Current Consumption

3.14.1.1 Input Pins

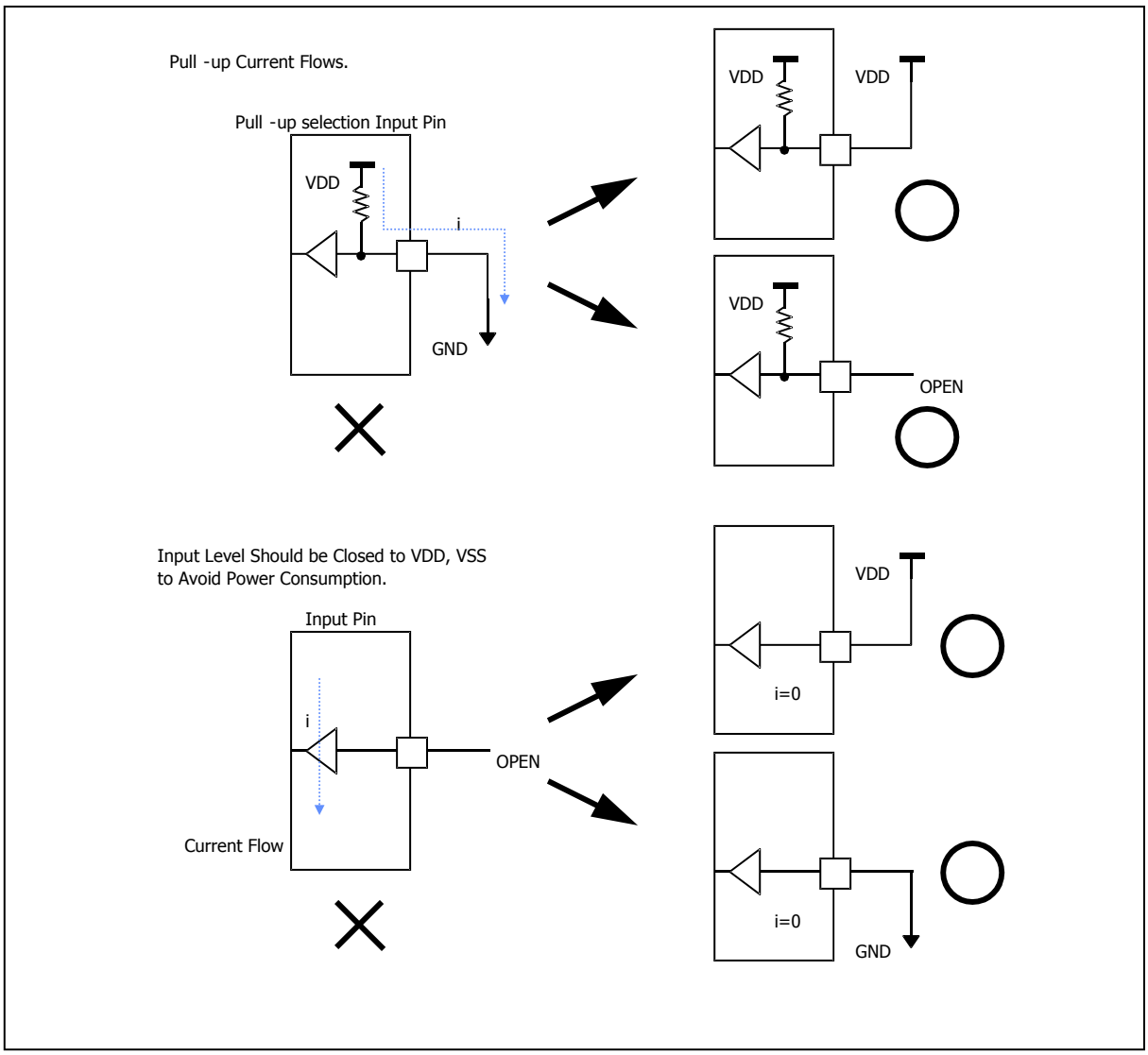


Figure 3.36 Input Pin Configuration for Minimizing Current Consumption

3.14.1.2 Output Pins

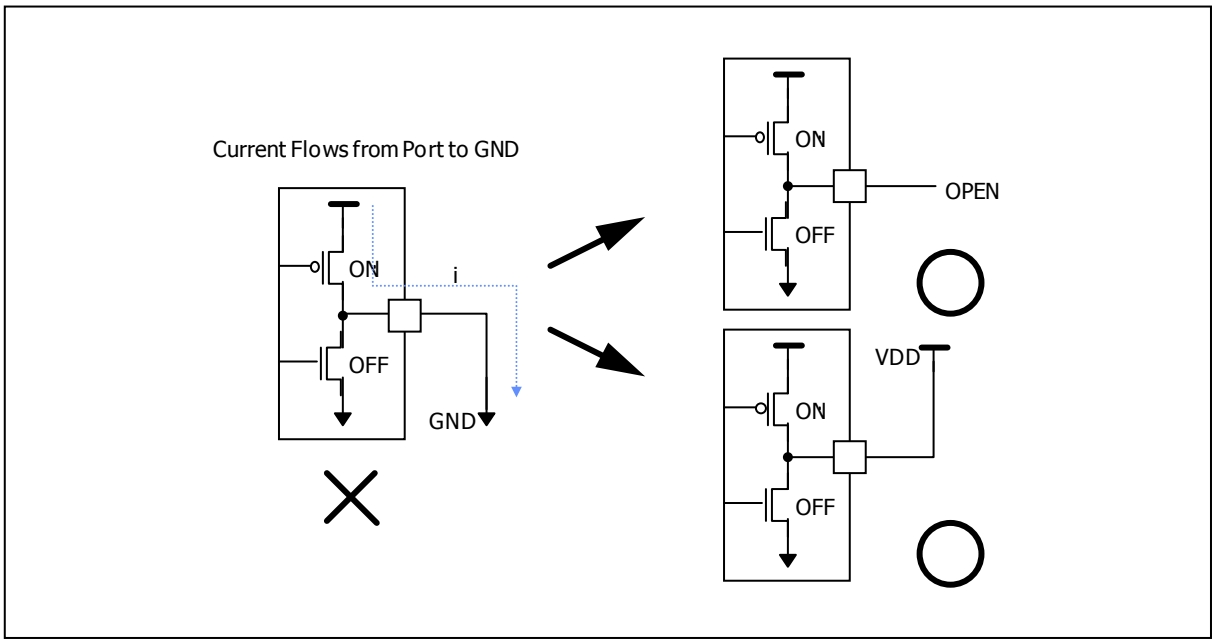


Figure 3.37 Output Pin Configuration for Minimizing Current Consumption

4. Serial Flash Programming Specification

4.1 Pin Diagram for Serial Flash

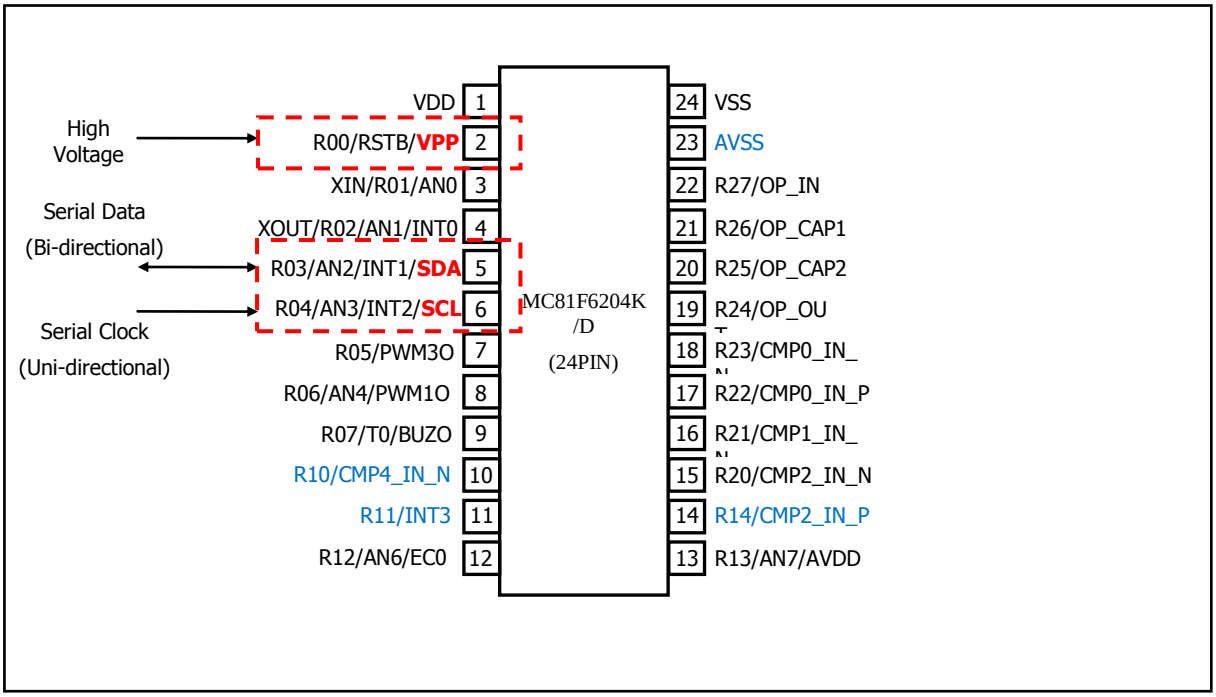


Figure 4.1 Ports for Serial Flash

4.2 Programming Region

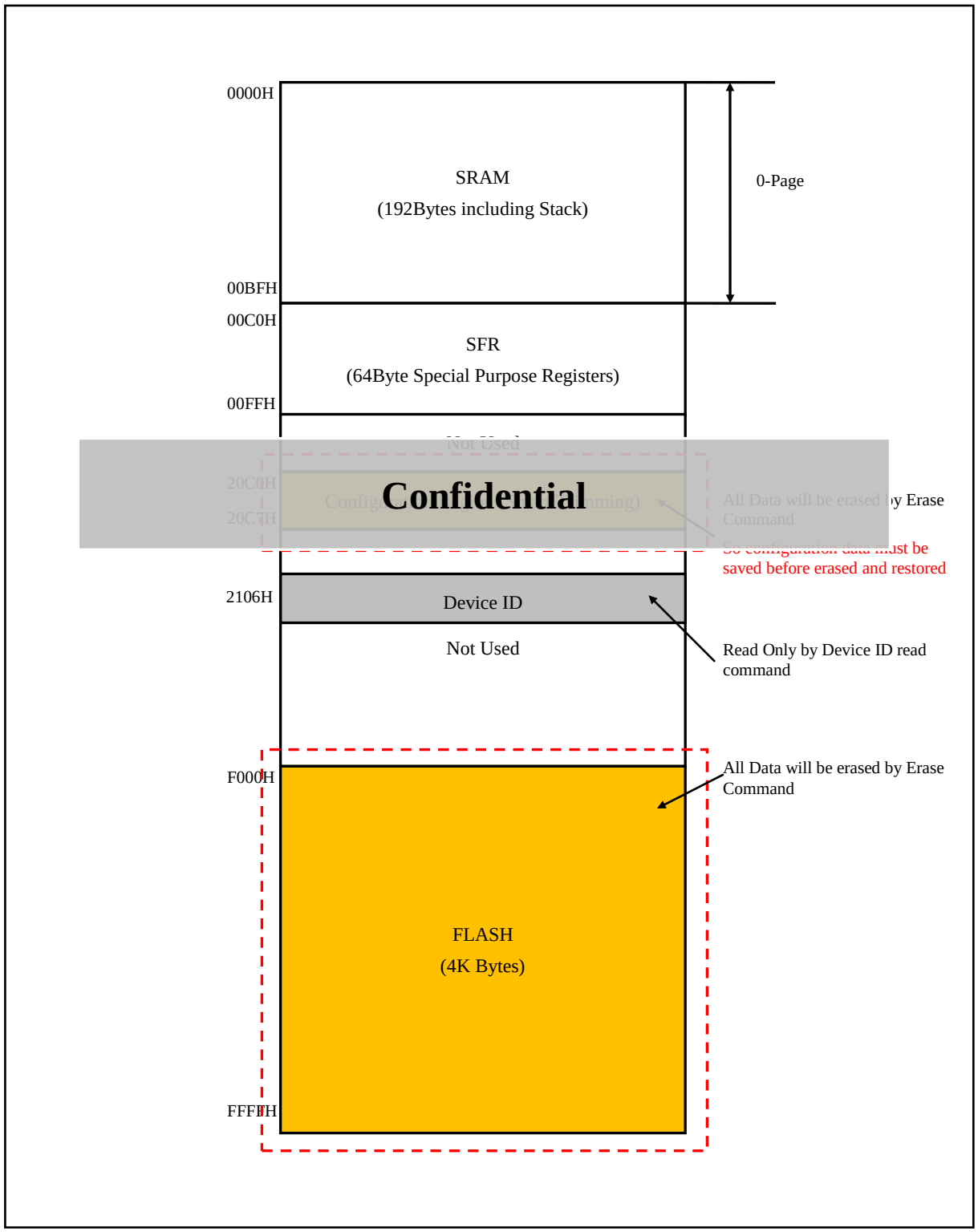


Figure 4.2 Programming Region

4.3 Flash Command (Confidential)

Byte	1'ST Byte			2'ND Byte	3'RD Byte	....	Comment	
Mode	Code	Address 2 (A19-A16)	Code	Address 1 (A15-A8)	Address 0 (A7-A0)	Data (D7-0)		
Bit n	**B23-B21**	**B20-B17**	**B16**	**B15-B8**	**B7-B0**			
PGM1B	010b	xxxxb	0	XXh	XXh	**h	20us	Main ROM PGM
			1	XXh	XXh	**h	40us	
PGM of Config 1	010	0000b	0	20h	C4h	Comment	20us	20C4 : xxxx,xxxxb 20C5 : xxxx,xxxxb 20C6 : xxxx,xxxxb 20C7 : xxxx,0xxxb
			1	20h	C4h	Comment	40us	
PGM of Config 2	010	0000b	0	20h	C0h	**h	20us	Config PGM - 4 bytes (20C0~20C3)
			1	20h	C0h	**h	40us	
Read Protection	010	0000b	0	20h	C7h	0000,1000b	20us	Read protection set
			1	20h	C7h	0000,1000b	40us	
Read	101b	xxxxb	1	XXh	XXh	**h	Main ROM Read	
Read of Config 1	101b	0000b	1	20h	C4h	**h	Config ROM Read - 4 bytes (20C4~20C7)	
Read of Config 2	101b	0000b	1	20h	C0h	**h	Config ROM Read - 4 bytes (20C0~20C3)	
PGM Verify	110b	xxxxb	0	XXh	XXh	**h	VPP Enable	
Chip Erase	100b	--yyb	1	XXh	XXh	**h	by = erase time (1, 2, 4, 8 ms)	
Erase Verify 2	100b	0000b	0	20h	C0h	**h	VPP Disable, Internal RC Sync.	
Pre Program	111b	0101b	0	20h	C0h	**h	Internal RC Sync.	
Read User	101b	0000b	1	21h	06h	**h	User ID Read(1 bytes)	

Byte	1'ST Byte			2'ND Byte	3'RD Byte	....	Comment	
Mode	Code	Address 2 (A19-A16)	Code	Address 1 (A15-A8)	Address 0 (A7-A0)	Data (D7-0)		
Bit n	**B23-B21**	**B20-B17**	**B16**	**B15-B8**	**B7-B0**			
ID								
PGM8B	011b	xxxxb	0	XXh	XXh	**h	20 us	Main ROM PGM
			1	XXh	XXh	**h	40 us	
Erase Verify	110b	xxxxb	1	XXh	XXh	**h	VPP Disable, SCL Sync.	
Cell VT Measure	001b	xxxxb	1	XXh	XXh	**h	Reference Cell VT Measure	
PGM REF Cell	001b	xxxxb	0	XXh	XXh	**h	Reference Cell Program	
Erase REF Cell	000b	1010	1	XXh	XXh	**h	Erase time = 256us	
Flash Control Register Setting	000b	0101b	0	AAh	BBh	**h	AA = FCON0 (*) BB = FCON1 (*)	

Table 4.1 Summary of Flash Command

	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
FCON0	Checker_ Board	VEEIUP[1:0]		DNWOPT	EVFY[1]	EVFY[0]	PVFY[1]	PVFY[0]
FCON1	Bulk Stress	Gate Stress	Not Used	VBOOT_REG37[1:0]		VBOOT_ ACT_PRE	VBOOT_ DIS_PRE	M_PUP_ DIS

Table 4.2 Flash Control Register

4.4 Write/Read on Configuration Region

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~D3		
PGM	010	0000	0	20h	C4h		20us	**20C4 : xxxx,xxxxb** **20C5 : xxxx,xxxxb**
			1	20h	C4h		40us	**20C6 : xxxx,xxxxb** **20C7 : xxxx,0xxxb**

Table 4.3 Configuration Region (20C4~20C7) Programming Command

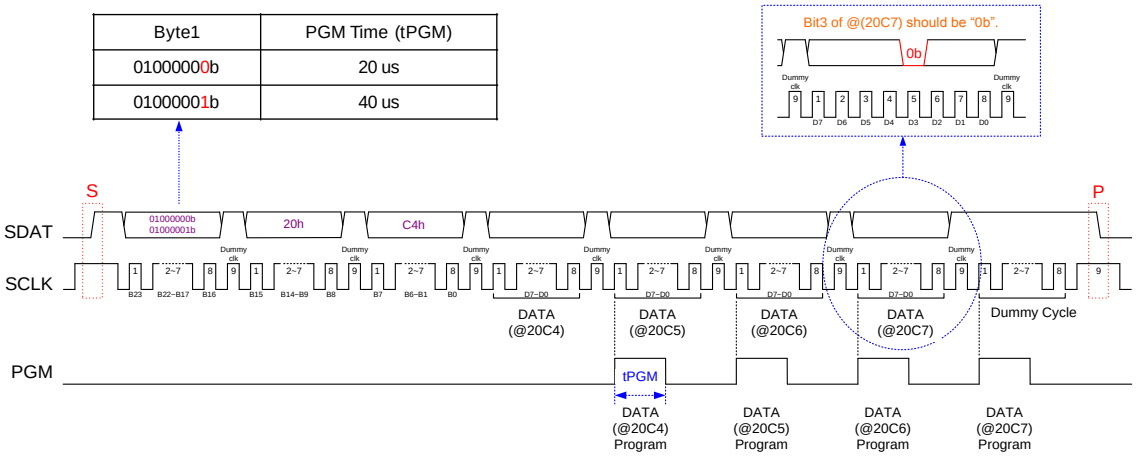


Figure 4.3 Programming on Configuration Region (20C4~20C7)

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~D3		
PGM	010	0000	0	20h	C0h		20us	**20C0 : xxxx,xxxxb** **20C1 : xxxx,xxxxb**
			1	20h	C0h		40us	**20C2 : xxxx,xxxxb** **20C3 : xxxx,xxxxb**

Table 4.4 Configuration Region (20C0~20C3) Programming Command

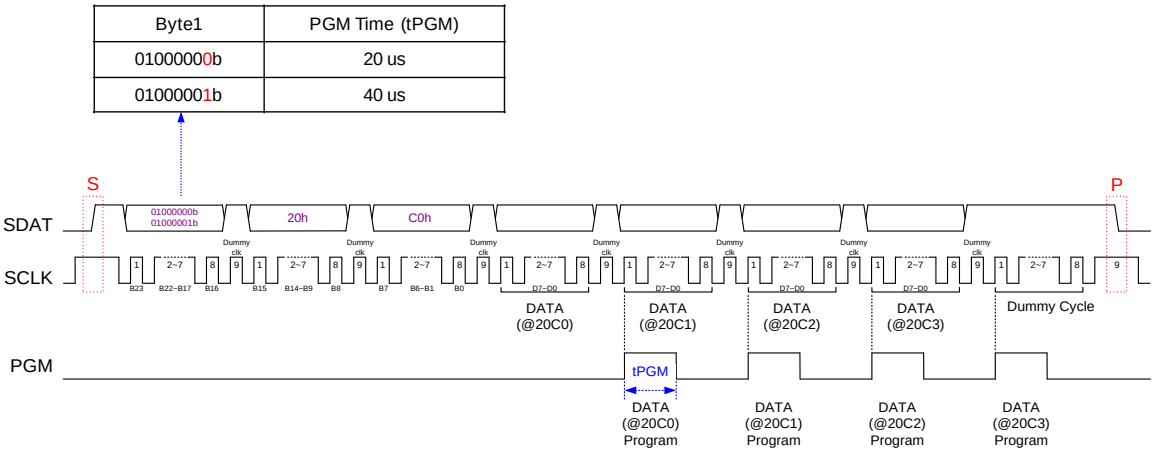
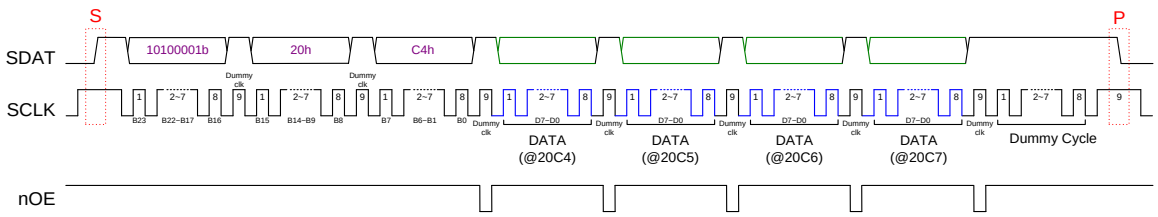


Figure 4.4 Programming on Configuration Region (20C0~20C3)

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~D3		
Read	101	0000	-	-	-	-	-	**Read Data (20C4 ~ 20C7) (Reverse Mode)**
			1	20h	C4h	Read Data	-	

Table 4.5 Configuration Region Read Command (20C4~20C7)

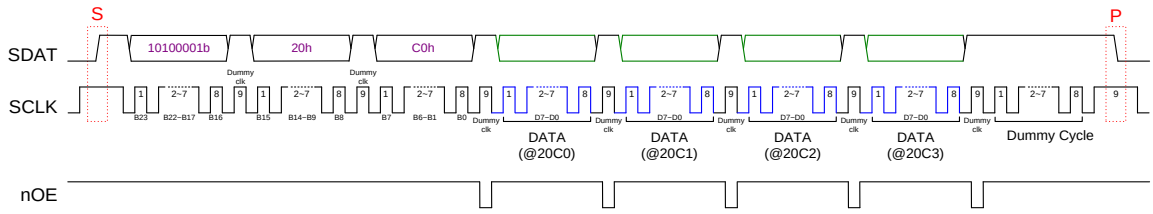


Config data can be read regardless of Read Protection bit setting.

Figure 4.5 Reading Configuration Region (20C4~20C7)

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~D3		
Read	101	0000	-	-	-	-	-	**Read Data (20C0 ~ 20C3) (Reverse Mode)**
			1	20h	C0h	Read Data	-	

Table 4.6 Configuration Region Read Command (20C0~20C3)



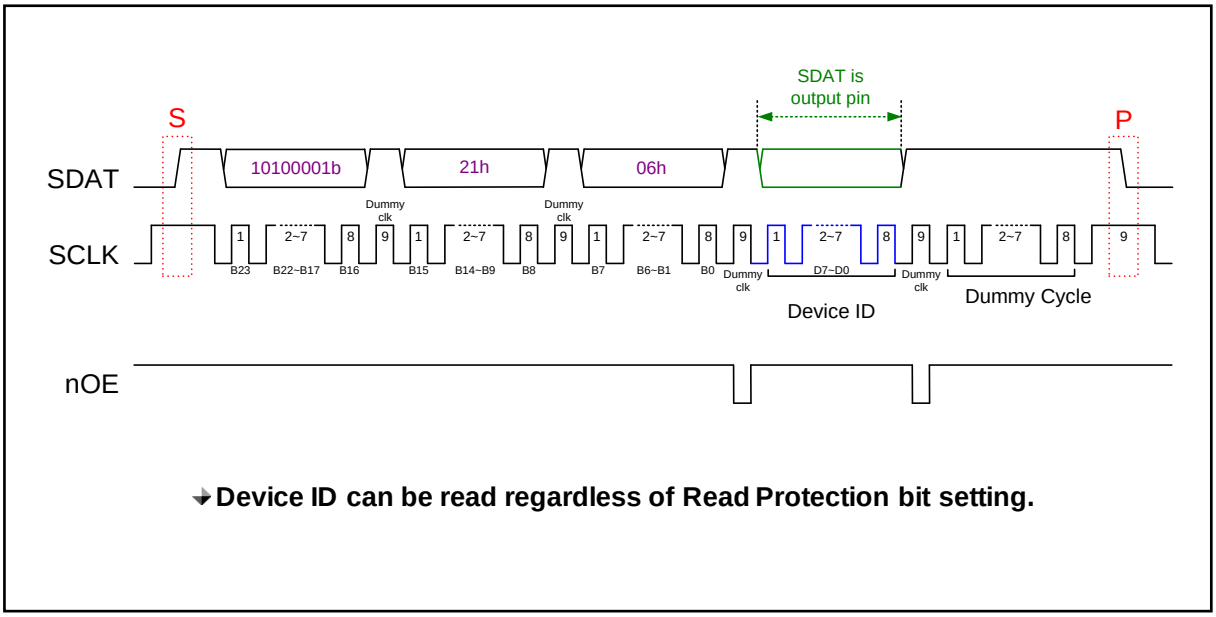
Config data can be read regardless of Read Protection bit setting.

Figure 4.6 Reading Configuration Region (20C0~20C3)

4.5 Reading Device ID

	1st Byte			2nd Byte	3rd Byte	1-th byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0		
Read	101	0000	-	-	-	-	-	**ID Data (2106h) (Reverse Mode)**
			1	21h	06h	ID	-	

Table 4.7 Device ID Read Command



Device ID can be read regardless of Read Protection bit setting.

4.6 Program and Verify

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~Dn		
PGM	010	xxxx	0	XXh	XXh	XXh	20us	**Main ROM Program**
			1	XXh	XXh	XXh	40us	

Table 4.8 Main ROM Program Command

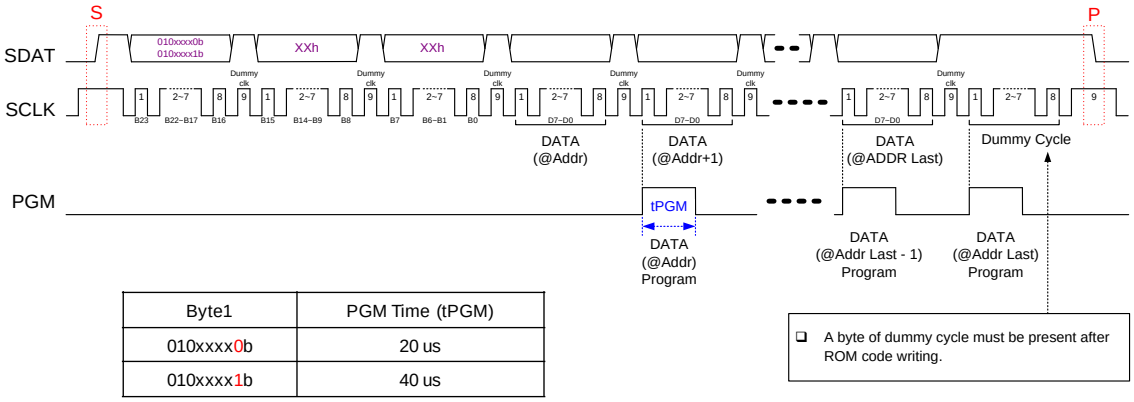


Figure 4.7 Main ROM Programming Timing Diagram

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Read Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~Dn		
Read	101	XXXX	-	-	-	-	-	**Main ROM Read**
			1	XXh	XXh	XXh	-	

Table 4.9 Main ROM Read Command

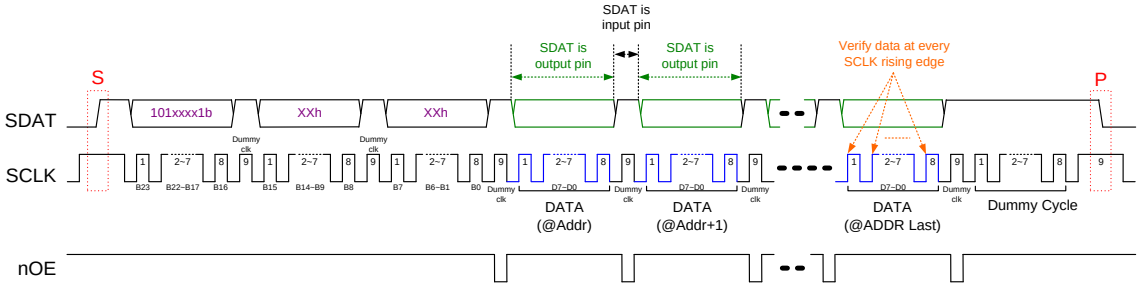


Figure 4.8 Main ROM Read Timing Diagram

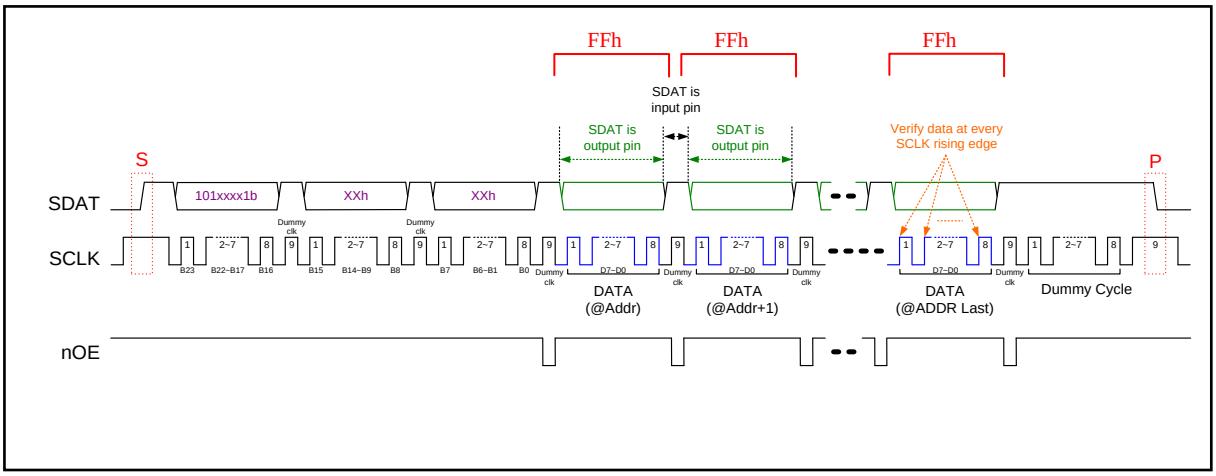
	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Read Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0~Dn		
PGM VFY	110	XXXX	0	XXh	XXh	XXh	-	**Main ROM Program Verify (FCON must be configured before PGM VFY executed)**
			-	-	-	-	-	

Table 4.10 Main ROM Program Verify Command

4.7 Read & Write after Setting Protection (lock) Bit

	1st Byte			2nd Byte	3rd Byte	N-th Byte	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Data		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	D0		
PGM	010	0000	0	20h	C7h	0000_1000b	20us	**Protection Bit Setting**
			1	20h	C7h	0000_1000b	40us	

Table 4.11 Protection(lock) Bit Setting Command



4.8 Erase Sequence

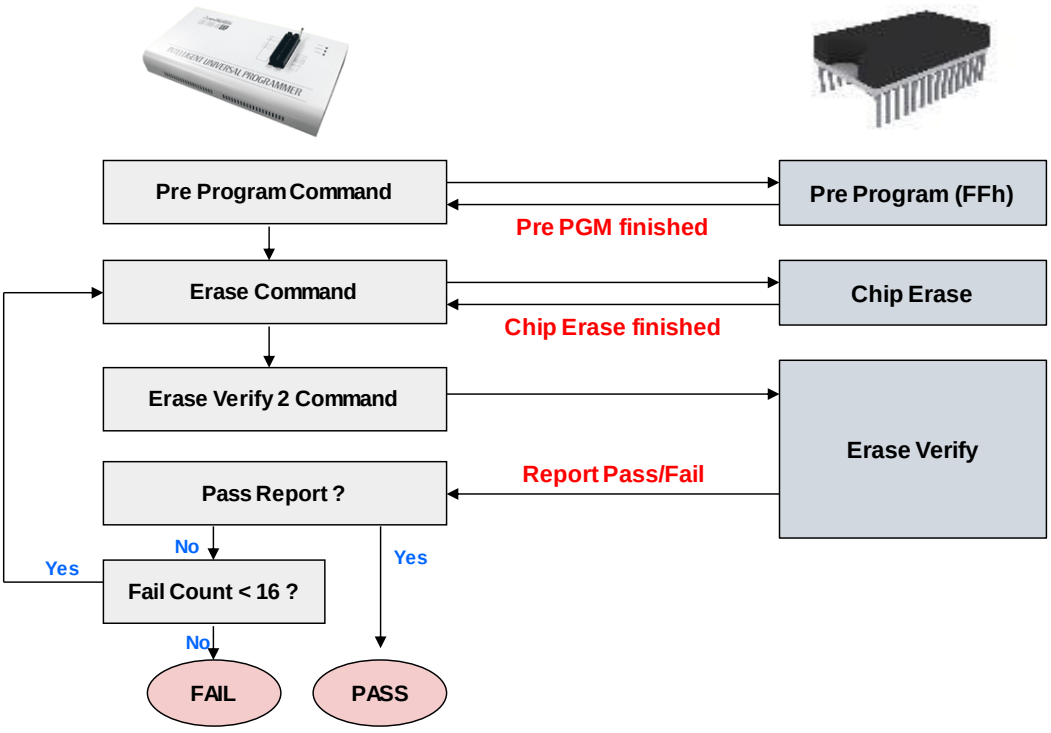
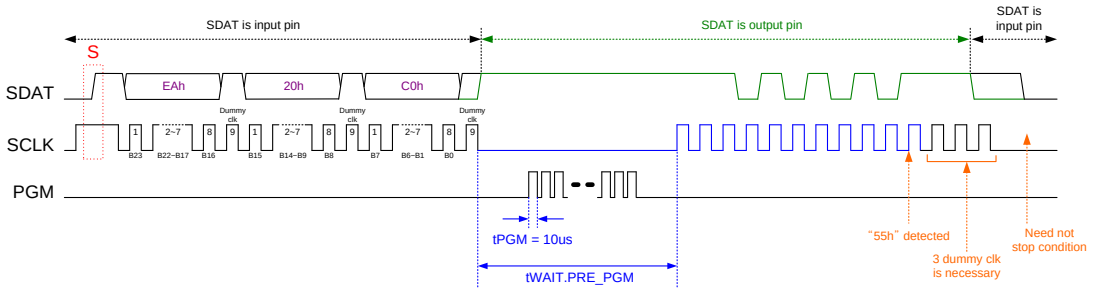


Figure 4.9 Erase Sequence

	1st Byte			2nd Byte	3rd Byte	Wait	Comment	
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Wait		
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	Wait		
Pre-Program	111	0101	0	20h	C0h	--	-	**Pre Program**

Table 4.12 Pre-Program Command

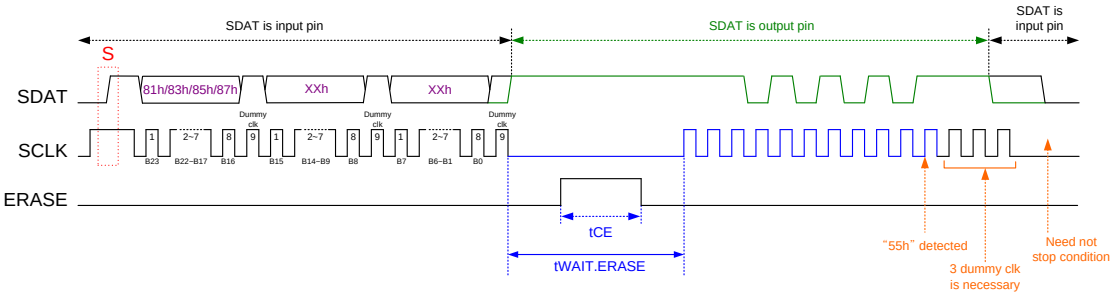


- **tWAIT.PRE_PGM = (Nbytes+64) x 27us + 50us**
- **In case of 4K Bytes ROM : tWAIT.PRE_PGM = (4096+64)x27us + 50us = 112,370us**

Figure 4.10 Pre-Program Timing Diagram

	1st Byte			2nd Byte	3rd Byte	Wait	Comment
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Wait	
Bit n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	Wait	
Erase	100	--yy	1	XXh	XXh	--	yy : Erase Time Control

Table 4.13 Chip Erase Command

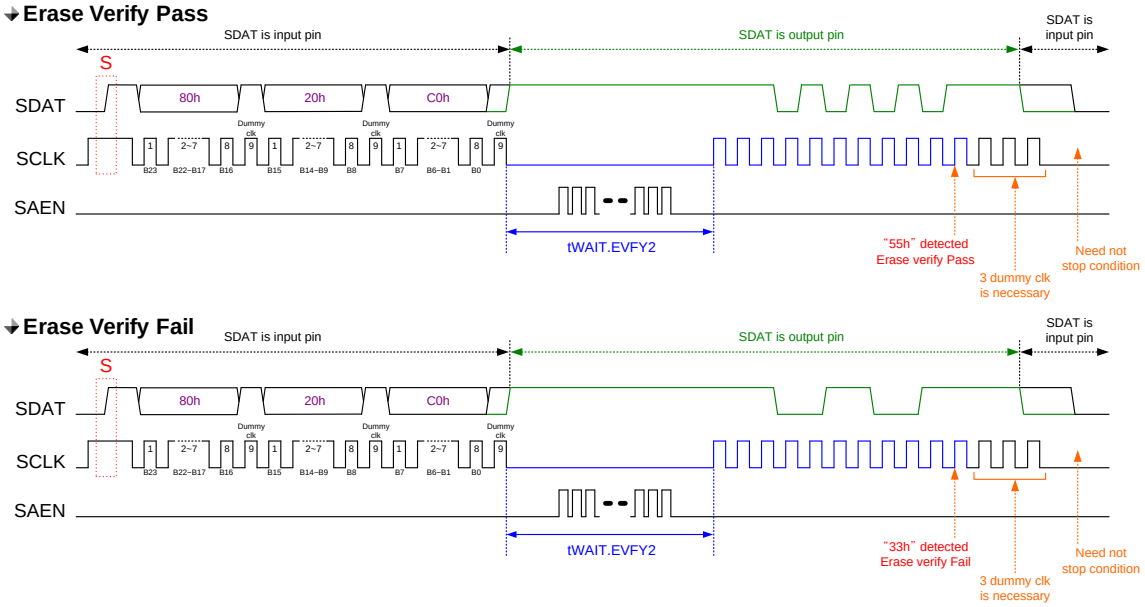


Byte1	Erase Time (tCE)	tWAIT.ERASE
81h	1 ms	1.5 ms
83h	2 ms	3 ms
85h	4 ms	6 ms
87h	8 ms	12 ms

Figure 4.11 Chip Erase Timing Diagram

	1st Byte			2nd Byte	3rd Byte	Wait	Comment
Mode	Code	Addr 2	Code	Addr 1	Addr 0	Wait	
Bit-n	B[23:21]	B[20:17]	B[16]	B[15:8]	B[7:0]	Wait	
Erase VFY	100	0000	0	20h	C0h	XX	VPP disabled, internal RC clock synced

Table 4.14 Erase Verify Command



- **tWAIT.EVFY2 = (Nbytes+64) x 1.7us + 50us**
- **In case of 4K Bytes ROM : tWAIT.EVFY2 = (4096+64)x1.7us + 50us = 7,098.2us**

Figure 4.12 Erase Verify Timing Diagram

4.9 AC Timing

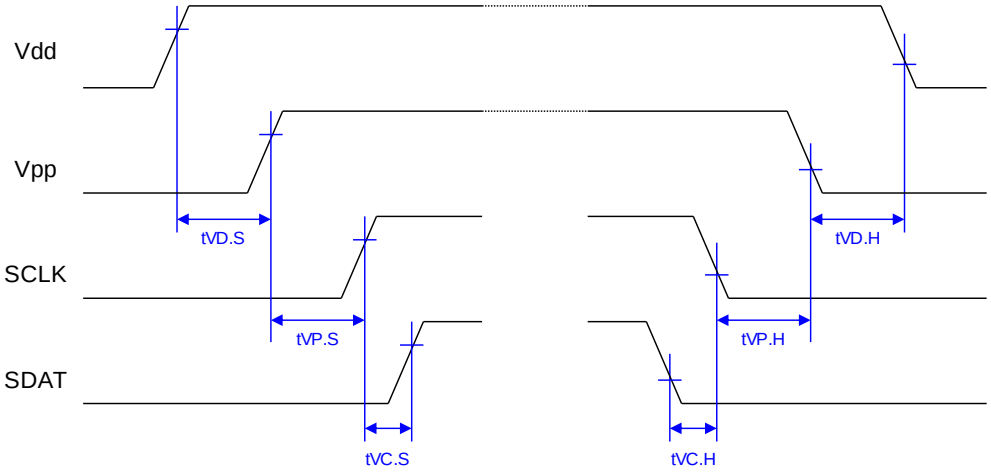


Figure 4.13 Power Sequence

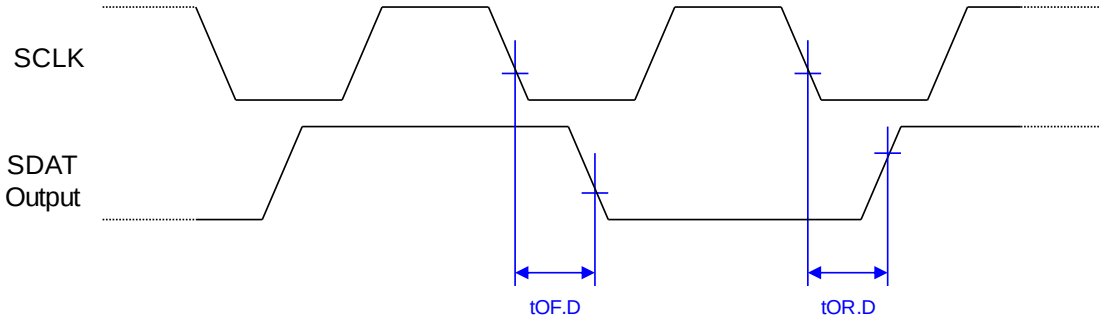


Figure 4.14 Serial Data / Clock Skew

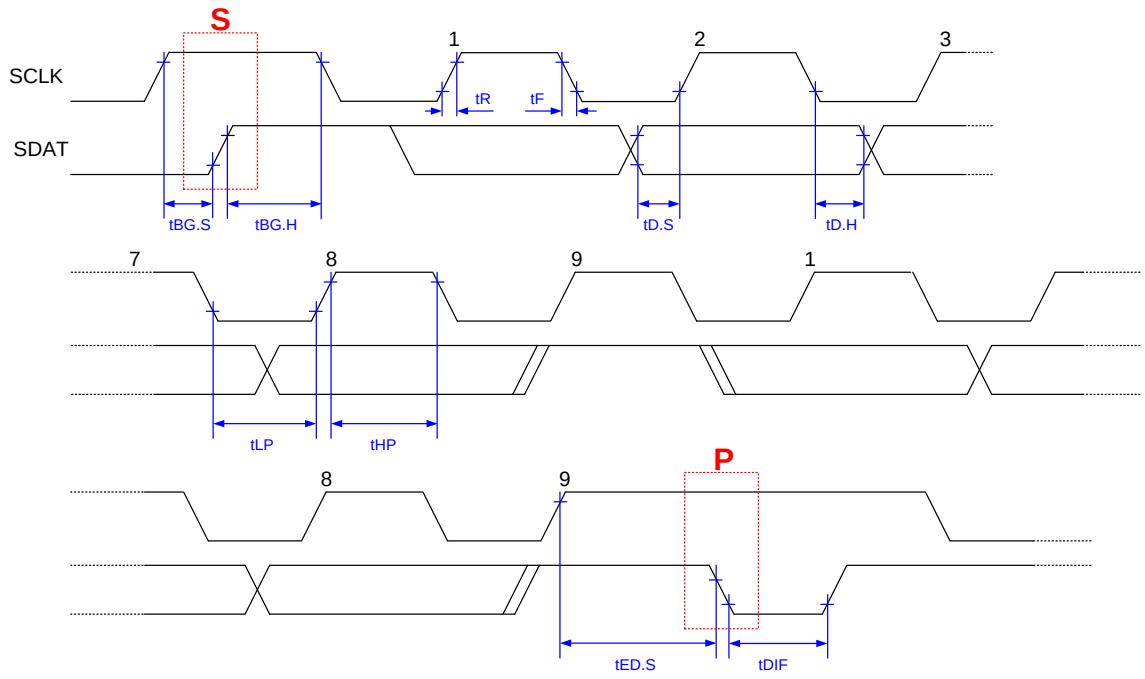


Figure 4.15 Whole Frame of Serial Data/ Clock Sequence

Symbol	Parameter	Min	Typ	Max	Unit	Comment
VDD	Logic power supply	-	5	-	V	
VPP	Power supply pin for programmable cell writing	-	9	-	V	
tVD.S	Vdd setup time	50	-	-	ms	
tVD.H	Vdd hold time	10	-	-	ms	
tVP.S/tVP.H	Vpp setup and hold time	10	-	-	ms	
tVC.S/tVC.H	SCLK setup and hold time	1	-	-	us	
tOR.D	Data out rising delay time	-	-	200	ns	
tOF.D	Data out falling delay time	-	-	200	ns	
fSCLK.PGM	SCLK clock frequency in program mode	-	-	125	KHz	tPGM = 20us

Symbol	Parameter	Min	Typ	Max	Unit	Comment
		-	-	62.5	KHz	tPGM = 40us
fSCLK.RD	SCLK clock frequency in read mode	-	-	2	MHz	
tBG.S/tBG.H	Begin setup and hold time	1	-	-	us	
tED.S	End setup and hold time	1	-	-	us	
tDIF	Time interval for new transition start	1	-	-	us	
tHP.PGM/tLP.PGM	High and low period of SCLK in program mode	3	-	-	us	tPGM = 20us
		6	-	-	us	tPGM = 40us
tHP.RD/tLP.RD	High and low period of SCLK in read mode	0.2	-	-	us	
tR/tF	Rising and falling time of SCLK and SDAT	-	-	20	ns	
tD.S/tD.H	Data setup and holdtime	150	-	-	ns	

5. EMULATOR EVA. BOARD SETTING

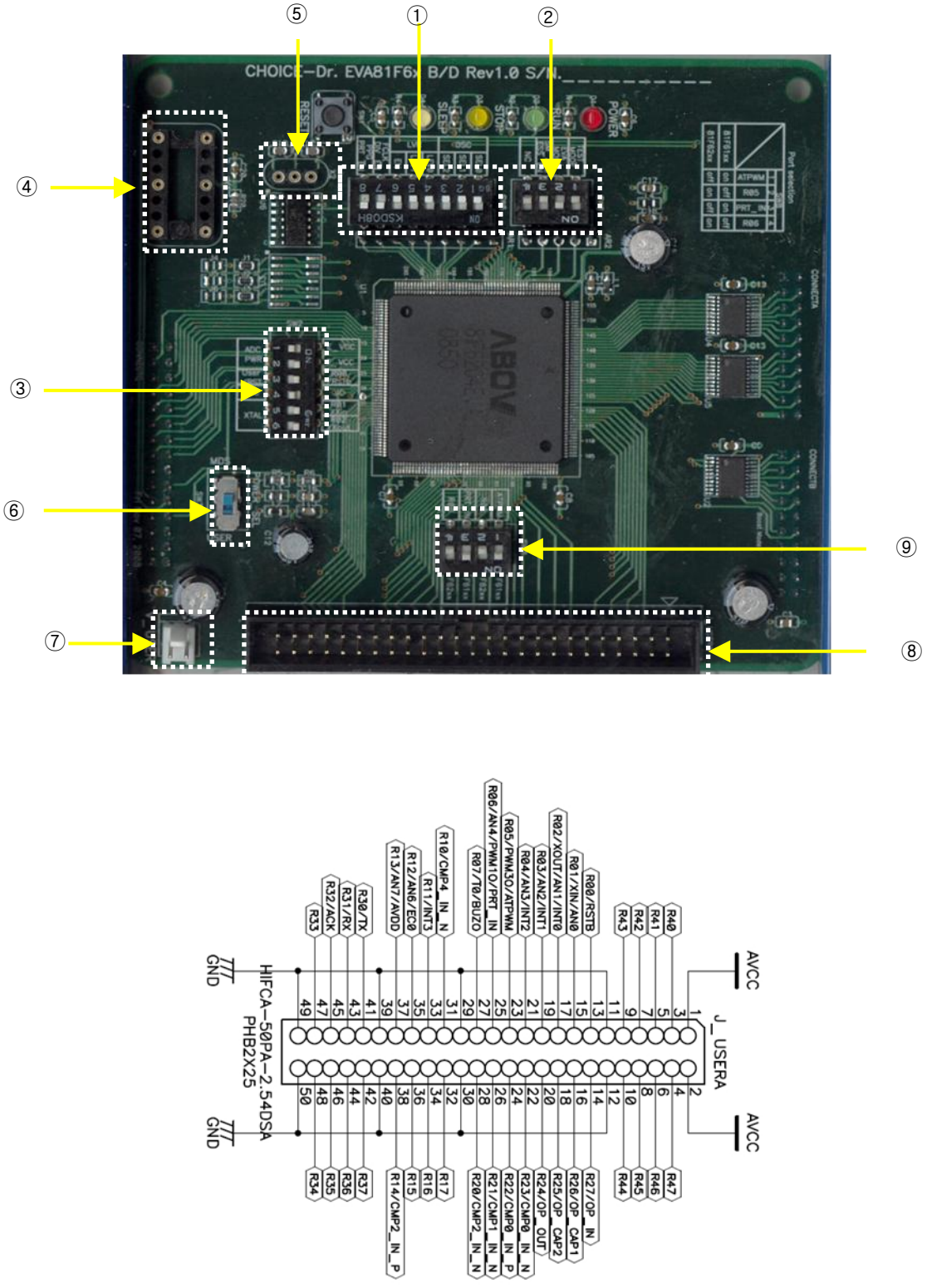


Figure 5.1 EVA. Board Dip Switch

5.1 DIP Switch Description

DIP S/W	Name	Description
① SW5	SW5.1 - OSC_SEL0 SW5.2 - OSC_SEL1 SW5.3 - OSC_SEL2	Rom Option bit 0~2 : OSC Selection bits (On : 1, Off : 0) 000: External RC – XOUT pin can be used as normal I/O 001: Internal RC; 4MHz – XOUT pin can be used as normal I/O 010: Internal RC; 2MHz – XOUT pin can be used as normal I/O 011: Internal RC; 1MHz – XOUT pin can be used as normal I/O 100: Internal RC; 8MHz – XOUT pin can be used as normal I/O 101: Not available 110: Not available 111: Crystal/ceramic oscillator
	SW5.4 – LVRS.0 SW5.5 – LVRS.1	Rom Option bit 5~6 : Low Voltage Reset Level Selection bit (On: 1, Off : 0) 00: 2.4V 10: 3.0V 01: 2.7V 11: 4.0V
	SW5.6 – LVREN	Rom Option bit 7 : Low Voltage Reset Enable bit On : (1) Disable (RESETB) Off : (0) Enable (R35)
	SW5.7 – FCLK_DIV_EN	FCLK 1/2 Selection On : (1) System Clock(SCLK) is FCLK/2 Off : (0) System Clock(SCLK) is FCLK.(Default)
	SW5.8 - PPG	PPG_PRT PAD Enable On : (1) ATPWM and PRT_IN Enabled Off : (0) Disable(Using R06/R05)
② SW6	SW6.1	TEST Mode (It is used at test mode at fabrication.) On : (1) Prohibited Off : (0) User Mode(Must be 0 at MDS).
	SW6.2	EVA Mode(It is used using MDS) On : (1) EVA Mode (Must be 1 at MDS). Off : (0) Normal MCU Mode
	SW6.3	SM ACCESS Enable Mode On : (1) Enable Smart Option Aceess Off : (0) Disable Smart Option Aceess(Must be 0 at MDS).
	SW6.4	No Connection
③ SW2	SW2.1 SW2.2	ADC Power Selection 01 : EVA_VCC Enable 10: Target_VCC Enable
	SW2.3	User RESET Selection 0 : RESETB(Low Active) input for EVA interface

DIP S/W	Name	Description
		1 : R00/RESETB Port Selection
	SW2.4	No Connection
	SW2.5 SW2.6	X-TAL Selection On : R01/XIN port Selection Off : X-TAL(X2) of EVA board Selection
④	X2	A Oscillator socket
⑤	X1	A Crystal/Resonator socket
⑥	SW3 – EVA PWR SEL	Eva.Board power source selection switch  Use MDS Power Use User's Power User's power source is supplied from the connector V_USER(⑦) which is described below.
⑦	V_USER	A connector for power source which can be used for Eva.Board.
⑧	J_USERA	A connecter for target system.
⑨	SW8.1	ATPWM Selection(MC81F6104) On : ATPWM port Enable Off : ATPWM port Disable
	SW8.2	R05 Selection(MC81F6204) On : R05 port Enable Off : R05 port Disable
	SW8.3	PRT_IN Selection(MC81F6104) On : PRT_IN port Enable Off : PRT_IN port Disable
	SW8.4	R06 Selection(MC81F6204) On : R06 port Enable Off : R06 port Disable

Note :
Only GND is connected between Eva.Board and the target system. VDD is not connected. So, the target system is required it's own power source.

6. IN SYSTEM PROGRAMMING

6.1 Getting Started / ISP Installation

The In-System Programming (ISP) is performed without removing the microcontroller from the system. The In-System Programming(ISP) facility consists of a series of internal hardware resources coupled with internal firmware through the serial port.

The In-System Programming (ISP) facility has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area.

The following section details the procedure for accomplishing the installation procedure.

1. Power off the target system.

Configure the target system as ISP mode.
(See ‘0

2. Hardware Conditions to Enter the ISP Mode' page 132)
3. Attach a USB-SIO-ISP B/D into the target system.
4. Run the ABOV USB-SIO-ISP software.
   - Down load the ISP S/W from http://*www.abov.co.kr*.
   - Unzip the download file and run USB-SIO-ISP.exe
5. Select a device in the USB-SIO-ISP S/W.
6. Power on the target system.
7. Execute ISP command such as read, program, auto... by pressing buttons on the USB-SIO-ISP S/W.

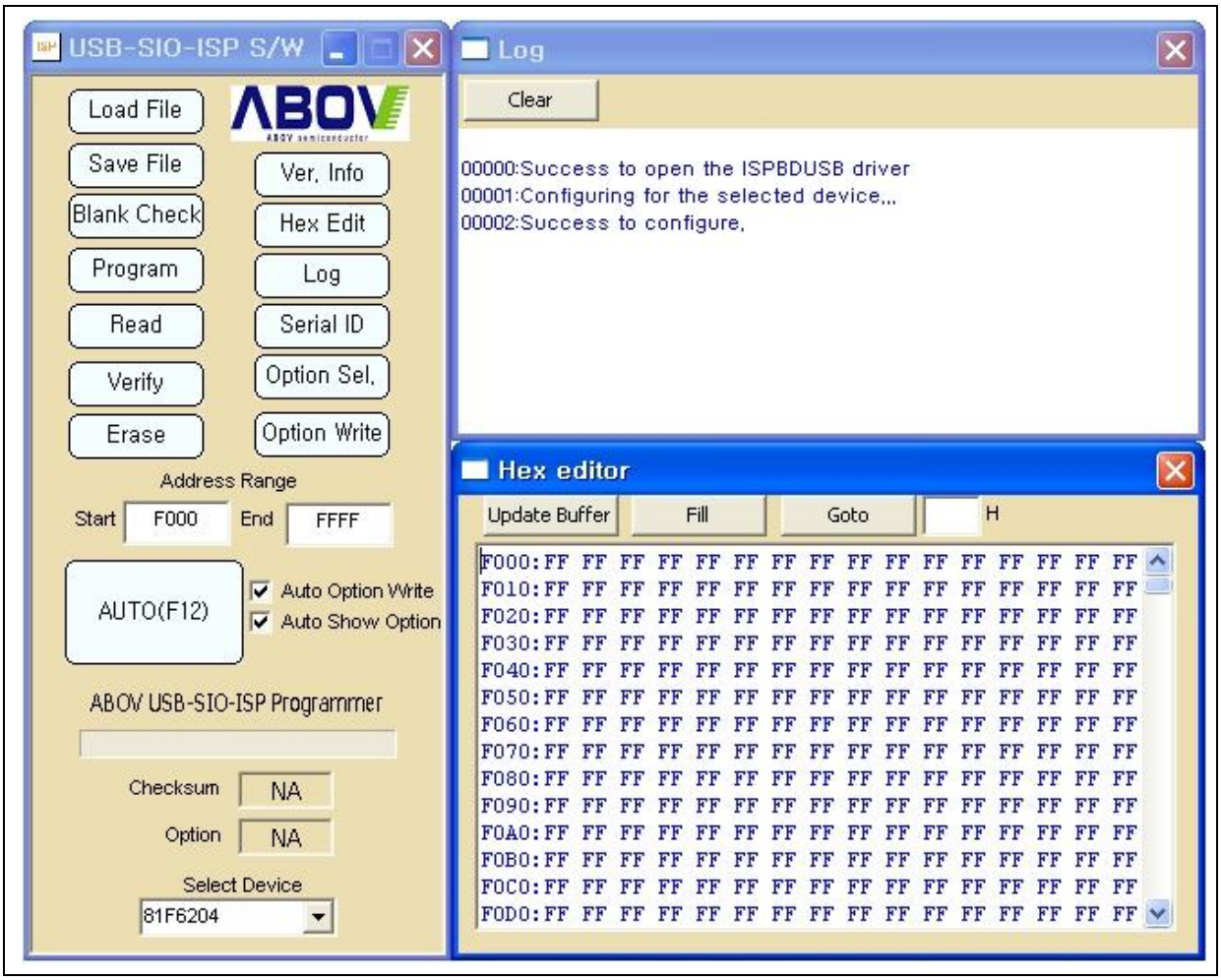


Figure 6.1 ISP Software

6.2 Basic ISP S/W Information

The **오류! 참조 원본을 찾을 수 없습니다.** is the ISP software based on MS-Windows. This software is only supporting devices with SIO.

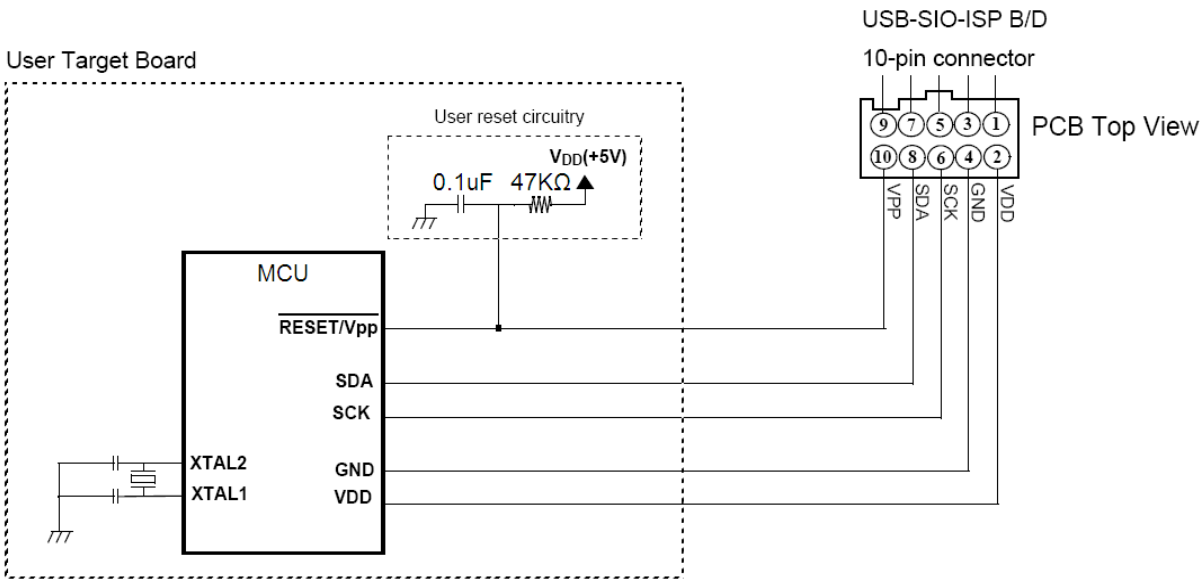
Function	Description
Load HEX File	Load the data from the selected file storage into the memory buffer.

Save HEX File	Save the current data in your memory buffer to a disk storage by using the Intel Motorola HEX format.
Blank Check	Verify whether or not a device is in an erased or unprogrammed state. Program This button enables you to place new data from the memory buffer into the target device.
Read	Read the data in the target MCU into the buffer for examination. The checksum will be displayed on the checksum box.
Verify	Assures that data in the device matches data in the memory buffer. If your device is secured, a verification error is detected.
Erase	Erase the data in your target MCU before programming it.
Option Selection	Set the configuration data of target MCU. The security locking is set with this button.
Option Write	Progam the configuration data of target MCU. The security locking is performed with this button.
AUTO	Following sequence is performed ; 1.Erase 2.Program 3.Verify 4.Option Write
Edit	Buffer Modify the data in the selected address in your buffer memory
Fill	Buffer Fill the selected area with a data.
Goto	Display the selected page.
Start _____	Starting address
End _____	End address
Checksum	Display the checksum(Hexdecimal) after reading the target device.
Select	Device Select target device.

Note:
MCU Configuration value is erased after erase operation. It must be configured to match with user target board. Otherwise, it is failed to enter ISP mode, or its operation is not desirable.

6.3 Hardware Conditions to Enter the ISP Mode

The boot loader can be executed by holding ALEB high, RST/ V_{PP} as +9V.



1. If other signals affect SIO communication in ISP mode, disconnect these pins by using a jumper or a switch.
2. If ALEB is sharing with other function. Toggle the port between ISP and user mode.

Figure 6.2 Hardware Conditions to Enter the ISP Mode

6.4 Sequence to enter ISP mode/user mode

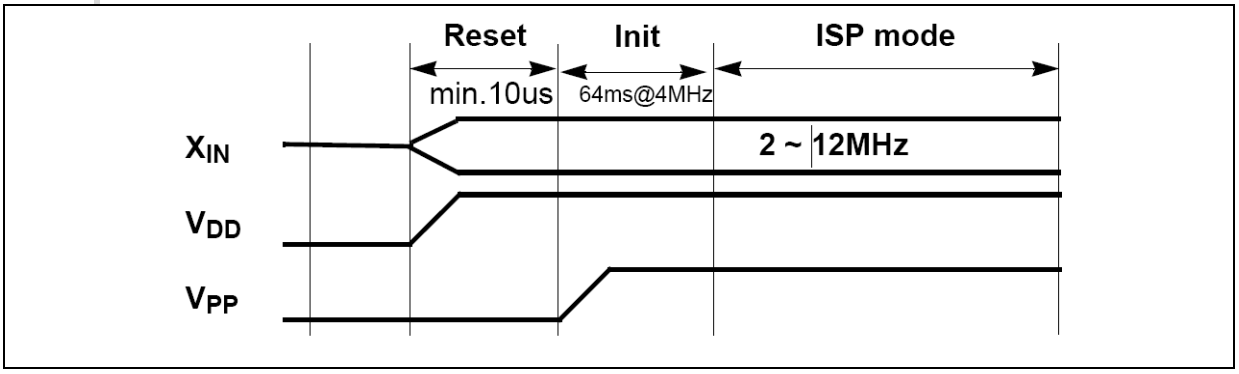


Figure 6.3 Timing diagram to enter the ISP mode

Note: Vpp is needed to rise within 64ms@4MHz after Vdd rising time(at lease 10us@4MHz after Vdd rising time).

Sequence to enter ISP mode from user mode.

1. Power off the target system.
2. Configure the target system as ISP mode.
3. Attach a ISP B/D into the target system.
4. Run the ISP S/W
5. Select the target device.
6. Power on the target system.

Sequence to enter user mode from ISP mode.

1. Close the ISP S/W.
2. Power off the target system.
3. Configure the target system as user mode
4. Detach a ISP B/D from the target system.
5. Power on.

6.5 USB-SIO-ISP Board

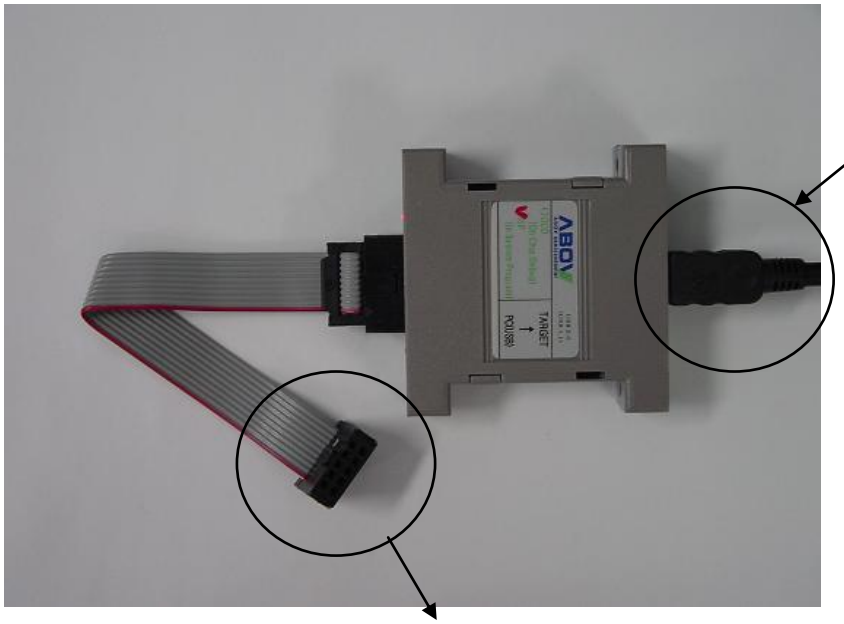
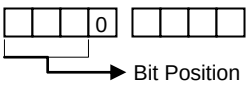
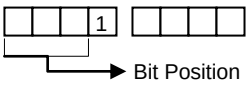


Figure 6.4 USB-SIO-ISP Board

7. INSTRUCTION SET

7.1 Terminology List

A	Accumulator
X	X - register
Y	Y - register
PSW	Program Status Word
#imm	8-bit Immediate data
dp	Direct Page Offset Address
!abs	Absolute Address
[ ]	Indirect expression
{ }	Register Indirect expression
{ }+	Register Indirect expression, after that, Register auto-increment
.bit	Bit Position
A.bit	Bit Position of Accumulator
dp.bit	Bit Position of Direct Page Memory
M.bit	Bit Position of Memory Data (000_H~$0FFF_H$)
rel	Relative Addressing Data
upage	U-page ($0FF00_H$~$0FFFF_H$) Offset Address
n	Table CALL Number (0~15)
+	Addition
x	Upper Nibble Expression in Opcode when it is even number (bit7~bit5, bit4=0) 
y	Upper Nibble Expression in Opcode when it is odd number (bit7~bit5, bit4=1) 
–	Subtraction
×	Multiplication
/	Division
( )	Contents Expression
∧	AND
∨	OR

⊕	Exclusive OR
~	NOT
←	Assignment / Transfer / Shift Left
→	Shift Right
↔	Exchange
=	Equal
≠	Not Equal

7.2 Instruction Map

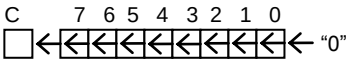
LOW / HIGH	00000 00	00001 01	00010 02	00011 03	00100 04	00101 05	00110 06	00111 07	01000 08	01001 09	01010 0A	01011 0B	01100 0C	01101 0D	01110 0E	01111 0F
000	-	SET1 dp.bit	BBS A.bit,rel	BBS dp.bit,rel	ADC #imm	ADC dp	ADC dp+X	ADC !abs	ASL A	ASL dp	TCALL 0	SETA1 .bit	BIT dp	POP A	PUSH A	BRK
001	CLRC	〃	〃	〃	SBC #imm	SBC dp	SBC dp+X	SBC !abs	ROL A	ROL dp	TCALL 2	CLRA1 .bit	COM dp	POP X	PUSH X	BRA rel
010	CLRG	〃	〃	〃	CMP #imm	CMP dp	CMP dp+X	CMP !abs	LSR A	LSR dp	TCALL 4	NOT1 M.bit	TST dp	POP Y	PUSH Y	PCALL Upage
011	DI	〃	〃	〃	OR #imm	OR dp	OR dp+X	OR !abs	ROR A	ROR dp	TCALL 6	OR1 OR1B	CMPX dp	POP PSW	PUSH PSW	RET
100	CLRV	〃	〃	〃	AND #imm	AND dp	AND dp+X	AND !abs	INC A	INC dp	TCALL 8	AND1 AND1B	CMPY dp	CBNE dp+X	TXSP	INC X
101	SETC	〃	〃	〃	EOR #imm	EOR dp	EOR dp+X	EOR !abs	DEC A	DEC dp	TCALL 10	EOR1 EOR1B	DBNE dp	XMA dp+X	TSPX	DEC X
110	SETG	〃	〃	〃	LDA #imm	LDA dp	LDA dp+X	LDA !abs	TXA	LDY dp	TCALL 12	LDC LDCB	LDX dp	LDX dp+Y	XCN	DAS (N/A)
111	EI	〃	〃	〃	LDM dp,#imm	STA dp	STA dp+X	STA !abs	TAX	STY dp	TCALL 14	STC M.bit	STX dp	STX dp+Y	XAX	STOP

LOW / HIGH	10000 10	10001 11	10010 12	10011 13	10100 14	10101 15	10110 16	10111 17	11000 18	11001 19	11010 1A	11011 1B	11100 1C	11101 1D	11110 1E	11111 1F
000	BPL rel	CLR1 dp.bit	BBC A.bit,rel	BBC dp.bit,rel	ADC {X}	ADC !abs+Y	ADC [dp+X]	ADC [dp]+Y	ASL !abs	ASL dp+X	TCALL 1	JMP !abs	BIT !abs	ADDW dp	LDX #imm	JMP [!abs]
001	BVC rel	〃	〃	〃	SBC {X}	SBC !abs+Y	SBC [dp+X]	SBC [dp]+Y	ROL !abs	ROL dp+X	TCALL 3	CALL !abs	TEST !abs	SUBW dp	LDY #imm	JMP [dp]
010	BCC rel	〃	〃	〃	CMP {X}	CMP !abs+Y	CMP [dp+X]	CMP [dp]+Y	LSR !abs	LSR dp+X	TCALL 5	MUL	TCLR1 !abs	CMPW dp	CMPX #imm	CALL [dp]
011	BNE rel	〃	〃	〃	OR {X}	OR !abs+Y	OR [dp+X]	OR [dp]+Y	ROR !abs	ROR dp+X	TCALL 7	DBNE Y	CMPX !abs	LDYA dp	CMPY #imm	RETI
100	BMI rel	〃	〃	〃	AND {X}	AND !abs+Y	AND [dp+X]	AND [dp]+Y	INC !abs	INC dp+X	TCALL 9	DIV	CMPY !abs	INCW dp	INC Y	TAY
101	BVS rel	〃	〃	〃	EOR {X}	EOR !abs+Y	EOR [dp+X]	EOR [dp]+Y	DEC !abs	DEC dp+X	TCALL 11	XMA {X}	XMA dp	DECW dp	DEC Y	TYA
110	BCS rel	〃	〃	〃	LDA {X}	LDA !abs+Y	LDA [dp+X]	LDA [dp]+Y	LDY !abs	LDY dp+X	TCALL 13	LDA {X}+	LDX !abs	STYA dp	XAY	DAA (N/A)
111	BEQ rel	〃	〃	〃	STA {X}	STA !abs+Y	STA [dp+X]	STA [dp]+Y	STY !abs	STY dp+X	TCALL 15	STA {X}+	STX !abs	CBNE dp	XYX	NOP

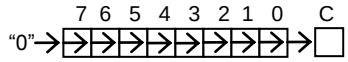
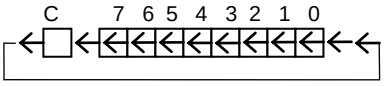
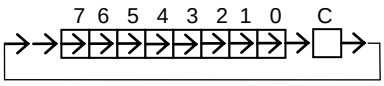
7.3 Instruction Set

7.3.1 Arithmetic / Logic

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	ADC #imm	04	2	2	Add with carry. A ← (A) + (M) + C	N V - - H - Z C
2	ADC dp	05	2	3		
3	ADC dp + X	06	2	4		
4	ADC !abs	07	3	4		
5	ADC !abs + Y	15	3	5		
6	ADC [dp + X]	16	2	6		
7	ADC [dp] + Y	17	2	6		
8	ADC { X }	14	1	3		
9	AND #imm	84	2	2	Logical AND A ← (A) ∧ (M)	N - - - - - Z -
10	AND dp	85	2	3		
11	AND dp + X	86	2	4		
12	AND !abs	87	3	4		
13	AND !abs + Y	95	3	5		
14	AND [dp + X]	96	2	6		
15	AND [dp] + Y	97	2	6		
16	AND { X }	94	1	3		
17	ASL A	08	1	2	Arithmetic shift left 	N - - - - - Z C
18	ASL dp	09	2	4		
19	ASL dp + X	19	2	5		
20	ASL !abs	18	3	5		
21	CMP #imm	44	2	2	Compare accumulator contents with memory contents (A) - (M)	N - - - - - Z C
22	CMP dp	45	2	3		
23	CMP dp + X	46	2	4		
24	CMP !abs	47	3	4		
25	CMP !abs + Y	55	3	5		
26	CMP [dp + X]	56	2	6		
27	CMP [dp] + Y	57	2	6		
28	CMP { X }	54	1	3		

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
29	CMPX #imm	5E	2	2	Compare X contents with memory contents (X) - (M)	N - - - - - Z C
30	CMPX dp	6C	2	3		
31	CMPX !abs	7C	3	4		
32	CMPY #imm	7E	2	2	Compare Y contents with memory contents (Y) - (M)	N - - - - - Z C
33	CMPY dp	8C	2	3		
34	CMPY !abs	9C	3	4		
35	COM dp	2C	2	4	1's Complement : (dp) ← ~(dp)	N - - - - - Z -
36	DAA	-	-	-	Unsupported	-
37	DAS	-	-	-	Unsupported	-
38	DEC A	A8	1	2	Decrement M ← (M) - 1	N - - - - - Z -
39	DEC dp	A9	2	4		
40	DEC dp + X	B9	2	5		
41	DEC !abs	B8	3	5		
42	DEC X	AF	1	2		
43	DEC Y	BE	1	2		
44	DIV	9B	1	12	Divide : YA/X Q:A, R:Y	N V - - H - Z -
45	EOR #imm	A4	2	2	Exclusive OR A ← (A) ⊕ (M)	N - - - - - Z -
46	EOR dp	A5	2	3		
47	EOR dp + X	A6	2	4		
48	EOR !abs	A7	3	4		
49	EOR !abs + Y	B5	3	5		
50	EOR [dp + X]	B6	2	6		
51	EOR [dp] + Y	B7	2	6		
52	EOR { X }	B4	1	3		
53	INC A	88	1	2	Increment M ← (M) + 1	N - - - - - Z -
54	INC dp	89	2	4		
55	INC dp + X	99	2	5		
56	INC !abs	98	3	5		

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
57	INC X	8F	1	2		
58	INC Y	9E	1	2		
59	LSR A	48	1	2	Arithmetic shift left 	N - - - - - Z C
60	LSR dp	49	2	4		
61	LSR dp + X	59	2	5		
62	LSR !abs	58	3	5		
63	MUL	5B	1	9	Multiply : YA ← Y × A	N - - - - - Z -
64	OR #imm	64	2	2	Logical OR A ← (A) ∨ (M)	N - - - - - Z -
65	OR dp	65	2	3		
66	OR dp + X	66	2	4		
67	OR !abs	67	3	4		
68	OR !abs + Y	75	3	5		
69	OR [dp + X]	76	2	6		
70	OR [dp] + Y	77	2	6		
71	OR { X }	74	1	3		
72	ROL A	28	1	2	Rotate left through carry 	N - - - - - Z C
73	ROL dp	29	2	4		
74	ROL dp + X	39	2	5		
75	ROL !abs	38	3	5		
76	ROR A	68	1	2	Rotate right through carry 	N - - - - - Z C
77	ROR dp	69	2	4		
78	ROR dp + X	79	2	5		
79	ROR !abs	78	3	5		
80	SBC #imm	24	2	2	Subtract with carry A ← (A) - (M) - ~(C)	N V - - H Z C
81	SBC dp	25	2	3		
82	SBC dp + X	26	2	4		
83	SBC !abs	27	3	4		
84	SBC !abs + Y	35	3	5		

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
85	SBC [dp + X]	36	2	6		
86	SBC [dp] + Y	37	2	6		
87	SBC { X }	34	1	3		
88	TST dlp	4C	2	3	Test memory contents for negative or zero (dp) – 00_H	N - - - - - Z -
89	XCN	CE	1	5	Exchange nibbles within the accumulator A_7~A_4 ↔ A_3~A_0	N - - - - - Z -

7.3.2 Register / Memory Operation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	LDA #imm	C4	2	2	Load accumulator A ← (M)	N - - - - - Z -
2	LDA dp	C5	2	3		
3	LDA dp + X	C6	2	4		
4	LDA !abs	C7	3	4		
5	LDA !abs + Y	D5	3	5		
6	LDA [dp + X]	D6	2	6		
7	LDA [dp] + Y	D7	2	6		
8	LDA { X }	D4	1	3		
9	LDA { X }+	DB	1	4	X-register auto-increment : A ← (M), X ← X + 1	
10	LDM dp, #imm	E4	3	5	Load memory with immediate data : (M) ← imm	- - - - - - - -
11	LDX #imm	1E	2	2	Load X-register X ← (M)	N - - - - - Z -
12	LDX dp	CC	2	3		
13	LDX dp + Y	CD	2	4		
14	LDX !abs	DC	3	4		
15	LDY #imm	3E	2	2	Load Y-register Y ← (M)	N - - - - - Z -
16	LDY dp	C9	2	3		
17	LDY dp + Y	D9	2	4		
18	LDY !abs	D8	3	4		
19	STA dp	E5	2	4	Store accumulator contents in memory (M) ← A	- - - - - - - -
20	STA dp + X	E6	2	5		
21	STA !abs	E7	3	5		
22	STA !abs + Y	F5	3	6		
23	STA [dp + X]	F6	2	7		
24	STA [dp] + Y	F7	2	7		
25	STA { X }	F4	1	4		
26	STA { X }+	FB	1	4	X-register auto-increment : (M) ← A, X ← X + 1	

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
27	STX dp	EC	2	4	Store X-register contents in memory (M) ← X	- - - - - - - -
28	STX dp + Y	ED	2	5		
29	STX !abs	FC	3	5		
30	STY dp	E9	2	4	Store Y-register contents in memory (M) ← Y	- - - - - - - -
31	STY dp + X	F9	2	5		
32	STY !abs	F8	3	5		
33	TAX	E8	1	2	Transfer accumulator contents to X-register : X ← A	N - - - - - Z -
34	TAY	9F	1	2	Transfer accumulator contents to Y-register : Y ← A	N - - - - - Z -
35	TSPX	AE	1	2	Transfer stack-pointer contents to X-register : X ← sp	N - - - - - Z -
36	TXA	C8	1	2	Transfer X-register contents to accumulator : A ← X	N - - - - - Z -
37	TXSP	8E	1	2	Transfer X-register contents to stack-pointer : sp ← X	N - - - - - Z -
38	TYA	BF	1	2	Transfer Y-register contents to accumulator : A ← Y	N - - - - - Z -
39	XAX	EE	1	4	Exchange X-register contents with accumulator : X ↔ A	- - - - - - - -
40	XAY	DE	1	4	Exchange Y-register contents with accumulator : Y ↔ A	- - - - - - - -
41	XMA dp	BC	2	5	Exchange memory contents with accumulator : (M) ↔ A	N - - - - - Z -
42	XMA dp + X	AD	2	6		
43	XMA {X}	BB	1	5		
44	XYX	FE	1	4	Exchange X-register contents with Y-register : X ↔ Y	- - - - - - - -

7.3.3 16 BIT Manipulation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	ADDW dp	1D	2	5	16-bits add without carry YA ← (YA) + (dp + 1) (dp)	N V - - H - Z C
2	CMPW dp	5D	2	4	Compare YA contents with memory pair contents : (YA) - (dp + 1) (dp)	N - - - - - Z C
3	DECW dp	BD	2	6	Decrement memory pair (dp + 1) (dp) ← (dp + 1) (dp) – 1	N - - - - - Z -
4	INCW dp	9D	2	6	Increment memory pair (dp + 1) (dp) ← (dp + 1) (dp) + 1	N - - - - - Z -
5	LDYA dp	7D	2	5	Load YA YA ← (dp + 1) (dp)	N - - - - - Z -
6	STYA dp	DD	2	5	Store YA (dp + 1) (dp) ← YA	- - - - - - - -
7	SUBW dp	3D	2	5	16-bits subtract without carry YA ← (YA) - (dp + 1) (dp)	N V - - H - Z C

7.3.4 BIT Manipulation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	AND1 M.bit	8B	3	4	Bit AND C-flag : C ← (C) ∧ (M.bit)	- - - - - - - C
2	AND1B M.bit	8B	3	4	Bit AND C-flag and NOT : C ← (C) ∧ ~(M.bit)	- - - - - - - C
3	BIT dp	0C	2	4	Bit test A with memory : Z ← (A) ∧ (M), N ← (M_7), V ← (M_6)	M M - - - - Z -
4	BIT !abs	1C	3	5		
5	CLR1 dp.bit	y1	2	4	Clear bit : (M.bit) ← “0”	- - - - - - - -
6	CLRA1 A.bit	2B	2	2	Clear A bit : (A.bit) ← “0”	- - - - - - - -
7	CLRC	20	1	2	Clear C-flag : C ← “0”	- - - - - - - 0
8	CLRG	40	1	2	Clear G-flag : G ← “0”	- - 0 - - - - -
9	CLRV	80	1	2	Clear V-flag : V ← “0”	- 0 - - 0 - - -
10	EOR1 M.bit	AB	3	5	Bit exclusive-OR C-flag : C ← (C) ⊕ (M.bit)	- - - - - - - C
11	EOR1B M.bit	AB	3	5	Bit exclusive-OR C-flag and NOT : C ← (C) ⊕ ~(M.bit)	- - - - - - - C
12	LDC M.bit	CB	3	4	Load C-flag : C ← (M.bit)	- - - - - - - C
13	LDCB M.bit	CB	3	4	Load C-flag with NOT : C ← ~(M.bit)	- - - - - - - C
14	NOT1 M.bit	4B	3	5	Bit complement : (M.bit) ← ~(M.bit)	- - - - - - - -

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
15	OR1 M.bit	6B	3	5	Bit OR C-flag : C ← C ∨ (M.bit)	- - - - - - - C
16	OR1B M.bit	6B	3	5	Bit OR C-flag and NOT : C ← C ∨ ~ (M.bit)	- - - - - - - C
17	SET1 dp.bit	x1	2	4	Set bit : (M.bit) ← “1”	- - - - - - - -
18	SETA1 A.bit	0B	2	2	Set A bit : (A.bit) ← “1”	- - - - - - - -
19	SETC	A0	1	2	Set C-flag : C ← “1”	- - - - - - - 1
20	SETG	C0	1	2	Set G-flag : G ← “1”	- - 1 - - - - -
21	STC M.bit	EB	3	6	Store C-flag : (M.bit) ← C	- - - - - - - -
22	TCLR1 !abs	5C	3	6	Test and clear bits with A : A – (M), (M) ← (M) ∧ ~(A)	N - - - - - Z -
23	TSET1 !abs	3C	3	6	Test and set bits with A : A – (M), (M) ← (M) ∨ (A)	N - - - - - Z -

7.3.5 Branch / Jump

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	BBC A.bit, rel	y2	2	4/6	Branch if bit clear : If (bit) = 0, then pc ← (pc) + rel	- - - - - - - -
2	BBC dp.bit, rel	y3	3	5/7		
3	BBS A.bit, rel	x2	2	4/6	Branch if bit set : If (bit) = 1, then pc ← (pc) + rel	- - - - - - - -
4	BBS dp.bit, rel	x3	3	5/7		
5	BCC rel	50	2	2/4	Branch if carry bit clear : If (C) = 0, then pc ← (pc) + rel	- - - - - - - -
6	BCS rel	D0	2	2/4	Branch if carry bit set : If (C) = 1, then pc ← (pc) + rel	- - - - - - - -
7	BEQ rel	F0	2	2/4	Branch if equal : If (Z) = 1, then pc ← (pc) + rel	- - - - - - - -
8	BMI rel	90	2	2/4	Branch if minus : If (N) = 1, then pc ← (pc) + rel	- - - - - - - -
9	BNE rel	70	2	2/4	Branch if not equal : If (Z) = 0, then pc ← (pc) + rel	- - - - - - - -
10	BPL rel	10	2	2/4	Branch if plus : If (N) = 0, then pc ← (pc) + rel	- - - - - - - -
11	BRA rel	2F	2	4	Branch always : pc ← (pc) + rel	- - - - - - - -
12	BVC rel	30	2	2/4	Branch if overflow bit clear : If (V) = 0, then pc ← (pc) + rel	- - - - - - - -
13	BVS rel	B0	2	2/4	Branch if overflow bit set : If (V) = 1, then pc ← (pc) + rel	- - - - - - - -
14	CALL !abs	3B	3	8	Subroutine call M(sp) ← (pc_H), sp ← sp – 1, M(sp) ← (pc_L), sp ← sp – 1, If !abs, pc ← abs ; if [dp], pc_L ← (dp), pc_H ← (dp + 1)	- - - - - - - -
15	CALL [dp]	5F	2	8		
16	CBNE dp, rel	FD	3	5/7	Compare and branch if not equal : if (A) ≠ (M), then pc ← (pc) + rel	- - - - - - - -
17	CBNE dp+X, rel	8D	3	6/8		
18	DBNE dp, rel	AC	3	5/7	Decrement and branch if not equal : if (M) ≠ 0, then pc ← (pc) + rel	- - - - - - - -
19	DBNE Y, rel	7B	2	4/6		
20	JMP !abs	1B	3	3	Unconditional jump : pc ← jump address	- - - - - - - -
21	JMP [!abs]	1F	3	5		
22	JMP [dp]	3F	2	4		
23	PCALL upage	4F	2	6	U-page call M(sp) ← (pc_H), sp ← sp – 1,	- - - - - - - -

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
					M(sp) ← (pc_L), sp ← sp – 1, pc_L ← (upage), pc_H ← “$0FF_H$”	
24	TCALL n	nA	1	8	Table call M(sp) ← (pc_H), sp ← sp – 1, M(sp) ← (pc_L), sp ← sp – 1, pc_L ← (Table vector L), pc_H ← (Table vector H)	- - - - - - - -

7.3.6 Control Operation / Etc

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	BRK	0F	1	8	Software interrupt : B ← “1”, M(sp) ← (pc_H), sp ← sp – 1, M(sp) ← (pc_L), sp ← sp – 1, M(sp) ← (PSW), sp ← sp – 1, pc_L ← ($0FFDE_H$), pc_H ← ($0FFDF_H$)	- - - 1 - 0 - -
2	DI	60	1	3	Disable interrupt : I ← “0”	- - - - - 0 - -
3	EI	E0	1	3	Enable interrupt : I ← “1”	- - - - - 1 - -
4	NOP	FF	1	2	No operation	- - - - - - - -
5	POP A	0D	1	4	sp ← sp + 1, A ← M(sp) sp ← sp + 1, X ← M(sp) sp ← sp + 1, Y ← M(sp) sp ← sp + 1, PSW ← M(sp)	- - - - - - - -
6	POP X	2D	1	4		
7	POP Y	4D	1	4		
8	POP PSW	6D	1	4		restored
9	PUSH A	0E	1	4	M(sp) ← A, sp ← sp - 1 M(sp) ← X, sp ← sp - 1 M(sp) ← Y, sp ← sp - 1 M(sp) ← PSW, sp ← sp - 1	- - - - - - - -
10	PUSH X	2E	1	4		
11	PUSH Y	4E	1	4		
12	PUSH PSW	6E	1	4		
13	RET	6F	1	5	Return from subroutine sp ← sp + 1, pc_L ← M(sp), sp ← sp + 1, pc_H ← M(sp)	- - - - - - - -
14	RETI	7F	1	6	Return from interrupt sp ← sp + 1, PSW ← M(sp), sp ← sp + 1, pc_L ← M(sp), sp ← sp + 1, pc_H ← M(sp)	restored
15	STOP	EF	1	3	Stop mode (halt CPU, stop oscillator)	- - - - - - - -