ABOV SEMICONDUCTOR Co., Ltd.
LIGHT-TO-DIGITAL CONVERTER

MC8201

Data Sheet (REV.1.5)

REVISION HISTORY

REVISION 1.0 (October 7, 2011)

- Initial Version

REVISION 1.1 (October 11, 2011)

- Modify PS description

REVISION 1.2 (November 15, 2011)

- Fix registers description

REVISION 1.3 (December 15, 2011)

- Fix ps algorithm description
- Fix ps register description and bit width
- Fix electrical specifications

REVISION 1.4 (January 4, 2012)

- Fix DC spec (VIL, VIH)

REVISION 1.5 (March 18, 2012)

- Fix registers description
- Revise PS algorithm (PS resolution is changed to 10/8-bit)

REVISION 1.5
Published by Design Team

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MC8201

Digital Proximity and Ambient Light Sensor

1. OVERVIEW

1.1 DESCRIPTION

The MC8201 integrates ALS(Ambient Light Sensor), PS(Proximity Sensor) and IR LED(Light Emitting Diode) driver in a single die, and merged with IR LED in a extremely small 8 pin package. It is an advanced digital ambient light sensor and proximity sensor, which can transform illuminance (light intensity) to a digital signal output and detect proximity of object.

For ambient light sensing, it combines an opened photodiode and a light shielded photodiode which is used to reduce dark noise. The opened photodiode is capable of providing a photovoltaic response and coated with Infra Red cut off filter on a CMOS integrated circuit. The photovoltaic response is converted into digital counter value by the ALS ADC of 16 bit resolution. It closely approximates the human eye spectral response of visible wavelength.

In addition, the MC8201 has another opened photodiode with IR pass filter in order to detect proximity of an object. When PS is enabled, the IR LED is turned on by the built-in IR LED driver. When the IR from the LED reaches an object and gets reflected back, the opened photodiode for proximity sensing converts the reflected IR light with center frequency of 850nm into current. The amount of current is converted into digital counter value by the PS ADC of 12-bit resolution. The counter value is inversely proportional to the square of the distance between the sensor and the object. The proximity detection feature operates well from bright sunlight to dark rooms. The wide dynamic range also allows for operation in short distance detection behind dark glass such as a cell phone. The operation voltage ranges from 2.4 to 3.6 volt.

The ALS features are ideal for reducing power consumption and adjusting brightness of display equipments like LCD, PDP, LED, virtual keyboard and portable projector, etc. The proximity detection feature is targeted esspecially for cell phones with touch screen. In cell phones, the proximity sensor can detect when a user positions the phone close to their ear and can disable the touch screen to prevent mal-functions due to touch events.

1.2 FEATURES

- CMOS technology
- Independently programmable exposure time for PS and ALS

Ambient Light Sensing

- Convert incident light intensity to digital data
- 16-bit ALS ADC resolution
- Automatic light flickering cancellation supporting
- Block off IR(Infrared) by IR cut off coating

- Excellent transmittance of glass package
- Spectral response close to human eye
- Linear ALS response for easy design
- Low dark noise

Proximity Detection

- Integrated IR LED and synchronous LED driver
- Accept only 940nm for precise detection with strong IR background noise cancellation like fluorescent, incandescent light and sunlight
- Excellent ambient light(Background IR noise) cancellation capability
- 10/8-bit PS ADC resolution

Additional Features

- I^2C protocol interface
- Low stop current - 1uA typical
- Operating rang 2.4 ~ 3.6V
- Small size package (L1.431mm x 1.511mm x H)
- 8-LGA package

1.3 ORDERING INFORMATION

DEVICE NAME	INTERFACE	TEMP. RANGE	PACKAGE TYPE	PACKAGE
MC8201	I^2C	-40 to +85	LGA	8-LGA

Table 1-1 Ordering Information

1.4 APPLICATIONS

- Cell phone
- Digital TV, Tablet PC, Notebook PC
- Navigation systems
- Display-equipped portable devices,etc..

1.5 BLOCK DIAGRAM

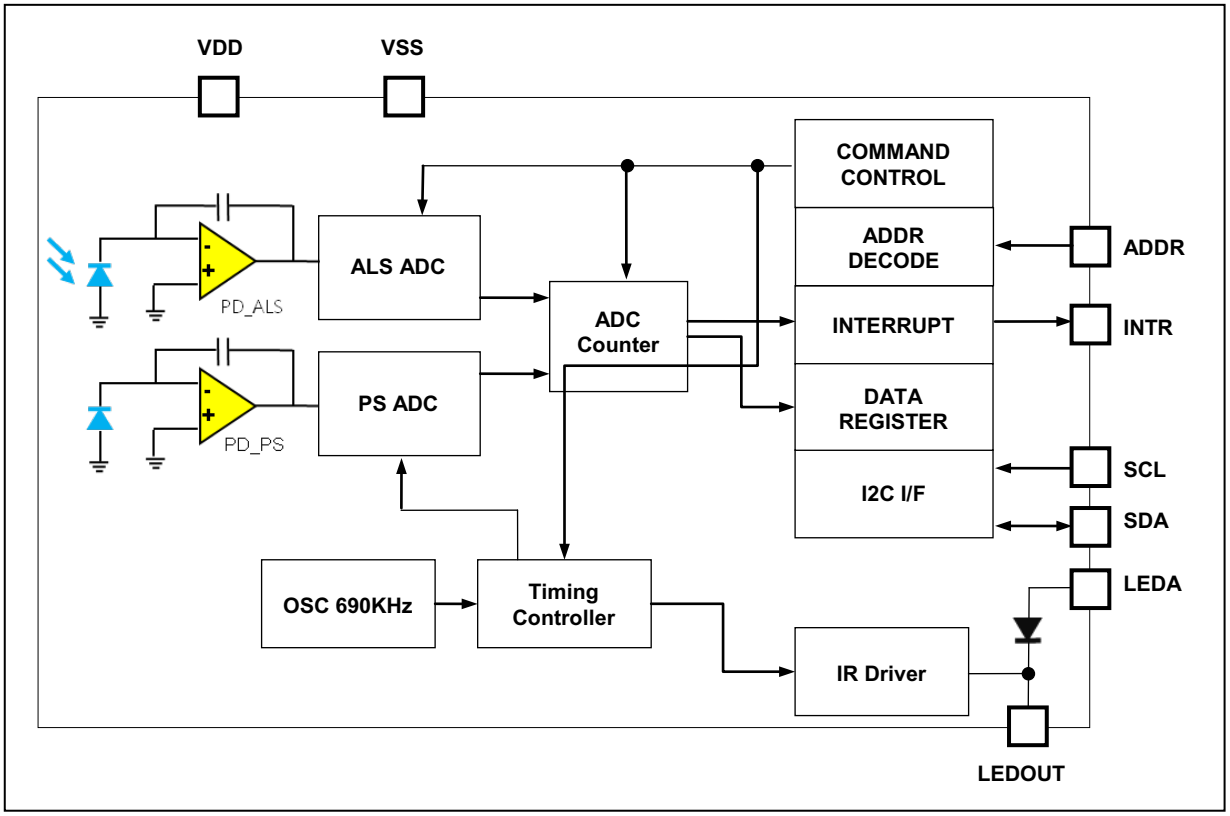

Figure 1-1 Block Diagram of MC8201

1.6 PIN CONFIGURATIONS

8 LGA (MC8201)

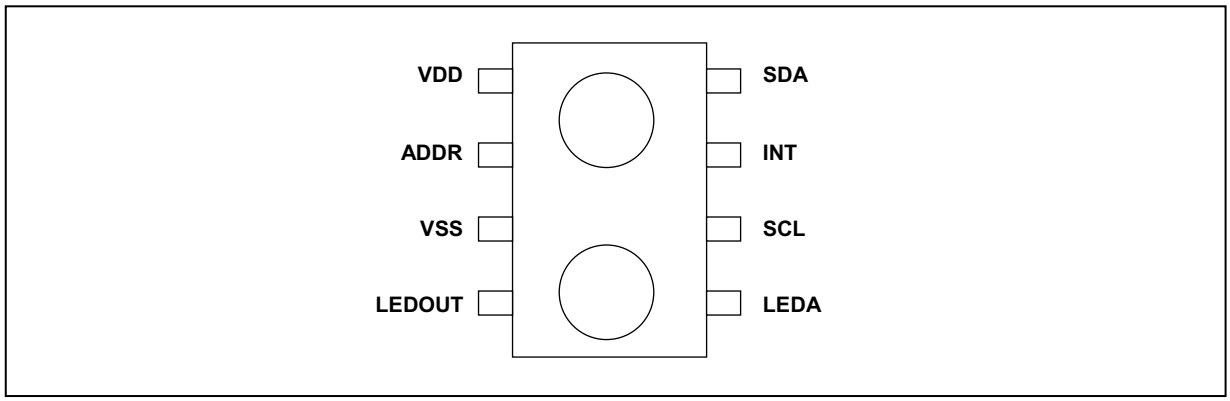

Figure 1-2 PKG Diagram

1.7 PKG DIAGRAM

Figure 1-3 PKG DIMENSION

수정!!!

수정!!!

1.8 PIN DESCRIPTION

PIN Number	PIN Name	Description	I/O
1	VDD	Power supply : 2.4 to 3.6V	Power
2	ADDR	Address Select	Input
3	VSS	Ground	Power
4	LEDOUT	LED driver for proximity emitter – up to 180mA	O(Open Drain)
5	LEDA	LED Anode, connect to VDD or V_{BATT} on PCB	I
6	SCL	I^2C Serial Clock Line	Input
7	INT	ALS, PS Interrupt	O(Open Drain)
8	SDA	I^2C Serial Data Line	O(Open Drain)

Table 1-2 Pin Description

1.9 SLAVE ADDRESS

ADDR	SLAVE ADDRESS
LOW / OPEN	1011_100
HIGH	0110_011

Table 1-3 Slave Address Selection

1.10 ELELCTRICAL CHARACTERISTICS

1.10.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit.	Remark
VDD	Supply voltage	0	4.0	V	
Tstg	Storage temperature range	-40	85	˚C	
VO	Digital ouput voltage range	-0.5	4.0	V	
IO	Digital output current	-1	20	mA	
VHBM	ESD tolerance, Human Body Model		2,000	V	

Table 1-4 Absolute Maximum Ratings

NOTE Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablility.

1.10.2 RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
VDD	Supply voltage	2.4	3.0	3.6	V	
TA	Operating temperature	-40		85	˚C	
VIL	SCL,SDA input low voltage			400	mV	
VIH	SCL,SDA input low voltage	1.4			V	

Table 1-5 Recommended Operating Condition

1.10.3 ELECTRICAL SPECIFICATIONS

(VDD =3.0V, VLED=3.0V, VSS =0V, f_{SCL}=400KHz, TA=+25℃±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
V_{DD}	Power Supply	2.4	-	3.6	V	
I_{STOP}	Power Down Current			1	uA	Power down
I_{DDALS}	Active Current for ALS			120	uA	
I_{DDPS}	Active Current for PS			100	uA	Exclude LED driving
λ_P	Peak Sensitivity wavelength of ALS		550		nm	
λ_{PPS}	Peak Sensitivity wavelength of PS		850		nm	
f_{OSC}	Internal Oscillator Frequency	552	690	828	KHz	
t_{INT}	ADC Integration/Conversion Time		100	500	ms	16-bit ADC data
V_{OL}	INT,SDA ouput low voltage	0		0.4	V	8mA sink current
A_{000L}	ADC Count Value of ALS	-	0	4	counts	@0Lux, white color LED
A_{001L}	@ATIME=14_H (100ms)		8		counts	@1Lux, white color LED
A_{250L}	AGC1=88_H	1600	2000	2400	counts	@250Lux, white color LED
DF_{ALS}	Full Scale ALS ADC Count			65535	counts	
DF_{PS}	Full Scale PS ADC Count			1023	counts	
f_{LED0}	IR LED Modulation Frequency	138.0	172.5	207.0	KHz	LDCTRL[0]=0_B
f_{LED1}		276.0	345.0	414.0	KHz	LDCTRL[0]=1_B
I_{LED1}			60		mA	TSSEL=01_B
I_{LED2}			120		mA	TSSEL=10_B
I_{LED3}			180		mA	TSSEL=11_B

Table 1-6 Electrical Specifications

1.10.4 I²C CHARACTERISTICS

The following table and figure show the timing codition of SDA and SCL bus lines for fast mode I²C bus devices. [NOTE1].

(VDD =3.0V, VSS =0V, TA=+25℃±10%)

Parameter	Symbol[NOTE2]	Min	Max	Unit
SCL clock frequency	t_{SCL}	0	400	KHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	us
LOW period of the SCL clock	t_{LOW}	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	0.6	-	us
Setup time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	0.9	us
Data setup time	$t_{SU;DAT}$	100	-	ns
Clock/data fall time	t_F	0	300	ns
Clock/data rise time	t_R	0	300	ns
Setup time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condtion	t_{BUF}	1.3	-	us

Table 1-7 Timing characteristics of I^2C

NOTE1 All timing is shown with respect to 30% VDD and 70% VDD.

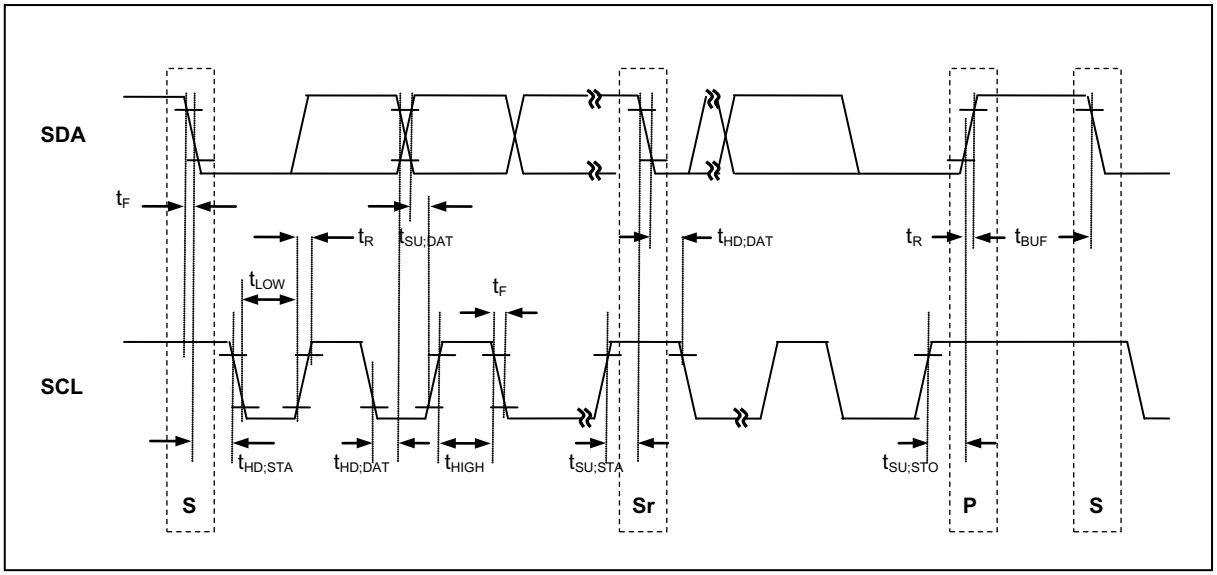

Figure 1-4 Definition of timing for fast mode devices on the I2C bus

1.10.5 OPTICAL CHARACTERISTICS

A. Response linearity by light source

MC8201 has high linearity performance by light illuminace in multi lighting booth system that can emit various lights by controlled its color temperature.

A .1. Fluorescent lamp 1

Color temperature (6500K)

Measurement Illuminace : 0~1,855lx

(graph 1. Spectrum of 6500K lamp)

Result under 6500K daylight

A .2. Fluorescent lamp 2

Color temperature (4200K)

Measurement Illuminace : 0~422lx

Result under 4200K fluorescent lamp

A .3. Incandescent lamp

Color temperature (2856K)

Illuminace : 0 ~ 1,960lx

(graph 2. Spectrum of 2856K lamp)

Result under 2856K fluorescent lamp

B. Spectral response

Spectrum of MC8201 is the below curve by using monochrometer and integrated sphere.

NOTE : Optical characteristics/data are included after full evaluation.

2. OPERATION

2.1 I²C

2.1.1 OVERVIEW

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I²C interface
- Up to 400KHz data transfer speed
- Support two 7-bit slave address
- Slave operation only

2.1.2 I²C BIT TRANSFER

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

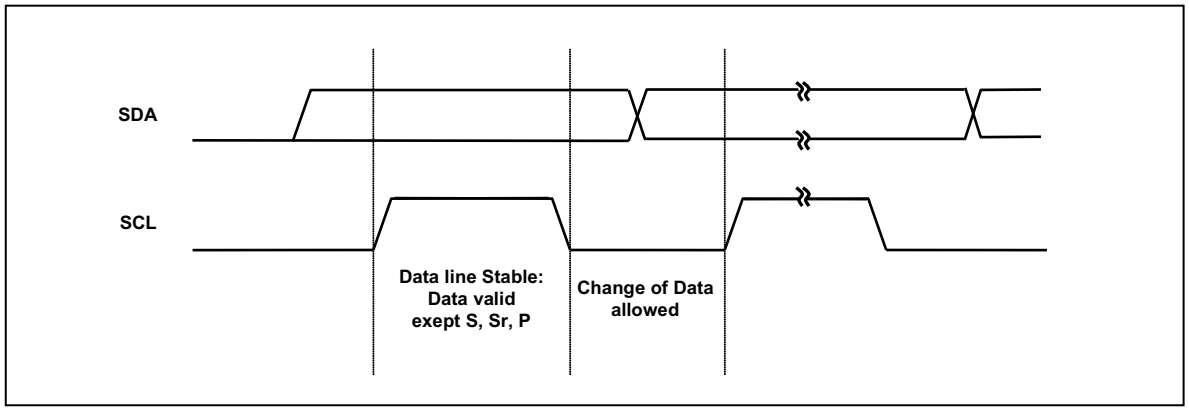

Figure 2-1 Bit Transfer on the I²C-Bus

2.1.3 START / REPEATED START / STOP

One master can issue a START (S) condition to notice other devices connected to the SCL, SDA lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

A high to low transition on the SDA line while SCL is high defines a START (S) condition.

A low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

START and STOP conditions are always generated by a master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

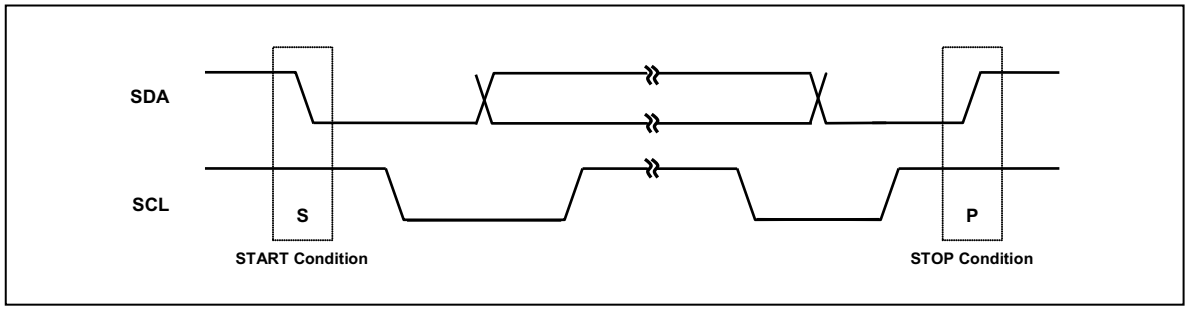

Figure 2-2 START and STOP Condition

2.1.4 DATA TRANSFER

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

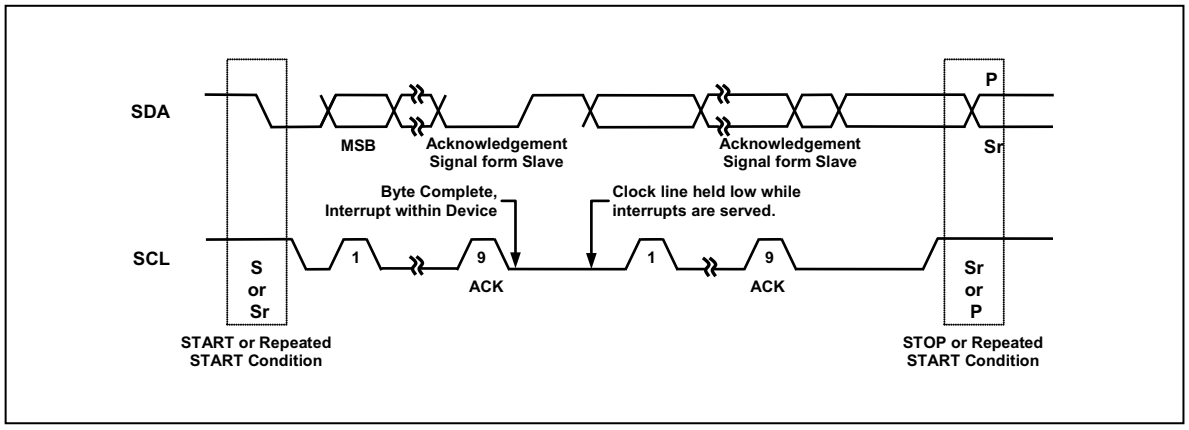

Figure 2-3 STOP or Repeated START Condition

2.1.5 ACKNOWLEDGE

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

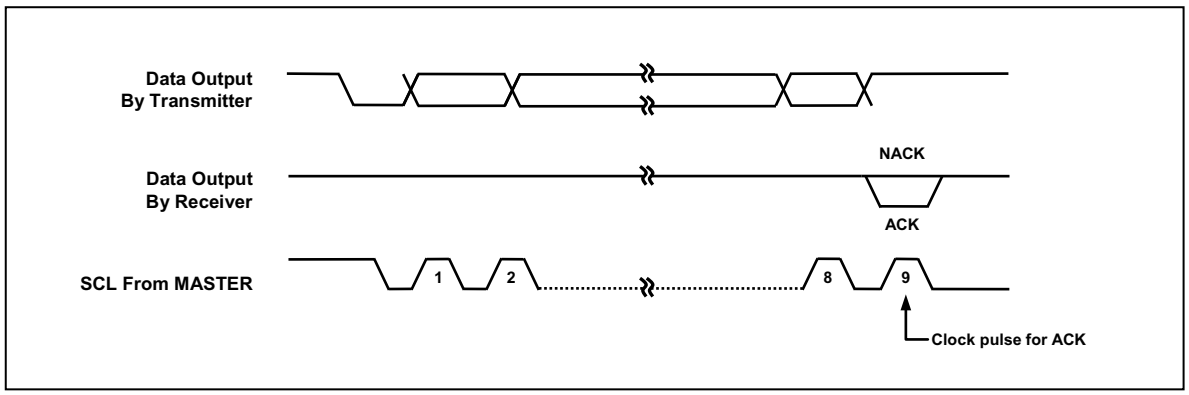

Figure 2-4 Acknowledge on the I²C-Bus

2.1.6 OPERATION

The I²C is byte-oriented serial protocol and data transfer between master and this slave device is initiated by a start condition(S) from master. After start condition, the master sends 7-bit slave address and 1-bit read-write control bit. We call these 8-bit data address packet. The next bytes followed by address packet are all data packet unless another start condition is detected before a stop condition.

The 2nd byte sent from master after address packet with write direction is interpreted as base register or memory address byte. And this base address is incremented only when master transmits more than 2 bytes after start condition because the 2nd byte is register address field.

The MC8201's I²C slave address is configured as "1011100_B" or "0100011_B" according to the input condition of ADDR pin.

2.1.6.1 WRITE PROTOCOL (MASTER TRANSMITTER)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the MC8201 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. The master transmits a number of data to be written and the slave always acknowledges for every data received. To finish transfer the master sends a stop condition regardless of the acknowledgement.

The destination address for incoming data byte increments automatically by one data packet. For example, if master transmits 5 data bytes including a base address(=register address in the following figure) byte and the base address is configured as 00_H, the internal address is defined as 00_H for 1st data byte, 01_H for 2nd data byte, 02_H for 3rd data byte and 03_H for 4th data byte. This applies to Read Protocol also.

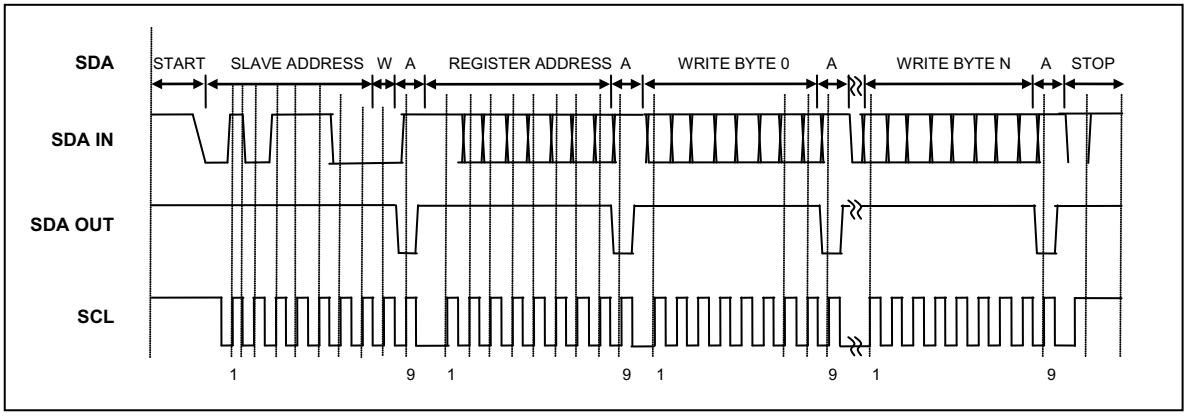

Figure 2-5 I2C Write Protocol

2.1.6.2 READ PROTOCOL (MASTER RECEIVER)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the MC8201 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. To initiate read operations, the master sends repeated start condition and slave address with Read bit. After this address packet, the master reads data bytes until it does not acknowledges. Note that to send a stop condition after receiving last data byte, the master must generate a NACK(not acknowledging) on the last data byte received. Like Write Protocol, the read address increases by 1 after every read byte.

Note that the transfer direction changes in this protocol.

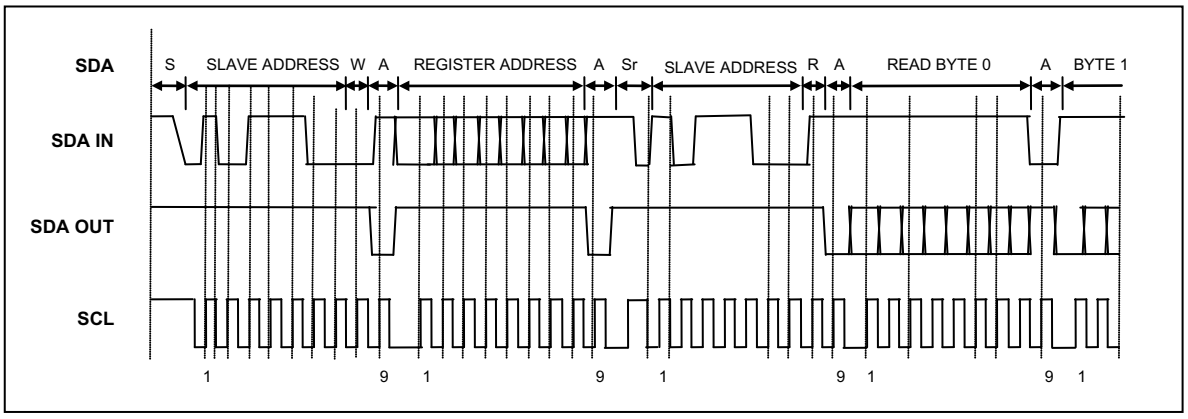

Figure 2-6 I2C Read Protocol

2.2 REGISTERS

2.2.1 OVERVIEW

The MC8201 is controlled and monitored by 23 registers. These registers provide a variety of control functions and can be read to determine results of the ADC conversions.

2.2.2 REGISTER MAP

Name	Address	Dir	Default	Description
ADDRSET	-	W	-	Address Set Register
CONTROL	00_H	R/W	00_H	Control Register
INTR	01_H	R/W	00_H	Interrupt Control Register
ATIME	02_H	R/W	FF_H	ALS Integration Time Register
PTIME	03_H	R/W	FF_H	PS Integration Time Register
WTIME	04_H	R/W	FF_H	Wait Time Register
AILTL	05_H	R/W	FF_H	ALS Interrupt Low Threshold Low Register
AILTH	06_H	R/W	03_H	ALS Interrupt Low Threshold High Register
AIHTL	07_H	R/W	FF_H	ALS Interrupt High Threshold Low Register
AIHTH	08_H	R/W	BF_H	ALS Interrupt High Threshold High Register
PILTL	09_H	R/W	FF_H	PS Interrupt Low Threshold Low Register
PILTH	$0A_H$	R/W	03_H	PS Interrupt Low Threshold High Register
PIHTL	$0B_H$	R/W	FF_H	PS Interrupt High Threshold Low Register
PIHTH	$0C_H$	R/W	03_H	PS Interrupt High Threshold High Register
PERSIST	$0D_H$	R/W	00_H	ALS/PS Interrupt Persistence Register
ADATAL	$0E_H$	R	FF_H	ALS ADC Data Low Register
ADATAH	$0F_H$	R	FF_H	ALS ADC Data High Register
PDATA0L	10_H	R	00_H	PS ADC Data0 Low Register
PDATA0H	11_H	R	00_H	PS ADC Data0 High Register
PDATA1L	12_H	R	FF_H	PS ADC Data1 Low Register
PDATA1H	13_H	R	03_H	PS ADC Data1 High Register
AGC0	14_H	R/W	00_H	ADC Gain control 0 Register
AGC1	15_H	R/W	00_H	ADC Gain control 1 Register
PLEDC	16_H	R/W	00_H	PS LED control Register

Table 2-1 Registers of MC8201

Caution : Do not access registers addressed between 17_H and $1F_H$. Writing to these registers may result in unexpected function.

2.2.3 REGISTER DESCRIPTION

ADDRSET (Address Set Register) **$--_H$**

7	6	5	4	3	2	1	0
-	-	-	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
-	-	-	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

ADDR[4:0] Base address for subsequent register access. When the I2C master initiates a write protocol with start bit and slave address transfer, the second byte is used to configure register address.

CONTROL (Control Register) **00_H**

7	6	5	4	3	2	1	0
ONESHOT	SOFTRST	PROXSEL	IRSEL	PSTYPE	PAEN	AAEN	POWER
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

ONESHOT Stops ADC integration on completion of one integration cycle.

0 Continuous operation.

1 Once an integration cycle is over, PS/ALS ADC will automatically stop and also the PAEN/AAEN bits in CONTROL register is to be cleared. To resume operation, re-assert PAEN or AAEN.

SOFTRST Soft reset. This bit is auto-cleared.

0 No operation

1 Reset internal registers

PROXSEL The INT pin operates as proximity detection output mode.

0 INT pin is used as PS or ALS interrupt pin

1 INT pin is used as proxmity detection output mode

IRSEL Selects the PDATA0H/L read data.

0 PDATA0 holds the value obtained by subtracting IR(LED off) ADC count from PS(LED on) ADC count.

1 PDATA0 holds the value obtained directly from IR(LED off) ADC count. Set this bit for test purpose.

PSTYPE PS mode select

0 PS TYPE 0 mode

1 PS TYPE 1 mode

PAEN PS ADC Enable. This bit enables the PS ADC channel to begin integration. This bit is effective only when POWER bit is set to '1'. NOTE

0 Disable Photo Diode and PS ADC.

1 Enable Photo Diode and PS ADC.

AAEN ALS ADC Enable. This bit enables the ALS ADC channel to begin integration. This bit is effective only when POWER bit is set to '1'. NOTE

0 Disable Photo Diode and ALS ADC.

1 Enable Photo Diode and ALS ADC.

POWER Power On. Enables internal RC oscillator(Typically 700KHz)

0 Turns off the MC8201.

1 Turns on the MC8201.

NOTE The real PAEN and AAEN bits are updated after internal oscillator is enabled. So reading CONTROL register will return "---- --00_B" when writing '1' to these bits while POWER bit is disabled or enabling PAEN, AAEN and POWER bits simultaneously.

By enabling PAEN or AAEN bits individually, MC8201 operates as PS only mode, ALS only mode or PS-ALS alternating mode.

INTR (Interrupt Control Register) **01_H**

7	6	5	4	3	2	1	0
PSX4EN	ALC_IR	PROXDET	PINTF	AINTF	INTEDGE	PINTEN	AINTEN
R/W	R/W	R	R	R	R/W	R/W	R/W

Initial value : 40_H

PSX4EN Enable proximity sensing4 times in row.

0 Proximity sensing is performed once in a ps time

1 Proximity sensing is performed 4 times in a ps time

ALC_IR Enable ALC function

0 Disable ALC

1 Enable ALC (default)

PROXDET Proximity detection result. When PS ADC counter value is greater than PIHT, this flag is set. When PS ADC counter value is less than PILT, this flag is cleared. For proper detection result, set PPER greater than 01_H.

0 Non-detect (Object is far)

1 Detect (Object is near)

PINTF PS Interrupt Flag. Indicates that the device is asserting an interrupt. Writing 0 to this bit clears PINTF.

0 No Interrupt or interrupt cleared.

1 PS interrupt requested.

AINTF ALS Interrupt Flag. Indicates that the device is asserting an interrupt. Writing 0 to this bit clears AINTF.

0 No Interrupt or interrupt cleared.

1 ALS interrupt requested.

INTEDGE Interrupt signal is triggered as pulse type at rising edge of internal clock,typically 1.4us period. The host needs not to clear interrupt.

0 Level interrupt

1 Edge interrupt

PINTEN Enables PS Interrupt generation.

0 PS Interrupt output is disabled.

1 PS Interrupt occurs on INT pin.

AINTEN Enables ALS Interrupt generation.

0 ALS Interrupt output is disabled.

1 ALS Interrupt occurs on INT pin.

ATIME (ALS Integration Time Register) 02_H

7	6	5	4	3	2	1	0
ATIME7	ATIME6	ATIME5	ATIME4	ATIME3	ATIME2	ATIME2	ATIME1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

ATIME[7:0] ALS Integration Time. Specifies the integration time in 5.0 ms intervals.
ALS Integration time = 5 ms x ATIME[7:0]
The maximum ALS integration time is about 1275.0 ms (11111111_B).

00000000 Prohibited. Writing "00_H" has no effect.

00000001 5.0 ms

00000010 10.0 ms

00001010 50.0 ms

00010100 100.0 ms

00101000 200.0 ms

01010000 400.0 ms

11111111 1275.0 ms

PTIME (PS Integration Time Register) 03_H

7	6	5	4	3	2	1	0
PTIME7	PTIME6	PTIME5	PTIME4	PTIME3	PTIME2	PTIME2	PTIME1
RW	RW	RW	RW	RW	RW	RW	RW

Initial value : FF_H

PTIME[7:0] PS Integration Time. Specifies the integration time in 0.37 ms intervals.
PS Integration time = 185 us x PTIME[7:0]
The maximum PS integration time is about 47.2 ms (11111111_B).

00000000	Prohibited. Writing "00_H" has no effect.
00000001	0.185 ms
00000010	0.37 ms
00001010	1.85 ms
00010100	3.7 ms
00101000	7.4 ms
01010000	14.8 ms
11111111	47.175 ms

WTIME (Wait Time Register) **04_H**

7	6	5	4	3	2	1	0
WTIME7	WTIME6	WTIME5	WTIME4	WTIME3	WTIME2	WTIME2	WTIME1
RW	RW	RW	RW	RW	RW	RW	RW

Initial value : FF_H

WTIME[7:0] Wait Time. Specifies the wait time between continuous ALS or PS operations in 5.38 ms intervals.
Wait time = 5.38 ms x WTIME[7:0]
The maximum wait time is about 1371.9 ms (11111111_B).

00000000	No wait
00000001	5.38 ms
00000010	10.76 ms
00001010	53.8 ms
00010100	107.6 ms
00101000	215.2 ms
01111000	645.6 ms
11111111	1371.9 ms

The WTIME is used to reduce average power consumption, because the PS and ALS ADC stop integrating during wait time period.

When PSEN=1 and ALSEN=0, the internal operating state machine repeats PS and WAIT state continuously.

When ALSEN=1 and PSEN=0, the internal operating state machine repeats ALS and WAIT state continuously.

When PSEN=1 and ALSEN=1, the internal operating mode is as follows : PS—ALS—WAIT—PS—ALS—WAIT—PS—ALS—WAIT…

NOTE Although setting a larger wait time contributes to reduce average consumption current, it makes update period and response time longer.

AILTL (ALS Interrupt Low Threshold Low Register) **05_H**

7	6	5	4	3	2	1	0
AILTL7	AILTL6	AILTL5	AILTL4	AILTL3	AILTL2	AILTL1	AILTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

AILTL[7:0] ALS ADC channel interrupt low threshold low register.

AILTH (ALS Interrupt Low Threshold High Register) 06_H

7	6	5	4	3	2	1	0
AILTH7	AILTH6	AILTH5	AILTH4	AILTH3	AILTH2	AILTH1	AILTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 03_H

AILTH[7:0] ALS ADC channel interrupt low threshold high register.

AIHTL (ALS Interrupt High Threshold Low Register) 07_H

7	6	5	4	3	2	1	0
AIHTL7	AIHTL6	AIHTL5	AIHTL4	AIHTL3	AIHTL2	AIHTL1	AIHTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

AIHTL[7:0] ALS ADC channel interrupt high threshold low register.

AIHTH (ALS Interrupt High Threshold High Register) 08_H

7	6	5	4	3	2	1	0
AIHTH7	AIHTH6	AIHTH5	AIHTH4	AIHTH3	AIHTH2	AIHTH1	AIHTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : BF_H

AIHTH[7:0] ALS ADC channel interrupt high threshold high register.

PILTL (PS Interrupt Low Threshold Low Register) 09_H

7	6	5	4	3	2	1	0
PILTL7	PILTL6	PILTL5	PILTL4	PILTL3	PILTL2	PILTL1	PILTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

PILTL[7:0] PS ADC channel interrupt low threshold low register.

PILTH (PS Interrupt Low Threshold High Register) $0A_H$

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PILTH1	PILTH0
-	-	-	-	-	-	R/W	R/W

Initial value : 03_H

PILTH[1:0] PS ADC channel interrupt low threshold high register.

PIHTL (PS Interrupt High Threshold Low Register) **$0B_H$**

7	6	5	4	3	2	1	0
PIHTL7	PIHTL6	PIHTL5	PIHTL4	PIHTL3	PIHTL2	PIHTL1	PIHTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

PIHTL[7:0] PS ADC channel interrupt high threshold low register.

PIHTH (PS Interrupt High Threshold High Register) **$0C_H$**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PIHTH1	PIHTH0
-	-	-	-	-	-	R/W	R/W

Initial value : $0F_H$

PIHTH[1:0] PS ADC channel interrupt high threshold high register.

The interrupt threshold registers store the values to be used as the high and low trigger points for the adc data registers. If the value of adc data register crosses below or equal to the low threshold specified, an interrupt can be asserted on the interrupt pin. Likewise, if the result from ADC conversion crosses above the high threshold specified, an interrupt can be asserted on the interrupt pin. Note these high and low threshold registers are 16-bit wide for ambient light sensing, 10/8-bit wide for proximity sensing.

When the device is in ALS mode, the concatenated AILTH and AILTL is used as interrupt low threshold(=AILT) and the concatenated AIHTH and AIHTL is used as interrupt high threshold(=AIHT).

Similarly, when the device is in PS mode, the concatenated PILTH and PILTL is used as interrupt low threshold(=PILT) and the concatenated PIHTH and PIHTL is used as interrupt high threshold(=PIHT). When PROXSEL bit is set, the proximity sensing result is output through the INT pin. The INT pin goes LOW when the PS ADC result is greater than or equal to PIHT and goes HIGH when the PS ADC result is less than PILT. So for proper operation with PROXSEL bit set to 1, the PILT should be non-zero value, otherwise the INT pin will be held LOW unless PINTF is cleared by host command.

Caution : Make sure that the PIHTH register and PILTH register are loaded with “00” when PS resolution is set to 8-bit for proper operation.

PERSIST (Interrupt Persistence Register) **$0D_H$**

7	6	5	4	3	2	1	0
PPER3	PPER2	PPER1	PPER0	APER3	APER2	APER1	APER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

PPER[3:0] PS Interrupt persistence. These bit field control the rate of PS interrupt request to host chip.

When PROXSEL bit is set, PPER should be greater than 0000_H for proper operation.

0000	Every PS cycle generates an interrupt.
0001	1 consecutive PS ADC value out of range.
0010	2 consecutive PS ADC value out of range.
...	…
1111	15 consecutive PS ADC value out of range.

APER[3:0] ALS Interrupt persistence. These bit field control the rate of ALS interrupt request to host chip.

0000	Every ALS cycle generates an interrupt.
0001	1 consecutive ALS ADC value out of range.
0010	2 consecutive ALS ADC value out of range.
...	…
1111	15 consecutive ALS ADC value out of range.

ADATAL (ALS ADC Data Low Register) $0E_H$

7	6	5	4	3	2	1	0
ADATAL7	ADATAL6	ADATAL5	ADATAL4	ADATAL3	ADATAL2	ADATAL1	ADATAL0
R	R	R	R	R	R	R	R

Initial value : FF_H

ADATAL[7:0] ALS ADC channel data low register.

The ALS ADC included in MC8201 is of 16-bit resolution, and the integrated values appear on two registers ADATAL and ADATAH respectively. All ALS ADC data registers are read-only.

ADATAH (ALS ADC Data High Register) $0F_H$

7	6	5	4	3	2	1	0
ADATAH7	ADATAH6	ADATAH5	ADATAH4	ADATAH3	ADATAH2	ADATAH1	ADATAH0
R	R	R	R	R	R	R	R

Initial value : FF_H

ADATAH[7:0] ALS ADC channel data high register.

PDATA0L (PS ADC Data 0 Low Register) 10_H

7	6	5	4	3	2	1	0
PDATA0L7	PDATA0L6	PDATA0L5	PDATA0L4	PDATA0L3	PDATA0L2	PDATA0L1	PDATA0L0
R	R	R	R	R	R	R	R

Initial value : 00_H

PDATA0L[7:0] PS ADC channel data 0 low register.

PDATA0H (PS ADC Data 0 High Register) 11_H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PDATA0H1	PDATA0H0
-	-	-	-	-	-	R	R

Initial value : 00_H

PDATA0H[7:0] PS ADC channel data 0 high register.

PDATA1L (PS ADC Data 1 Low Register) 12_H

7	6	5	4	3	2	1	0
PDATA1L7	PDATA1L6	PDATA1L5	PDATA1L4	PDATA1L3	PDATA1L2	PDATA1L1	PDATA1L0

R	R	R	R	R	R	R	R

Initial value : FF_H

PDATA1L[7:0] PS ADC channel data 1 low register.

PDATA1H (PS ADC Data 1 High Register) 13_H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PDATA1H1	PDATA1H0
-	-	-	-	-	-	R	R

Initial value : 03_H

PDATA1H[3:0] PS ADC channel data 1 high register.

The PS ADC included in MC8201 is of 10/8-bit resolution, and the integrated values appear on two registers PDATA0(PDATA0H:PDATA0L) and PDATA1(PDATA1H:PDATA1L) respectively. All PS ADC data registers are read-only.

The PDATA0H and PDATA0L registers are updated 1 time during 1 PS cycle and the loading data is selected by IRSEL bit in CONTROL register. If IRSEL bit is '0', the result of subtracting IR(LED off) ADC count from PS(LED on) ADC count is loaded into PDATA0. If IRSEL bit is '1', the IR(LED off) ADC count is directly transferred into PDATA0.

Caution : The PDATA1L/H registers are used for test purpose.

AGC0 (ADC Gain Control 0 Register) 14_H

7	6	5	4	3	2	1	0
PS_RES	-	-	-	-	-	VGAIN1	VGAIN0
R/W	-	-	-	-	-	R/W	R/W

Initial value : 03_H

PS_RES Select PS resolution

0 10-bit resolution

1 8-bit resolution

VGAIN[1:0] ADC Voltage Gain Control. This VGAIN affects on both ALS and PS operations.

00 x2.0

01 x1.4

10 x1.2

11 x1.0

Caution : Do not alter AGC0[7:2]. Writing non-zero value to these bits may result in mal-function.

AGC1 (ADC Gain Control 1 Register) 15_H

7	6	5	4	3	2	1	0
PGAIN3	PGAIN2	PGAIN1	PGAIN0	AGAIN3	AGAIN2	AGAIN1	AGAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 88_H

PGAIN[3:0] PS ADC gain control [NOTE]

0000 Not available 1000 x1.0

0001	x8.0	1001	x0.89
0010	x4.0	1010	x0.80
0011	x2.67	1011	x0.73
0100	x2.0	1100	x0.67
0101	x1.6	1101	x0.62
0110	x1.33	1110	x0.57
0111	x1.14	1111	x0.53

AGAIN[3:0] ALS ADC gain control [NOTE]

0000	Not available	1000	x1.0
0001	x8.0	1001	x0.89
0010	x4.0	1010	x0.80
0011	x2.67	1011	x0.73
0100	x2.0	1100	x0.67
0101	x1.6	1101	x0.62
0110	x1.33	1110	x0.57
0111	x1.14	1111	x0.53

[NOTE] Grayed gains are not recommended.

PLEDC (PS LED Control Register) 16_H

7	6	5	4	3	2	1	0
LEDCTRL1	LEDCTRL0	-	TSSEL1	TSSEL0	-	DUTY1	DUTY0
R/W	R/W	-	R/W	R/W	-	R/W	R/W

Initial value : 00_H

LEDCTRL[1:0] LED Drive Control (DC / Duty 50% / Modulation Frequency)

- 00 LED Drive = FREQ
- 01 LED Drive = FREQ/2
- 10 LED Drive = DC (according to FREQ, max 8 PS time step)
- 11 LED Drive = 50% duty (according to FREQ, max 8 PS time step)

TSSEL[1:0] LED Drive Strength

- 00 not available
- 01 60mA
- 10 120mA
- 11 180mA

DUTY[1:0] Duty of LED Modulation Frequency

- 00 25% duty cycle
- 01 12.5% duty cycle
- 10 6.25% duty cycle
- 11 3.125 % duty cycle

2.3 PS/ALS OPERATION

2.3.1 FSM

The following shows detailed flow for the internal state machine. The device starts in shutdown mode after power-on. It start PS or ALS operation by setting POWER bit in CONTROL register, which enables internal oscillator.

If PAEN bit is set and AAEN bit is cleared, the state machine will step through the proximity states of Ambient Light Cancellation(ALC), IR and Proxmity sensing(IR and PS). After that, it moves to Ambient light sensing(ALS) state if AAEN bit is set, or to Wait state(WAIT) if AAEN bit is cleared.

If AAEN bit is set and PAEN bit is cleared, the state machine skips IR and Proxmitiy sensing state and goes directly to Ambient light sensing state.

If both PAEN bit and AAEN bit are set, the device starts IR and Proxmity sensing, and continues to move to Ambient light sensing state.

If WTIME register is cleared to 00_H, the Wait state is skipped.

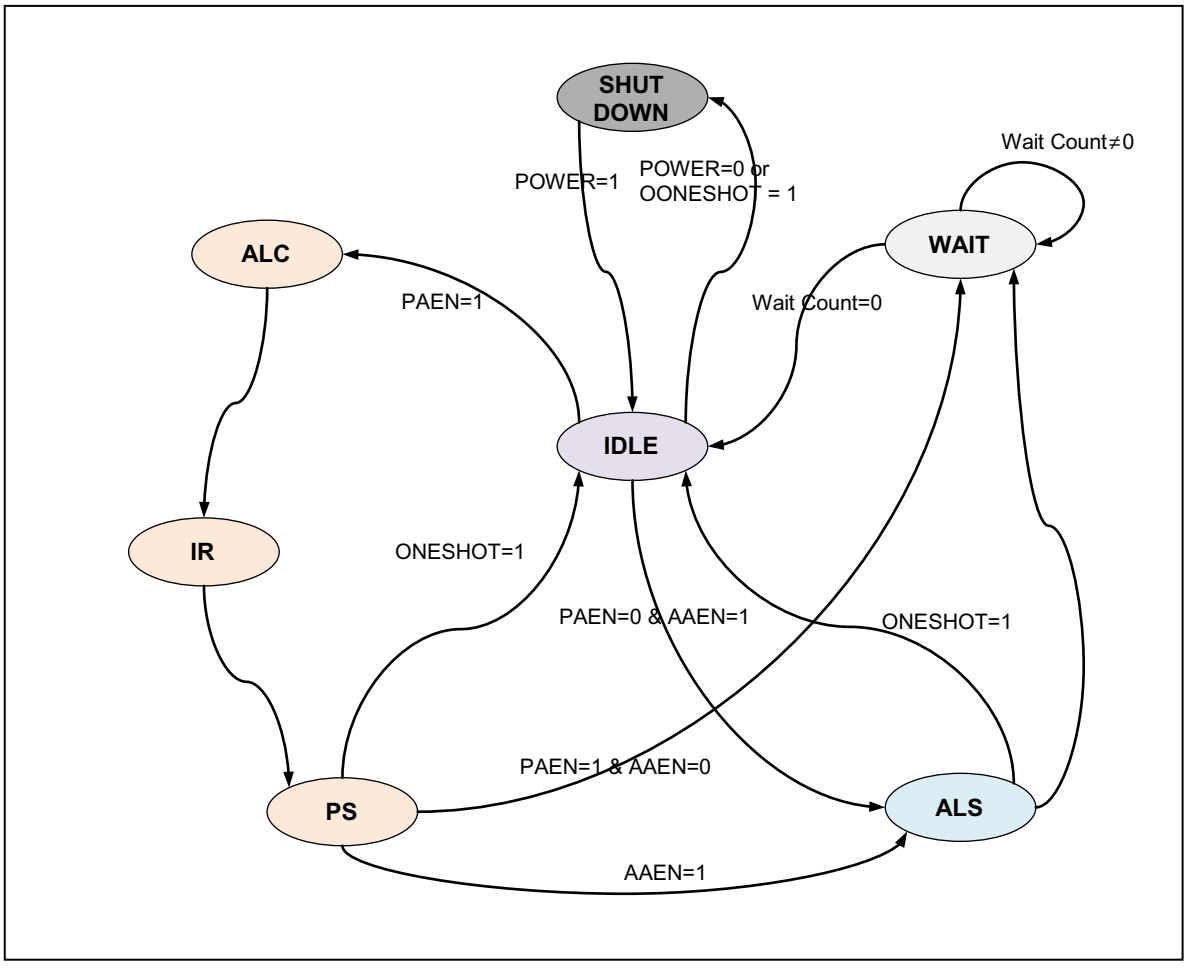

Figure 2-7 PS-ALS Operating State Machine

2.3.2 ALS OPERATION

ALS operation is enabled by setting AAEN bit, and after pre-defined ALS period the ALS ADC counter value is transferred to ADATAH and ADATAL registers which can be read via I2C read transaction.

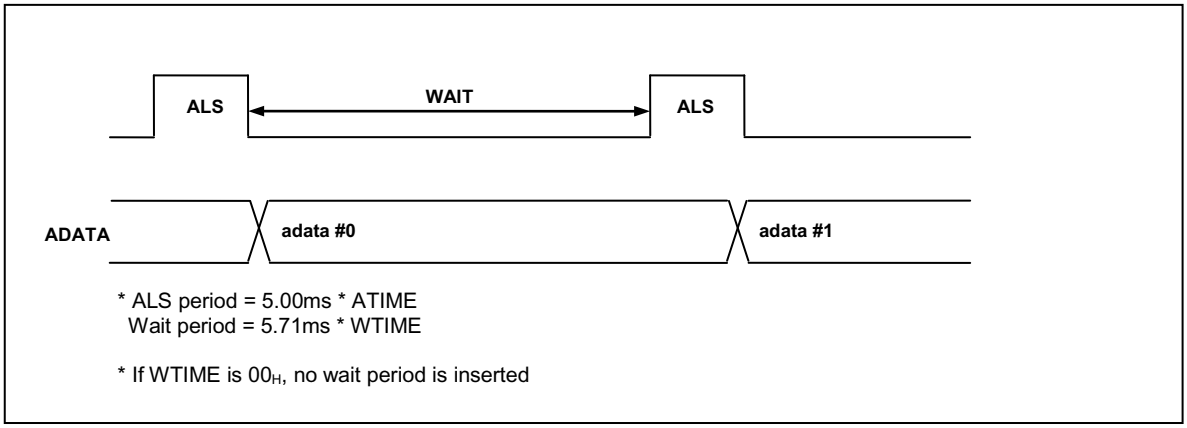

Figure 2-8 ALS Operation

2.3.3 PS OPERATION

As shown in below figure, a typical PS cycle is composed of 3 steps, which are ALC(Ambient Light Cancellation), IR(IR Sensing) and PS(Proximity Sensing) respectively. When PAEN bit is enabled, the device starts proximity sensing and the ALC function is inserted automatically for ambient light cancellation, which offers superior performance in bright sunlight conditions. During IR sensing period, the PS ADC output is directly proportional to the IR intensity and the ADC result, padc2 is stored into PDATA1H/L registers. After that, the device starts PS sensing. The PS ADC output(padc3) is directly proportional to the total IR intensity from the background IR noise and from the IR LED driven by the device. After PS step, the result of subtracting padc2 from padc3 is stored into PDATA0H/L registers.

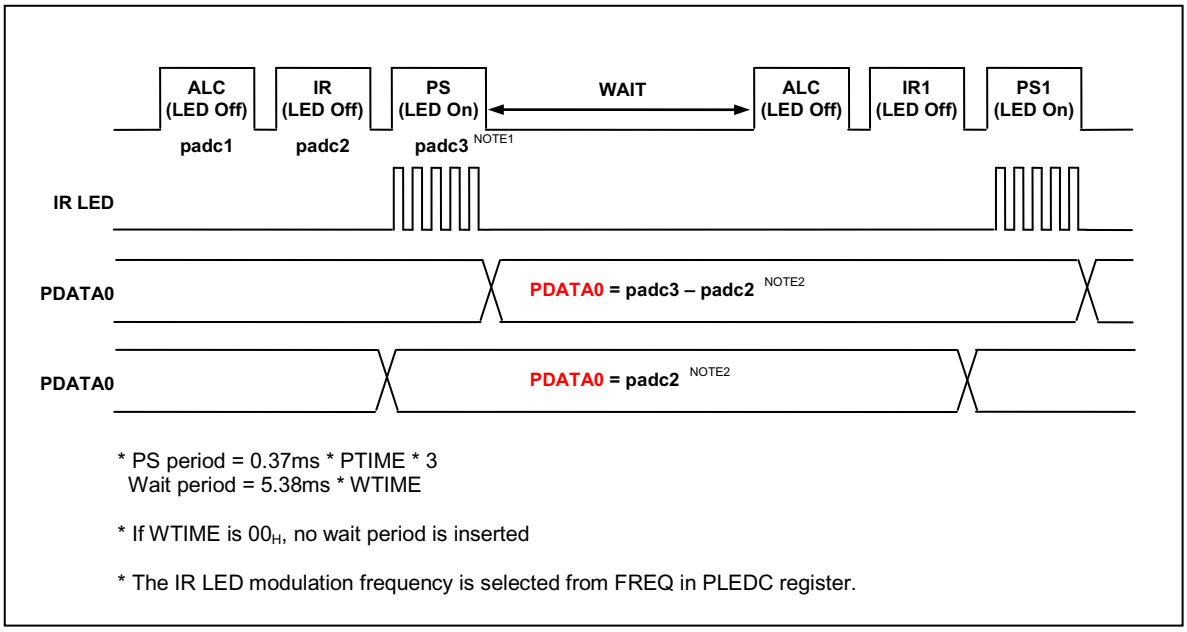

Figure 2-9 PS Type 0 Operation

NOTE1 In above figures, padc1 is 1st ADC(ALC) result with LED on or off according to PSTYPE, padc2 is 2nd ADC(IR) result with LED off and padc3 is 3rd ADC(PS) result with LED on.

NOTE2 When IRSEL bit in CONTROL register is '0', PDATA0H/L = padc3 – padc2. When IRSEL bit is '1', PDATA0H/L = padc3. PDATA1H/L holds temporary PS ADC results.

2.3.4 PS-ALS ALTERNATING OPERATION

PS-ALS alternating mode is enabled by setting both AAEN and PAEN bits to 1. In this mode of operation, PS operation is done followed by ALS operation and optional WAIT cycle.

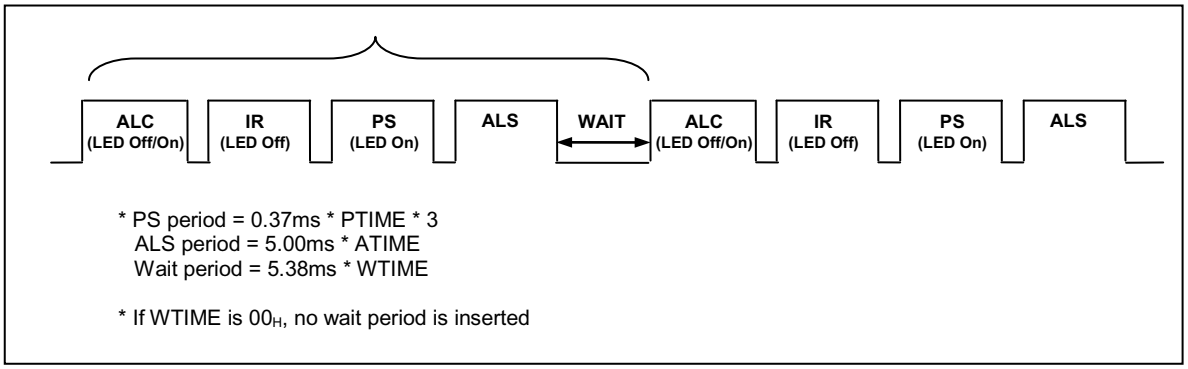

Figure 2-10 ALS-PS Alternating Operation

2.3.5 INTERRUPT

2.3.5.1 INTERRUPT OUTPUT MODE

INT pin operates as interrupt output mode by setting AINTEN or PINTEN bit. In this mode of operation, the PROXSEL bit should be cleared.

ALS Interrupt

An ALS interrupt can be requested when ALS ADC result is greater than or equal to AITH or less than AILT after one ALS cycle. If APER(ALS Persistence) value is non-zero, it is needed the ALS ADC results are out of range APER consecutive times. The result of interrupt judgement for ALS is stored into AINTF bit in INTR register.

PS Interrupt

A PS interrupt can be requested when PS ADC result is greater than or equal to PITH or less than PILT after one PS cycle. If PPER(PS Persistence) value is non-zero, it is needed the PS ADC results are out of range PPER consecutive times. The result of interrupt judgement for PS is stored into PINTF bit in INTR register.

There are two kinds of output mode, level or pulse interrupt. Below is the description of the level interrupt type.

Transition from H to L in INT pin means that an interrupt condition is generated, and the INT pin remains L level until corresponding interrupt flag(AINTF or PINTF) is cleared. Any interrupt is cleared by writing 0 to it's flag bit in INTR register.

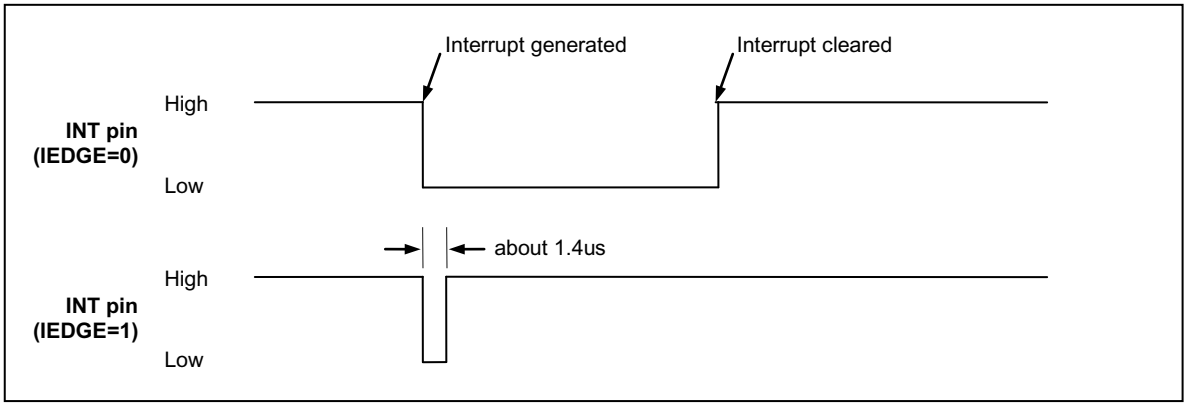

Figure 2-11 ALS or PS Interrupt output (level or pulse interrupt)

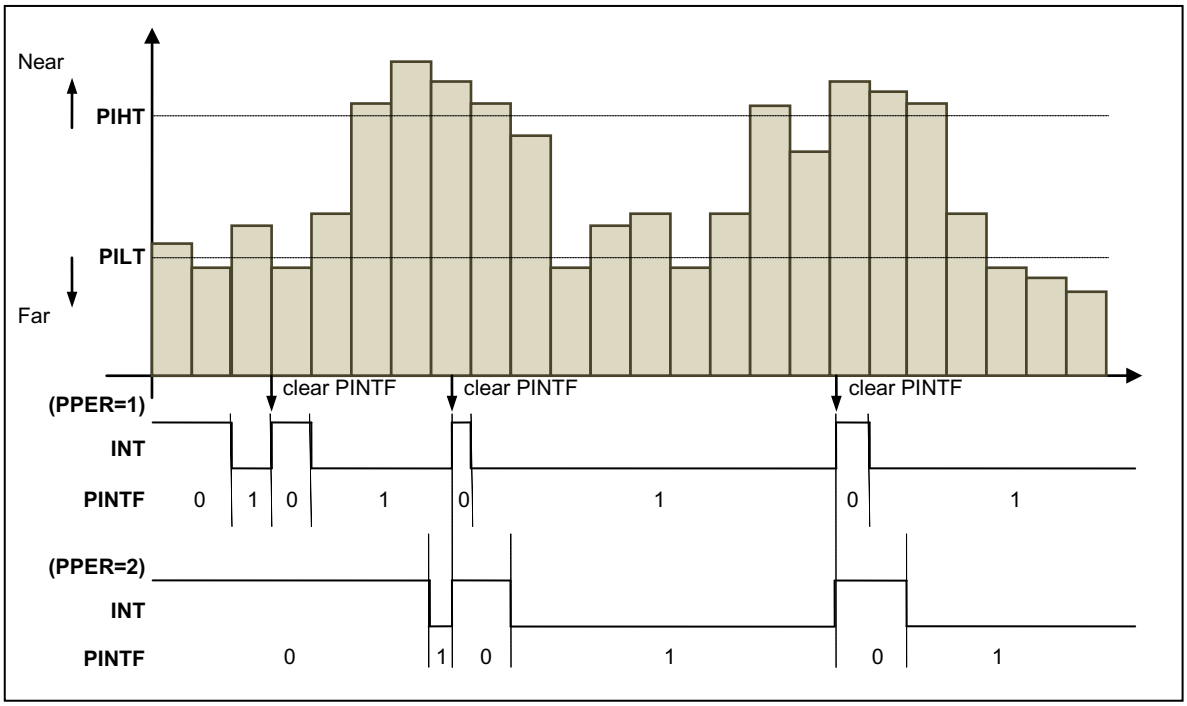

Figure 2-12 PS Interrupt Output (PPER=1 or 2 & INTEDGE=0)

2.3.5.2 PROXIMITY DETECTION MODE

INT pin operates as proximity detection result output mode by setting PROXSEL bit. The sensing result whether an object is detected or not appears on INT pin.

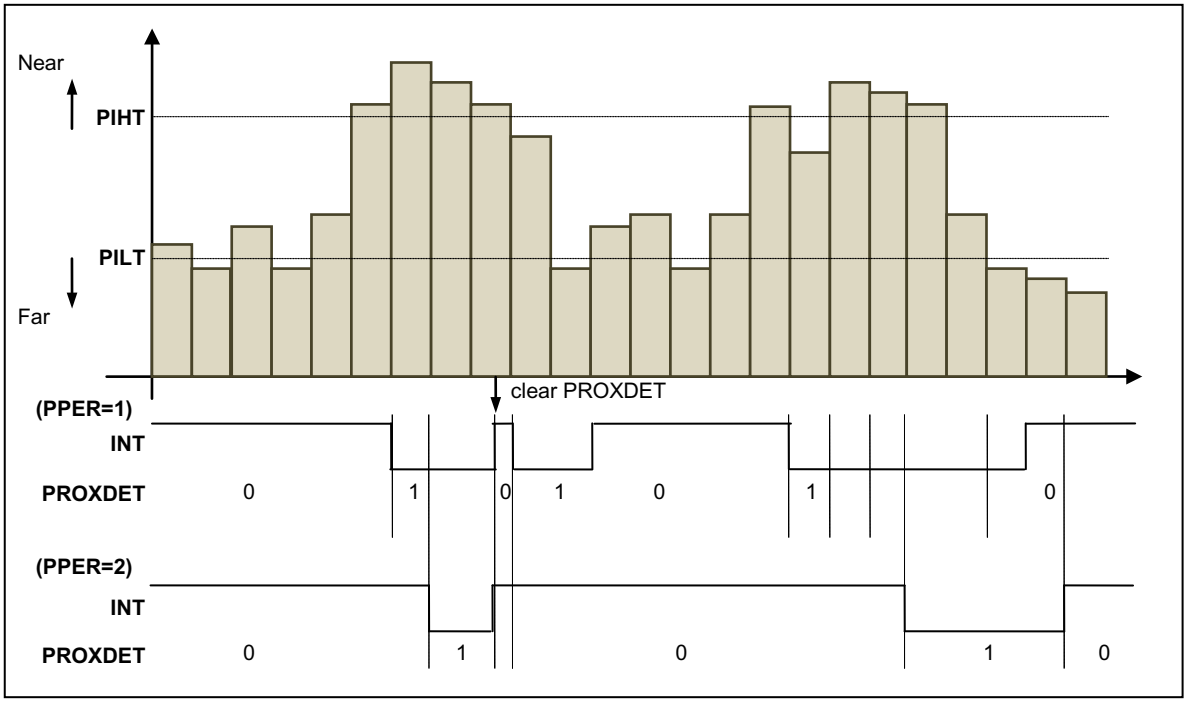

Figure 2-13 PS Detection (PPER=1 or 2)

Unlike interrupt output mode, the PS ADC result(padc3-padc2) appears on INT pin directly. That is, the INT pin is LOW(Detection condition is met) when PS ADC result is greater than or equal to PIHT, the INT pin goes HIGH(Non-detection is occurred) when PS ADC result is less than PILT. If PPER value is non-zero, the detection and non-detection conditions are judged when PS ADC results are out of range PPER consecutive times. Note that the INT pin goes high or is released only when PS ADC result is less than PILT. So it is required that the PILT should be a non-zero value.

2.3.6 LED DRIVE CONTROL

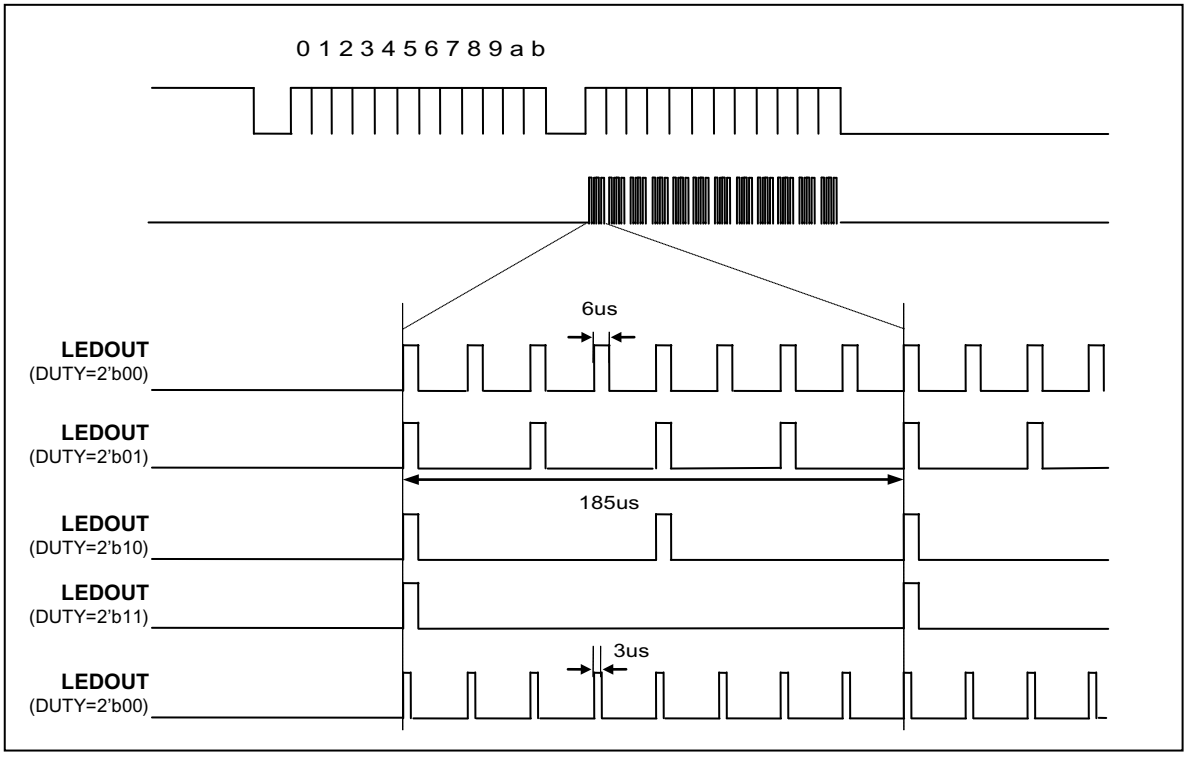

Figure 2-14 PS Detection (PPER=1 or 2)

Unlike interrupt output mode, the PS ADC result(padc3-pa

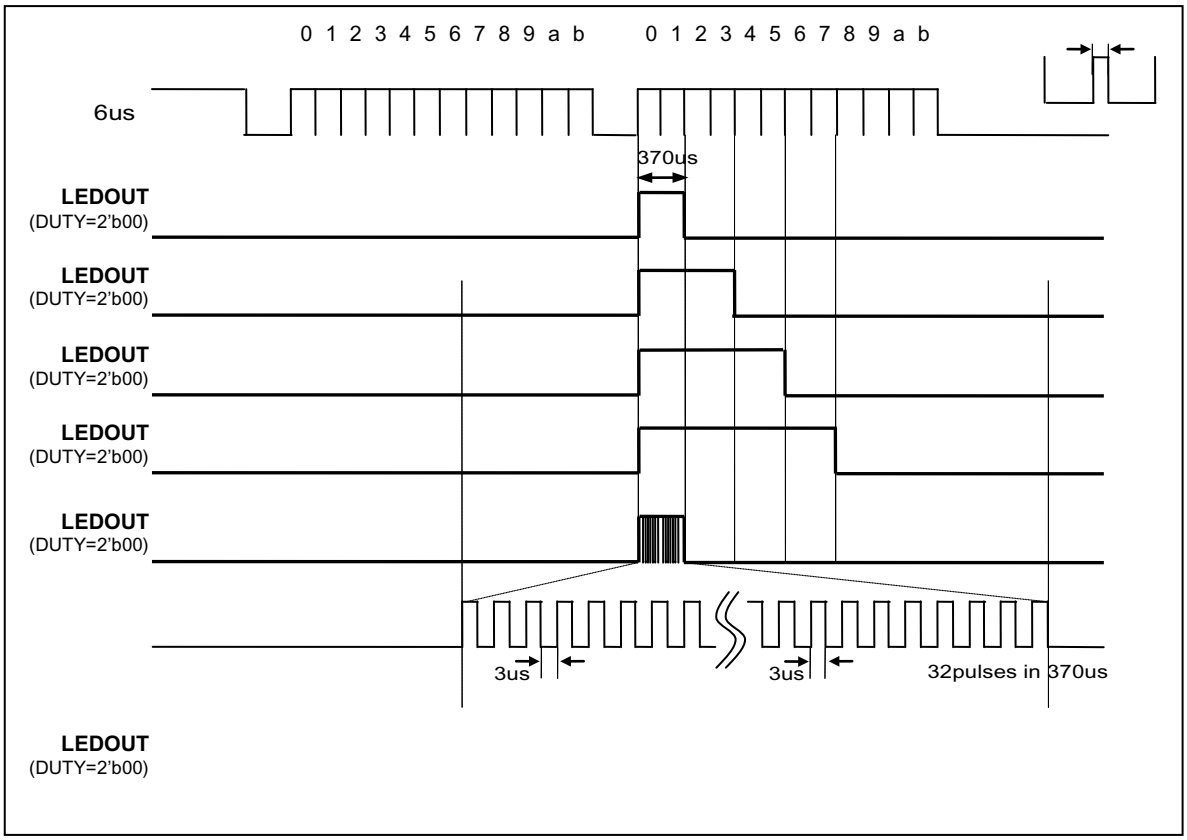

Figure 2-15 PS Detection (PPER=1 or 2)

Unlike interrupt output mode, the PS ADC result(padc3-pa

2.3.7 POWER CONSUMPTION

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 60uA of power.

2.4 APPLICATION INFORMATION : SOFTWARE

2.4.1 OVERVIEW

After applying VDD, the device will initially be in the power down mode. To start PS or ALS sensing operation, set the POWER bit in CONTROL register to enable internal RC oscillator. The PTIME, ATIME or WTIME registers should be configured for the preferred integration and wait time, and then the PAEN or AAEN bits in CONTROL register should be set to 1 to enable each ADC channel.

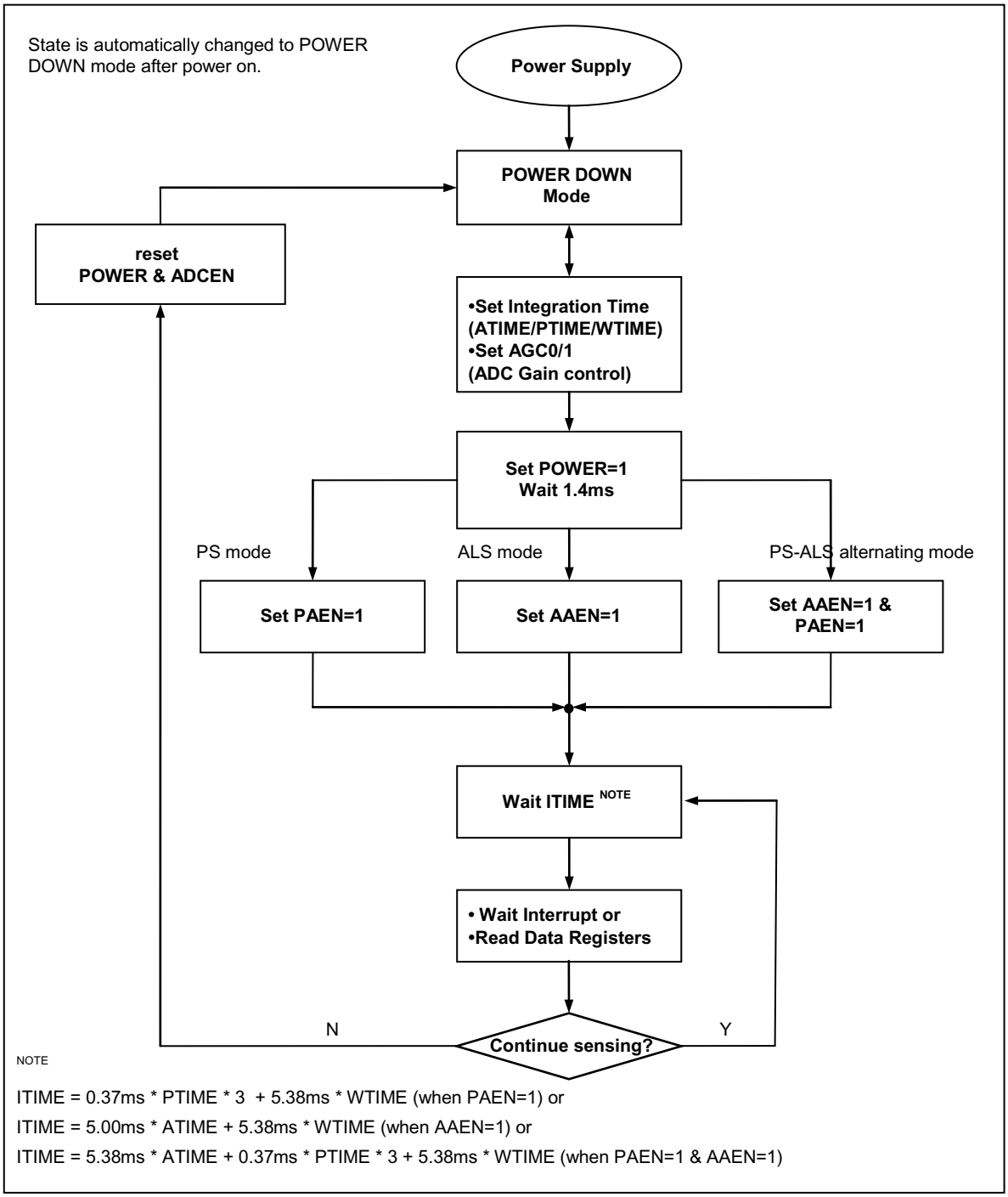

Figure 2-16 Operating Modes

3. APPENDIX

A. Brief Application Note

A capacitor should be located close to VDD pin of MC8201 to reduce power noise. The pull up resistors of two line serial bus are recommended to be around 10K ohm, especially a pull up registor for INT connected to host controller must be 100Kohm.

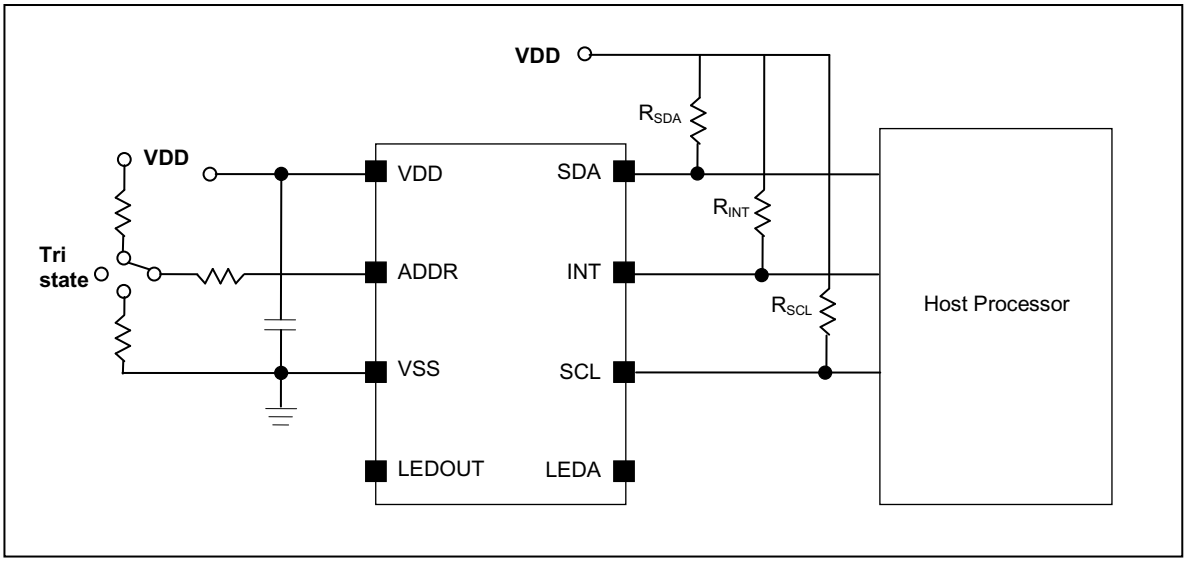

Figure 3-1 Hardware pin connection diagram

B. Notice

The below explains matters to be attended to when customer develops a program for MC8201.

1) Operation voltage 2.4 to 3.6V

2) Set SLAVE address (Determined by ADDR pin condition during power-up)
Input Low : 0x5C(1011100) => In Master IIC situation when writing and its value is 0xB 8 and when reading , its value is 0xB9
Input High : 0x23(0100011) => In Master IIC situation when writing, value is 0x46 and when reading, value is 0x47
Floating : 0x5C(1011100) => In Master IIC situation when writing, value is 0xB8 and when reaing, value is 0xB9

3) IIC speed is the standard, about 100kHz.
When writing IIC Multi bytes (Single byte read and write rarely is used)

- Multi bytes Writing :
START(M)+SlaveAddress_W(0xB8,M)+ACK(S)+REG_ADDR(0xxx,M)+ACK(S)+WRITE_BYTE0+ACK(S)…+STOP(M)

For example) When ADDR pin is low, you want to write 0x33 in CONTROL (address 00_H) Register. You should follow the below sequence.

START+0xB8+ACK+0x00+ACK+0x33+ACK+STOP

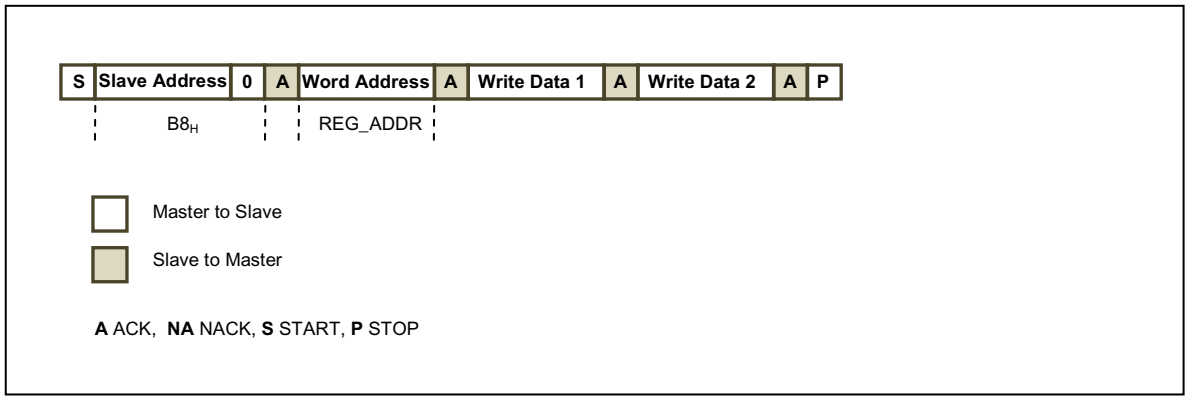

Figure 3-2 I2C write example

When reading IIC Multi bytes

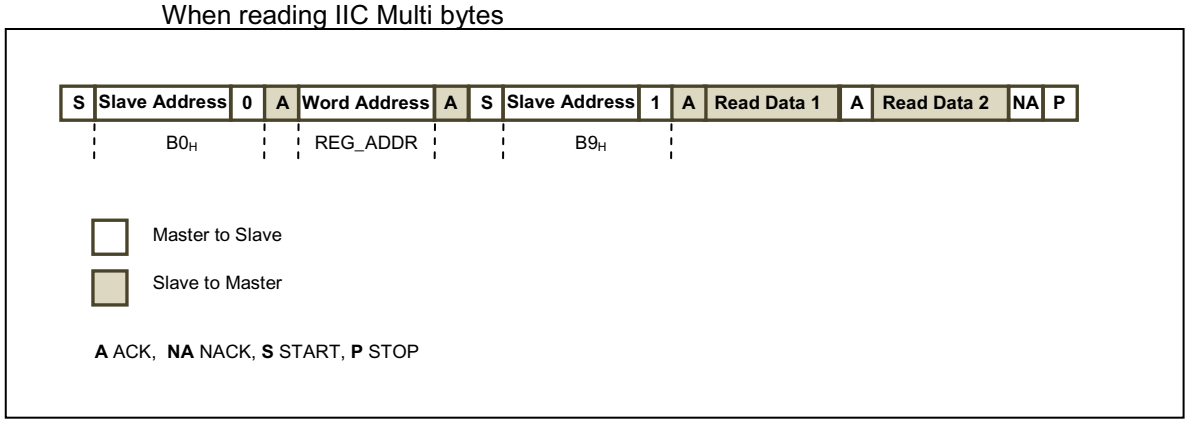

Figure 3-3 I2C read example

- Multi bytes reading:

  START(M)+SlaveAddress_W(0xB8,M)+ACK(S)+REG_ADDR(0xxx,M)+ACK(S)+START +

  SlaveAddress_R(0xB9,M)+ACK(S)+READ_BYTE0(S)+ACK(M)…+NACK+STOP(M)

  For example) When ADDR pin is low, you want to read values of ADATAL and ADATAH (address $0E_H$~$0F_H$) register. You should follow the below sequence.

  START+0xB8+ACK+0x0E+ACK+START+0xB9+ACK+??+ACK+…??+NACK+STOP

- After sending IIC Read/Write Command, delay time needs about 2msec for protocol transferring and MC8201 writing time)