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MC92600UM/D
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REV 2

MC92600

Quad 1.25 Gbaud SERDES

User's Manual

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About This Book

The primary objective of this reference manual is to describe the functionality of the MC92600 for software and hardware developers.

Information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

Audience

It is assumed that the reader has the appropriate general knowledge regarding the design and layout requirements for high speed (Gbps) digital signaling and understanding of the basic principles of Ethernet and Fibre Channel communications protocols to use the information in this manual.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Introduction," gives an overview of the device features and shows a block diagram of the major functional blocks of the part.
- Chapter 2, "Transmitter," describes the MC92600 transmitter, its interfaces and operational options.
- Chapter 3, "Receiver," gives a description of the receiver.
- Chapter 4, "System Design Considerations," describes the system considerations for the MC92600, including clock configuration, device startup and initialization, and proper use of the configuration control signals.
- Chapter 5, "Test Features," covers the system accessible test modes.
- Chapter 6, "Electrical Specifications and Characteristics," describes the DC and AC electrical characteristics.
- Chapter 7, "Package Description," provides the package parameters and mechanical dimensions and signal pin to ball mapping tables for the MC92600 device.
- Appendix A, "Ordering Information," provides the Motorola part numbering nomenclature for the MC92600 transceiver.

- Appendix B, “8B/10B Coding Scheme,” provides tables of the fibre channel-specific 8B/10B encoding and decoding is based on the ANSI FC-1 fibre channel standard.
- “Glossary of Terms and Abbreviations” contains an alphabetical list of terms, phrases, and abbreviations used in this book.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

General Information

The following documentation, published by Morgan-Kaufmann Publishers, 340 Pine Street, Sixth Floor, San Francisco, CA, provides useful information about the PowerPC architecture and computer architecture in general:

- *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition, by International Business Machines, Inc.

  For updates to the specification, see http://www.austin.ibm.com/tech/ppc-chg.html.
- *Computer Architecture: A Quantitative Approach*, Second Edition, by John L. Hennessy and David A. Patterson
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, David A. Patterson and John L. Hennessy

Related Documentation

Motorola documentation is available from the sources listed on the back cover of this manual; the document order numbers are included in parentheses for ease in ordering:

- Reference manuals—These books provide details about individual device implementations. The *MC92600 QUAD SERDES Evaluation Kit Manual* (MC92600EVK/D) describes how to use the design verification board and should be read in conjunction with this manual, the *MC92600 Quad 1.25 Gbaud SERDES User’s Manual* (MC92600UM/D).
- Addenda/errata to reference manuals—Because some devices have follow-on parts an addendum is provided that describes the additional features and functionality changes. These addenda are intended for use with the corresponding reference’s manuals.
- Hardware specifications—Hardware specifications provide specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations. This manual contains all the hardware specifications for the MC92600.

- Application notes—These short documents address specific design issues useful to programmers and engineers working with Motorola processors.
- White Paper-These documents provide detail on a specific design platform and are useful to programmers and engineers working on a specific product. *MC92610 3.125 Gbaud Reference Design Platform* (BR1570/D) describes the technical design process used in developing a high-speed backplane reference design.
- Additional literature is published as new processors become available. For a current list of documentation, refer to http://www.motorola.com/semiconductors.

Conventions

This document uses the following notational conventions:

	Book titles in text are set in italics
	Internal signals are set in italics, for example, *loop_back_data*
0x	Prefix to denote hexadecimal number
0b	Prefix to denote binary number
x	In some contexts, such as signal encodings, an un-italicized x indicates a don’t care.
x	An italicized *x* indicates an alphanumeric variable.
n	An italicized *n* indicates an numeric variable.

Signals

A bar over a signal name indicate that the signal is active low—for example, $\overline{\text{XMIT\_A\_IDLE}}$ and $\overline{\text{XMIT\_B\_IDLE}}$. Active low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as XMIT_EQ_EN and DROP_SYNC are referred to as asserted when they are high and negated when they are low.

Chapter 1
Introduction

The purpose of this user's manual is to explain the functionality of the MC92600 Quad 1.25 Gbaud SERDES transceiver and enables its use by software and hardware developers. The audience for this publication, therefore, consists of hardware designers and application programmers who are building data path switches and high-speed backplane intercommunication applications.

1.1 Overview

The MC92600 is a high-speed, full-duplex, serial data interface that can be used to transmit or receive data between chips across a board, through a backplane, or through cabling. The MC92600 has four transceivers each transmits and receives coded data at a rate of 1.0 gigabit per second (Gbps) through each of the four 1.25 gigabaud links. The MC92600's rich feature set makes it easily adaptable to many applications.

The MC92600 is carefully designed for low-power consumption. Its 0.25 micron CMOS implementation nominally consumes 780mW with all links operating at full speed.

1.2 Features

The following are the features of the MC92600:

- Four full-duplex differential data links.
- Each transceiver can operate at 1.25 Gbaud or 0.625 Gbaud.
- Low power, approximately 800mW under typical conditions, while operating all transceivers at full speed.
- Internal 8B/10B encoder/decoder is accessed through the byte interface or is bypassed in 10-bit interface mode.
- Single and double data rate interfaces.
- Received data may be aligned to the recovered clock or to the reference clock.
- Drives 50 or 75 ohm media (100 or 150 ohm differential) for lengths of up to 1.5 meters board/backplane, or 10 meters of coax.

- Link-to-link synchronization supports aligned word transfers. Tolerates ±40 bit-times of link-to-link media delay skew.
- Selectable transmitter/receiver byte alignment modes enable unaligned transfers or aligned transfers with automatic realignment.
- Repeater mode configures the MC92600 into a 4-link receive-transmit repeater.
- Tolerates frequency offset in excess of ±250ppm.
- On-chip receiver link termination.
- Receiver link inputs “hot swap” compatible.
- On-chip 50 ohm series source termination of TTL parallel outputs.
- Built-in self test for production test and on-board diagnostics.

1.3 Block Diagram

The MC92600 is a highly integrated device containing all of the logic needed to facilitate the application and test of a high-speed serial interface. No external components, other than the normal power supply decoupling network are required.

A block diagram of the MC92600 device is shown in Figure 1-1.

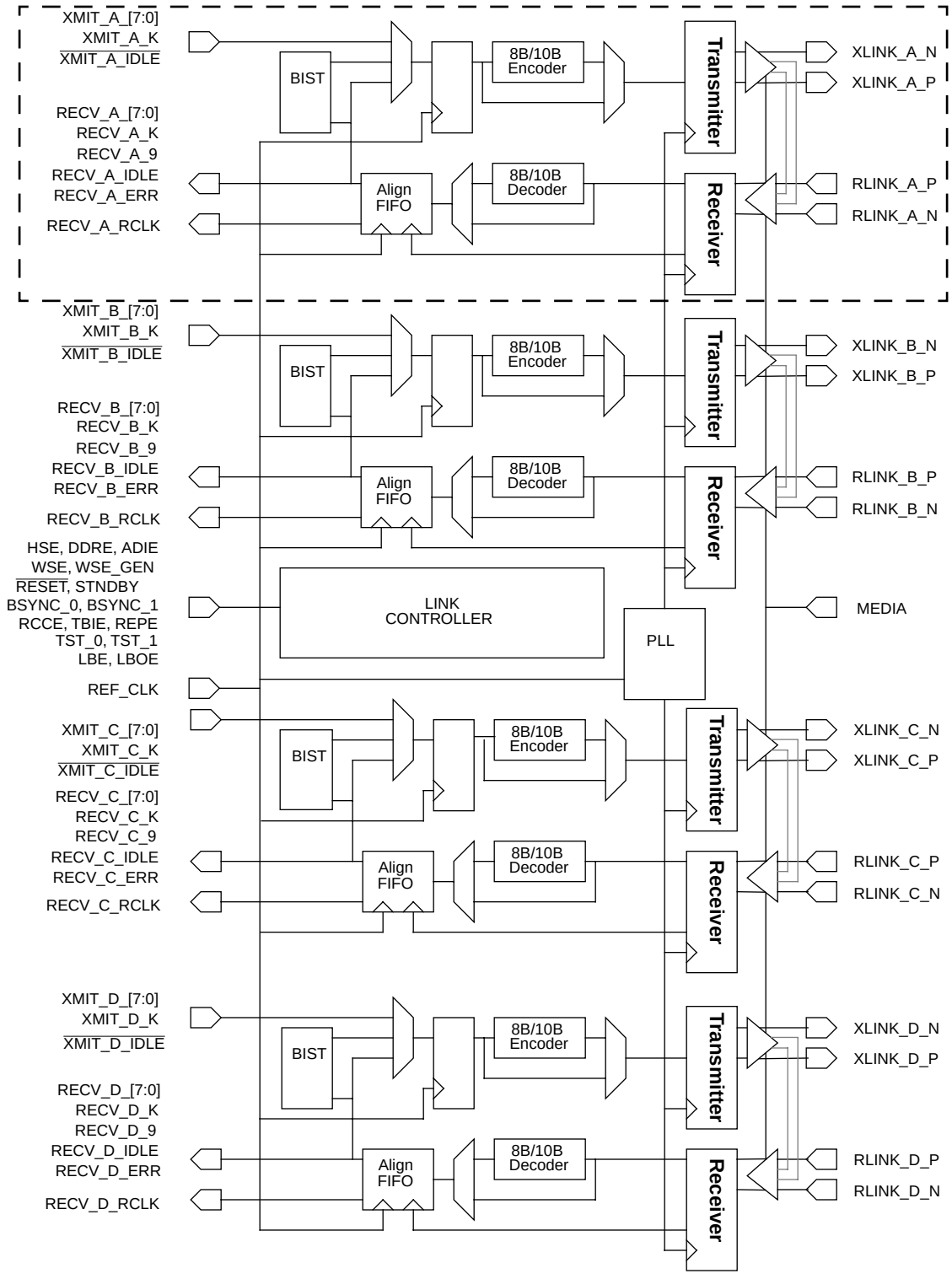


Figure 1-1. MC92600 Block Diagram

1.4 References

This section contains the indexed references in the document.

[1] *Fibre Channel, Gigabit Communications and I/O for Computer Networks*, Benner, 1996.

[2] *Byte Oriented DC Balanced 8B/10B Partitioned Block Transmission Code*, U.S. Patent #4,486,739, Dec. 4, 1984.

1.5 Revision History

Table 1-1 contains a brief description of the technical updates made to this document.

Table 1-1. Revision History Table

Document Revision	Substantive Changes
Rev 1	First release of the MC92600 User's Manual
Rev 2	Second release of the MC92600 User's Manual with minor edits.

Chapter 2
Transmitter

This chapter describes the MC92600 transmitter, and has five sections:

- Section 2.1, “Transmitter Block Diagram”
- Section 2.2, “Transmitter Interface Signals”
- Section 2.3, “Transmission Modes”
- Section 2.4, “Types of Transmission Data”
- Section 2.5, “Device Operations”

The transmitter takes the data byte presented at its data input, creates a transmission character using its 8B/10B encoder (if not in 10-bit interface mode), and serially transmits the character out of the differential link output pads. A detailed explanation of the 8B/10B coding scheme is offered in Appendix B, “8B/10B Coding Scheme.”

2.1 Transmitter Block Diagram

A block diagram of the MC92600 transmitter is shown in Figure 2-1.

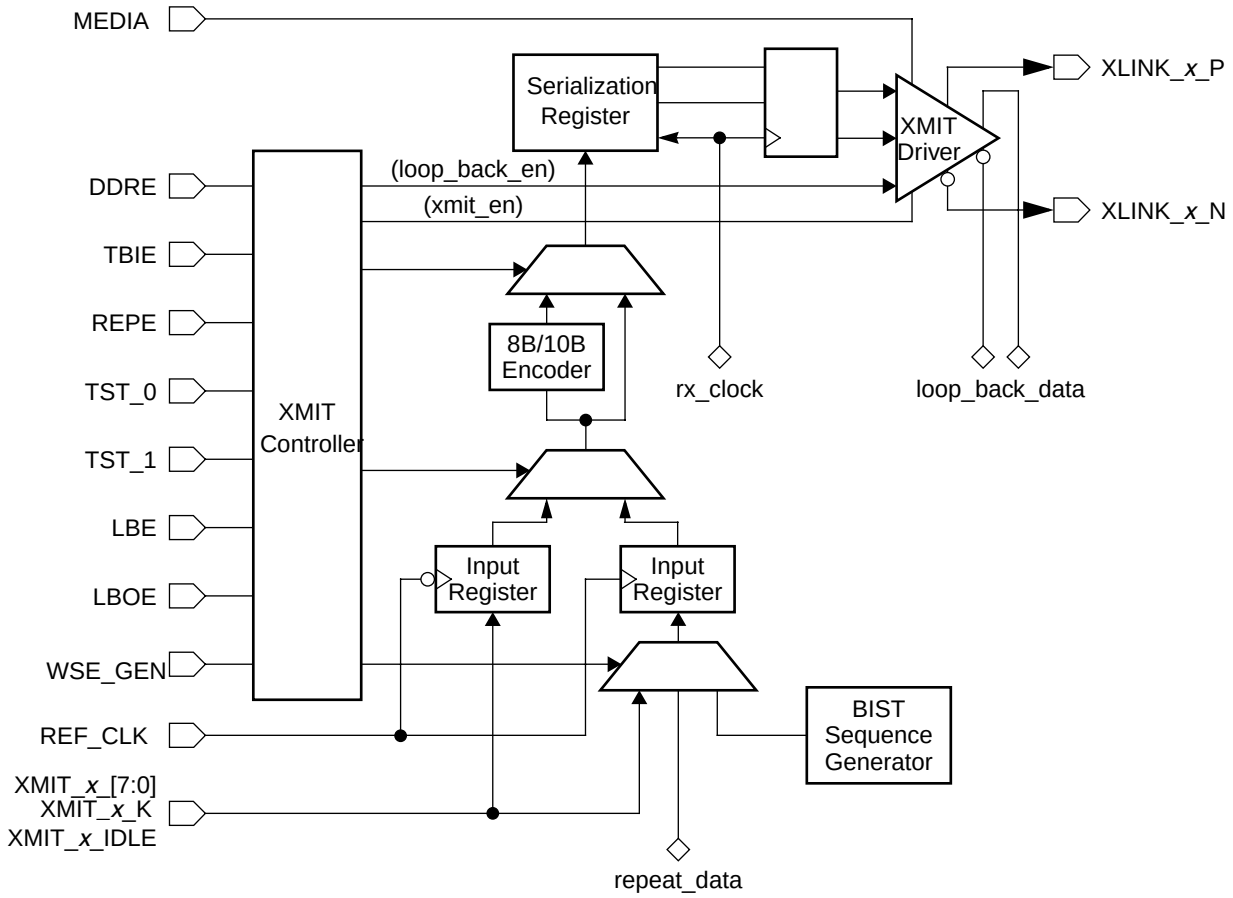


Figure 2-1. MC92600 Transmitter Block Diagram

2.2 Transmitter Interface Signals

This section describes the interface signals of the MC92600 transmitters. Each signal is described, including its name, description, function, direction, and active state in Table 2-1. The table's signal names use the letter "*x*" as a place holder for links "A" through "D". Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 2-1. MC92600 Transmitter Interface Signals

Signal Name	Description	Function	Direction	Active State
XMIT_*x*_7 through XMIT_*x*_0	Transmit byte	Uncoded data/control byte to transmit. The least significant 8 bits of coded data to transmit in TBI mode.	Input	—
XMIT_*x*_K	Special data indicator	Indicates that transmit byte is a special control byte. Must be decoded with $\overline{\text{XMIT\_}x\text{\_IDLE}}$ and WSE_GEN to determine action, see Table 2-2. Coded transmit data bit 8 in TBI mode. This signal also affects receiver operation. See Section 3.2.	Input	High
$\overline{\text{XMIT\_}x\text{\_IDLE}}$	Transmit idle character bar	Transmit an idle character. Must be decoded with XMIT_*x*_K and WSE_GEN to determine action, see Table 2-2. Coded transmit data bit 9 in TBI mode.	Input	Low
WSE_GEN	Word synchronization event generate	Transmit a disparity-style word synchronization event. Must be decoded with $\overline{\text{XMIT\_}x\text{\_IDLE}}$ and XMIT_*x*_K to determine action, see Table 2-2. This signal also affects receiver operation. See Section 3.2.	Input	High
LBE	Loop back enable	Activate digital loopback path, such that data transmitted is looped back to its receiver.	Input	High
LBOE	Loop back output enable	Indicates that link outputs remains active when LBE is asserted. When LBOE is low, link outputs are disabled when LBE is asserted.	Input	High
TBIE	10-bit interface enable	Indicates that coded 10-bit data is at inputs and to bypass internal 8B/10B coding.	Input	High
REPE	Repeater mode enable	When enabled, the transmitter obtains transmit data from the receiver.	Input	High
HSE	Half speed enable	When enabled, link is operated at half-speed. Both data and link interfaces run at half speed.	Input	High
DDRE	Double data rate enable	Indicates that the data interfaces are running at double data rate (data is sampled on the rising and falling edges of reference clock).	Input	High
REF_CLK	Reference clock	System reference clock to which the transmit interfaces are timed. Frequency requirement is dependent on HSE and DDRE settings. See Section 3.6 and Table 3.6 for configuration options.	Input	—

Table 2-1. MC92600 Transmitter Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
MEDIA	Media impedance select	Indicates the impedance of the transmission media. Low indicates 50Ω and high indicates 75Ω.	Input	—
XLINK_*x*_N/ XLINK_*x*_P	Link serial transmit data	Differential serial transmit data output pads.	Output	—
Internal Signals				
rx_clock	High speed transceiver clock	Internal, differential high-speed clock used to transmit and receive link data.	Input	—
repeat_data	Received repeat data	Repeater mode, received data to retransmit.	Input	—
loop_back_data	Loop back data	Differential loop back transmit data.	Output	—

2.3 Transmission Modes

MC92600 accepts two transmission modes: double data rate mode and repeater mode.

2.3.1 Double Data Rate Mode

Double data rate (DDR) mode enables sampling and storage of the data inputs to the transmitter on the rising and falling edges of REF_CLK. Data is placed in the transmit data input register. DDR mode is used to lower reference clock frequency while maintaining throughput, reducing board design complications. Table 4-1, "Legal Reference Clock Frequency Ranges" shows legal reference clock frequencies for all modes of operation. DDR mode is enabled by asserting DDRE.

2.3.2 Repeater Mode

Repeater mode configures the MC92600 into a 4-link receive-transmit repeater so that data can enter serially and exit serially. In this mode, the data to transmit is obtained from its receiver (transmitter A gets receiver A's data, transmitter B gets receiver B's data, and so on). The transmit input signals, XMIT_*x*_7 through XMIT_*x*_0, XMIT_*x*_K, and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ are ignored. Repeater mode is enabled by setting REPE high.

In repeater mode transmit data is sampled and stored in the transmit data input register on the rising edge of the reference clock (REF_CLK). See Section 3.5.4.5, "Repeater Mode" for more information on repeater mode.

NOTE

When using repeater mode ground all parallel inputs because input I/Os do not have internal pulldowns.

2.4 Types of Transmission Data

The MC92600 can handle both coded and uncoded data.

2.4.1 Transmitting Uncoded Data

Uncoded data is presented in 8-bit bytes to the transmit data input register through the XMIT_*x*_7 through XMIT_*x*_0 signals. The uncoded data is coded into 10-bit transmission characters using an on-chip 8B/10B encoder. The 8B/10B coding ensures DC balance across the link and sufficient transition density to facilitate reliable data recovery. The XMIT_*x*_7 through XMIT_*x*_0 signals are interpreted as data when the XMIT_*x*_K signal is low.

The 8B/10B code includes special control codes. Special control codes may be transmitted by setting the XMIT_*x*_K high, $\overline{\text{XMIT\_}x\text{\_IDLE}}$ high, and WSE_GEN low as indicated in Table 2-2. The transmit byte is assumed to be a control code in this state. The transmitter generates an idle character (K28.5) when XMIT_*x*_K is high, $\overline{\text{XMIT\_}x\text{\_IDLE}}$ is low, and WSE_GEN is low as indicated in Table 2-2. An idle character of proper running disparity is generated when this state is asserted; the state on the XMIT_*x*_7 through XMIT_*x*_0 signals is ignored. This eases generation of idle characters needed for byte and word synchronization and allows the link to maintain alignment when transmission of data is not needed.

When using the device in a system where word alignment is required (see Section 3.5.2, “8B/10B Decoder Operation”), it may be desirable to generate disparity-style word synchronization events. This is especially important where compatibility with older transceivers is required. A disparity style word synchronization event is generated by setting WSE_GEN high and XMIT_*x*_K high for each transmitter for which word synchronization event generation is desired. The transmitter generates one of two unique 16-character idle (K28.5) sequences depending on the current running disparity:

I+, I+, I-, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-

or

I-, I-, I+, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+

where I+ stands for idle of positive disparity, and I- stands for idle of negative disparity.

Table 2-2. Transmitter Control States

WSE_GEN	$\overline{\text{XMIT\_}x\text{\_IDLE}}$	XMIT_*x*_K	Description
Low	Don’t care	Low	Transmit data present on XMIT_*x*_7–0 inputs.
High	Don’t care	Low (on all four transmitters)	Transmit data present on XMIT_*x*_7–0 inputs and force invalidation of receivers’ current byte and word alignment.
Low	Low	High	Transmit idle (K28.5), ignore XMIT_*x*_7–0 inputs.

Table 2-2. Transmitter Control States

WSE_GEN	$\overline{\text{XMIT\_}x\text{\_IDLE}}$	XMIT_*x*_K	Description
Low	High	High	Transmit control present on XMIT_*x*_7–0 inputs.
High	don't care	High	Transmit disparity-style word synchronization event, ignore XMIT_*x*_7–0 inputs.

The transmitter inputs, XMIT_*x*_7–XMIT_*x*_0, XMIT_*x*_K and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ are ignored for the next 15 byte-times while the sequence is transmitted.

NOTE

The transmitter control signals WSE_GEN and XMIT_*x*_K also affect the receiver. When WSE_GEN is high and XMIT_*x*_K is low on all four links, the receiver invalidates its current byte alignment and word synchronization. See Section 3.3.2.1, "Word Synchronization Method" for more information on this function.

2.4.2 Transmitting Coded Data

10-bit coded data may be transmitted, bypassing the internal 8B/10B encoder. 10-bit interface (TBI) mode is enabled by asserting TBIE. In this mode, the ten bits of data to transmit are presented on the XMIT_*x*_7–XMIT_*x*_0 inputs, and bits 8 and 9 on the XMIT_*x*_K and $\overline{\text{XMIT\_}x\text{\_IDLE}}$ inputs, respectively.

Special care must be taken when using TBI mode. The 10-bit data must exhibit the same properties as 8B/10B coded data. DC balance must be maintained and there must be sufficient transition density to ensure reliable data recovery at the receiver. The receiver requires that the K28.5 idle character be periodically transmitted to enable byte and word synchronization. This 10-bit pattern ('0011111010' or '1100000101', ordered from bit 0 through 9) is used for alignment and link-to-link synchronization when operating in any of the byte or word synchronization modes. The pattern of idles and data required to achieve byte or word synchronization depends on the configuration of the receiver, see Section 3.3.1, "Byte Alignment." The appropriate sequence must be applied through the 10-bit interface. The automated facilities to generate idles and word-synchronization events are disabled in TBI mode.

The WSE_GEN input does not cause the generation of word synchronization events in TBI mode. However, WSE_GEN does work in conjunction with XMIT_*x*_K to invalidate receiver byte alignment and word synchronization as described in the previous section.

2.5 Device Operations

The MC92600 transmitter is comprised of several components whose operations are described in the following sections.

2.5.1 8B/10B Encoder Operation

The 8B/10B encoder transforms 8-bit data/control characters from the input register into 10-bit transmission characters. The fibre channel 8B/10B coding standard is followed [1,2]. Running disparity is maintained and the appropriate transmission characters are produced, maintaining DC balance and sufficient transition density to allow reliable data recovery at the receiver. See Appendix B, “8B/10B Coding Scheme” for a detailed description of 8B/10B coding.

The inputs to the 8B/10B encoder are the data byte (XMIT_*x*_7 through XMIT_*x*_0), special code signal (XMIT_*x*_K) and transmit idle signal ($\overline{\text{XMIT\_}x\text{\_IDLE}}$).

Data and legal control bytes are coded according to the 8B/10B method. Illegal control bytes produce unpredictable transmission characters, leading to disparity and coding errors, ultimately reducing link reliability.

The 8B/10B encoder produces an idle character of proper running disparity when $\overline{\text{XMIT\_}x\text{\_IDLE}}$ is low, XMIT_*x*_K is high, and WSE_GEN is low, as indicated in Table 2-2, "Transmitter Control States.” The 8B/10B encoder is bypassed in TBI mode.

2.5.2 Transmit Driver Operation

The transmit driver drives transmission characters serially across the link. Two bits per transceiver clock, one each on the rising and falling transceiver clock (rx_clock) edges, are transmitted differentially from the XLINK_*x*_P (positive) and XLINK_*x*_N (negative) outputs. The rx_clock runs at 625 MHz for 1 Gbps (1.25 gigabaud) operation and at 312.5 MHz for 500 Mbps (625 megabaud) operation.

The transmit driver is a controlled impedance driver. The impedance of the driver is programmable to 50Ω or 75Ω through the MEDIA signal. Drive impedance is 50Ω when MEDIA is low and 75Ω when MEDIA is high.

A special loop-back mode is supported for test. Asserting the LBE signal high enables loop-back mode causing the state being driven on XLINK_*x*_P/XLINK_*x*_N to be looped back to the input amplifier of the link’s receiver. Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the XLINK_*x*_P/XLINK_*x*_N output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally. When in loop-back mode, the LBOE signal controls the action of the XLINK_*x*_P/XLINK_*x*_N output signals. When

LBOE is low, the transmit driver holds the XLINK_*x*_P/XLINK_*x*_N output signals high and low, respectively. When LBOE is high, the XLINK_*x*_P/XLINK_*x*_N output signals continue to operate normally. See Chapter 5, “Test Features” for more information on test modes.

NOTE

For normal transmitter operation (TST_0, TST_1 and LBE all low) LBOE *must also be low* or the receivers will not function. See Section 5.7, “Board Level Manufacturing Test Mode” for more information.

The electrical specifications of the transmitter’s driver are found in Table 6-3, "DC Electrical Specifications for 3.3V Power Supply” or in Table 6-4, "DC Electrical Specifications for 2.5V Power Supply.”

2.5.3 Transmit Data Input Register Operation

The transmit data input register accepts data to be transmitted and synchronizes it to the internal clock domain. Transmit data is normally uncoded 8-bit data, however, transmission of coded 10-bit data is supported in 10-bit interface (TBI) mode. TBI mode is enabled by asserting TBIE high.

Transmit data is sampled and stored in the input register on the rising edge of the reference clock (REF_CLK). The transmitter supports double data rate (DDR) mode where data is sampled and stored on both the rising and falling edges of REF_CLK. DDR mode is enabled by asserting DDRE high.

Chapter 3
Receiver

This section describes the MC92600 receiver, its interfaces, and operation. This chapter has the following sections:

- Section 3.1, “Receiver Block Diagram”
- Section 3.2, “Receiver Interface Signals”
- Section 3.3, “Alignment Modes”
- Section 3.4, “Receiver Clock Timing Modes”
- Section 3.5, “Device Operations”
- Section 3.6, “Receiver Interface Error Codes”
- Section 3.6, “Receiver Interface Error Codes”

The receiver is a dual-rate receiver, operating at 1 Gbps or 500 Mbps (1.25 or 0.625 Gbaud) rates. The receiver is based upon a 16X oversampled transition tracking loop data recovery method. A block diagram of the MC92600 receiver is found in Figure 3-1.

3.1 Receiver Block Diagram

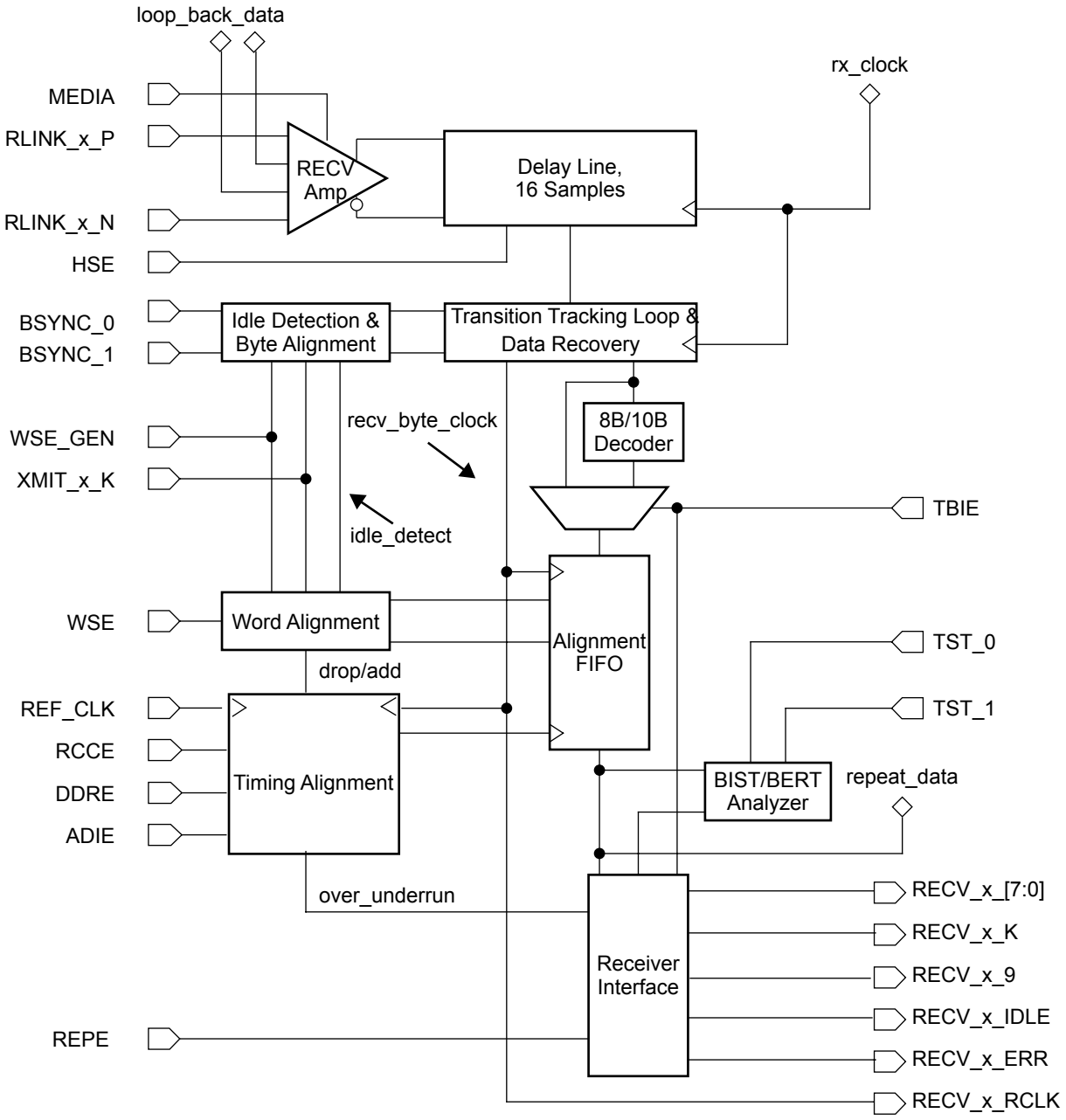


Figure 3-1. Receiver Block Diagram

3.2 Receiver Interface Signals

This section describes the interface signals of the MC92600 receiver. Each signal is described, including its name, function, direction and active state in Table 3-1. The table's signal names use the letter "*x*" as a place holder for links "A" through "D". Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 3-1. MC92600 Receiver Interface Signals

Signal Name	Description	Function	Direction	Active State
RECV_*x*_7 through RECV_*x*_0	Received byte (bits 7–0)	Received and decoded data/control byte. The least significant 8 bits of received coded data in TBI mode.	Output	—
RECV_*x*_K	Special data indicator/ Received bit 8	Indicates that received byte is a special control byte. Received coded bit 8 in TBI mode. Errors are coded using this signal. See Section 3.6 for error codes.	Output	—
RECV_*x*_9	Received bit 9	Received coded bit 9 in TBI mode. Unused in 8-bit mode.	Output	—
RECV_*x*_IDLE	Receiver idle detect	Indicates that the receiver detected an idle character (operates in Byte and TBI modes). Errors are coded using this signal. See Section 3.6 for error codes.	Output	—
RECV_*x*_ERR	Receiver error	Indicates that the receiver detected an error. RECV_*x*_IDLE and RECV_*x*_K must be decoded to determine error condition. See Section 3.6 for error codes.	Output	—
RECV_*x*_RCLK	Receiver recovered Byte clock	Internally generated clock used for reading receiver outputs when RCCE is asserted.	Output	—
WSE_GEN	Word synchronization Event generate	This signal when asserted coincident with XMIT_*x*_K set low on all four links invalidates current byte alignment and word synchronization. This signal also affects transmitter operation. See Section 2.2.	Input	—
XMIT_*x*_K	Special data indicator	This signal when set low on all four links coincident with WSE_GEN asserted invalidates current byte alignment and word synchronization. This signal also affects transmitter operation. See Section 2.2.	Input	—
TBIE	10-bit interface enable	Indicates that the receiver interface is in 10-bit mode and that the 8B/10B decoder is bypassed.	Input	High
HSE	half-speed enable	Indicates to operate link at half-speed. Both data and link interfaces run at half speed.	Input	High
WSE	Word synchronization enable	Indicates that all four receivers are being used in unison to receive synchronized data.	Input	High

Table 3-1. MC92600 Receiver Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
DDRE	Double data rate enable	Indicates that the data interfaces are running at double data rate (data is output on the rising and falling edges of clock.) Establishes DDR mode.	Input	High
BSYNC_0	Byte alignment mode	Defines the of word synchronization event method. See Section 3.3.2.	Input	High
BSYNC_1	Byte alignment mode	Indicates the type of byte alignment to employ in the receiver. See Section 3.3.1.	Input	—
RCCE	Recovered clock enable	Indicates that the output data is synchronized to its recovered byte clock. Otherwise output data is synchronized to the reference clock.	Input	High
ADIE	Add/delete idle enable	Indicates that the receiver is free to add/delete idle characters to/from the output data stream to maintain alignment.	Input	High
REPE	Repeater mode enable	When enabled, the transmitter obtains transmit data from the receiver.	Input	High
TST_0/ TST_1	Test mode	Indicates operating/test mode of the chip. See Chapter 5.	Input	—
REF_CLK	Reference clock	System reference clock to which the receiver interfaces may be timed. Provided frequency is dependent on HSE and DDRE settings.	Input	—
RLINK_*x*_N/ RLINK_*x*_P	Link serial receive data	Differential serial receive data input pads.	Input	—
Internal Signals				
rx_clock	High speed transceiver clock	Internal, differential high speed clock used to transmit and receive link data.	Input	—
loop_back_data	Loop back data	Differential loop back receive data.	Input	—
repeat_data	Received repeat data	Repeater mode, received data to re-transmit.	Output	—

3.3 Alignment Modes

The MC92600 supports two types of alignment, byte alignment and word alignment. Byte alignment deals with the MC92600 being configured as four separate receivers. Word alignment deals with four receivers being configured to work together.

3.3.1 Byte Alignment

The receiver supports three modes of byte alignment as defined by the BSYNC_0, BSYNC_1 and WSE signals. As described in Table 3-2, the three types of byte alignment modes: byte alignment with realignment, byte alignment with idle realignment and disparity-based word alignment, and non-aligned data.

Table 3-2. Byte Alignment Modes

Byte Alignment Mode	BSYNC_0	BSYNC_1	WSE
Byte aligned with realignment	High	Low	Low
Byte aligned with idle realignment and disparity word alignment, see Section 3.3.2.1.	High	Low	High
Non-aligned	High	High	Low

NOTE

In byte alignment modes and not word synchronization (WSE = low), BSYNC_0 must be high.

3.3.1.1 Byte-Aligned with Realignment

At power-up, the receiver starts an alignment procedure, searching for the 10-bit pattern defined by the 8B/10B idle code. Synchronization logic checks for the distinct idle sequence, ‘0011111010’ and ‘1100000101’ (ordered bit 0 to bit 9), characteristic of the K28.5 idle pattern. The search is done on the 10-bit data in the receiver, and is therefore independent of TBI mode. Alignment requires a minimum of four, error-free, received idle characters to ensure proper alignment and lock. Non-idle characters may be interspersed with the idle characters. The disparity of the idle characters is not important to alignment and can be positive, negative or any combination. The receiver begins to forward received characters once locked on an alignment. However, if word synchronization is enabled (WSE = high), received characters are not forwarded to the receiver interface until the first, valid, non-idle character is received. Alignment remains locked until one of three events occurs that indicate loss of alignment:

- Alignment is lost when a misaligned idle sequence is detected. A misaligned idle sequence is defined as four idle characters with an alignment different from the current alignment. Non-idle characters may be dispersed between the four misaligned idles, however, a properly aligned idle character breaks the sequence. Alignment is changed to the newly detected alignment without interrupting data flow through the receiver if in Byte Aligned Mode (WSE = low). However, if in Word Aligned Mode (WSE = high) word alignment is lost.
- Alignment is also lost when the number of received characters with 8B/10B coding errors outnumbers the non-error characters by four. Misalignment detection of this

type is not available in TBI mode. The receiver restarts its alignment procedure and halts data flow until alignment is achieved.

- Finally, the user may force loss of alignment by asserting WSE_GEN high and XMIT_*x*_K low on all four receivers simultaneously. The receiver restarts its alignment procedure and halts data flow until alignment is achieved.

When establishing byte alignment, or when data flow is halted due to misalignment, the receiver's RECV_*x*_ERR signal is asserted high and the "Not Byte Sync" error is reported as described in Section 3.6, "Receiver Interface Error Codes."

3.3.1.2 Byte-Aligned with Idle Realignment and Disparity Word Alignment

This alignment mode is the same as the one described in Section 3.3.1.1, "Byte-Aligned with Realignment." The difference in this alignment mode is related to the style of word synchronization. Word synchronization between receivers is accomplished by synchronizing the received characters to a unique word synchronization event in the incoming character stream. In this byte alignment mode, the word synchronization event is defined to be a disparity-based idle sequence as described in Section 2.4.1, "Transmitting Uncoded Data." See Section 3.3.2.1, "Word Synchronization Method," for more information on word synchronization.

3.3.1.3 Non-Aligned

In this mode no attempt is made to align the incoming data stream. The bits are simply accumulated into 10-bit characters and forwarded. This mode should be used only with 10-bit interface mode (TBIE = high) and with word synchronization disabled (WSE = low).

3.3.2 Word Alignment

The four receivers in the MC92600 can be used cooperatively to receive 32-bit aligned word transfers. Word alignment is enabled by setting the word synchronization enable input, WSE, high.

Word alignment, or word synchronization, is possible in both byte interface mode or in TBI mode. However, word synchronization is dependent on the detection of simultaneously transmitted word synchronization events that contain idle characters. Therefore, if operating in TBI mode, the idle character must be a supported member of the code set.

3.3.2.1 Word Synchronization Method

Word synchronization aligns characters in the receiver's alignment FIFO. Synchronization is accomplished by lining up word synchronization events detected by each of the receivers, such that all are coincident at the same stage of their FIFO.

A word synchronization event is defined differently depending on the state of the BSYNC_0 and BSYNC_1 signals. Table 3-3 shows the type of word synchronization event used.

Table 3-3. Word Synchronization Events

Word Synchronization Event	BSYNC_0	BSYNC_1
4 idle/1 non-idle	Low	don't care
Disparity-based idle sequence	High	Low

There are two types of word synchronization events: the 4/1 idle sequence and the disparity-based idle sequence.

- The 4/1 idle sequence is defined as four consecutive idle characters followed by a non-idle character.
- The disparity-based idle sequence is 16 consecutive idle characters with improper disparity on the second and fourth idle character in the sequence. The disparity-based idle sequence is described further in Section 2.4.1, "Transmitting Uncoded Data."

Word synchronization events must be generated at all concerned transmitters simultaneously in order for synchronization to be achieved. Word synchronization events must be received at all concerned receivers within 40 bit-times of each other.

Word synchronization events are used to establish a relationship between the received bytes in each of the receivers. The bytes of a word are matched and presented simultaneously at the receiver interface. Once synchronization is achieved, the receiver tolerates +/- 6 bit-times of drift between receivers. If drift exceeds +/- 6 bit-times, the receiver will continue to operate. However, the received bytes will no longer be synchronized properly because the receiver remains locked onto the initially established synchronization. Word synchronization remains locked until one of three events occurs that indicate loss of synchronization.

Word synchronization lock can be lost in three ways:

- When one or more of the receivers lose or change byte alignment. Byte alignment loss is described in Section 3.3.1.1, "Byte-Aligned with Realignment."
- When overrun/underrun is detected on one or more of the receivers but not on all simultaneously, see Section 3.4.2, "Reference Clock Timing Mode" for more about overrun/underrun.

- When explicitly invalidated by asserting WSE_GEN high and XMIT_*x*_K low on all four receivers.

When lock is lost, word synchronization must be re-established before data flow through the receiver resumes.

The receiver interface is disabled during initial word alignment. No data is produced at its outputs until word alignment is achieved and the first non-idle character is received. When establishing word alignment, or when word alignment is lost, the receiver's RECV_*x*_ERR signal is asserted high and the "Not Word Sync" error is reported as described in Section 3.6, "Receiver Interface Error Codes."

3.3.2.2 Word Synchronization Recommended Settings

Word alignment can only be used with certain operating modes and has limited application in others. Table 3-4 describes the relationship between modes and word synchronization.

Table 3-4. Word Synchronization Settings

Mode	Signals	Recommended State	Description
Word synchronization	WSE	High	Enables word synchronization.
Byte synchronization	BSYNC_0, BSYNC_1	Any mode except non-aligned	Word synchronization depends upon idle character detection. Byte alignment is required for idle detection.
Add/delete idle	ADIE	High	When enabled, allows the receiver to add/delete idle patterns to maintain word alignment. This is the recommended operating mode when the reference clock is being used to time the receiver interface (RCCE = Low) and there is a frequency offset between the transmitter and receiver. Idles are added or dropped to maintain word alignment.
10-bit interface	TBIE	don't care	When enabled, the idle character must be part of the TBI code set. When disabled, the idle is naturally supported by the 8B/10B codes.
Recovered clock	RCCE	don't care	Does not affect word synchronization.
Half-speed enable	HSE	don't care	Does not affect word synchronization.
Double data rate	DDRE	don't care	Does not affect word synchronization.

3.4 Receiver Clock Timing Modes

The receiver interface is timed to the recovered clock or to the reference clock depending on the state of the recovered clock enable, RCCE, signal. RCCE asserted enables timing relative to the recovered clock, and set low enables timing relative to the reference clock.

3.4.1 Recovered Clock Timing Mode

The recovered clock signal, RECV_*x*_RCLK, is generated by the receiver and, on average, runs at the reference clock frequency of the transmitter at the other end of the link. The recovered clock is not generated by a clock recovery PLL, but is generated by the receiver bit-accumulation and byte-alignment logic. The RECV_*x*_RCLK signal is asserted high, generating a rising edge, whenever a new byte (character) is accumulated and available.

To track a transmitter frequency that is offset from the receiver's reference clock frequency, the duty cycle and period of the recovered clock is modulated. The MC92600 is designed to tolerate up to ±250 ppm of frequency offset. For example: if the transmitter is running 100 ppm faster than the receiver, then a short cycle is generated approximately every 2,000 received bytes. The short cycle has a period equal to eight bit-times instead of the normal ten bit-times. This implies that logic using received data timed to the recovered clock must be able to operate with a period equal to eight bit-times (6.4 ns for 1.25 gigabaud). Each short cycle recovers two bit-times of offset. Generally, the number of received bytes (characters) between short cycles is equal to:

$(2 * 10^6) / (10 * N)$ bytes

where:

N is the frequency offset in ppm.

Alternately, if the transmitter is running 100 ppm slower than the receiver, then a long cycle is generated approximately every 2,000 received bytes. The long cycle has a period equal to twelve bit-times instead of ten bit-times. The above equation is also used to compute the period between long cycles.

Data is timed to the rising edge of the recovered clock signal except in double data rate mode where data is timed to the rising and falling edges of the recovered clock.

If the receivers are being operated in word synchronization mode (WSE = high), the data for all four receivers are timed relative to link A's recovered clock RECV_A_RCLK.

NOTE

Recovered clocks RECV_B_RCLK, RECV_C_RCLK, and RECV_D_RCLK are not aligned to the data in word synchronization mode and should not be used.

3.4.2 Reference Clock Timing Mode

Data is timed relative to the reference clock when RCCE is low. Synchronization between the recovered clock and the reference clock is handled by the receiver interface. Frequency offset between the transmitter's reference clock and the receiver's reference clock causes overrun/underrun situations. Overrun occurs when the transmitter is running faster than the receiver. Underrun occurs when the transmitter is running slower than the receiver.

In an overrun situation, a byte of data needs to be dropped to maintain synchronization between the clock domains. The receiver interface searches for an idle byte to drop when overrun is imminent. However, the idle is dropped only if add/delete idle (ADI) mode is enabled by setting ADIE high. When enabled, idle patterns are dropped to maintain synchronization. If sufficient idle patterns are not available to drop, receiver overrun may occur. When overrun occurs, the overrun/underrun error is reported as described in Section 3.6, “Receiver Interface Error Codes,” for one byte clock period. Overrun error is also reported if ADI mode is disabled and overrun occurs, even if idles are available to drop.

A sufficient number of idles must be transmitted to guard against overrun. The frequency of idles can be computed based upon the maximum frequency offset between transmitter and receiver in the system. The number of bytes (characters) that can be transmitted between idles is:

$(10^6 / N) - 1$ bytes

where:

N is the frequency offset in ppm.

In an underrun situation, a byte of data needs to be added to maintain synchronization between the clock domains. The receiver interface adds an idle byte when underrun is imminent. However, the idle is added only if add/delete idle (ADI) mode is enabled by asserting ADIE. If ADI mode is disabled and underrun occurs, the overrun/underrun error is reported as described in Section 3.6 for one byte clock period.

Data is timed to the rising edge of the reference clock signal except in double data rate mode where data is timed to the rising and falling edges of the reference clock.

3.5 Device Operations

The MC92600 receiver is comprised of several devices and operations that are described in the following sections.

3.5.1 Receiver Input Amplifier

The input amplifier connects directly to the link input pads RLINK_*x*_P and RLINK_*x*_N. It is a differential amplifier with an integrated analog multiplexer for loop-back testing. Link termination resistors are integrated with the amplifier. The termination resistance is programmable to be 100Ω differential or 150Ω differential through the MEDIA signal. Termination resistance is 100Ω when MEDIA is low and 150Ω when MEDIA is high.

The input amplifier facilitates a loop-back path for production and in-system testing. When the MC92600 is in loop-back mode (LBE is high), the input amplifier selects the loop-back differential input signals and ignores the state on the RLINK_*x*_P and RLINK_*x*_N signals.

This allows in-system loop-back BIST independent of the current input state. See Chapter 5 for more information on test modes.

The input amplifier's electrical specifications may be found in Table 6-3, "DC Electrical Specifications for 3.3V Power Supply" and in Table 6-4, "DC Electrical Specifications for 2.5V Power Supply."

3.5.2 8B/10B Decoder Operation

The 8B/10B decoder takes the 10-bit character from the transition tracking loop and decodes it according to the 8B/10B coding standard [1,2]. The decoder does two types of error checking. First it checks that all characters are a legal member of the 8B/10B coding space. The decoder also checks for running disparity errors. If the running disparity exceeds the limits set in the 8B/10B coding standard then a disparity error is generated. See Appendix B, "8B/10B Coding Scheme."

An illegal character or disparity error sets the RECV_*x*_ERR signal high, coincident with the received data for a 1-byte output period. The "Code Error" or "Disparity Error" is reported as described in Section 3.6, "Receiver Interface Error Codes." It is difficult to determine the exact byte that caused the disparity error, so it should not be associated with a particular received byte. It is rather a general indicator of the improper operation of the link. Its intended use is for the system to monitor link reliability.

The 8B/10B decoder is bypassed when operating in 10-bit interface mode (TBIE = high.)

3.5.3 Transition Tracking Loop and Data Recovery

The received differential data from the input amplifier is sent to the transition tracking loop for data recovery. The MC92600 uses an oversampled transition tracking loop method for data recovery. The differentially received data is sampled and processed digitally providing for low bit error rate (better than 10 -12) data recovery of a distorted bit stream.

The transition tracking loop is tolerant of frequency offset between the transmitter and receiver. The MC92600 reliably operates with ±250 ppm of frequency offset. The MC92600 is tolerant of frequency offset between the transmitter and receiver. The MC92600 reliably operates with +250 ppm of frequency offset. The device's transition tracking loop method is different than the typical PLL clock recovery method. Its receiver compensates for overrun and underrun caused by frequency offset by modulating the duty-cycle and period of the received byte clock.

Recovered data is accumulated into 10-bit characters. Characters are aligned to their original 10-bit boundaries if a byte alignment mode is enabled.

3.5.4 Receiver Interface Modes

The receiver interface facilitates transfer of received data to the system. It also provides information on the status of the link. Table 3-1, "MC92600 Receiver Interface Signals," describes each of the signals involved in receiver operation.

The receiver interface, through which received data is obtained, may be operated in byte mode or in 10-bit interface mode. Several timing mode options exist for the receiver interface. Each of the operating modes are described in the following sections.

- Section 3.5.4.1, “Byte Interface Mode”
- Section 3.5.4.2, “10-Bit Interface Mode”
- Section 3.5.4.3, “Double Data Rate Mode”
- Section 3.5.4.4, “Half-Speed Mode”
- Section 3.5.4.5, “Repeater Mode”

3.5.4.1 Byte Interface Mode

The receiver interface may be operated in byte mode or in 10-bit interface (TBI) mode. Received data is a byte (8 bits) of uncoded data when in byte mode. Byte interface mode is enabled by setting the TBIE signal low.

NOTE

Do not use non-aligned mode in byte interface mode. See Section 3.3.1, “Byte Alignment” for more information on byte alignment modes.

The internal 8B/10B decoder is used to decode data from the 10-bit character received. The received byte is on the RECV_*x*_7 through RECV_*x*_0 signals.

The RECV_*x*_K is asserted when the byte represents a special 8B/10B code, otherwise it is low, indicating that the byte is normal data.

The RECV_*x*_IDLE is asserted when the byte is the special 8B/10B idle (K28.5) code. This can be used by system logic for synchronization or data parsing. RECV_*x*_IDLE is set low when the byte is normal data or a non-idle special code. RECV_*x*_IDLE is asserted and RECV_*x*_K is set low to indicate that an underrun/overrun error occurred. See Section 3.6, “Receiver Interface Error Codes” for more information on error conditions.

The RECV_*x*_ERR is set low when the receiver is operating normally, and is asserted when received data contains an error or the receiver is in an error state. The state of the RECV_*x*_IDLE and RECV_*x*_K signals are decoded to determine the error condition. Table 3.6, "Receiver Interface Error Codes” describes the error codes and their meaning.

The receiver interface is timed to the recovered clock, RECV_*x*_RCLK, or to the reference clock, REF_CLK, depending on the state of the RCCE signal.

3.5.4.2 10-Bit Interface Mode

Received data is ten bits of coded data when in TBI mode. The internal 8B/10B decoder is not used, and it is assumed that decoding is done externally. 10-bit data is made up from the collection of signals— RECV_*x*_9, RECV_*x*_K, and RECV_*x*_7 through RECV_*x*_0 making up bits 9 through 0, respectively. 10-bit interface mode is enabled by setting the TBIE signal high.

The RECV_*x*_IDLE is asserted when the 10-bit character is the special 8B/10B idle (K28.5) code. This can be used by system logic for synchronization or data parsing. RECV_*x*_IDLE is set low when the data is normal data or a non-idle special code.

The RECV_*x*_ERR is set low when the receiver is operating normally, and is asserted when the receiver is in an error state. The state of the RECV_*x*_IDLE signal is decoded to determine the error condition. Table 3-6 describes the error codes and their meaning.

The receiver interface is timed to the recovered clock, RECV_*x*_RCLK, or to the reference clock, REF_CLK, depending on the state of the RCCE signal.

3.5.4.3 Double Data Rate Mode

Double data rate (DDR) mode, enabled when DDRE is asserted, allows the received data to be output on the rising *and* falling edges of a reference or recovered clock. DDR mode is used to lower reference clock frequency while maintaining throughput, reducing board design complications. It is important to note that in DDR mode the legal range of reference clock frequencies is reduced. Table 4-1, "Legal Reference Clock Frequency Ranges” shows legal reference clock frequencies for all modes of operation.

3.5.4.4 Half-Speed Mode

Half-speed (HS) mode, enabled when HSE is asserted, operates the receiver in its lower speed range. In HS mode, the link speed is 500 Mbps (625 Mbaud.) The receiver interface operates at half speed as well, in pace with received data.

3.5.4.5 Repeater Mode

Repeater mode configures the MC92600 into a 4-link receive-transmit repeater. In this mode, received data is forwarded to the transmitter for re-transmission. Link A’s receiver forwards to link A’s transmitter, link B’s receiver to link B’s transmitter, and so on. The receiver’s data outputs and status signals reflect the received data and the current status of the receiver. See Section 2.3.2, “Repeater Mode” for more information on repeater mode.

3.6 Receiver Interface Error Codes

The receiver's status and data error conditions are coded on the RECV_*x*_ERR, RECV_*x*_IDLE and RECV_*x*_K signals. When RECV_*x*_ERR is low, the receiver is operating normally and no error conditions exist (with exception of underrun/overrun error in byte mode.) When RECV_*x*_ERR is high, the data on the receiver's output is questionable due to an error condition or lack of synchronization. Initially, RECV_*x*_ERR is asserted indicating that the receiver is in one of its start-up phases. Table 3-5 describes the error conditions and their signal coding for byte interface mode.

Table 3-5. Receiver Interface Error Codes (Byte Interface)

RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE	Priority	Description
Low	Low	Low	8	Normal operation, valid data character received.
Low	Low	High	3	Overrun/Underrun—The receiver interface synchronization logic detected an overrun/underrun condition. Data may be dropped or repeated.
Low	High	Low	7	Normal operation, valid control character received.
Low	High	High	6	Normal operation, valid idle (K28.5) character received.
High	Low	Low	4	Code Error—The 8B/10B decoder detected an illegal character.
High	Low	High	5	Disparity Error—The 8B/10B decoder detected a disparity error.
High	High	Low	1	Not byte Sync—The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	High	2	Not Word Sync—The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

Table 3-6 describes the error conditions and their signal coding for 10-bit interface mode.

Table 3-6. Receiver Interface Error Codes (10-Bit Interface)

RECV_*x*_ERR	RECV_*x*_IDLE	Priority	Description
Low	Low	4	Normal operation, non-idle character received.
Low	High	3	Normal operation, idle (K28.5) character received.
High	Low	1	Not byte/word sync—The receiver is in start-up or has lost byte or word alignment and is searching for alignment.
High	High	2	Overrun/Underrun—The receiver interface synchronization logic detected and overrun/underrun condition. Data may be dropped or repeated.

Chapter 4
System Design Considerations

This chapter describes the system considerations of the MC92600 Quad DDR, including device-startup, initialization, and the proper use of the standby and repeater modes.

4.1 Reference Clock Configuration

The legal ranges of reference clock frequencies vary depending on the operating modes selected. Table 4-1 shows the ranges allowed for each mode of operation.

Table 4-1. Legal Reference Clock Frequency Ranges

DDRE	HSE	Reference Frequency Min (MHz)	Reference Frequency Max (MHz)	Link Transfer Rate (Gigabaud)
Low	Low	95.00	135.0	1.350–0.950
Low	High	47.50	67.50	0.675–0.475
High	Low	47.50	67.50	1.350–0.950
High	High	23.75	33.75	0.675–0.475

4.2 Start-up

The MC92600 begins a start-up sequence upon application of the reference clock (REF_CLK input) to the device. This is considered a cold start-up. The receiver requires that byte alignment is reached before data can be transmitted. If word synchronization is selected, then word alignment must occur. The steps in the cold start-up sequence are as follows:

1. PLL start-up
2. Receiver initialization and byte alignment
3. Word alignment (if enabled)
4. Run

The expected duration of each step in the start-up sequence is shown in Table 4-2. A cold start-up can be initiated at any time by asserting the $\overline{\text{RESET}}$ signal low. It is recommended that $\overline{\text{RESET}}$ be set low at initial start-up, however, it is not strictly required.

Table 4-2. Start-up Sequence Step Duration

Start-up Step	Typical Duration (in Bit Times)*	Note
PLL start-up	10240 + 25 µs	
Receiver initialization	50	WSE = low
	160	WSE = high
Word alignment	50	WSE = low
	160	WSE = high

* Example: if the Reference Clock Frequency is 125 MHz, then the bit time equals 800 ps.

4.3 Standby Mode

Standby mode puts the MC92600 into a low power, inactive state. When STNDBY is asserted, the device will force all transmitter link outputs to their disabled state as defined in Section 2.5.2, “Transmit Driver Operation,” and will disable all internal clocking. An important feature of standby mode is that the internal PLL is not disabled. It remains operating and locked to the reference clock. Keeping the internal PLL enabled greatly reduces the time needed to recover from standby mode to run mode, because only the receiver initialization and word alignment start-up steps are required.

4.4 Repeater Mode

To send 32 bytes of data the MC92600 can be configured into a four-link receive-transmit repeater by setting REPE high. In repeater mode data received on link A's receiver is forwarded to link A's transmitter, link B's receiver to link B's transmitter, and so on. The following configuration inputs may be used to control how the repeater handles data that passes through it: 10-bit interface, byte alignment, word synchronization, add/drop idle, half-speed, and double data rate modes.

Certain configurations are more effective than others for various applications. The transmitter at the source, the receiver at the destination, and the repeater must have compatible configurations to ensure proper operation. The following sections describe how each configuration control affects repeater operation.

Table 4-3. Settings for Repeater Mode

Mode	Signals	Recommended State	Description
Word Synchronization Mode	WSE	Don’t care	Enables word synchronization if desired. See Section 4.4.3 for more details.
Byte Alignment Mode	BSYNC_1	Don’t care	Byte alignment is required for idle detection. Both alignment modes are supported in repeater mode. See Section 4.4.2 for more details.
Add / Drop Idle Mode	ADIE	High	When enabled, allows the receiver to add/delete idle patterns to maintain word alignment. This is the recommended operating mode. Recovered clock mode cannot be run in repeater mode therefore, add/delete idles must be enabled
10-bit Interface	TBIE	Don’t care	When enabled, the idle character must be part of the TBI code set. When disabled, the idle is naturally supported by the 8B/10B codes.
Recovered Clock	RCCE	Illegal	Recovered clock mode cannot be run in repeater mode. Repeater mode uses reference clock mode exclusively.

Table 4-3. Settings for Repeater Mode (continued)

Mode	Signals	Recommended State	Description
Half-Speed Enable	HSE	Don't care	User programmable depending on desired reference clock frequency. See Section 4.4.6 for mode details.
Double Data Rate	DDRE	Don't care	User programmable depending on desired reference clock frequency. See Section 4.4.6 for mode details.

4.4.1 10-Bit Interface Mode

When the device is in TBI mode (TBIE = high) the internal 8B/10B encoder and decoder are bypassed and the 10-bit data received is forwarded directly to the transmitter. Running disparity is assumed correct and is not checked. This is important when using disparity-based word synchronization where incorrect running disparity is used as a word synchronization event marker. 10-bit mode must be enabled for disparity-based word alignment to operate properly because it allows the improper disparity to pass through the repeater.

When byte interface mode is enabled (TBIE = low), received data is passed through the 8B/10B decoder where it is converted into its eight-bit data or control byte. Running disparity and code validity are checked and reported with the received byte at the receiver interface as described in Section 3.5.4, "Receiver Interface Modes." The decoded byte is re-coded by the transmitter's 8B/10B encoder for transmission.

NOTE

Byte interface mode must not be used with non-aligned mode or disparity-based word synchronization.

4.4.2 Byte Alignment Mode

The byte alignment mode must be consistent with the transmitter and receiver with which the repeater is being used. All byte alignment modes are supported in repeater mode.

When establishing byte alignment for the link through the repeater, the byte alignment sequence must be repeated twice, once for the repeater and once for the destination's receiver. For example, if the byte aligned with realignment mode is enabled (BSYNC_0/BSYNC_1 = high/low), at least eight idle characters must be transmitted, four for repeater alignment and four for the destination's receiver alignment.

4.4.3 Word Synchronization Mode

Word synchronization may be used in repeater mode. This allows the incoming bytes to be synchronized into their corresponding words, removing cable skew from the transmission

source and re-establishing synchronization. All word synchronization modes are supported in repeater mode.

Similar to byte alignment, the word synchronization sequence must be repeated twice, once for the repeater and once for the destination's receiver. If the 4 idle/1 non-idle word synchronization event mode is being used, a 4 idle/1 non-idle word synchronization event must be followed by a second 4 idle/1 non-idle word synchronization event to enable the entire link to establish word synchronization. Note that byte alignment must be established prior to word synchronization. See Section 4.4.2, "Byte Alignment Mode," on page 4-4.

4.4.4 Recovered Clock Mode

The MC92600 Quad's four transmitters are timed exclusively to the reference clock domain. Recovered clock mode cannot be used in repeater mode. The setting on the recovered clock enable input, RCCE, is ignored when in repeater mode and all data is timed to the reference clock.

4.4.5 Add/Drop Idle Mode

Repeater mode is timed exclusively to the reference clock domain as stated above. A frequency offset between the source transmitter and the repeater will cause the repeater's receiver to eventually overrun/underrun. To ensure that overrun/underrun does not cause data to be lost, add/drop idle mode must be used. Add/drop idle mode is enabled by setting ADIE high. The repeater adds or drops idles from the data stream to maintain alignment to the reference clock. The guidelines for idle density are discussed in Section 3.4.2, "Reference Clock Timing Mode."

4.4.6 Half-Speed Mode, Double Data Rate Mode

Half-speed mode and double data rate mode simply affect the frequency of the reference clock that must be provided and the timing of the receiver interface. All combinations of these modes are supported in repeater mode. See Section 3.5.4.4, "Half-Speed Mode" for more information on half-speed mode and Section 3.5.4.3, "Double Data Rate Mode" for more information on double data rate mode.

4.5 Configuration and Control Signals

The MC92600 has many configuration and control signals that are asynchronous to all inputs clocks. Most of the signals affect internal configuration state and must be set at power-up. If their state is changed after power-up, some require that the chip be reset by setting $\overline{\text{RESET}}$ low and then releasing high. While other configuration signals are meant to be changed during normal operation and do not require chip reset. However, these signals may still affect device operation. Table 4-4 lists all of the MC92600 asynchronous

configuration and control signals and describes the effect of changing their state after power up.

Table 4-4. Asynchronous Configuration and Control Signals

Signal Name	Description	Effect of Changed State
TBIE	Ten-Bit Interface Enable	Device must be reset.
HSE	Half-Speed Enable	Device must be reset.
DDRE	Double data rate enable	Device must be reset.
BSYNC_0	Word Sync. Event Method	Device must be reset.
BSYNC_1	Byte Alignment Mode	Device must be reset.
ADIE	Add/Drop Idle Enable	Device must be reset.
RCCE	Recovered Clock Enable	Device must be reset.
REPE	Repeater Mode Enable	Device must be reset.
WSE	Word Synchronization Enable	Device must be reset.
TST_0, TST_1	Test mode definers	Must be low and remain low during normal operation
LBE	Loop Back Enable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
LBOE	Loopback Output Enable	Enable/disable transmit links during testing (LBOE = high), no recovery action necessary
STNDBY	Puts PLL Standby mode	Receiver must re-establish byte and word synchronization.
$\overline{\text{RESET}}$	System Reset Bar	Device is reset.

4.6 Power Supply Requirements

The board design should have a minimum of two solid planes of one ounce copper. One plane is to be used as a ground plane and the second plane is to be used for the 1.8V supply. It is recommended that the board has its own 1.8V and 3.3V regulators with less than 50 mV ripple.

4.7 Phase-Locked Loop (PLL) Power Supply Filtering

An analog power supply is required for the internal PLL. The PLLAVDD signal provides power for the analog portions of the PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 4-1. For maximum effectiveness, the filter circuit is placed as close as possible to the PLLAVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the PLLAGND ball. The 0.01µF capacitor is closest to the ball, followed by the 1µF

capacitor, and finally the 1Ω resistor to Vdd on the 1.8V power plane. The capacitors are connected from PLLAVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

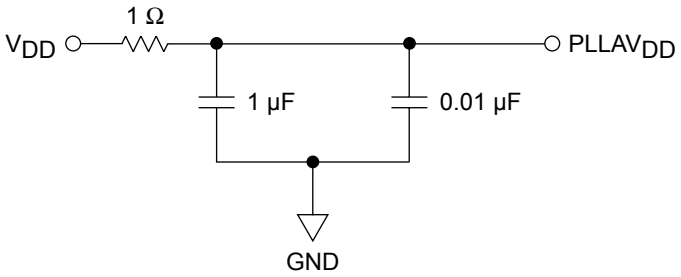


Figure 4-1. PLL Power Supply Filter Circuit

4.8 Decoupling Recommendations

The MC92600 requires a clean, tightly regulated source of power to ensure low jitter on transmit, and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

- Only surface mount technology (SMT) capacitors should be used, to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.
- The board should have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 1.8V (Vdd and XVdd) balls of the device. The board should also have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 3.3V (OVdd) balls of the device. Where the board has blind vias, these capacitors should be placed directly below the MC92600 supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the MC92600, as close to the supply and ground connections as possible.
- A 1uF ceramic chip capacitor should exist on each side of the MC92600 device. This should be done for both the 1.8V supply and the 3.3V supply.
- Between the MC92600 device and the voltage regulator should be a 10uF, low equivalent series resistance (ESR) SMT tantalum chip capacitor, and a 100uF, low ESR SMT tantalum chip capacitor. This should be done for both the 1.8V supply and the 3.3V supply.

Chapter 5
Test Features

The MC92600 supports several test modes for in-system built-in self test (BIST) and production testing. Test modes are selected through the TST_0, TST_1, LBE and LBOE signals. Table 5-1 shows test mode state selection.

Table 5-1. Test Mode State Selection

TST_1	TST_0	LBE	LBOE	Description
Low	Low	Low	Low	Normal operation, no test mode enabled
Low	Low	High	Don't care	Loop back system test mode (Section 5.1)
Low	High	Low	Don't care	BIST sequence system test mode (Section 5.2)
Low	High	High	Don't care	Loop back BIST sequence system test mode (Section 5.3)
Low	Low	Low	High	Board level production test mode (Section 5.4)
High	Don't care	Don't care	Don't care	Reserved

5.1 Loop Back System Test

The MC92600 can be configured in loop back mode where the transmitted data is looped back to its receiver independent of the receiver's link inputs. This is enabled by setting LBE high. The characters transmitted are controlled by the normal transmitter controls. If the transceiver is working properly, the data/control characters transmitted are received by the receiver. This allows system logic to use various data sequences to test the operation of the transceiver.

The loop-back signals are electrically isolated from the XLINK_*x*_P/XLINK_*x*_N output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally. When in loop-back mode, the LBOE signal controls the action of the XLINK_*x*_P/XLINK_*x*_N output signals. When LBOE is low, the transmit driver holds the XLINK_*x*_P/XLINK_*x*_N output signals high and low, respectively. When LBOE is high, the XLINK_*x*_P/XLINK_*x*_N output signals continue to operate normally.

The receiver's link input signals, RLINK_*x*_P and RLINK_*x*_N, are also electrically isolated during loop back mode, such that their state does not affect the loop back path.

5.2 BIST Sequence System Test Mode

The MC92600 transmitter has an integrated, 23rd order, pseudo-noise (PN) pattern generator. Stimulus from this generator may be used for internal built-in self testing (BIST). The receiver has a 23rd order signature analyzer that is synchronized to the incoming PN stream and may be used to count character mismatch errors relative to the internal PN reference pattern.

To properly use the BIST sequence system test mode, the system must provide the proper stimulus in a special sequence. The sequence of steps to run a BIST test is as follows:

1. Select the reference clock frequency at which you wish to run the BIST test. See Table 4-1 , "Legal Reference Clock Frequency Ranges" for pin settings for HSE and DDRE modes.
2. Enter test mode by setting the test mode inputs as described in Table 5-1.
3. Transmit two 4/1 word synchronization event sequences.
4. Transmit to the receiver an 8B/10B encoded PN sequence as described above.

The transmitter will automatically go through steps 3 and 4 upon entering this test mode. Upon completion of testing, the transceiver will need to be re-synchronized before normal operation can resume.

This implementation of the 23-bit PN generator and analyzer uses the polynomial:

$f = 1 + x^5 + x^{23}$

The total mismatch error count is reset to zero when BIST mode is entered. The count is updated continuously while in BIST mode. The value of the count is presented on the receiver interface signals: RECV_*x*_7 through RECV_*x*_0, making up the eight-bit error count, ordered bits 7 through 0, respectively. The value of the count is sticky in that the count will not wrap to zero upon overflow, but rather stays at the maximum count value (11111111).

The RECV_*x*_ERR, RECV_*x*_K and RECV_*x*_IDLE have special meaning during this test mode. They report the status of the receiver and PN analysis logic. Table 5-2 , "BIST Error Codes" describes the BIST error codes and their meaning.

Table 5-2. BIST Error Codes

RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE	Description
Low	Low	Low	BIST running, no PN mismatch this character.
High	Low	Low	BIST running, PN mismatch error this character.
High	Low	High	Receiver byte/word synchronized, PN analyzer is not locked.
High	High	Low	Not byte sync—The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	High	Not word sync—The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

The BIST sequence makes use of the 8B/10B encoder/decoder. Therefore, this test mode overrides the setting on TBIE signal and forces byte interface mode. Additionally, the BIST sequence requires that a normal byte alignment mode be used. The settings on BSYNC_0 and BSYNC_1 are overridden, forcing the device into the byte aligned with realignment mode. In addition to the above signals, the generation of disparity-based word synchronization events is blocked. The WSE_GEN signal is ignored when this test mode is enabled.

BIST is run at the speed indicated by the frequency of the reference clock and by the speed range selected by half-speed mode (HSE). The settings of DDRE, WSE and RCCE are not altered and BIST will follow their setting

5.3 Loop Back BIST Sequence System Test Mode

This test mode is the combination of the loop back and BIST sequence system test modes. The device operates as described in Section 5.1, “Loop Back System Test” and Section 5.2, “BIST Sequence System Test Mode.” However, the need to go through the start-up sequence is eliminated because the transmitter automatically goes through the proper sequence.

5.4 Board Level Manufacturing Test Mode

In this test mode all TTL output drivers (all data outputs, status outputs, and recovered clock outputs) are placed in a high impedance state to facilitate common board level manufacturing testing practices.

Note, however, that the transmitter link output drivers are still active.

In normal operational modes (TST_0, TST_1 and LBE all low), LBOE must also be low. If LBOE is high, the transmitters will be functioning properly, however, the receivers will appear to be non-functional because all TTL output drivers are in a high impedance state.

Chapter 6
Electrical Specifications and Characteristics

This chapter explains the electrical specifications and characteristics of the MC92600 device. This chapter consists of the following sections:

- Section 6.1, “General Characteristics”
- Section 6.2, “DC Electrical Characteristics”
- Section 6.3, “AC Electrical Characteristics”

6.1 General Characteristics

This section presents the general technical parameters, the maximum and recommended operating conditions for the MC92600.

6.1.1 General Parameters

The following list provides a summary of the general parameters of the MC92600.

Technology	0.25µm lithography, HiP4 CMOS, 5 layer metal
Packages:	196 molded plastic ball grid array (MAPBGA), 15mm body size
	217 plastic ball grid array (PBGA), 23 mm body size
Core power supply	1.8V ± 0.15V dc

TTL I/O power supply 3.3V ± 0.3V dc or 2.5V ± 0.2V dc

Link I/O power supply 1.8V ± 0.15V dc

6.2 DC Electrical Characteristics

The tables in this section describe the MC92600 DC electrical characteristics. Table 6-1 shows the absolute maximum ratings for the MC92600 device.

Table 6-1. Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Core supply voltage	V_{dd}	-0.3	2.2	V
PLL supply voltage	AV_{dd}	-0.3	2.2	V
TTL I/O supply voltage	OV_{dd} [1]	-0.3	4.0	V
Link I/O supply voltage	XV_{dd}	-0.3	2.2	V
TTL input voltage	V_{in}	-0.3	OV_{dd} + 0.3	V
Link input voltage	V_{in}	-0.3	XV_{dd} + 0.3	V
Storage temperature range	T_{stg}	-55	150	°C

[1] OV_{dd} must not exceed V_{dd}/AV_{dd} by more than 2.2V at any time including during power-up.

Functional and tested operating conditions are given in Table 6-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums are not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Table 6-2. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	V_{dd}	1.65	1.95	V
PLL Supply Voltage	AV_{dd}	1.65	1.95	V
TTL I/O Supply Voltage	OV_{dd}	2.3	3.6	V
Link I/O Supply Voltage	XV_{dd}	1.65	1.95	V
TTL Input Voltage	V_{in}	0	OV_{dd}	V
Link input voltage	V_{in}	0	XV_{dd}	V
Junction temperature - MC92600JUB or MC92600ZTB	T_J	0	105	°C
Junction temperature - MC92600CJUB	T_J	-40	105	°C
Ambient temperature [1] - MC92600JUB or MC92600ZTB	T_a	0	70	°C
Ambient temperature[1] - MC92600CJUB	T_a	-40	70	°C

[1] Operating Ambient Temperature is dependent on proper thermal management to meet operating Junction Temperature specifications.

6.2.1 Characteristics of the 3.3V Device

Table 6-3 displays the 3.3V electrical characteristics of the MC92600 device. Voltage symbols of Table 6-3 are defined in Table 6-2Characteristics of the 2.5V Device.

Table 6-3. DC Electrical Specifications for 3.3V Power Supply

Characteristic [1, 2, 3]	Symbol	Min	Typical	Max	Unit
TTL input high voltage	V_{IH}	2.0	—	—	V
TTL input low voltage	V_{IL}	—	—	0.8	V
TTL input leakage current, Vin = OV_{dd}	I_{IH}	—	—	10	µA
TTL input leakage current, Vin = GND	I_{IL}	—	—	10	µA
TTL output high voltage, IOH = -6 mA	V_{OH}	2.4	—	—	V
TTL output low voltage, IOL = 6 mA	V_{OL}	—	—	0.4	V
TTL input capacitance	C_{in}	—	—	10	pF
TTL output impedance, Vout = OV_{dd}/2	R_{out}	40	—	62	Ω
Link common mode input impedance	R_{cm}	2	—	4	kΩ
Link differential input impedance, MEDIA = low/high	R_{diff}	85/127.5	—	125/180	Ω
Link common mode input level	V_{cm}	0.725	—	1.225	V
Link differential input amplitude	ΔV_{in}	0.4	—	3.2	V_{p-p}
Link input capacitance	C_{in}	—	—	3	pF
Link common mode output level	V_{cm}	0.725	—	1.075	V
Link differential output amplitude, 100/150 Ω diff load, MEDIA = low/high	ΔV_{out}	1.3	—	2.2	V_{p-p}
Link differential output impedance, MEDIA = low/high	R_{out}	—	100/150	—	Ω
Power dissipation: 8B/10B mode	—	—	941 [4]	1098	mW
Power dissipation: 10 bit mode	—	—	969[4]	1130	mW

1 $V_{dd} = AV_{dd} = XV_{dd} = 1.8 \pm 0.15$ V dc; $OV_{dd} = 3.3 \pm 0.3$ V dc; GND = 0 V dc; $0 \le T_J \le 105^oC$ for MC92600JUB and MC92600ZTB or $-40 \le T_J \le 105^oC$ for MC92600CJUB

2 These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

3 Recommended supply power-up order is V_{dd}, AV_{dd}, OV_{dd}, XV_{dd}, however, any order is acceptable as long as maximum ratings are not exceeded

4 Simulation-based values. Typical tester values yield 780mW.

Table 6-4 displays the 2.5V electrical characteristics of the MC92600 device. The table's voltage symbols are defined in Table 6-2.

Table 6-4. DC Electrical Specifications for 2.5V Power Supply

Characteristic [1, 2, 3]	Symbol	Min	Typical	Max	Unit
TTL input high voltage	V_{IH}	1.6	—	—	V
TTL input low voltage	V_{IL}	—	—	0.8	V
TTL input leakage current, Vin = OV_{dd}	I_{IH}	—	—	5	µA
TTL input leakage current, Vin = GND	I_{IL}	—	—	5	µA
TTL output high voltage, IOH = -6 mA	V_{OH}	1.9	—	—	V
TTL output low voltage, IOL = 6 mA	V_{OL}	—	—	0.4	V
TTL input capacitance	C_{in}	—	—	10	pF
TTL output impedance, Vout = $OV_{dd}/2$	R_{out}	45	—	70	Ω
Link common mode input impedance	R_{cm}	2	—	4	kΩ
Link differential input impedance, MEDIA = low/high	R_{diff}	85/127.5	—	125/180	Ω
Link common mode input level	V_{cm}	0.725	—	1.225	V
Link differential input amplitude	ΔV_{in}	0.4	—	3.2	V_{p-p}
Link input capacitance	C_{in}	—	—	3	pF
Link common mode output level	V_{cm}	0.725	—	1.075	V
Link differential output amplitude, 100/150 Ω diff load, MEDIA = low/high	ΔV_{out}	1.3	—	2.2	V_{p-p}
Link differential output impedance, MEDIA = low/high	R_{out}	—	100/150	—	Ω
Power dissipation: 8B/10B mode	—	—	873 [4]	1014	mW
Power dissipation: 10 bit mode	—	—	889 [4]	1055	mW

1 $V_{dd} = AV_{dd} = XV_{dd} = 1.8 \pm 0.15$ V dc; $OV_{dd} = 2.5 \pm 0.2$ V dc; GND = 0 V dc; $0 \le T_J \le 105^oC$ for MC92600JUB and MC92600ZTB or $-40 \le T_J \le 105^oC$ for MC92600CJUB

2 These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

3 Recommended supply power-up order is V_{dd}, AV_{dd}, OV_{dd}, XV_{dd}, however, any order is acceptable as long as maximum ratings are not exceeded.

4 Simulation-based values. Typical tester values yield 780mW.

6.3 AC Electrical Characteristics

This section describes the AC electrical characteristics of the MC92600 device.

6.3.1 Parallel Port Interface Timing

The following figures and tables show the timing for the transmitter and receiver parallel interface.

6.3.1.1 Transmitter (DDRE = Low)

The transmitter timing diagram for DDRE = Low is shown in Figure 6-1.

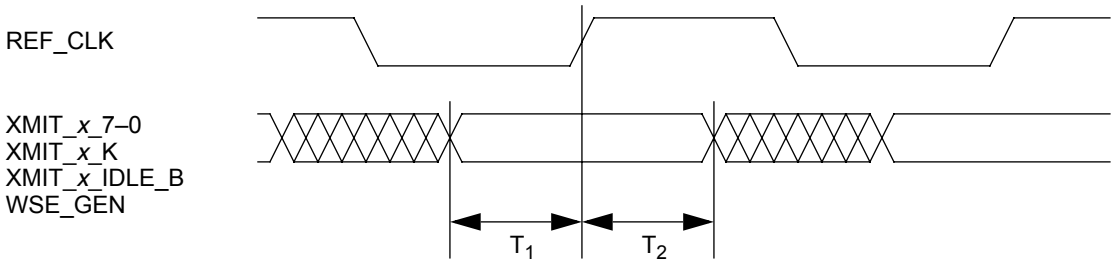


Figure 6-1. Transmitter Interface Timing Diagram (DDRE = Low)

Table 6-5 shows the timing specifications for DDRE = Low.

Table 6-5. Transmitter Timing Specification (DDRE = Low)

Symbol	Characteristic	Min	Max	Unit
T1	Setup time to rising edge of REF_CLK	0.5	-	ns
T2	Hold time to rising edge of REF_CLK	0.6	-	ns

6.3.1.2 Transmitter (DDRE = High)

The transmitter timing diagram for DDRE = High is shown in Figure 6-2.

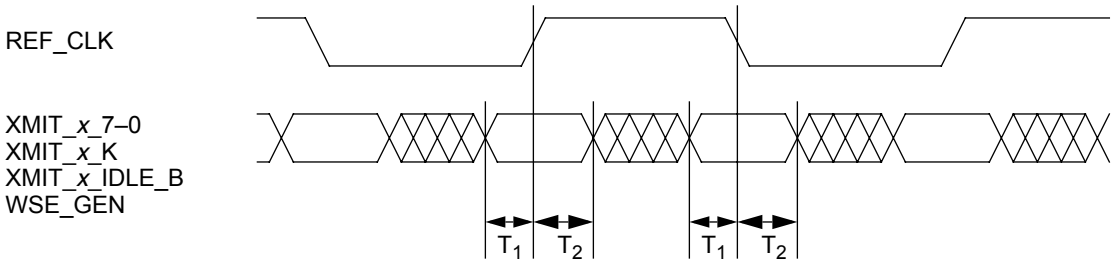


Figure 6-2. Transmitter Interface Timing Diagram (DDRE = High)

Table 6-6 shows the timing specifications for DDRE = High.

Table 6-6. Transmitter Timing Specification (DDRE = High)

Symbol	Characteristic	Min	Max	Unit
T_1	Setup time to rising/falling edge of REF_CLK	0.5	-	ns
T_2	Hold time to rising/falling edge of REF_CLK	0.6	-	ns

6.3.1.3 Receiver (DDRE = Low, RCCE = Low)

The receiver timing diagram for DDRE = Low, RCCE = Low is shown in Figure 6-3.

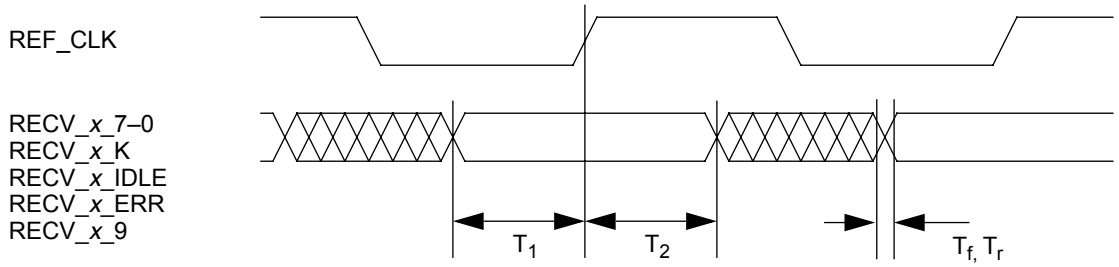


Figure 6-3. Receiver Interface Timing Diagram (DDRE = Low, RCCE = Low)

shows the timing specifications for DDRE = Low, RCCE = Low.

Table 6-7. Receiver Timing Specification (DDRE = Low, RCCE = Low)

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising edge of REF_CLK [1]	3.0	-	ns
	Output valid time before rising edge of REF_CLK [2]	11.0	-	ns
T_2	Output valid time after rising edge of REF_CLK[1,2, 3]	2.0	-	ns
	Output valid time after rising edge of REF_CLK[1,2, 4]	1.744	-	ns
T_f	Output fall time [5]	-	1.8	ns
T_r	Output rise time[5]	-	1.8	ns

1 Full speed, HSE = Low.
2 Half speed, HSE_High.
3 Operating Junction Temperature, T_J = 0 to +105 ^oC
4 Operating Junction Temperature, T_J = -40 to +105 ^oC
5 10 pF output load.

6.3.1.4 Receiver (DDRE = High, RCCE = Low)

The receiver timing diagram for DDRE = High, RCCE = Low is shown in Figure 6-4.

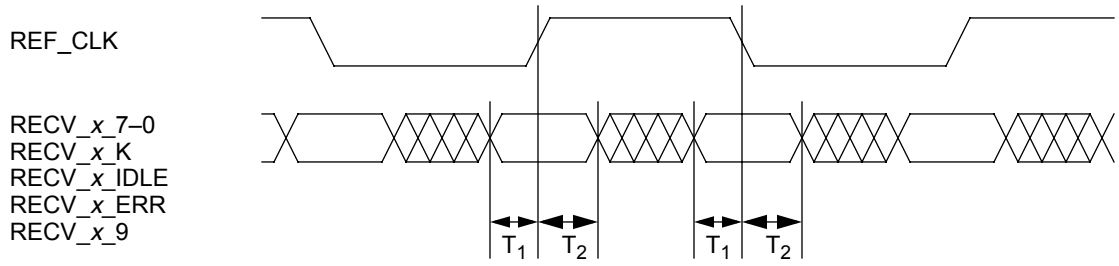


Figure 6-4. Receiver Interface Timing Diagram (DDRE = High, RCCE = Low)

Table 6-8 shows the timing specifications for DDRE = High, RCCE = Low.

Table 6-8. Receiver Timing Specification (DDRE = High, RCCE = Low

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising/falling edge of REF_CLK [1, 2]	2.2	-	ns
	Output valid time before rising/falling edge of REF_CLK[1, 3]	10.2	-	ns
T_2	Output valid time after rising/falling edge of REF_CLK[2,3, 4]	2.0	-	ns
	Output valid time after rising/falling edge of REF_CLK[2,3, 5]	1.744	-	ns

1 REF_CLK duty cycle 45/55.
2 Full speed, HSE = Low.
3 Half speed, HSE = High.
4 Operating Junction Temperature, T_J = 0 to +105 ^{o}C
5 Operating Junction Temperature, T_J = -40 to +105 ^{o}C

6.3.1.5 Receiver (DDRE = Low, RCCE = High)

The receiver timing diagram for DDRE = Low, RCCE = High is shown in Figure 6-5.

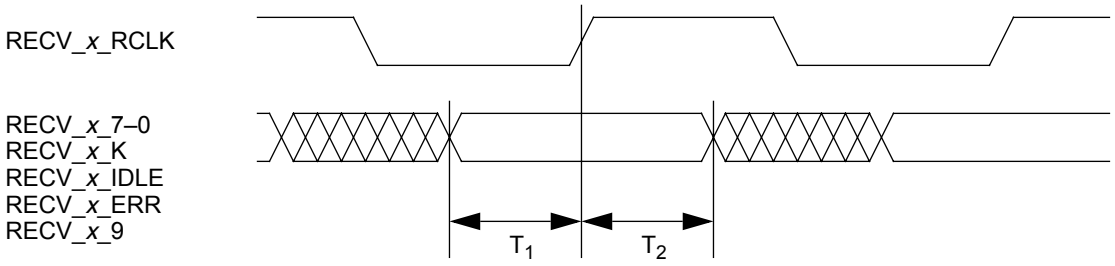


Figure 6-5. Receiver Interface Timing Diagram (DDRE = Low, RCCE = High

Table 6-9 shows the timing specifications for DDRE = Low, RCCE = High.

Table 6-9. Receiver Timing Specification (DDRE = Low, RCCE = High)

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising edge of RECV_x_RCLK [1]	2.5	—	ns
	Output valid time before rising edge of RECV_x_RCLK [2]	5.7	—	ns
T_2	Output valid time after rising edge of RECV_x_RCLK[1]	3.4	—	ns
	Output valid time after rising edge of RECV_x_RCLK[2]	6.6	—	ns

1 Full speed, HSE = Low.
2 Half speed, HSE = High.

6.3.1.6 Receiver (DDRE = High, RCCE = High)

The receiver timing diagram for DDRE = High, RCCE = High is shown in Figure 6-6.

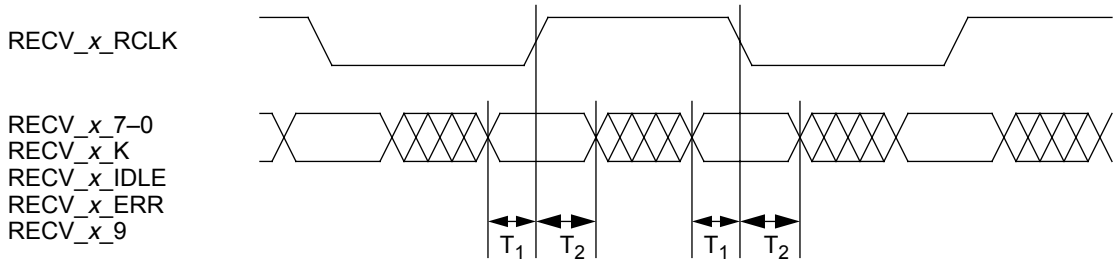


Figure 6-6. Receiver Interface Timing Diagram (DDRE = High, RCCE = High)

Table 6-10 shows the timing specifications for DDRE = High, RCCE = High.

Table 6-10. Receiver Timing Specification (DDRE = High, RCCE = High)

Symbol	Characteristic	Min	Max	Unit
T_1	Setup time to rising/falling edge of RECV_x_RCLK [1]	2.5	-	ns
	Setup time to rising/falling edge of RECV_x_RCLK [2]	5.7	-	ns
T_2	Hold time to rising/falling edge of RECV_x_RCLK[1]	3.4	-	ns
	Hold time to rising/falling edge of RECV_x_RCLK[2]	6.6	-	ns

1 Full speed, HSE = Low.
2 Half speed, HSE = High.

6.3.2 Reference Clock Timing

The timing diagram for the reference clock is shown in Figure 6-7.

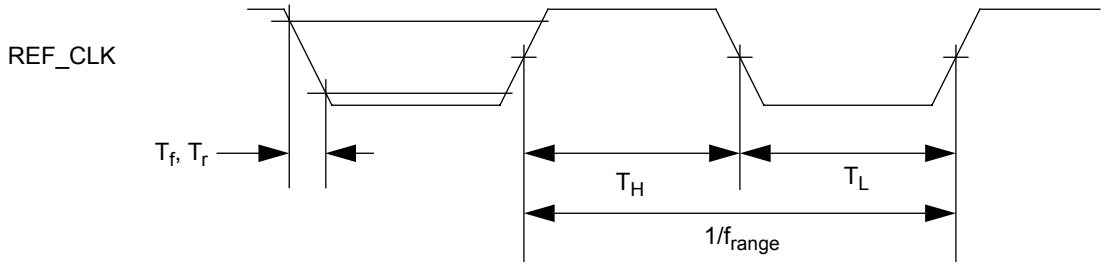


Figure 6-7. Reference Clock Timing Diagram

Table 6-11 shows the timing specifications for the reference clock.

Table 6-11. Reference Clock Specification

Symbol	Characteristic	Min	Max	Unit
T_r	REF_CLK rise time [1]	—	2.0	ns
T_f	REF_CLK fall time[1]	—	2.0	ns
T_H	REF_CLK pulse width high [2]	3.2	—	ns

Table 6-11. Reference Clock Specification (continued)

Symbol	Characteristic	Min	Max	Unit
T_L	REF_CLK pulse width low[2]	3.2	—	ns
f_{range}	REF_CLK frequency range [3]	95	135	MHz
	REF_CLK frequency range [4]	47.5	67.5	MHz
	REF_CLK frequency range [5]	23.75	33.75	MHz
T_D	REF_CLK duty cycle [6]	40	60	%
	REF_CLK duty cycle [7]	45	55	%
f_{offset}	REF_CLK to REF_CLK frequency offset	-250	250	ppm
T_j	REF_CLK input jitter [8]	-	80	ps
T_{lock}	PLL lock time [9]	-	20,480 + 25 µs	bit-times

1 Measured between 10-90% points.
2 Measured between 50-50% points.
3 Full speed (HSE = Low), normal data rate (DDRE = Low).
4 Half speed (HSE = High), normal data rate (DDRE = Low); and full speed (HSE = Low), double data rate (DDRE = High).
5 Half speed (HSE = High), double data rate (DDRE = High).
6 Normal data rate (DDRE = Low).
7 Double data rate (DDRE = High).
8 Total peak-to-peak jitter
9 Lock time after compliant REF_CLK signal applied.

6.3.3 Receiver Recovered Clock Timing

The timing diagram for the recovered clock is shown in Figure 6-8.

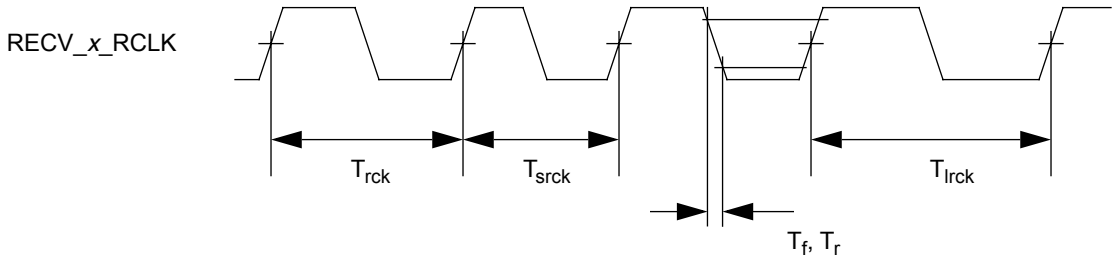


Figure 6-8. Recovered Clock Timing Diagram

Table 6-12 shows the timing specifications for the recovered clock.

Table 6-12. Recovered Clock Specification

Symbol	Characteristic	Min	Max	Unit
Trck	RECV_*x*_RCLK normal cycle period [1]	8.0	-	ns
Tsrck	RECV_*x*_RCLK short cycle period[1]	6.4	-	ns
Tlrck	RECV_*x*_RCLK long cycle period[1]	9.6	-	ns
Tr	RECV_*x*_RCLK rise time [2]	-	1.8	ns
Tf	RECV_*x*_RCLK fall time[2]	-	1.8	ns

1 Measured between 50-50% points, 125 MHz REF_CLK, full speed (HSE = Low), normal data rate (DDRE = Low).

2 Measured between 10-90% points.

6.3.4 Serial Data Link Timing

This following sections cover the input and output data link timing.

6.3.4.1 Link Differential Output

The transmitter timing diagram for the link differential output is shown in Figure 6-9.

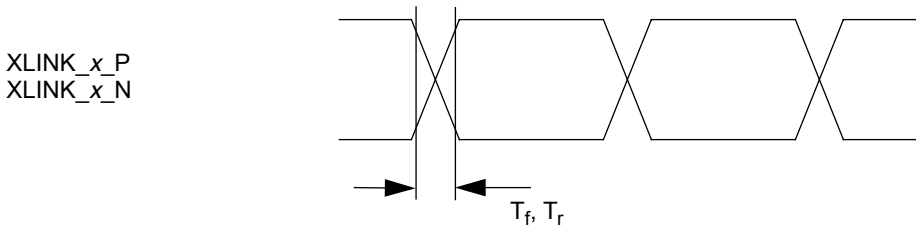


Figure 6-9. Link Differential Output Timing Diagram

Table 6-13 shows the timing specifications for the link differential output.

Table 6-13. Link Differential Output Specification

Symbol	Characteristic	Min	Max	Unit
T_f	Link output fall time [1]	-	200	ps
T_r	Link output rise time [1]	-	200	ps
T_j	Total jitter [2]	-	0.24	UI
T_{dj}	Deterministic jitter [2]	-	0.12	UI
T_{ds}	Differential skew [2]	-	25	ps
X_{lat}	Transmit latency [3]	-	25	bit-times

1 Measured between 10-90% points.

2 Measured between 50-50% points, 125 MHz REF_CLK, 1.25 gigabaud rate.

3 REF_CLK to first bit transmit.

6.3.4.2 Link Differential Input

The receiver timing diagram for the link differential input is shown in Figure 6-10.

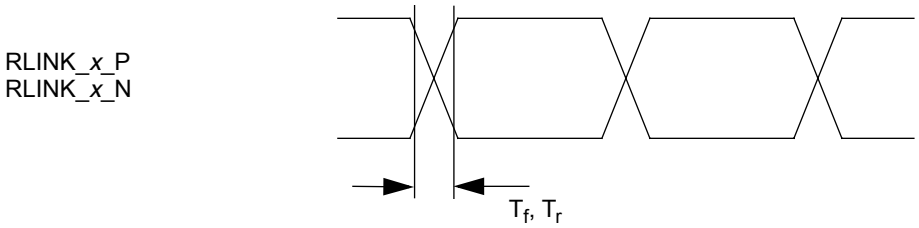


Figure 6-10. Link Differential Input Timing Diagram

Table 6-14 shows the timing specifications for the link differential input.

Table 6-14. Link Differential Input Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_f	Link input fall time [1]	300	-	ps
T_r	Link input rise time[1]	300	-	ps
T_{jtol}	Total jitter tolerance [2]	0.71	-	UI
T_{djtol}	Deterministic jitter tolerance [2]	0.45	-	UI
T_{dstol}	Differential skew tolerance [2]	175	-	ps
R_{lat}	Receive latency [3]	-	62	bit-times

1 Measured between 10-90% points.
2 Measured between 50-50% points, 125 MHz REF_CLK, 1.25 gigabaud rate.
3 Bit 0 at receiver input to parallel data out.

Chapter 7
Package Description

The MC92600 is offered in two packages, a 196 MAPBGA and a 217 PBGA. The 196 MAPBGA utilizes an aggressive 1 mm ball pitch and 15 mm body size for application where board space is limited. The 217 PBGA utilizes a standard 1.27 mm ball pitch and 23 mm body size that eases board routing.

7.1 196 MAPBGA Package Parameter Summary

- Package Type—Fine pitch ball grid array
- Package Outline—15 mm x 15 mm
- Package Height—1.60 mm Max
- Number of Balls—196
- Ball Pitch—1 mm
- Ball Diameter—0.45–0.55 mm

7.2 217 PBGA Package Parameter Summary

- Package Type—Plastic ball grid array
- Package Outline—23 mm x 23 mm
- Package Height—2.32 mm Max
- Number of Balls—217
- Ball Pitch—1.27 mm
- Ball Diameter—0.60–0.90 mm

7.3 Nomenclature and Dimensions of the 196 MAPBGA Package

Figure 7-1 provides the bottom surface nomenclature and package outline drawing of the 196 MAPBGA package. Figure 7-2 provides the package dimensions. Figure 7-3 provides a graphic of the package pin signal mappings.

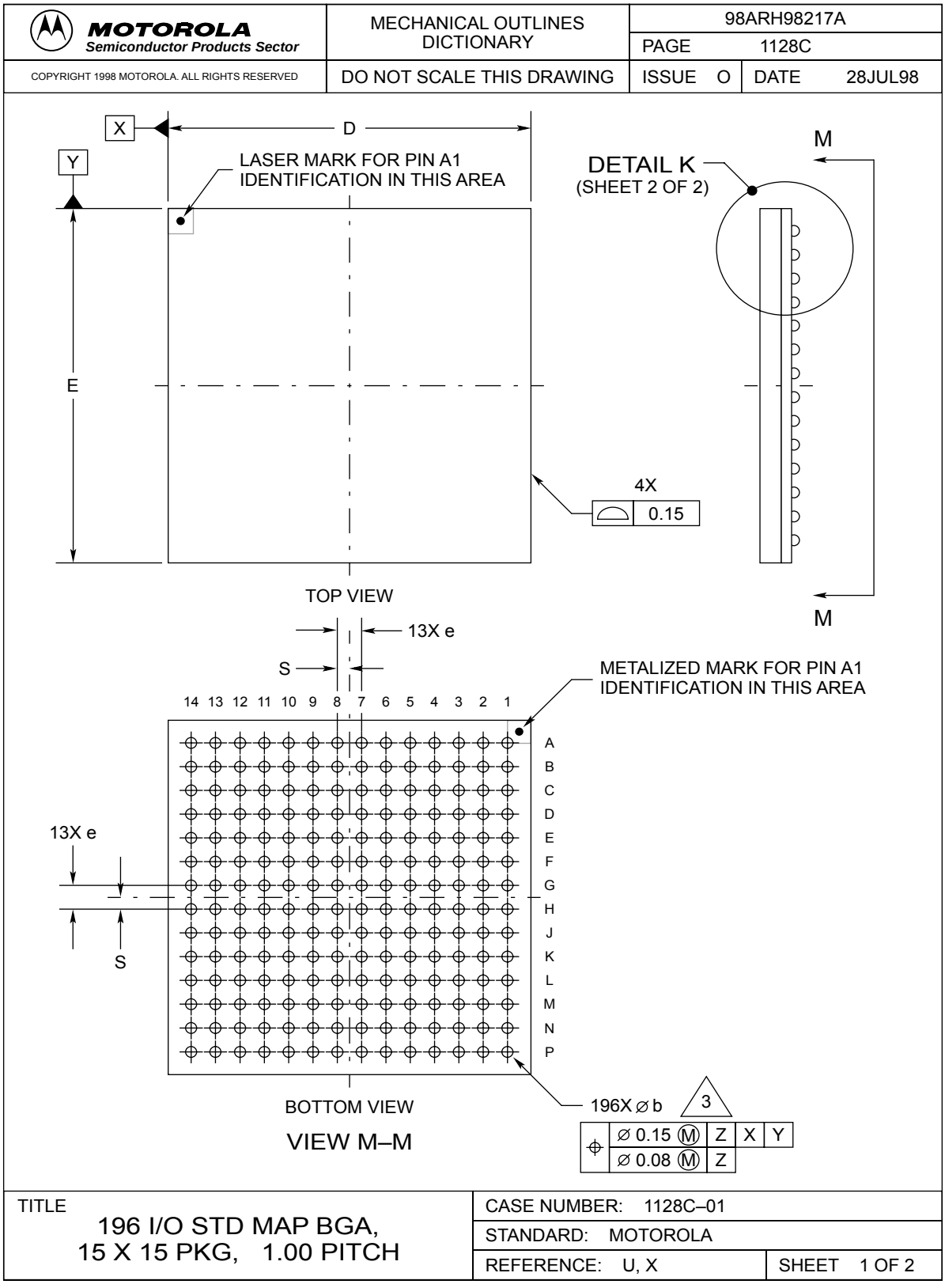
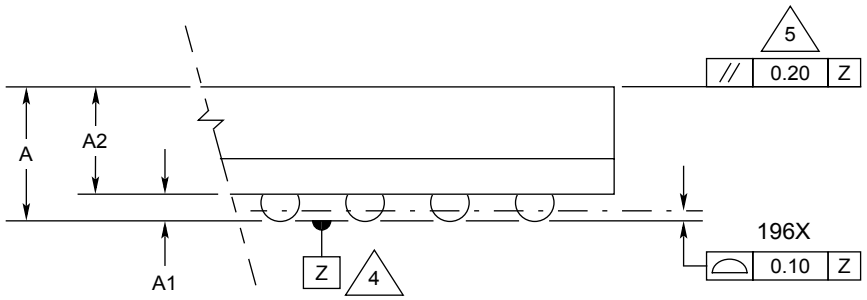


Figure 7-1. 196 MAPBGA Nomenclature

MOTOROLA Semiconductor Products Sector	MECHANICAL OUTLINES DICTIONARY	98ARH98217A	
		PAGE 1128C	
COPYRIGHT 1998 MOTOROLA. ALL RIGHTS RESERVED	DO NOT SCALE THIS DRAWING	ISSUE O	DATE 28JUL98



DETAIL K
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

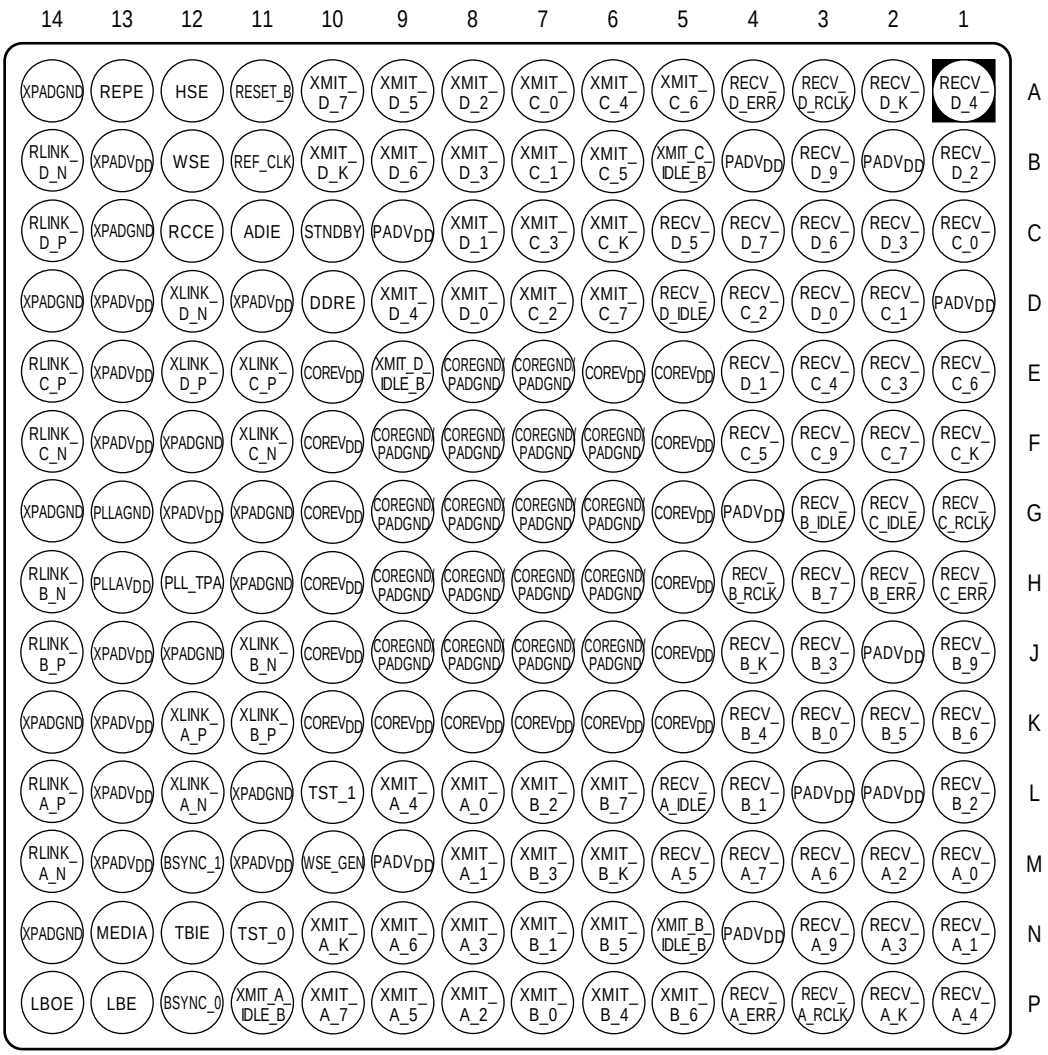
NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE	CASE NUMBER: 1128C–01	
196 I/O STD MAP BGA 15 X 15 PKG, 1.00 PITCH	STANDARD: MOTOROLA	
	REFERENCE: U, X	SHEET 2 OF 2

Figure 7-2. 196 MAPBGA Dimensions

.



View G-G (Bottom View)

Figure 7-3. 196 MAPBGA Package

7.4 Nomenclature and Dimensions of the 217 MAPBGA Package

Figure 7-4 provides the bottom surface nomenclature and package outline drawing of the 217 MAPBGA package. Figure 7-5 provides the package dimensions. Figure 7-6 provides a graphic of the package pin signal mappings.

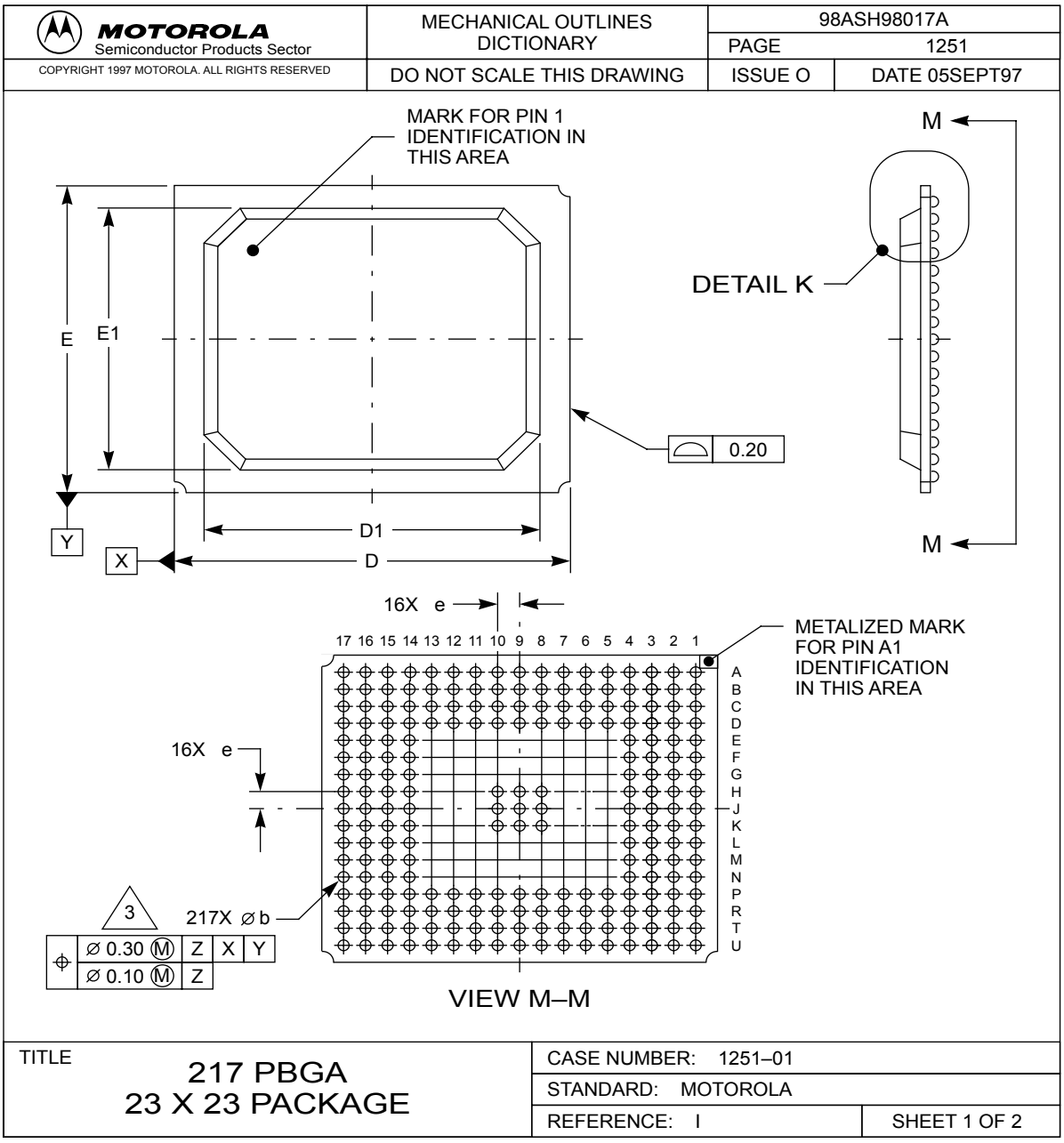
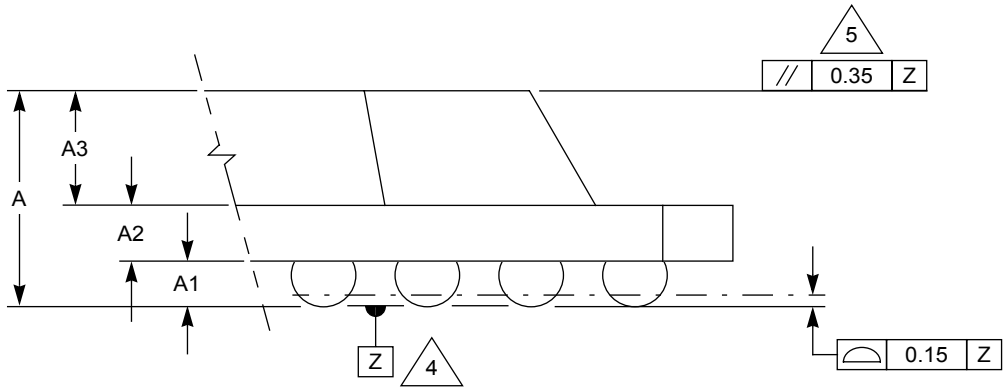


Figure 7-4. 217 PBGA Nomenclature

MOTOROLA Semiconductor Products Sector	MECHANICAL OUTLINES DICTIONARY	98ASH98017A	
		PAGE	1251
COPYRIGHT 1997 MOTOROLA. ALL RIGHTS RESERVED	DO NOT SCALE THIS DRAWING	ISSUE O	DATE 05SEPT97



DETAIL K
VIEW ROTATED 90° CLOCKWISE

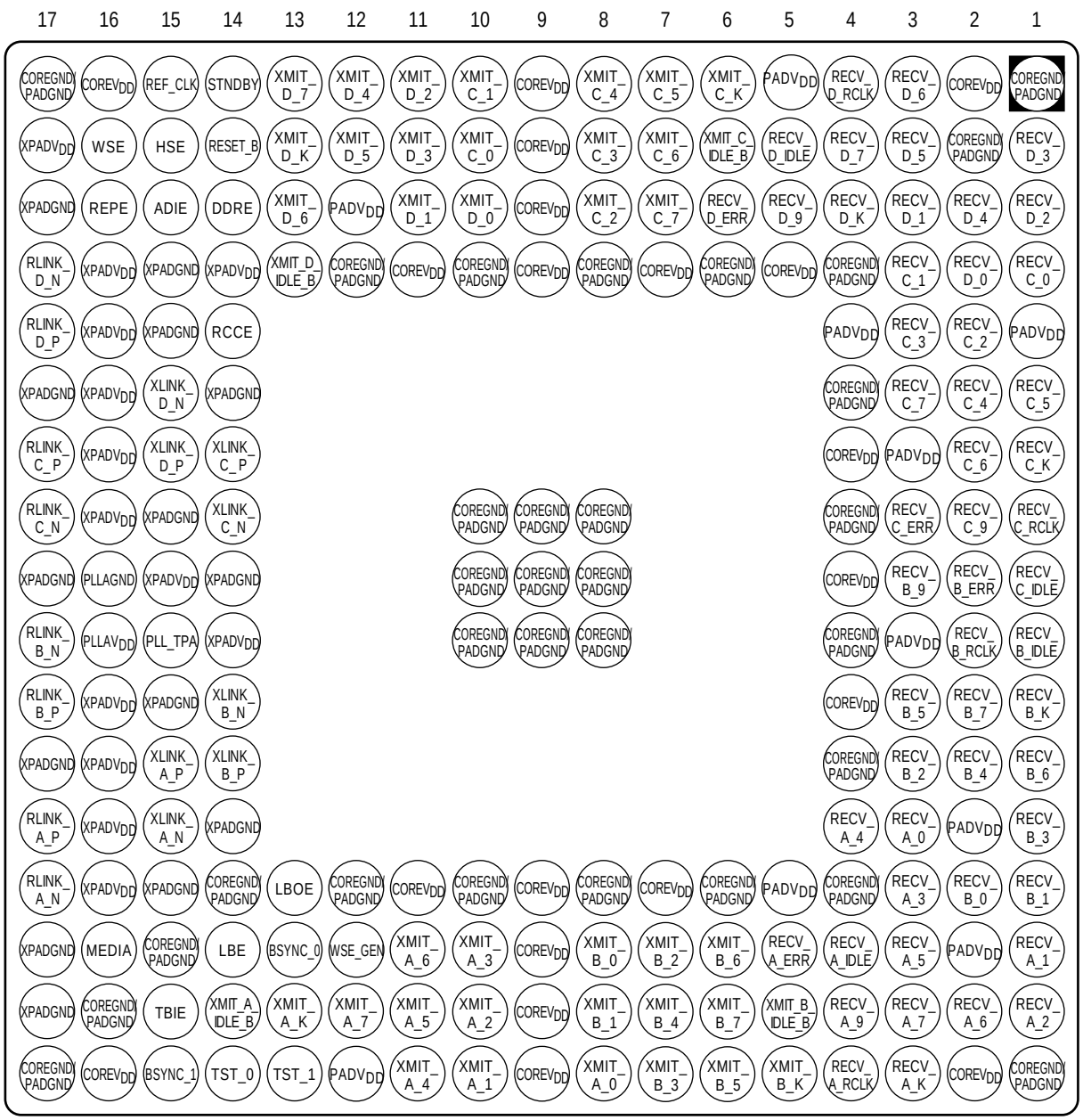
DIM	MIN	MAX
A	1.92	2.32
A1	0.50	0.70
A2	0.36 REF	
A3	1.12	1.22
b	0.60	0.90
D	23.00	
D1	19.00 BSC	20.20
E		
E1	19.00 23.00	20.20
e	BSC	
	1.27 BSC	

NOTES

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACK-

TITLE	CASE NUMBER: 1251–01	
217 PBGA 23 X 23 PACKAGE	STANDARD: MOTOROLA	
	REFERENCE: I	SHEET 2 OF 2

Figure 7-5. 217 PBGA Dimensions



View M-M (Bottom View)

Figure 7-6. 217 PBGA Package

7.5 Package Thermal Characteristics

Thermal values for the 196 MAPBGA and 217 PBGA are listed below in Table 7-1. The values listed below assume the customer will be mounting these packages on a thermally enhanced mother board. This is defined as a minimum 4-layer board with one ground plane. The values listed below were measured in accordance with established JEDEC (Joint Electron Device Engineering Council) standards.

Table 7-1. MC92600 Package Option Thermal Resistance Values

Symbol	Description	196 MAPBGA	217 PBGA	Units
θ_{ja-0}	Thermal resistance from junction to ambient, still air	38	26.5	$^{o}C/W$
θ_{ja-2}	Thermal resistance from junction to ambient, 200 LFM [1]	34	25.1	$^{o}C/W$
θ_{ja-4}	Thermal resistance from junction to ambient, 400 LFM[1]	33	23.6	$^{o}C/W$

[1] Linear feet per minute

7.6 MC92600 Chip Pinout Listing

The MC92600 is offered in two packages, a 196 MAPBGA and a 217 PBGA package. Table 7-2 list the MC92600 signal to ball location mapping for the 196 MAPBGA and 217 PBGA package. Also shown are signaling direction (input or output), and the type of logic interface.

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
XMIT_A_0	Transmitter A, data bit 0	L8	U8	Input	TTL
XMIT_A_1	Transmitter A, data bit 1	M8	U10	Input	TTL
XMIT_A_2	Transmitter A, data bit 2	P8	T10	Input	TTL
XMIT_A_3	Transmitter A, data bit 3	N8	R10	Input	TTL
XMIT_A_4	Transmitter A, data bit 4	L9	U11	Input	TTL
XMIT_A_5	Transmitter A, data bit 5	P9	T11	Input	TTL
XMIT_A_6	Transmitter A, data bit 6	N9	R11	Input	TTL
XMIT_A_7	Transmitter A, data bit 7	P10	T12	Input	TTL

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
XMIT_A_K	Transmitter A, special character (data bit 8 for TBI mode)	N10	T13	Input	TTL
$\overline{\text{XMIT\_A\_IDLE}}$	Transmitter A, idle enable bar, (data bit 9 for TBI mode)	P11	T14	Input	TTL
RECV_A_0	Receiver A, data bit 0	M1	N3	Output	TTL
RECV_A_1	Receiver A, data bit 1	N1	R1	Output	TTL
RECV_A_2	Receiver A, data bit 2	M2	T1	Output	TTL
RECV_A_3	Receiver A, data bit 3	N2	P3	Output	TTL
RECV_A_4	Receiver A, data bit 4	P1	N4	Output	TTL
RECV_A_5	Receiver A, data bit 5	M5	R3	Output	TTL
RECV_A_6	Receiver A, data bit 6	M3	T2	Output	TTL
RECV_A_7	Receiver A, data bit 7	M4	T3	Output	TTL
RECV_A_K	Receiver A, special character (data bit 8 for TBI mode)	P2	U3	Output	TTL
RECV_A_9	Receiver A, data bit 9 for TBI mode	N3	T4	Output	TTL
RECV_A_IDLE	Receiver A, idle detect	L5	R4	Output	TTL
RECV_A_ERR	Receiver A, error detect	P4	R5	Output	TTL
RECV_A_RCLK	Receiver A, receive data clock	P3	U4	Output	TTL
RLINK_A_P	Receiver A, positive link input	L14	N17	Input	Link
RLINK_A_N	Receiver A, negative link input	M14	P17	Input	Link
XLINK_A_P	Transmitter A, positive link out	K12	M15	Output	Link
XLINK_A_N	Transmitter A, negative link out	L12	N15	Output	Link
XMIT_B_0	Transmitter B, data bit 0	P7	R8	Input	TTL
XMIT_B_1	Transmitter B, data bit 1	N7	T8	Input	TTL
XMIT_B_2	Transmitter B, data bit 2	L7	R7	Input	TTL
XMIT_B_3	Transmitter B, data bit 3	M7	U7	Input	TTL
XMIT_B_4	Transmitter B, data bit 4	P6	T7	Input	TTL
XMIT_B_5	Transmitter B, data bit 5	N6	U6	Input	TTL
XMIT_B_6	Transmitter B, data bit 6	P5	R6	Input	TTL
XMIT_B_7	Transmitter B, data bit 7	L6	T6	Input	TTL
XMIT_B_K	Transmitter B, special character (data bit 8 for TBI mode)	M6	U5	Input	TTL
$\overline{\text{XMIT\_B\_IDLE}}$	Transmitter B, idle enable bar, (data bit 9 for TBI mode)	N5	T5	Input	TTL

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
RECV_B_0	Receiver B, data bit 0	K3	P2	Output	TTL
RECV_B_1	Receiver B, data bit 1	L4	P1	Output	TTL
RECV_B_2	Receiver B, data bit 2	L1	M3	Output	TTL
RECV_B_3	Receiver B, data bit 3	J3	N1	Output	TTL
RECV_B_4	Receiver B, data bit 4	K4	M2	Output	TTL
RECV_B_5	Receiver B, data bit 5	K2	L3	Output	TTL
RECV_B_6	Receiver B, data bit 6	K1	M1	Output	TTL
RECV_B_7	Receiver B, data bit 7	H3	L2	Output	TTL
RECV_B_K	Receiver B, special character (data bit 8 for TBI mode)	J4	L1	Output	TTL
RECV_B_9	Receiver B, data bit 9 for TBI mode	J1	J3	Output	TTL
RECV_B_IDLE	Receiver B, idle detect	G3	K1	Output	TTL
RECV_B_ERR	Receiver B, error detect	H2	J2	Output	TTL
RECV_B_RCLK	Receiver B, receive data clock	H4	K2	Output	TTL
RLINK_B_P	Receiver B, positive link input	J14	L17	Input	Link
RLINK_B_N	Receiver B, negative link input	H14	K17	Input	Link
XLINK_B_P	Transmitter B, positive link out	K11	M14	Output	Link
XLINK_B_N	Transmitter B, negative link out	J11	L14	Output	Link
XMIT_C_0	Transmitter C, data bit 0	A7	B10	Input	TTL
XMIT_C_1	Transmitter C, data bit 1	B7	A10	Input	TTL
XMIT_C_2	Transmitter C, data bit 2	D7	C8	Input	TTL
XMIT_C_3	Transmitter C, data bit 3	C7	B8	Input	TTL
XMIT_C_4	Transmitter C, data bit 4	A6	A8	Input	TTL
XMIT_C_5	Transmitter C, data bit 5	B6	A7	Input	TTL
XMIT_C_6	Transmitter C, data bit 6	A5	B7	Input	TTL
XMIT_C_7	Transmitter C, data bit 7	D6	C7	Input	TTL
XMIT_C_K	Transmitter C, special character (data bit 8 for TBI mode)	C6	A6	Input	TTL
$\overline{\text{XMIT\_C\_IDLE}}$	Transmitter C, idle enable bar, (data bit 9 for TBI mode)	B5	B6	Input	TTL
RECV_C_0	Receiver C, data bit 0	C1	D1	Output	TTL
RECV_C_1	Receiver C, data bit 1	D2	D3	Output	TTL
RECV_C_2	Receiver C, data bit 2	D4	E2	Output	TTL

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
RECV_C_3	Receiver C, data bit 3	E2	E3	Output	TTL
RECV_C_4	Receiver C, data bit 4	E3	F2	Output	TTL
RECV_C_5	Receiver C, data bit 5	F4	F1	Output	TTL
RECV_C_6	Receiver C, data bit 6	E1	G2	Output	TTL
RECV_C_7	Receiver C, data bit 7	F2	F3	Output	TTL
RECV_C_K	Receiver C, special character (data bit 8 for TBI mode)	F1	G1	Output	TTL
RECV_C_9	Receiver C, data bit 9 for TBI mode	F3	H2	Output	TTL
RECV_C_IDLE	Receiver C, idle detect	G2	J1	Output	TTL
RECV_C_ERR	Receiver C, error detect	H1	H3	Output	TTL
RECV_C_RCLK	Receiver C, receive data clock	G1	H1	Output	TTL
RLINK_C_P	Receiver C, positive link input	E14	G17	Input	Link
RLINK_C_N	Receiver C, negative link input	F14	H17	Input	Link
XLINK_C_P	Transmitter C, positive link out	E11	G14	Output	Link
XLINK_C_N	Transmitter C, negative link out	F11	H14	Output	Link
XMIT_D_0	Transmitter D, data bit 0	D8	C10	Input	TTL
XMIT_D_1	Transmitter D, data bit 1	C8	C11	Input	TTL
XMIT_D_2	Transmitter D, data bit 2	A8	A11	Input	TTL
XMIT_D_3	Transmitter D, data bit 3	B8	B11	Input	TTL
XMIT_D_4	Transmitter D, data bit 4	D9	A12	Input	TTL
XMIT_D_5	Transmitter D, data bit 5	A9	B12	Input	TTL
XMIT_D_6	Transmitter D, data bit 6	B9	C13	Input	TTL
XMIT_D_7	Transmitter D, data bit 7	A10	A13	Input	TTL
XMIT_D_K	Transmitter D, special character (data bit 8 for TBI mode)	B10	B13	Input	TTL
$\overline{\text{XMIT\_D\_IDLE}}$	Transmitter D, idle enable bar, (data bit 9 for TBI mode)	E9	D13	Input	TTL
RECV_D_0	Receiver D, data bit 0	D3	D2	Output	TTL
RECV_D_1	Receiver D, data bit 1	E4	C3	Output	TTL
RECV_D_2	Receiver D, data bit 2	B1	C1	Output	TTL
RECV_D_3	Receiver D, data bit 3	C2	B1	Output	TTL
RECV_D_4	Receiver D, data bit 4	A1	C2	Output	TTL
RECV_D_5	Receiver D, data bit 5	C5	B3	Output	TTL

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
RECV_D_6	Receiver D, data bit 6	C3	A3	Output	TTL
RECV_D_7	Receiver D, data bit 7	C4	B4	Output	TTL
RECV_D_K	Receiver D, special character (data bit 8 for TBI mode)	A2	C4	Output	TTL
RECV_D_9	Receiver D, data bit 9 for TBI mode	B3	C5	Output	TTL
RECV_D_IDLE	Receiver D, idle detect	D5	B5	Output	TTL
RECV_D_ERR	Receiver D, error detect	A4	C6	Output	TTL
RECV_D_RCLK	Receiver D, receive data clock	A3	A4	Output	TTL
RLINK_D_P	Receiver D, positive link input	C14	E17	Input	Link
RLINK_D_N	Receiver D, negative link input	B14	D17	Input	Link
XLINK_D_P	Transmitter D, positive link out	E12	G15	Output	Link
XLINK_D_N	Transmitter D, negative link out	D12	F15	Output	Link
TBIE	10-bit interface enable	N12	T15	Input	TTL
HSE	Half speed enable	A12	B15	Input	TTL
DDRE	Double data rate enable	D10	C14	Input	TTL
BSYNC_0	Byte synchronization mode Select 0	P12	R13	Input	TTL
BSYNC_1	Byte synchronization mode select 1	M12	U15	Input	TTL
ADIE	Add/Drop idle enable	C11	C15	Input	TTL
REPE	Repeater mode enable	A13	C16	Input	TTL
RCCE	Recovered clock enable	C12	E14	Input	TTL
REF_CLK	Reference clock	B11	A15	Input	TTL
MEDIA	Media impedance select	N13	R16	Input	TTL
WSE	Word synchronization enable	B12	B16	Input	TTL
WSE_GEN	Generate word synchronization event	M10	R12	Input	TTL
PLL_TPA	PLL analog test point	H12	K15	Output	Analog
TST_0	Test mode select 0	N11	U14	Input	TTL
TST_1	Test mode select 1	L10	U13	Input	TTL
LBE	Loop back enable	P13	R14	Input	TTL
LBOE	Loop back output enable	P14	P13	Input	TTL
STNDBY	Standby mode enable	C10	A14	Input	TTL
$\overline{\text{RESET}}$	System reset bar	A11	B14	Input	TTL

Table 7-2. Signal to Ball Mapping for 196 MAPBGA and 217 PBGA Packages

Signal Name	Description	Ball Number (196 MAPBGA)	Ball Number (217 PBGA)	Direction	I/O Type
COREVDD	Core logic supply	E5, E6, F5, G5, H5, J5, K5, K6, K7, K8, K9, K10, J10, H10, G10, F10, E10	P9, P7, D9, A2, A9, B9, U9, T9, C9, R9, U16, U2, P11, L4, J4, G4, D11, D7, D5, A16	Vdd	Supply
COREGND/PADGND	Core logic ground / TTL I/O ground	E7, E8, F6, F7, F8, F9, H6, H7, H8, H9, G6, G7, G8, G9, J6, J7, J8, J9	P14, R15, U17, U1, T16, P12, P10, P8, P6, P4, M4, K10, K9, K8, K4, J10, J9, J8, H10, H9, H8, H4, F4, D12, D10, D8, D6, D4, B2, A17, A1	GND	Ground
PLLAVDD	PLL analog supply	H13	K16	AVdd	Supply
PLLAGND	PLL analog ground	G13	J16	GND	Ground
PADVDD	TTL I/O supply	B2, D1, G4, J2, L2, L3, N4, M9, C9, B4	E4,E1, G3, K3, N2, R2, P5, U12, C12, A5	OVdd	Supply
XPADVDD	Link I/O supply	L13, K13, G12, E13, D11, D13, M11, M13, J13, F13, B13	N16, M16, J15, G16, F16, B17, K14, L16, D16, E16, H16, P16, D14	XVdd	Supply
XPADGND	Link I/O Ground	K14, J12, G11, F12, D14, N14, L11, G14, A14, H11, C13	M17, L15, J14, H15, F17, E15, N14, R17, J17, F14, C17, P15, T17, D15	GND	Ground

Appendix A
Ordering Information

Figure A-1 provides the Motorola part numbering nomenclature for the MC92600 SERDES. For product availability, contact your local Motorola Semiconductor sales representative.

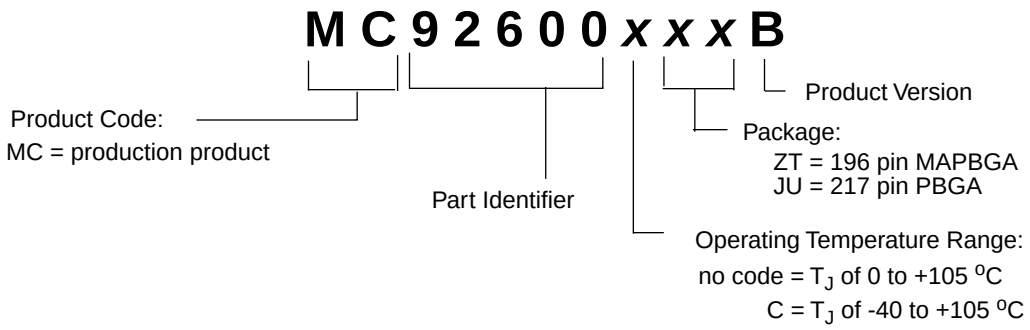


Figure A-1. Motorola Part Number Key

Appendix B
8B/10B Coding Scheme

The MC92600 provides fibre channel-specific 8B/10B encoding and decoding based on the FC-1 fibre channel standard. Given 8 bits entering a channel, the 8B/10B encoding converts them to 10 bits thereby increasing the transition density of the serially transmitted signal.

B.1 Overview

The FC-1 standard applies an algorithm that ensures that no more than five 1's or 0's are transmitted consecutively, giving a transition density equal to 2.5 for each 10 bit data block. Such a density ensures proper DC balance across the link and is sufficient for good clock recovery.

In the 8B/10B notation scheme, bytes are referred to as transmission characters, and each bit is represented by letters. Unencoded bits, the 8 bits that have not passed through a 8B/10B encoder, are represented by letters "A" through "H", which are bits 0 through7.

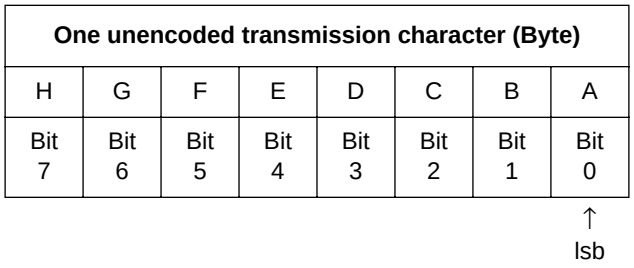


Figure B-1. Unencoded Transmission Character Bit Ordering

Encoded bits, those that have passed through an encoder, are represented with the letters "a" through "j", representing bits 0–9 respectively. Character (bit) ordering in the fibre channel nomenclature is little-endian, with "a" being the least significant bit in a byte.

One coded transmission character (Byte)									
j	h	g	f	i	e	d	c	b	a
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
									↑ lsb

Figure B-2. Encoded Transmission Character Bit Ordering

B.1.1 Naming Transmission Characters

Transmission characters are given names based on the type of data in the byte and the bit values of the character. Two types of transmission characters are specified: data and special. Data characters are labeled “D” characters and special characters are labeled “K” characters. Each transmission character has a bit value and a corresponding decimal value. These elements are combined to provide each character with a name, see Table B-1.

Table B-1. Components of a Character Name

H G F	E D C B A	8B/10B notation
0 0 1	1 1 1 0 0	Data bit value
1	28	Decimal value of the bit value
D or K		Kind of transmission character
D28.1 = Data name assigned to this data byte if it is a data character. K28.1 = Data name assigned to this data byte if it is a special character.		

B.1.2 Encoding

Following is a simplified sequence of steps in 8B/10B coding:

1. An 8-bit block of unencoded data (a transmission character) is picked up by a transmitter.
2. The transmission character is broken into sub-blocks of three bits and five bits. The letters H G and F comprise the 3-bit block, and the letters E D C B and A comprise the 5-bit block.
3. The 3-bit and 5-bit sub-blocks pass through a 3B/4B encoder and a 5B/6B encoder, respectively. A bit is added to each sub-block, such that the transmission character is encoded and expanded to a total of 10-bits.
4. At the time the character is expanded into 10 bits, it is also encoded into the proper running disparity, either positive (RD+) or negative (RD-) depending on certain calculations (see Section B.1.3, “Calculating Running Disparity”). At start-up, the transmitter assumes negative running disparity.

5. The positive or negative disparity transmission character (see Figure B-3) is passed to the transmit driver, available for differentialization (See Section 2.5.2, “Transmit Driver Operation”).

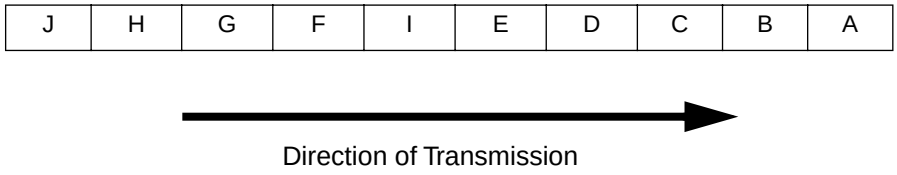


Figure B-3. Character Transmission

B.1.3 Calculating Running Disparity

Running disparity improves error detection and recovery. The rules for calculating the running disparity for sub-blocks are as follows (reference *Fibre Channel, Gigabit Communications and I/O for Computer Networks*):

- Running disparity at the end of any sub-block is positive if (1) the encoded sub-block contains more 1s than 0s, (2) if the 6-bit sub-block is 6’b00 0111, or (3) if the 4-bit sub-block is 4’b0011.
- Running disparity at the end of any sub-block is negative if (1) the encoded sub-block contains more 0 than 1 bits, (2) if the 6-bit sub-block is 6’b11 1000, or (3) if the 4-bit sub-block is 4’b1100.
- Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

B.2 Data Tables

Table B-2 displays the full valid data character 8B/10B codes. The values in the “Data Value HGFEDCBA” column are the possible bit values of the unencoded transmission characters. The current RD values are the possible positive and negative running disparity values.

Table B-2. Valid Data Characters

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	010101 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table B-3 displays the full valid special character 8B/10B codes.

Table B-3. Valid Special Characters

Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdie fghj
K28.0	000 11100	001111 0100	110000 1011	K28.6	110 11100	001111 0110	110000 1001
K28.1	001 11100	001111 1001	110000 0110	K28.7	111 11100	001111 1000	110000 0111
K28.2	010 11100	001111 0101	110000 1010	K23.7	111 10111	111010 1000	000101 0111
K28.3	011 11100	001111 0011	110000 1100	K27.7	111 11011	110110 1000	001001 0111
K28.4	100 11100	001111 0010	110000 1101	K29.7	111 11101	101110 1000	010001 0111
K28.5	101 11100	001111 1010	110000 0101	K30.7	111 11110	011110 1000	100001 0111

Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book. Some of the terms and definitions included in the glossary are reprinted from IEEE Std 754-1985, *IEEE Standard for Binary Floating-Point Arithmetic*, copyright ©1985 by the Institute of Electrical and Electronics Engineers, Inc., with the permission of the IEEE.

A

Asserted. Indicates active state of signal has been set. Refers to either inputs or outputs.

B

BERC. Bit Error Rate Checking.

BERT. Bit Error Rate Testing.

BIST. Built-In Self-Test.

Bit alignment. Refers to the transition tracking loop recovering data bits from the serial input stream.

Byte. Eight bits of uncoded data.

Byte alignment. Receiver identification of character boundaries through use of Idle character recognition.

C

Character. An 8B/10B encoded byte of data.

G

Gigabit. A unit of speed of data transfer. One gigabit indicates a data throughput of 1 billion bits per second requiring a transfer rate of 1.25 billion symbols per second of 8B/10B encoded data.

Gigabaud. A unit of speed of symbol transfer. One gigabaud indicates a data throughput of 800 million bits per second requiring a transfer rate of 1.0 billion symbols per second of 8B/10B encoded data.

I

ISI. Inter Symbol Interference, a distortion caused by the high-frequency loss characteristics of the transmission media.

N

Negated. Indicates inactive state of signal has been set. Refers to either inputs or outputs.

P

PLL. Phase Locked Loop.

PPM. parts per million.

R

Running disparity. The amount of DC imbalance over a history of symbols transmitted over a link. Equal to the difference between the number of one and zero symbols transmitted.

S

Symbol. One piece of information sent across the link; different from a bit in that bit implies data where symbol is encoded data.

W

Word synchronization. Alignment of four or more receivers' data by adjusting for differences in media and systemic delay between them such that data is presented by the receivers in the same grouping as they were transmit.

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U

W

X