ABOV SEMICONDUCTOR Co., Ltd.
8-BIT MICROCONTROLLERS

MC95FB204

User's Manual (Ver. 1.7)

ABOV
SEMICONDUCTOR

REVISION HISTORY

VERSION 1.7 (July 17, 2012) This book

The specification for internal RC oscillator characteristics is changed from ±5% to ±8%.

(Min. : 7.6 → 7.35MHz, Max. : 8.4 → 8.65MHz)

VERSION 1.6 (May 25, 2012)

The notice for ADCRH&ADCM2 reading is added at ADC register description.

VERSION 1.5 (May 18, 2012)

The description for " Reference Voltage Out(1.80V VDC)" is added at 11. CC/CV block.

The errata for each function are fixed at the 11. CC/CV block, 12. Clock Generator and 18.RESET paragraphs.

Company logo is added at the rear end of header.

VERSION 1.4 (May 15, 2012)

The maximum values for IDD2/IDD4/IDD5 specification are changed to 2mA/1.5mA/1.5mA.

POR level is corrected to 1.8V±0.1V at 7.5 Power-On Reset Characteristics.

TBD values are corrected to 10ms/20uA/1uA at 7.7 Internal WDTRC Oscillator Characteristics.

VERSION 1.3 (December 02, 2011)

"Instructions on how to use the input port" is added at the Appendix D.

VERSION 1.2 (December 24, 2010)

MC95FB104(16pin PKG) is eliminated.

Fixed some errata in 12.5 12-Bit A/D Converter on page 83 and 87.

VERSION 1.1 (July 7, 2010)

Fixed some errata in 16.Memory Programming on page 106 and 17.Configure Option on page 120.

VERSION 1.0 (July 2, 2010)

7.10 CC/CV Characteristics at page 29 are chagned.

The paragraph "11.The CC/CV Block" at page 61 are changed.

VERSION 0.3 Preliminary (March 19, 2010)

Device name is changed to MC95FB204 from MC94FB204.

The name of PSR0,1 are changed ALCPR0,1 and they(ALCPR0,1) are corrected to read/writeable register from write only.

P22 pull-up register(P22PU=1) value is corrected to 1 at initial status because it is combined with RESET pin.

200mV CC regulation voltage is eliminated at CC/CV block and the voltage of Ictrl pin is assigned to CC reference voltage. Also Ictrl pin is assigned to AN12.

VERSION 0.2 Preliminary (September 22, 2009)

Voltage input hign/low characteristics are changed.

VERSION 0.1 Preliminary (September 8, 2009)

Version 1.7
Published by FAE Team

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MC95FB204

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER FOR BATTERY CHARGER

1. Overview

1.1 Description

The MC95FB204 is advanced CMOS 8-bit microcontroller with embedded CC/CV circuit. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 4K bytes of FLASH, 256 bytes of RAM, general purpose I/O, 8/16-bit timer/counter, watchdog timer, on-chip POR, 12-bit A/D converter, 10-bit PWM output, on-chip oscillator and clock circuitry. The MC95FB204 also supports power saving modes to reduce power consumption.

Device Name	FLASH	RAM	ADC	I/O PORT	Package
MC95FB204	4K bytes	256 bytes	10 channel	17	20 SOP/TSSOP

1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible,2 clock per cycle)
- **4K Bytes On-chip FLASH**
  - Endurance : 100,000 times
  - Retention : 10 years
- **256 Bytes SRAM**
- **General Purpose I/O**
  - 17 Ports (P2[2:0], P1[5:0], P0[7:0])
- **One Basic Interval Timer**
- **Timer/ Counter**
  - 8Bit×2ch(16Bit×1ch)
- **One 10-bit PWM**
- **Watch Dog Timer**
- **12 Bit A/D Converter**
  - 10 External ADC Input channels
  - 4 Internal source : V_{SENSE} , I_{CTRL} of CC/CV, 1.8V VDC, Ext. VDD
- **Interrupt Sources**
  - External (2)
  - Timer (2)
  - ADC (1)
  - WDT (1)
  - BIT (1)
- **On-Chip RC-Oscillator**
  - 8MHz(±8%,INT-RC), 1MHz(±30%,WDTRC)
- **Power On Reset**
- **Minimum Instruction Execution Time**
  - 250ns (@8MHz, NOP Instruction)
- **Power down mode**
  - IDLE, STOP1, STOP2 mode
- **Operating Frequency**
  - 1.0 MHz ~ 8.0 MHz
- **Operating Voltage**
  - 2.2 ~ 5.5V (@1~8MHz)
  - 3.0 ~ 5.5V (@CC/CV block)
- **Operating Temperature : -40 ~ +85℃**
- **Package Type**
  - 20 SOP / TSSOP
  - Pb free package

1.3 Ordering Information

Table 1-1 Ordering Information of MC95FB204

Device name	ROM size	RAM size	Package
MC95FB204D	4Kbyte	256 byte	20 SOP
MC95FB204R			20 TSSOP

1.4 Development Tools

1.4.1 Compiler

We do not provide the compiler. Please contact third parties.

The MC95FB204 core is Mentor 8051. Anyway, device ROM size is smaller than 64KB. Developer can use all kinds of third party's standard 8051 compiler.

1.4.2 OCD emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two wires interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And also the OCD controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- DSCL (MC95FB204 P06 port)
- DSDA (MC95FB204 P07 port)

OCD connector diagram: Connect OCD and user system

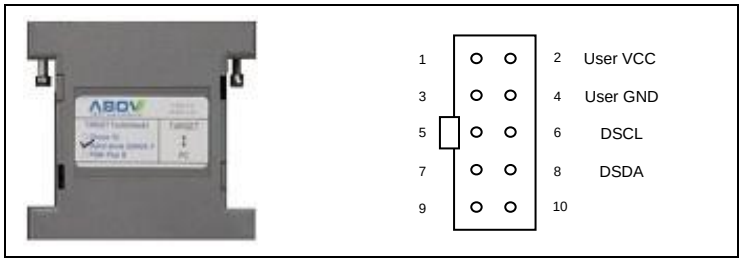


Figure 1.1 OCD Debugger and Pin description

1.4.3 Programmer

Single programmer:

PGMplus USB: It programs MCU device directly.

Figure 1.2 Single Programmer

OCD emulator: It can write code in MCU device too.

Because of, OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer:

It programs 8 MCU devices at once.

So, it is mainly used in mass production line.

Gang programmer is standalone type, it means it does not require host PC.

Figure 1.3 Gang Programmer

2. Block Diagram

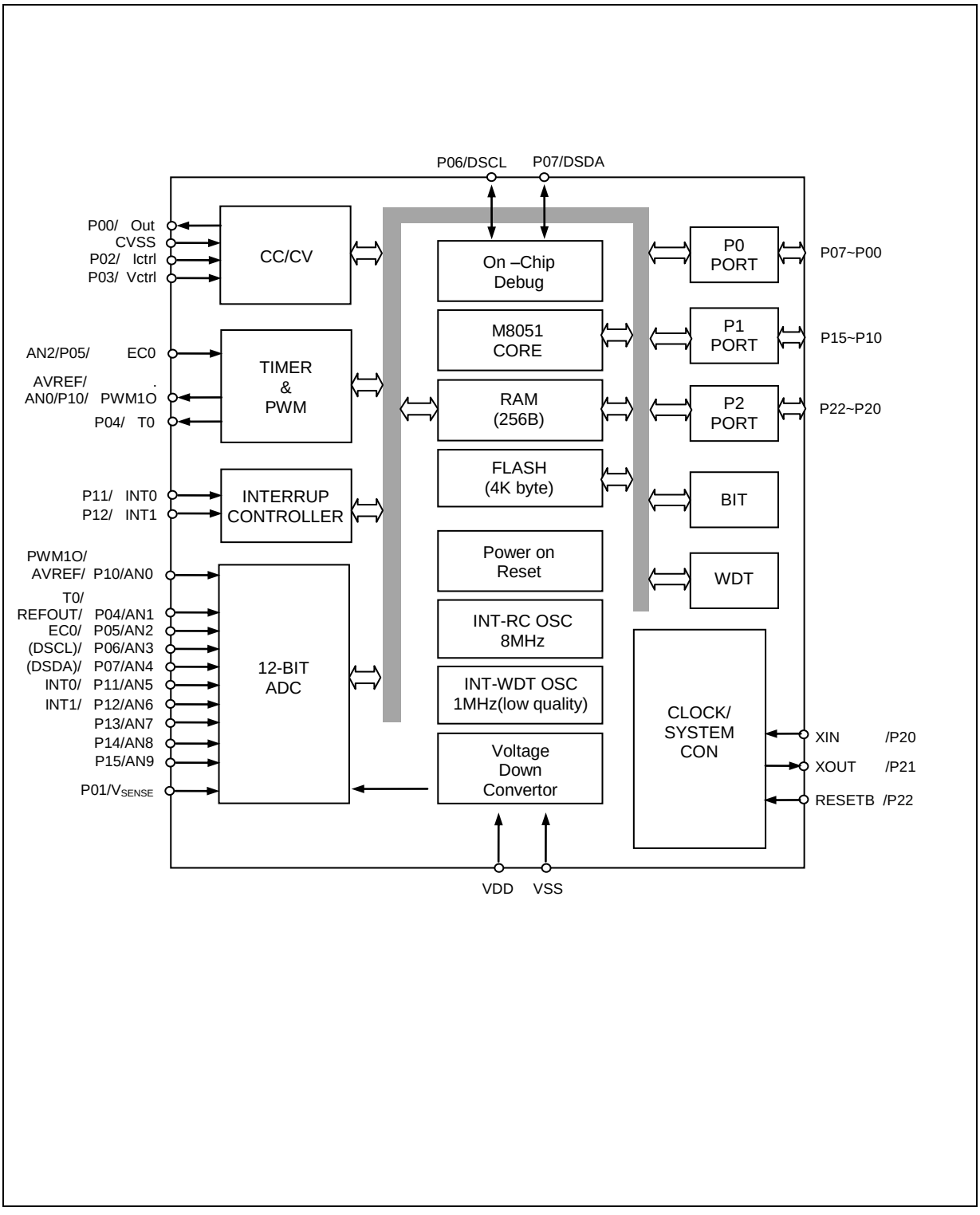


Figure 2.1 MC95FB204 block diagram

3. Pin Assignment

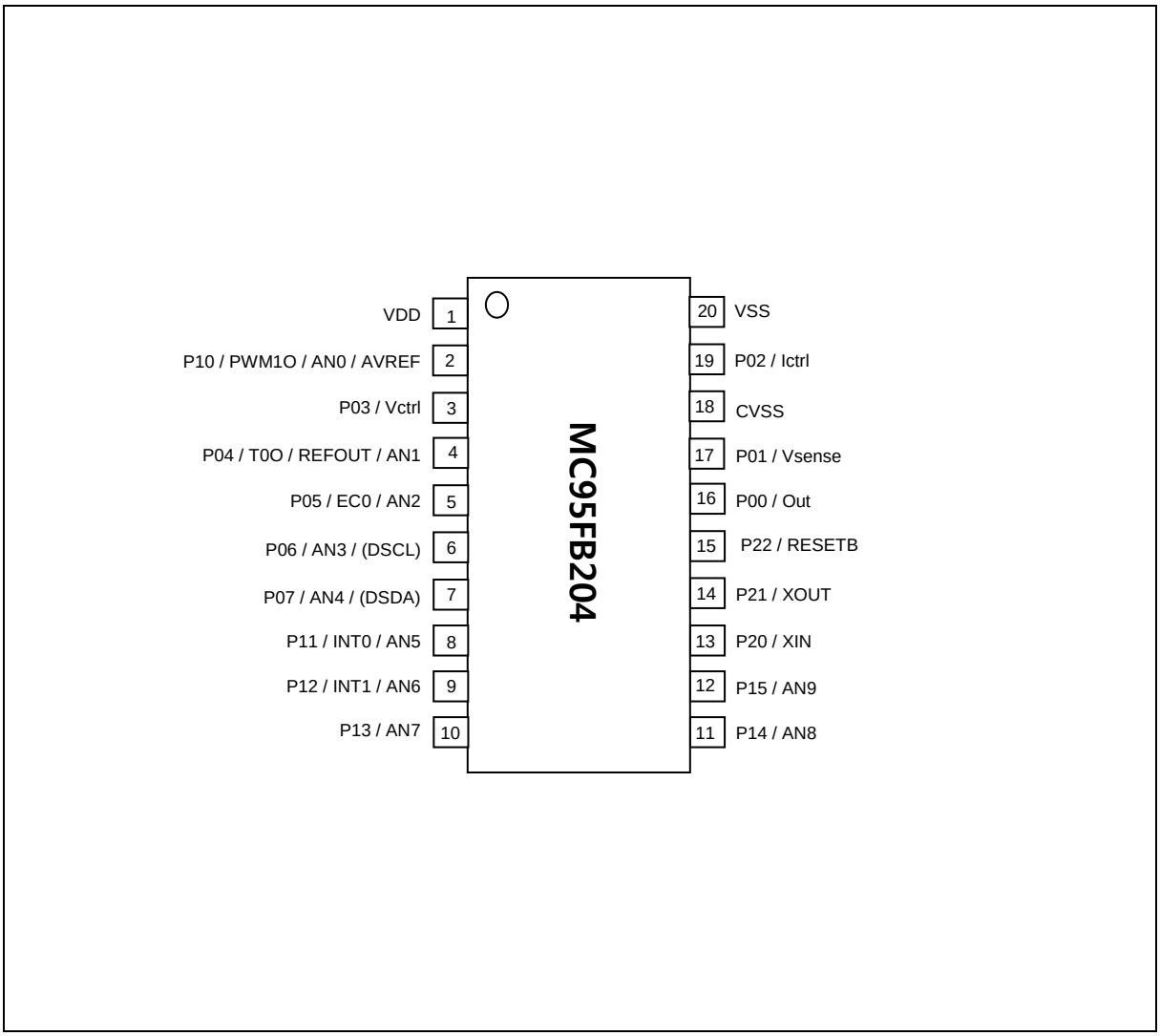


Figure 3.1 MC95FB204 20 SOP/TSSOP Pin assignment

NOTE)

- On On-Chip Debugging, ISP uses P0[6:7] pin as DSCL, DSDA.
- Above functions are written in pin priority order. Most left side function has a lowest priority.
  For example, In pin 2, if P10, PWM1O, AN0 and AVREF are set, AVREF will be operated.

4. Package Diagram

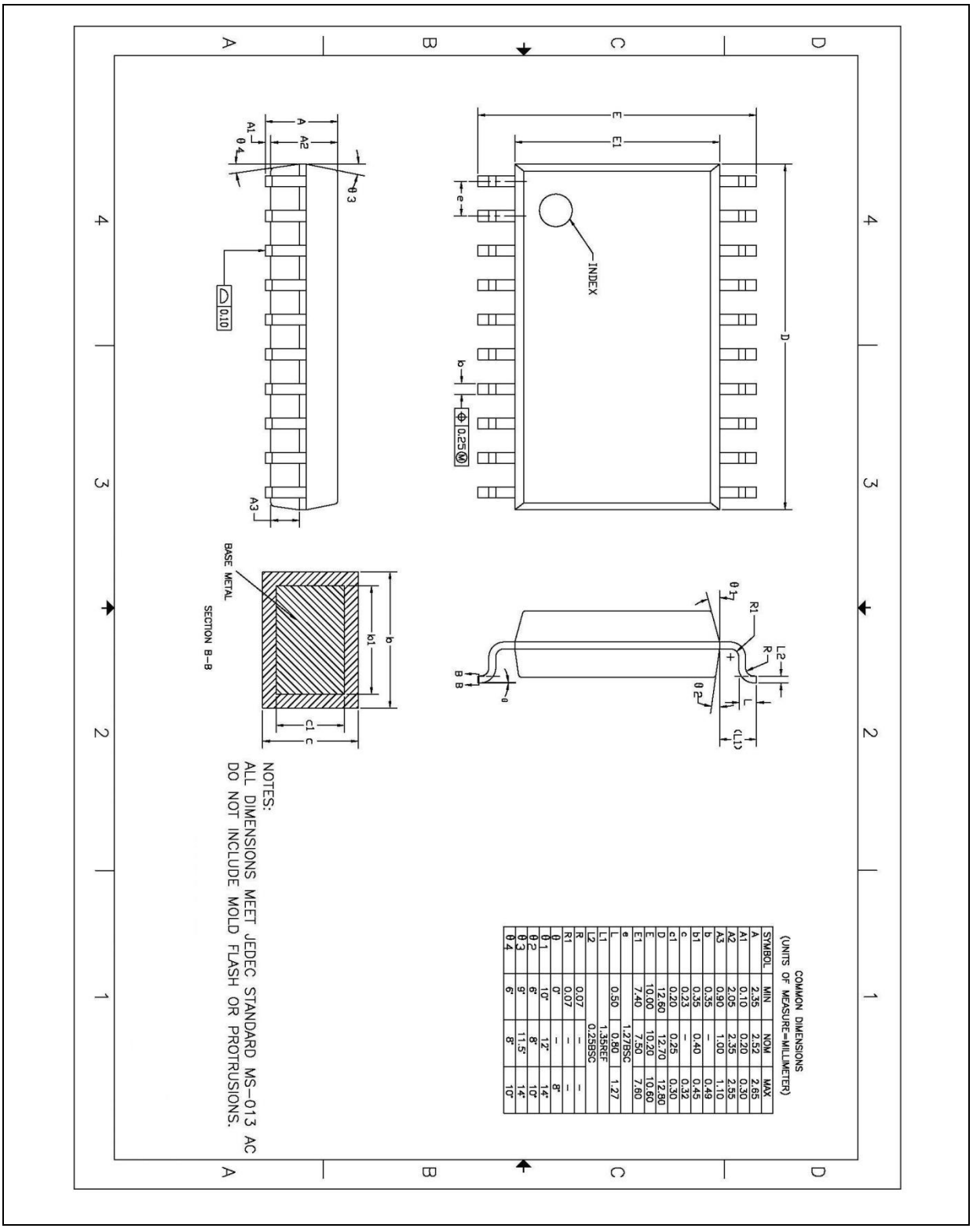
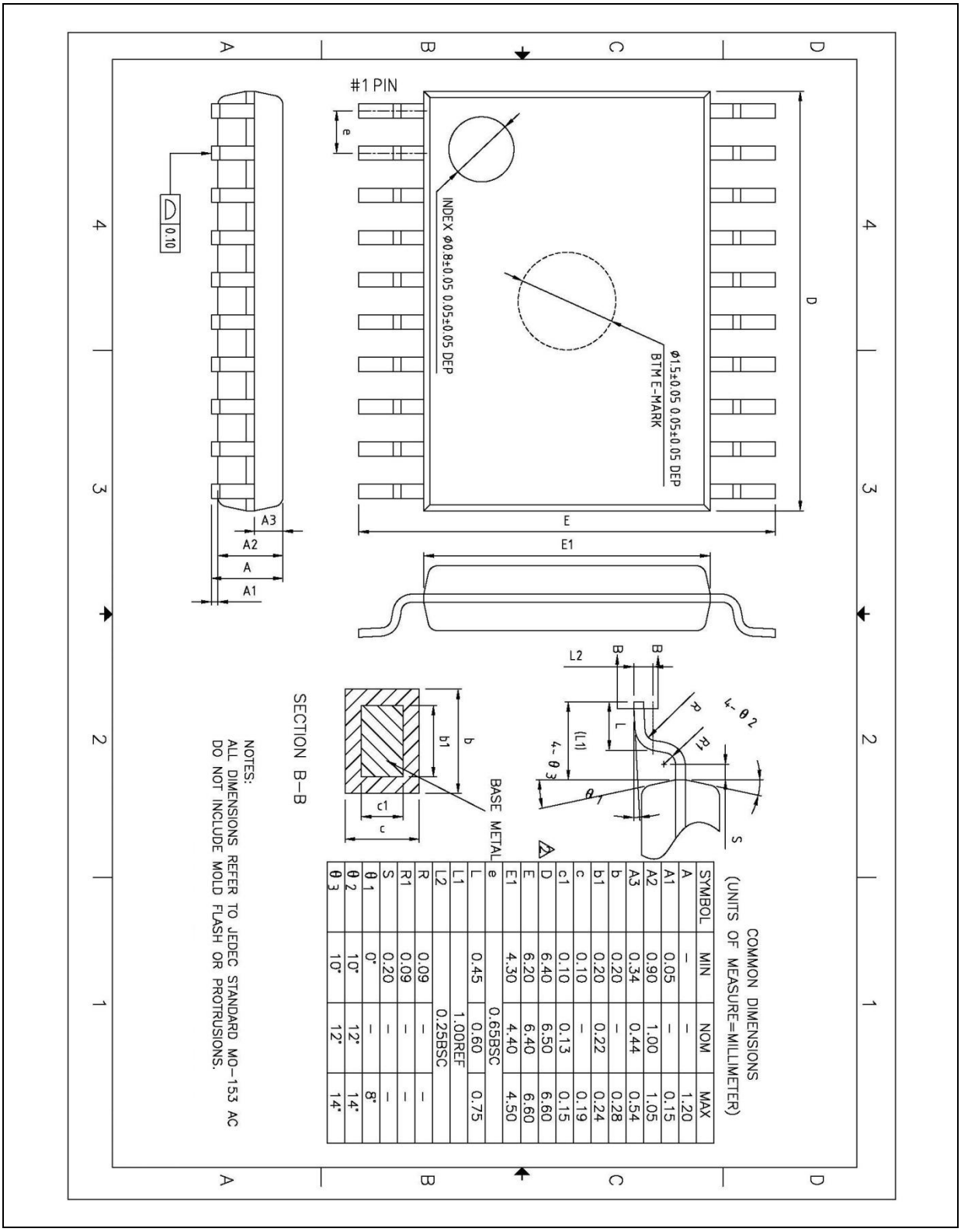


Figure 4.1 20 pin SOP package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

Figure 4.2 20 pin TSSOP package

5. Pin Description

Table 5-1 Normal pin description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port P0 8-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port. But P00 can be used regardless of input/output mode Open Drain enable register can be used via software when this port is used as output port AN0~AN7 can be selected by ADCM register	Input	Out
P01				Vsense
P02				Ictrl
P03				Vctrl
P04				REFOUT/AN1/T0
P05				AN2/EC0
P06				AN3
P07				AN4
P10	I/O	Port P1 7-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port AN8, AN9 can be selected by ADCM register	Input	AN0/AVREF/PWM1O
P11				AN5/INT0
P12				AN6/INT1
P13				AN7
P14				AN8
P15				AN9
-				-
-				-
P20	I/O	Port P2 3-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port	Input	XIN
P21				XOUT
P22	I			RESETB
-	-			-

6. Port Structures

6.1 General Purpose I/O Port

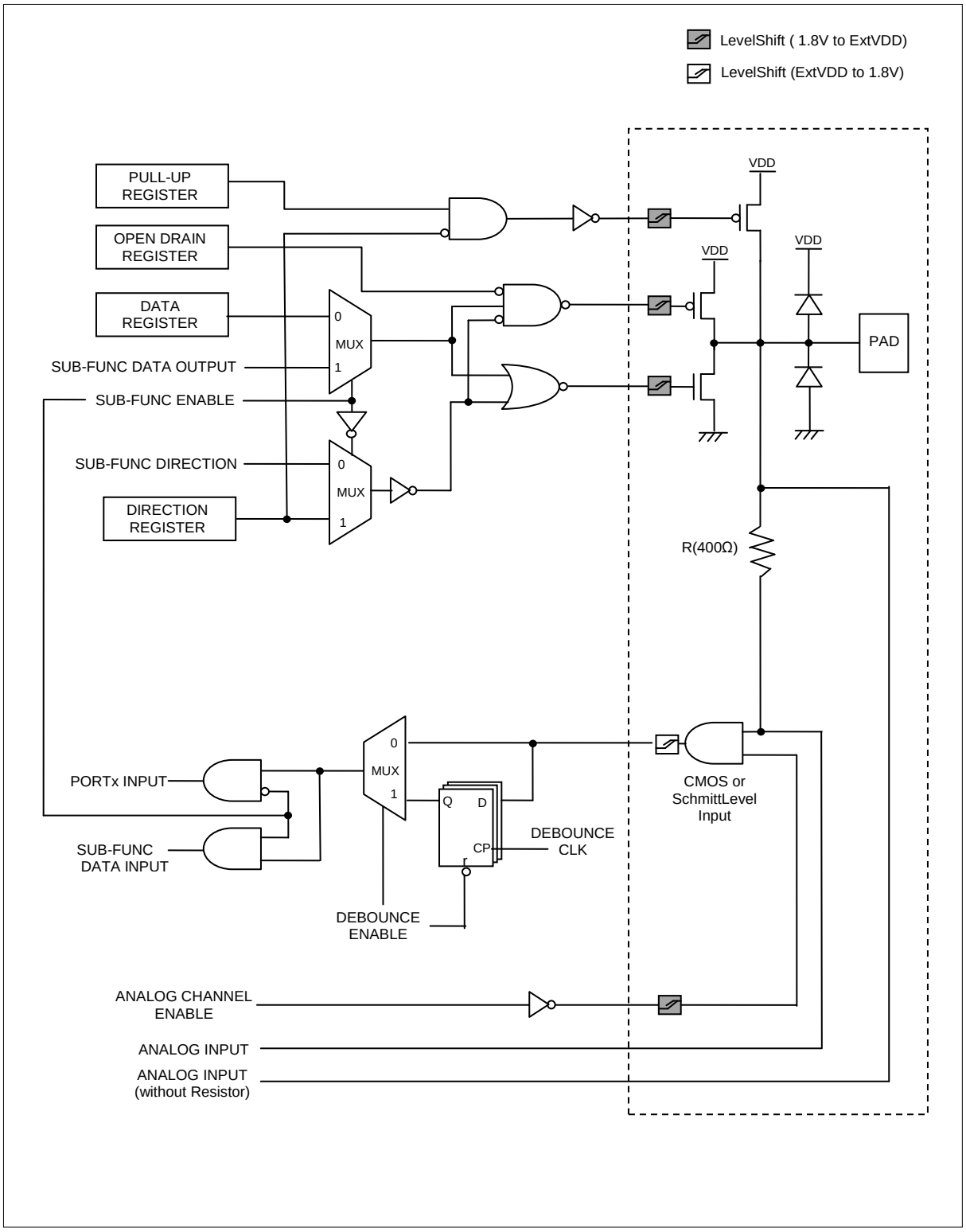


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

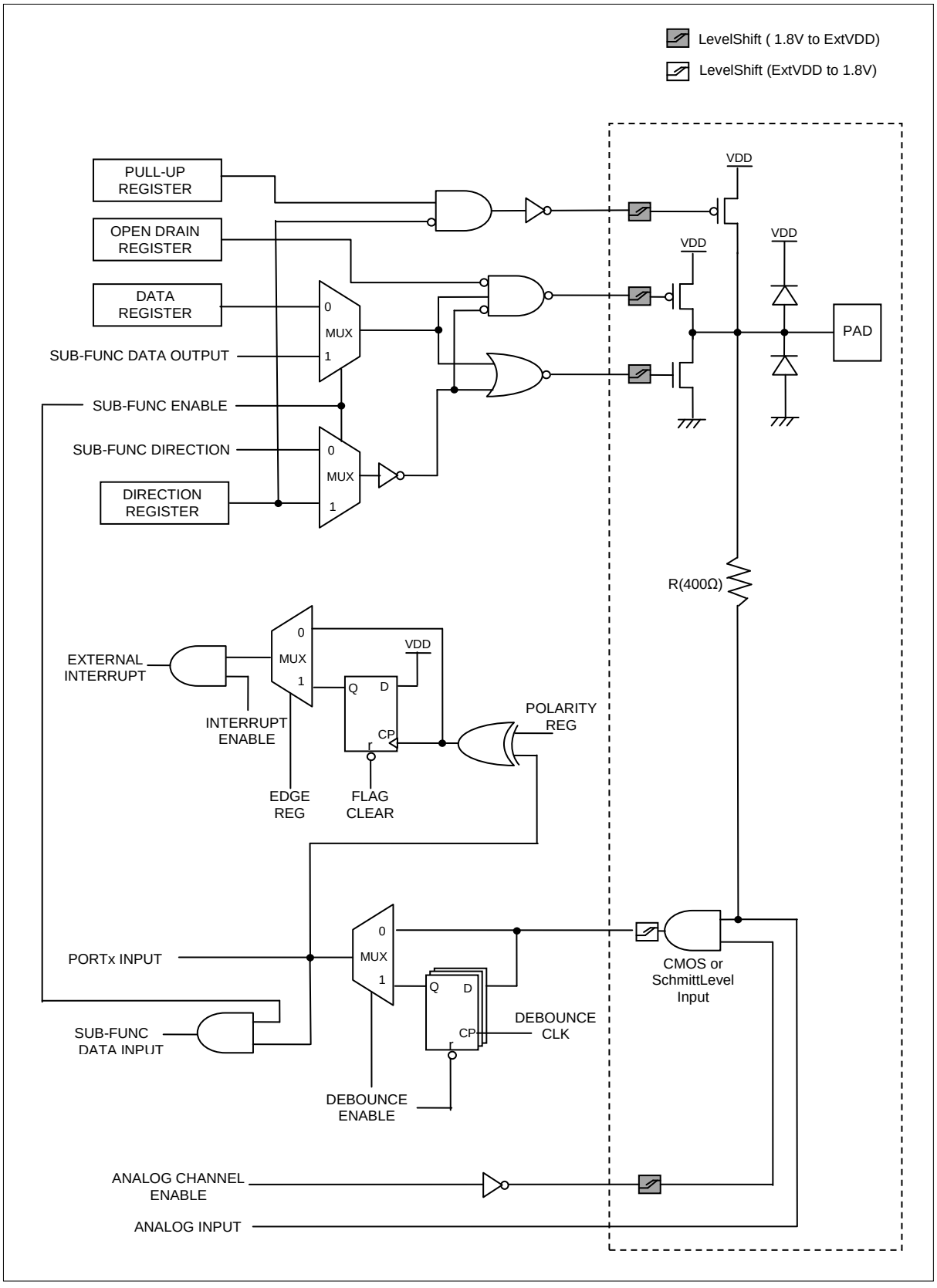


Figure 6.2 External Interrupt I/O Port

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~+6.5	V
	VSS	-0.3~+0.3	V
Normal Voltage Pin	VI	-0.3~VDD+0.3	V
	VO	-0.3~VDD+0.3	V
	IOH	10	mA
	∑IOH	80	mA
	IOL	20	mA
	∑IOL	160	mA
Total Power Dissipation	PT	600	mW
Storage Temperature	TSTG	-45~+125	℃

Note) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-2 Recommended Operation Conditions

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage	VDD	fXIN=1.0~8MHz	2.2	-	5.5	V
Operating Temperature	TOPR	VDD=2.2~5.5V	-40	-	85	℃
Operating Frequency	FOPR	fXIN	1	-	8	MHz
	FRC8	Internal RC-OSC	-	8	-	MHz
	FRC1	Internal WDT RC-OSC	-	1	-	MHz

7.3 A/D Converter Characteristics

Table 7-3 A/D Converter Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Resolution		-	-	12	-	bits
Total Accuracy		AVDD=VDD=5.12V fXIN=4MHz		-	±3(Avref base)	lsb
Integral Linear Error	INL		-	-	±2	lsb
Differential Linearity Error	DLE		-	-	±1	lsb
Zero Offset Error	ZOE		-		±3	lsb
Full Scale Error	FSE		-		±3	lsb
Conversion Time	tCON	12bit conversion Max. 3MHz	-	60	-	cycle
Analog Input Voltage	VAN	-	VSS	-	AVDD=VDD	V
Analog Power Voltage	AVDD	-	-	*AVDD=VDD	-	V
Analog Reference Voltage	AVREF	-	2.2	-	AVREF=AVDD	V
Analog Ground Voltage	AVSS	-	-	VSS	-	V
Analog Input Leakage Current		AVDD=VDD=5.12V	-	-	10	uA
ADC Operating Current	IDD	AVDD=VDD=5.12V	-	1	3	mA
	SIDD		-	-	1	uA

(TA=-40℃ ~ +85℃, VDD=AVDD=2.2V ~ 5.5V, VSS=0V)

7.4 Voltage Dropout Converter Characteristics

Table 7-4 Voltage Dropout Converter Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	2.2	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Regulation Voltage		-	1.62	1.8	1.98	V
Drop-out Voltage		-	-	-	0.02	V
Current Drivability		RUN/IDLE	-	10	-	mA
		SUB-ACTIVE	-	1	-	mA
		STOP1	-	50	-	uA
		STOP2	-	10	-	uA
Operating Current	IDD1	RUN/IDLE	-	-	1	mA
	IDD2	SUB-ACTIVE	-	-	0.1	mA
	SIDD1	STOP1	-	-	5	uA
	SIDD2	STOP2	-	-	0.1	uA
Drivability Transition Time	TRAN1	SUB to RUN	-	-	1	uS
	TRAN2	STOP to RUN	-	-		

Note) -STOP1: WDT running - STOP2: WDT disable

7.5 Power-On Reset Characteristics

Table 7-5 Power-On Reset Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	VSS	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
RESET Release Level		-	1.7	1.8	1.9	V
Operating Current	IDD	-	-	-	10	uA
	SIDD	-	-	-	1	uA

7.6 Internal RC Oscillator Characteristics

Table 7-6 Internal RC Oscillator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	2.2	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Frequency		-	7.35	8.0	8.65	MHz
Hysteresis		-	-	-	10	mS
Operating Current	IDD	-	-	-	-	uA
	SIDD	-	-	-	1	uA

7.7 Internal WDTRC Oscillator Characteristics

Table 7-7 Internal WDTRC Oscillator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	2.2	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Frequency		-	-	1	-	MHz
Stabilization Time		-	-	-	10	mS
Operating Current	IDD	-	-	-	20	uA
	SIDD	-	-	-	1	uA

7.8 DC Characteristics

Table 7-8 DC Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Low Voltage	VIL1	RESETB (External Reset Active) P00~P03, P10~P12, P22	-0.3	-	0.2VDD	V
	VIL2	P04~P07, P13~P16, P20~P21	-0.3	-	0.2VDD	V
Input High Voltage	VIH1	RESETB (External Reset Active) P00~P03, P10~P12, P22	0.8VDD	-	VDD+0.3	V
	VIH2	P04~P07, P13~P16, P20~P21	0.7VDD	-	VDD+0.5	V
Output Low Voltage	VOL1	P0,P1,P2 (IOL=20mA, VDD=4.5V)	-	-	1	V
Output High Voltage	VOH1	P0,P1,P2 (IOH=-8.57mA, VDD=4.5V)	3.5	-	-	V
Input High Leakage Current	IIH	P0,P1,P2			1	uA
Input Low Leakage Current	IIL	P0,P1,P2	-1			uA
Pull-Up Resister	RPU	P0,P1,P2	20	-	50	kΩ
Power Supply Current	IDD1	Run Mode, fXIN=8MHz@5V	-	-	15	mA
	IDD2	Sleep Mode, fXIN=8MHz@5V	-	-	2	mA
	IDD4	STOP1 Mode,WDT Active@5V	-	-	1.5	mA
	IDD5	STOP2 Mode,WDT Disable@5V	-	-	1.5	mA

(VDD =2.2~5.5V, VSS =0V, fXIN=8.0MHz, TA=-40~+85℃)

Note) -STOP1: WDT running - STOP2: WDT disable

7.9 AC Characteristics

Table 7-9 AC Characteristics

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Operating Frequency	fMCP	XIN	1	-	10	MHz
System Clock Cycle Time	tSYS	-	100	-	1000	ns
Oscillation Stabilization Time (8MHz)	tMST1	XIN, XOUT	-	-	10	ms
External Clock “H” or “L” Pulse Width	tCPW	XIN	90	-	-	ns
External Clock Transition Time	tRCP,tFCP	XIN	-	-	10	ns
Interrupt Input Width	tIW	INT0~INT3	2	-	-	tSYS
RESETB Input Pulse “L” Width	tRST	RESETB	8	-	-	tSYS
External Counter Input “H” or “L” Pulse Width	tECW	EC0,EC1	2	-	-	tSYS
Event Counter Transition Time	tREC,tFEC	EC0,EC1	-	-	20	ns

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

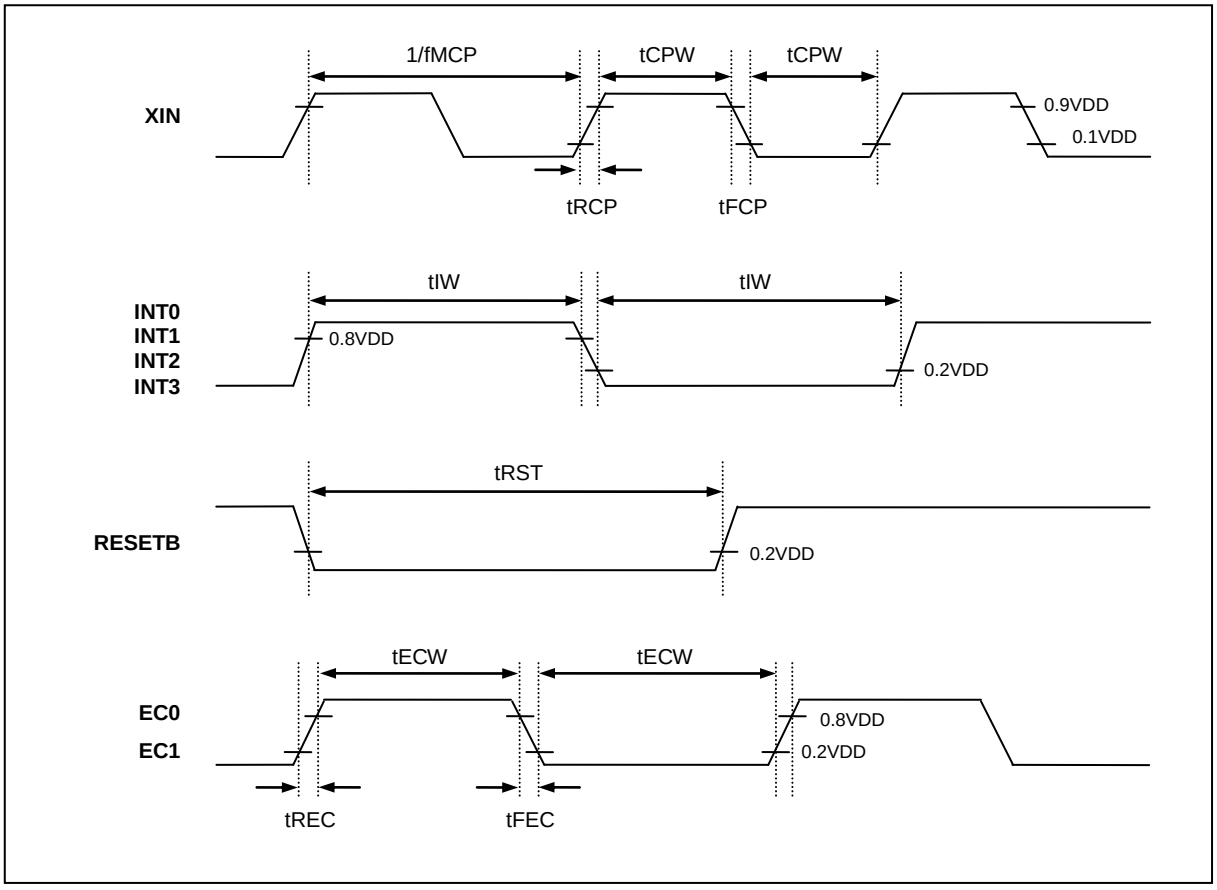


Figure 7.1 AC Timing

7.10 CC/CV Characteristics

Table 7-10 CC/CV Characteristics

Parameter	Symbol	TEST CONDITION	MIN	TYP	MAX	Unit
Current Consumption - not taking the output sinking current into account	I_{CC}			0.2	0.4	mA
		0 < TA < 85℃			0.5	
Transconduction gain(Vctrl). sink current only(1)	Gmv		1	3.5		mA /mV
		0 < TA < 50℃	0.5			
Voltage control loop reference(2)	Vref		1.204	1.210	1.216	V
		0 < TA < 50℃	1.186		1.234	
Input bias current (Vctrl)	Iibv			50		nA
		0 < TA < 85℃				
Transconduction gain (Ictrl). sink current only	Gmi		1.5	7		mA /mV
		0 < TA < 50℃	0.8			
Input offset voltage deviation(3) (Vsense vs. Ictrl)	V_{SENSE}	I_O = 2.5mA	15	20	25	mV
		0 < TA < 50℃ I_O = 2.5mA	8	20	32	
Current out of pin ICTRL at -200mV	Iibi			25		uA
		0 < TA < 85℃				
Low output voltage at 10mA sinking current	V_{OL}			200		mV
Output short circuit current. Output to vcc. Sink current only	I_{OS}			27	65	mA
		0 < TA < 50℃				

(VDD =3.0v~5.5v, TA= 25℃, unless otherwise specified)

1. If the voltage on VCTRL (the positive input of the amplifier) is higher than the negative amplifier input(Vref = 1.210 V), and it is increased by 1mV, the sinking current at the output OUT will be increased by 3.5 mA.

2. The internal Voltage Reference is set at 1.210 V (bandgap reference). The voltage control loop precision takes into account the cumulative effects of the internal voltage reference deviation as well as the input offset voltage of the trans-conductance operational amplifier. The internal Voltage Reference is fixed by bandgap, and trimmed to 0.5 % accuracy at room temperature.

3. The current control loop precision takes into account the cumulative effects of the Ictrl voltage reference deviation as well as the input offset voltage of the trans-conduction operational amplifier.

7.11 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

8. Memory

The MC95FB204 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be assessed by 8-bit addresses, which can be more quickly stored and manipulated by 8-bit CPU. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

Program memory can only be read, not written to. There can be up to 64K bytes of Program memory. In the MC95FB204 FLASH version of these devices the 4K bytes of Program memory are provided on-chip. Data memory can be read and written to up to 256 bytes internal memory (DATA) including the stack area.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64K bytes, but this device has just 4K bytes program memory space.

Figure 8.1 shows a map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 0, for example, is assigned to location 000BH. If external interrupt 0 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

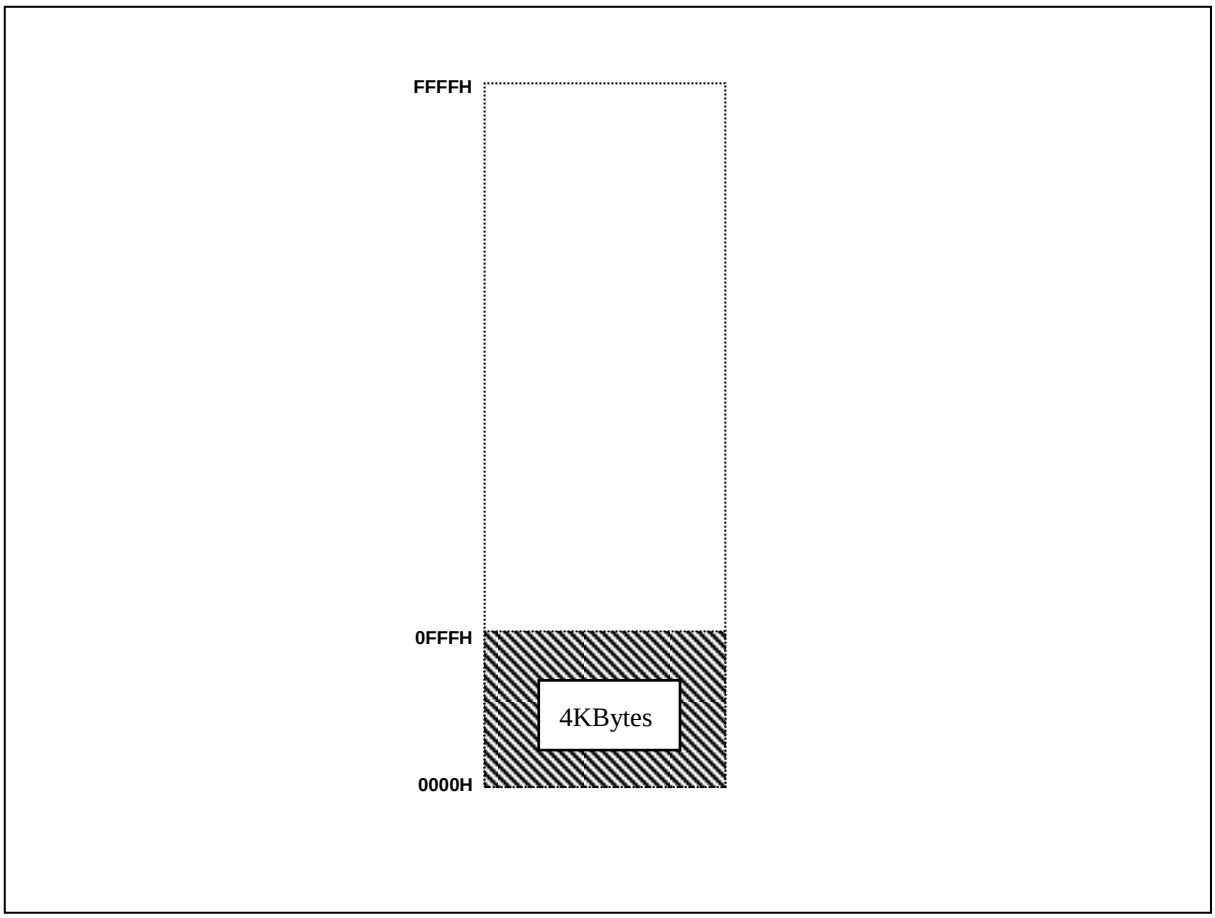


Figure 8.1 Program memory

- User Function Mode: 4KBytes Included Interrupt Vector Region
- Non-volatile and reprogramming memory: Flash memory based on EEPROM cell

8.2 Data Memory

Figure 8.2 shows the internal Data memory space available.

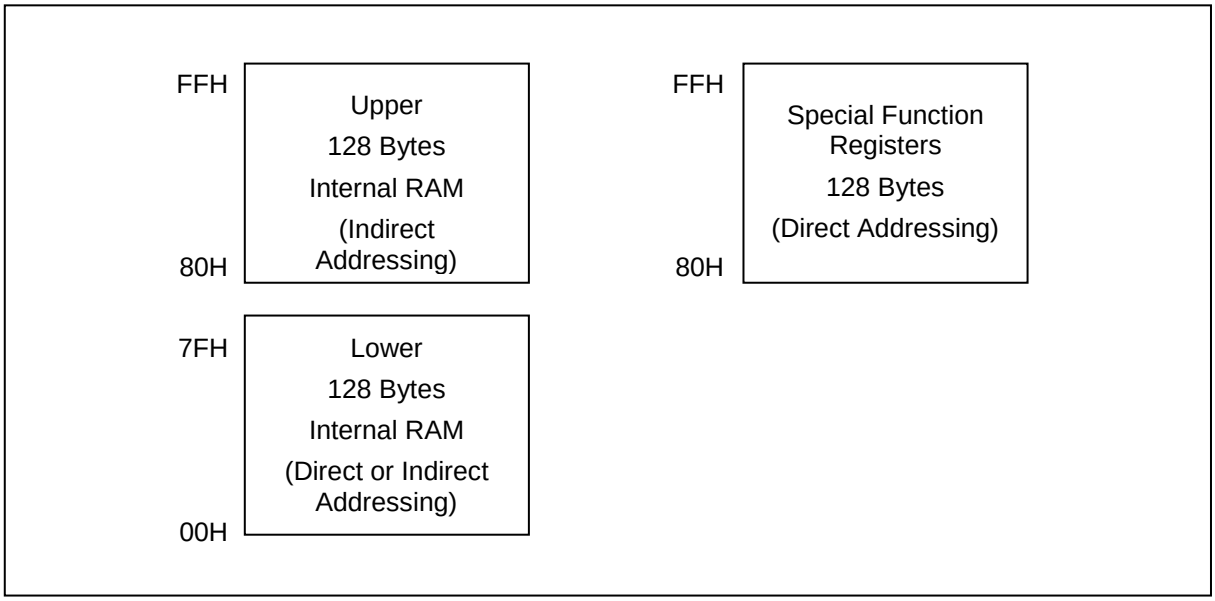


Figure 8.2 Data memory map

The internal memory space is divided into three blocks, which are generally referred to as the lower 128, upper 128, and SFR space.

Internal Data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 8.2 shows the upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8-3. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient used of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for user RAM and stack pointer.

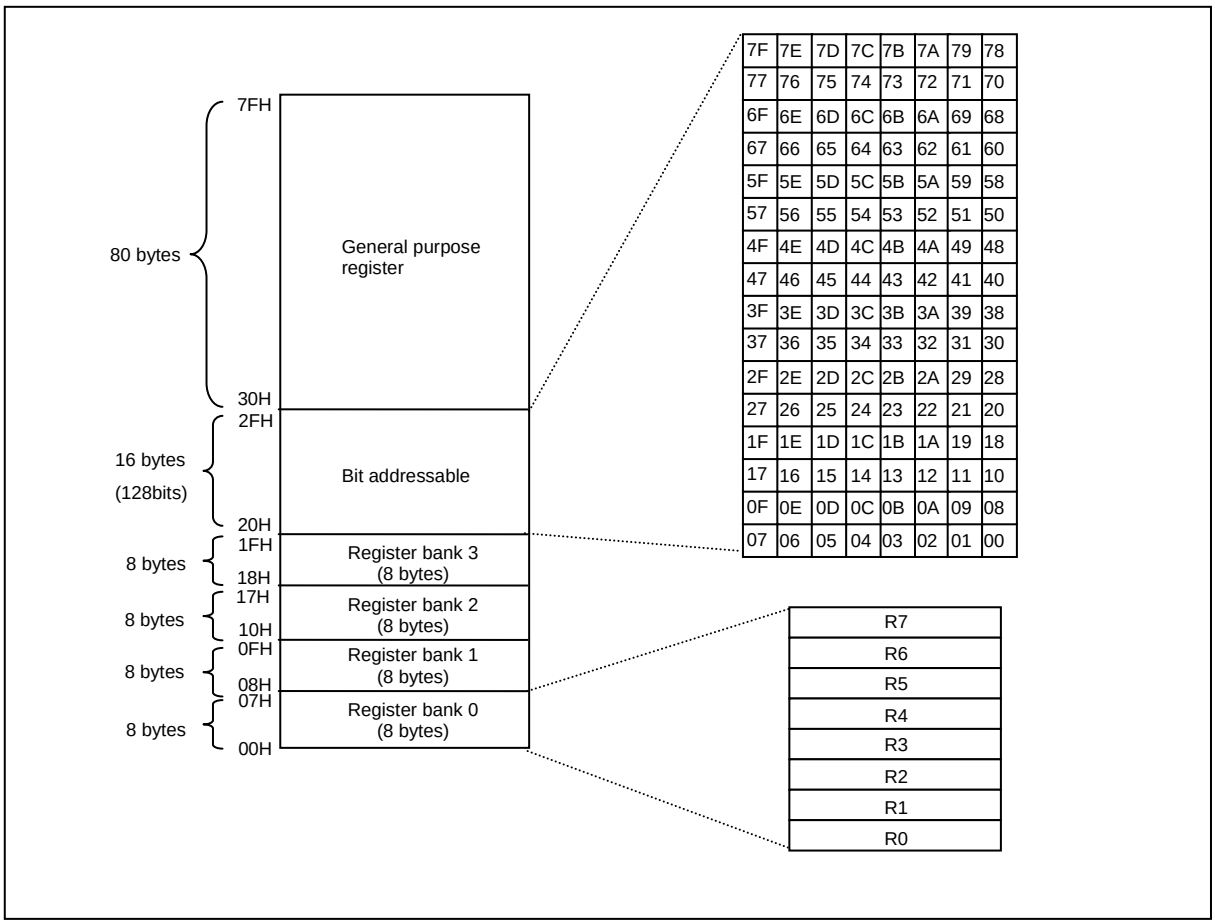


Figure 8.3 Lower 128 bytes RAM

8.3 SFR Map

8.3.1 SFR Map Summary

-	*Reserved*
	M8051 Compatible

Table 8-1 SFR Map Summary

	0H/8H(1)	1H/9H	2H/AH	3H/BH	4H/CH	5H/DH	6H/EH	7H/FH
F8H	IP1	FUSE_ CONF2	FUSE_ CAL2	FUSE_ CAL1	FUSE_ CAL0	FUSE_ CONF	TEST_ REGB	TEST_ REGA
F0H	B	-	FARL	FARM	FARH	FDR	FTR	-
E8H	-	-	FMR	FCR	FSR	FTCR	-	-
E0H	ACC	-	-	-	-	-	-	FUSE_ CAL3
D8H	P2DB	-	-	-	-	-	-	FUSE_ PKG16
D0H	PSW	-	-	-	-	-	-	-
C8H	P1DB	-	-	-	-	-	-	-
C0H	P0DB	-	-	-	-	-	-	-
B8H	IP	P2OD	-	-	-	-	-	-
B0H	P2IO	P1OD	T0CR	T0/ T0DR/ CDR0	T1CR	T1DR/ PWM1PR/	T1/ PWM1DR/ CDR1	PWM1HR
A8H	IE	IE1	IE2	IE3	EIFLAG	EIEDGE	EIPOLA	EIENAB
A0H	P1IO	P0OD	EO	-	-	-	-	-
98H	P0IO	P2PU	ADCM	ADCRH	ADCRL	-	CC_CVR	-
90H	P2	P1PU	ALCPR0	ALCPR1	-	-	TFLG	-
88H	P1	P0PU	SCCR	BCCR	BITR	WDTMR	WDTR	-
80H	P0	SP	DPL	DPH	DPL1	DPH1	-	PCON

Note: 1) Some write only registers are not bit-addressable.

2) Grey words registers are specifically designed for factory test purpose.

8.3.2 SFR Map

Table 8-2 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	Port 0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reserved			-	-	-	-	-	-	-	-
87H	Power Control Register	PCON	R/W	0	0	0	0	0	0	0	0
88H	Port 1 Data Register	P1	R/W	-	0	0	0	0	0	0	0
89H	Port 0 Pull-up Resistor Option Register	P0PU	R/W	0	0	0	0	0	0	0	0
8AH	System Clock Control Register	SCCR	R/W	0	0	0	0	0	1	0	0
8BH	BIT Clock Control Register	BCCR	R/W	0	-	-	-	0	1	0	1
8CH	Basic Interval Timer Register	BITR	R/W	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Mode Register	WDTMR	R/W	0	0	0	0	0	0	0	0
8EH	Watch Dog Timer Register	WDTR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCR	R	0	0	0	0	0	0	0	0
8FH	Reserved	-	-	-	-	-	-	-	-	-	-
90H	Port 2 Data Register	P2	R/W	-	-	-	-	-	0	0	0
91H	Port 1 Pull-up Resistor Option Register	P1PU	R/W	-	0	0	0	0	0	0	0
92H	ADC Leakage Current Protection Register 0	ALCPR0	R/W	0	0	0	0	0	0	0	0
93H	ADC Leakage Current Protection Register 1	ALCPR1	R/W	-	-	-	-	-	-	0	0
96H	Timer Flag Register	TFLG	R/W	0	0	0	0	-	-	-	-
98H	Port 0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
99H	Port 2 Pull-up Resistor Option Register	P2PU	R/W	-	-	-	-	-	1	0	0
9AH	A/D Converter Mode Register	ADCM	R/W	1	0	0	0	1	1	1	1
9BH	A/D Converter Result High Register	ADCRH	R	X	X	X	X	X	X	X	X
9CH	A/D Converter Result Low Register	ADCRL	R/W	X	X	X	X	X	X	X	X
9DH	Reserved		-	-	-	-	-	-	-	-	-
9EH	CC CV Control Register	CC_CVR	R/W	0	0	0	1	0	0	0	0

(Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	Port 1 Direction Register	P1IO	R/W	-	0	0	0	0	0	0	0
A1H	Port 0 Open Drain Register	P0OD	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	0	0	0	0	0	0	0	0
A3H	Reserved	-	-	-	-	-	-	-	-	-	-
A4H	Reserved	-	-	-	-	-	-	-	-	-	-
A5H	Reserved	-	-	-	-	-	-	-	-	-	-
A6H	Reserved	-	-	-	-	-	-	-	-	-	-
A7H	Reserved	-	-	-	-	-	-	-	-	-	-
A8H	Interrupt Enable Register	IE	R/W	0	0	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	0	0	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	0	0	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	0	0	0	0	0	0	0	0
ACH	External Interrupt Flag Register	EIFLAG	R/W	-	-	-	-	-	-	0	0
ADH	External Interrupt Edge Register	EIEDGE	R/W	-	-	-	-	-	-	0	0
AEH	External Interrupt Polarity Register	EIPOLA	W	-	-	-	-	-	-	0	0
AFH	External Interrupt Enable Register	EIENAB	R/W	-	-	-	-	-	-	0	0
B0H	Port 2 Direction Register	P2IO	R/W	-	-	-	-	-	0	0	0
B1H	Port 1 Open Drain Register	P1OD	R/W	-	0	0	0	0	0	0	0
B2H	Timer 0 Mode Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Register	T0	R	0	0	0	0	0	0	0	0
	Timer 0 Data Register	T0DR	W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	CDR0	R	0	0	0	0	0	0	0	0
B4H	Timer 1 Mode Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
B5H	Timer 1 Data Register	T1DR	W	1	1	1	1	1	1	1	1
	Timer 1 PWM Period Register	PWM1PR	W	1	1	1	1	1	1	1	1
B6H	Timer 1 Register	T1	R	0	0	0	0	0	0	0	0
	Timer 1 PWM Duty Register	PWM1DR	R/W	0	1	1	1	1	1	1	1
	Timer 1 Capture Data Register	CDR1	R	0	0	0	0	0	0	0	0
B7H	Timer 1 PWM High Register	PWM1HR	R/W	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Control Register 0	IP	R/W	0	0	0	0	0	0	0	0
B9H	Port 2 Open Drain Register	P2OD	R/W	-	-	-	-	-	0	0	0
BAH	Reserved	-	-	-	-	-	-	-	-	-	-
BBH	Reserved	-	-	-	-	-	-	-	-	-	-
BCH	Reserved	-	-	-	-	-	-	-	-	-	-
BDH	Reserved	-	-	-	-	-	-	-	-	-	-
BEH	Reserved	-	-	-	-	-	-	-	-	-	-
BFH	Reserved	-	-	-	-	-	-	-	-	-	-

(Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	Port 0 Debounce Register	P0DB	R/W	0	0	0	0	0	0	0	0
C1H	Reserved	-	-	-	-	-	-	-	-	-	-
C2H	Reserved	-	-	-	-	-	-	-	-	-	-
C3H	Reserved	-	-	-	-	-	-	-	-	-	-
C4H	Reserved	-	-	-	-	-	-	-	-	-	-
C5H	Reserved	-	-	-	-	-	-	-	-	-	-
C6H	Reserved	-	-	-	-	-	-	-	-	-	-
C7H	Reserved	-	-	-	-	-	-	-	-	-	-
C8H	Port 1 Debounce Register	P1DB	R/W	-	0	0	0	0	0	0	0
C9H	Reserved	-	-	-	-	-	-	-	-	-	-
CAH	Reserved	-	-	-	-	-	-	-	-	-	-
CBH	Reserved	-	-	-	-	-	-	-	-	-	-
CCH	Reserved	-	-	-	-	-	-	-	-	-	-
CDH	Reserved	-	-	-	-	-	-	-	-	-	-
CEH	Reserved	-	-	-	-	-	-	-	-	-	-
CFH	Reserved	-	-	-	-	-	-	-	-	-	-
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	-	-	-	-	-	-	-	-	-	-
D2H	Reserved	-	-	-	-	-	-	-	-	-	-
D3H	Reserved	-	-	-	-	-	-	-	-	-	-
D4H	Reserved	-	-	-	-	-	-	-	-	-	-
D5H	Reserved	-	-	-	-	-	-	-	-	-	-
D6H	Reserved	-	-	-	-	-	-	-	-	-	-
D7H	Reserved	-	-	-	-	-	-	-	-	-	-
D8H	Port 2 Debounce Register	P2DB	R/W	-	-	-	-	-	0	0	0
D9H	Reserved	-	-	-	-	-	-	-	-	-	-
DAH	Reserved	-	-	-	-	-	-	-	-	-	-
DBH	Reserved	-	-	-	-	-	-	-	-	-	-
DCH	Reserved	-	-	-	-	-	-	-	-	-	-
DDH	Reserved	-	-	-	-	-	-	-	-	-	-
DEH	Reserved	-	-	-	-	-	-	-	-	-	-
DFH	Reserved	-	-	-	-	-	-	-	-	-	-

(Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Reserved	-	-	-	-	-	-	-	-	-	-
E2H	Reserved	-	-	-	-	-	-	-	-	-	-
E3H	Reserved	-	-	-	-	-	-	-	-	-	-
E4H	Reserved	-	-	-	-	-	-	-	-	-	-
E5H	Reserved	-	-	-	-	-	-	-	-	-	-
E6H	Reserved	-	-	-	-	-	-	-	-	-	-
E7H	Reserved	-	-	-	-	-	-	-	-	-	-
E8H	Reserved	-	-	-	-	-	-	-	-	-	-
E9H	Reserved	-	-	-	-	-	-	-	-	-	-
EAH	Flash Mode Register	FMR	R/W	0	0	0	0	0	0	0	0
EBH	Flash Control Register	FCR	R/W	0	0	0	0	0	0	1	1
ECH	Flash Status Register	FSR	R/W	1	0	-	-	0	0	0	0
EDH	Flash Timer Control Register	FTCR	R/W	0	0	0	0	0	0	0	0
EEH	Reserved	-	-	-	-	-	-	-	-	-	-
EFH	Reserved	-	-	-	-	-	-	-	-	-	-
F0H	Reserved	-	-	-	-	-	-	-	-	-	-
F1H	Reserved	-	-	-	-	-	-	-	-	-	-
F2H	Flash Address Low Register	FARL	W	0	0	0	0	0	0	0	0
F3H	Flash Address Middle Register	FARM	W	0	0	0	0	0	0	0	0
F4H	Flash Address High Register	FARH	W	0	0	0	0	0	0	0	0
F5H	Flash Data Register	FDR	R/W	0	0	0	0	0	0	0	0
F6H	Flash Test Register	FTR	R/W	0	0	0	0	0	0	0	0
F7H	Reserved	-	-	-	-	-	-	-	-	-	-
F8H	Reserved	-	-	-	-	-	-	-	-	-	-
F9H	Fuse 16 pin setting	FUSE_PKG	R	-	-	-	-	-	-	-	0
FAH	VDC Pseudo-Calibration Data	FUSE_CAL2	R	-	-	-	-	-	0	0	0
FBH	INTOSC Pseudo- Calibration Data	FUSE_CAL1	R	1	0	0	0	0	0	0	0
FCH	WDTOSC Pseudo- Calibration Data	FUSE_CAL0	R	-	0	0	0	0	0	0	0
FDH	Pseudo-Configure Data	FUSE_CONF	R	-	-	-	0	0	0	0	0
FEH	Function Test Register B	TEST_B	R/W	0	0	0	0	0	0	0	0
FFH	Function Test Register A	TEST_A	R/W	0	0	0	0	0	0	0	1

8.3.3 Compiler Compatible SFR

ACC (Accumulator) : E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ACC Accumulator

B (B Register) : F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

B B Register

SP (Stack Pointer) : 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 07H

SP Stack Pointer

DPL (Data Pointer Low Byte) : 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL Data Pointer Low Byte

DPH (Data Pointer High Byte) : 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH Data Pointer High Byte

PSW (Program Status Word) : D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

CY Carry Flag

AC	Auxiliary Carry Flag
F0	General Purpose User-Definable Flag
RS1	Register Bank Select bit 1
RS0	Register Bank Select bit 0
OV	Overflow Flag
F1	User-Definable Flag
P	Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of ‘1’ bits in the accumulator

9. I/O Ports

9.1 I/O Ports

The MC95FB204 has three I/O ports (P0, P1 and P2). Each port can be easily configured by software as I/O pin, internal pull up and open drain pin to meet various system configurations and design requirements. Also P0 includes function that can generate interrupt according to change of state of the pin.

9.2 Port Register

9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

9.2.2 Direction Register (PxIO)

Each I/O pin can independently used as an input or an output through the PxIO register. Bits cleared in this read/write register will select the corresponding pin in Px to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to them in 1-bit units with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset. (Only P1[6:4] port pull-up resistor selection have default ON state for 16-pin Package). Pull-up operation is only enable in input mode.

9.2.4 Open-drain Selection Register (PxOD)

There is internally open-drain selection register (PxOD) in P0, P1, P2. The open-drain selection register controls the open-drain enable/disable of each port. Ports become push-pull by a system reset. You should connect an external resistor in open-drain output mode.

9.2.5 ADC Leakage Current Protection Register (ALCPR)

ALCPRx registers prevent the input leakage current when ports are connected to analog inputs. If the bit of ALCPRx is ‘1’, the dynamic current path of the schmitt AND gate of the port is cut off and the digital input of the corresponding port is always ‘0’.

9.2.6 Register Map

Table 9-1 Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	98H	R/W	00H	P0 Direction Register
P0PU	89H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	A1H	R/W	00H	P0 Open-drain Selection Register
P0DB	C0H	R/W	00H	P0 Debounce Enable Register
P1	88H	R/W	00H	P1 Data Register
P1IO	A0H	R/W	00H	P1 Direction Register
P1PU	91H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	B1H	R/W	00H	P1 Open-drain Selection Register
P1DB	C8H	R/W	00H	P1 Debounce Enable Register
P2	90H	R/W	00H	P2 Data Register
P2IO	B0H	R/W	00H	P2 Direction Register
P2PU	99H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	B9H	R/W	00H	P2 Open-drain Selection Register
P2DB	D8H	R/W	00H	P2 Debounce Enable Register
ALCPR0	92H	R/W	00H	ADC Leakage Current Protection Register 0
ALCPR1	93H	R/W	00H	ADC Leakage Current Protection Register 1

9.3 P0 Port

9.3.1 P0 Port Description

P0 is 8-bit I/O port. P0 control registers consist of Data register (P0), direction register (P0IO), debounce enable register (P0DB), pull-up register selection register (P0PU), open-drain selection register (P0OD) and ADC leakage current protection register(ALCPR0).

9.3.2 Register description for P0

P0 (P0 Data Register) : 80H

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0[7:0] I/O Data

P0IO (P0 Direction Register) : 98H

7	6	5	4	3	2	1	0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0IO[7:0] P0 data I/O direction.

0 Input
1 Output

P0PU (P0 Pull-up Resistor Selection Register) : 89H

7	6	5	4	3	2	1	0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0PU[7:0] Configure pull-up resistor of P0 port
0 disable
1 enable

P0OD (P0 Open-drain Selection Register) : A1H

7	6	5	4	3	2	1	0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0OD[7:0] Configure open-drain of P0 port
0 disable
1 enable

P0DB (P0 Debounce Enable Register) : C0H

7	6	5	4	3	2	1	0
P07DB	P06DB	P05DB	P04DB	P03DB	P02DB	P01DB	P00DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0DB[7:0] Configure debounce of P0 port
0 disable
1 enable

ALCPR0 (ADC Leakage Current Protection Register 0) : 92H

7	6	5	4	3	2	1	0
ALCPR07	ALCPR06	ALCPR05	ALCPR04	ALCPR03	ALCPR02	ALCPR01	ALCPR00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ALCPR0[7:0] AN7~ AN0 ADC leakage current protection register
0 Disable analog channel AN[7:0].
1 Enable analog channel AN[7:0].

9.4 P1 Port

9.4.1 P1 Port Description

P1 is 7-bit I/O port. P1 control registers consist of Data register (P1), direction register (P1IO), debounce enable register (P1DB), pull-up register selection register (P1PU), open-drain selection register (P1OD) and ADC leakage current protection register(ALCPR1).

9.4.2 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
-	P16	P15	P14	P13	P12	P11	P10
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1[6:0] I/O Data

P1IO (P1 Direction Register) : A0H

7	6	5	4	3	2	1	0
-	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1IO[6:0] P1 data I/O direction

0 Input

1 Output

P1PU (P1 Pull-up Resistor Selection Register) : 91H

7	6	5	4	3	2	1	0
-	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1PU[6:0] Configure pull-up resistor of P1 port

0 disable

1 enable

P1OD (P1 Open-drain Selection Register) : B1H

7	6	5	4	3	2	1	0
-	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1OD[6:0] Configure open-drain of P1 port

0 disable

1 enable

P1DB (P1 Debounce Enable Register) : C8H

7	6	5	4	3	2	1	0
-	P16DB	P15DB	P14DB	P13DB	P12DB	P11DB	P10DB
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1DB[6:0] Configure debounce of P1 port

0 disable

1 enable

ALCPR1 (ADC Leakage Current Protection Register 1) : 93H

7	6	5	4	3	2	1	0
-	-	ALCPR13	ALCPR12	ALCPR11	ALCPR10	ALCPR09	ALCPR08
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ALCPR09 P15/AN9 ADC leakage current protection register

0 Disable analog channel AN9.

1 Enable analog channel AN9.

ALCPR08 P14/AN8 ADC leakage current protection register

0 Disable analog channel AN8.

1 Enable analog channel AN8.

9.5 P2 Port

9.5.1 P2 Port Description

P2 is 3-bit I/O port. P2 control registers consist of Data register (P2), direction register (P2IO), debounce enable register (P2DB), pull-up register selection register (P2PU), open-drain selection register (P2OD).

9.5.2 Register description for P2

P2 (P2 Data Register) : 90H

7	6	5	4	3	2	1	0
-	-	-	-	-	P22	P21	P20
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

P2[2:0] I/O Data

P2IO (P2 Direction Register) : B0H

7	6	5	4	3	2	1	0
-	-	-	-	-	P22IO	P21IO	P20IO
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

P2IO[2:0] P2 data I/O direction

0 Input

1 Output

P2PU (P2 Pull-up Resistor Selection Register) : 99H

7	6	5	4	3	2	1	0
-	-	-	-	-	P22PU	P21PU	P20PU
-	-	-	-	-	R/W	R/W	R/W

Initial value : **04H**

Note : P22PU is 1 at initial state because P22 is combined with RESET.

P2PU[2:0] Configure pull-up resistor of P2 port

0 disable

1 enable

P2OD (P2 Open-drain Selection Register) : 0DH

7	6	5	4	3	2	1	0
-	-	-	-	-	P22OD	P21OD	P20OD
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

P2OD[2:0] Configure open-drain of P2 port

0 disable

1 enable

P2DB (P2 Debounce Enable Register) : D8H

7	6	5	4	3	2	1	0
-	-	-	-	-	P22DB	P21DB	P20DB
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

P2DB[2:0] Configure debounce of P2 port

0 disable

1 disable

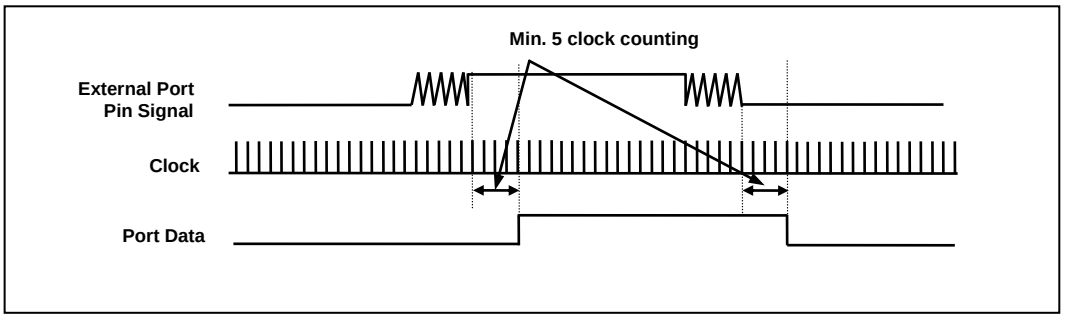


Figure 9.1 Debounce Function

10. Interrupt Controller

10.1 Overview

The MC95FB204 supports up to 25 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

- receive the request from 24 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is serviced
- Each interrupt source can control by EA bit and each IEx bit
- Interrupt latency: 3~9 machine cycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, IE3). Bits of IE, IE1, IE2, IE3 register each individually enable/disable a particular interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to '0', all interrupts are disabled: when EA is set to '1', interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The MC95FB204 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels by writing to IP or IP1.

Interrupt default mode is level-trigger basically but if needed, it is able to change edge-trigger mode. Table 10-1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority sets two bit which is to IP and IP1 register about group. Interrupt service routine services higher priority. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If the request of same or lower priority level is received, that request is not serviced.

Table 10-1 Interrupt Group Priority Level

Interrupt Group	→				
0 (Bit0)	Interrupt0	Interrupt6	Interrupt12	Interrupt18	Highest
1 (Bit1)	Interrupt1	Interrupt7	Interrupt13	Interrupt19	
2 (Bit2)	Interrupt2	Interrupt8	Interrupt14	Interrupt20	
3 (Bit3)	Interrupt3	Interrupt9	Interrupt15	Interrupt21	
4 (Bit4)	Interrupt4	Interrupt10	Interrupt16	Interrupt22	
5 (Bit5)	Interrupt5	Interrupt11	Interrupt17	Interrupt23	Lowest

10.2 External Interrupt

The external interrupt on INT0 and INT1 pins receive various interrupt request depending on the edge selection register EIEDGE (External Interrupt Edge register) and EIPOLA (External Interrupt Polarity register) as shown in Figure 10.1. Also each external interrupt source has control setting bits. The EIFLAG (External interrupt flag register) register provides the status of external interrupts.

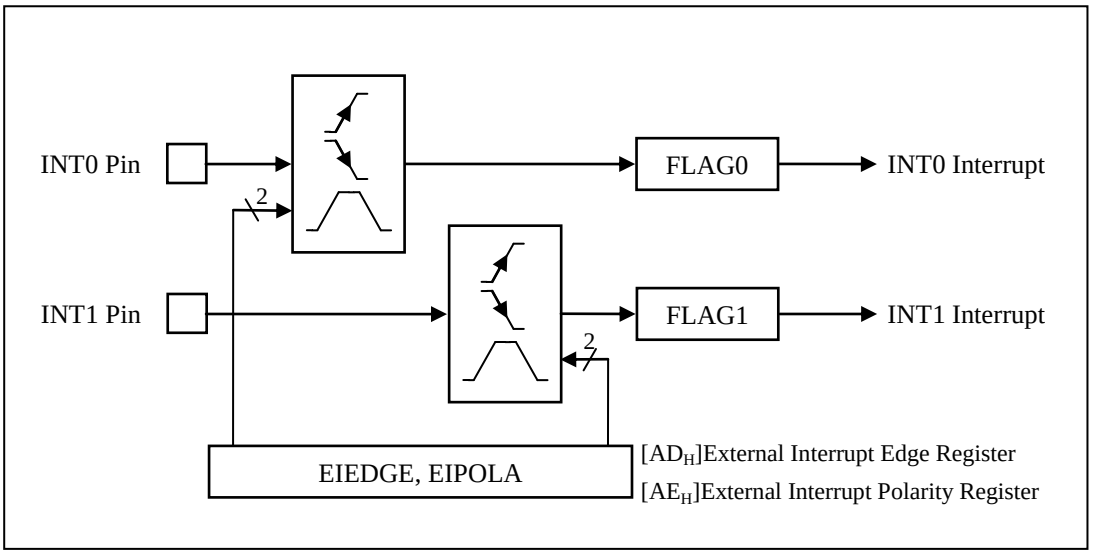


Figure 10.1 External Interrupt Description

10.3 Block Diagram

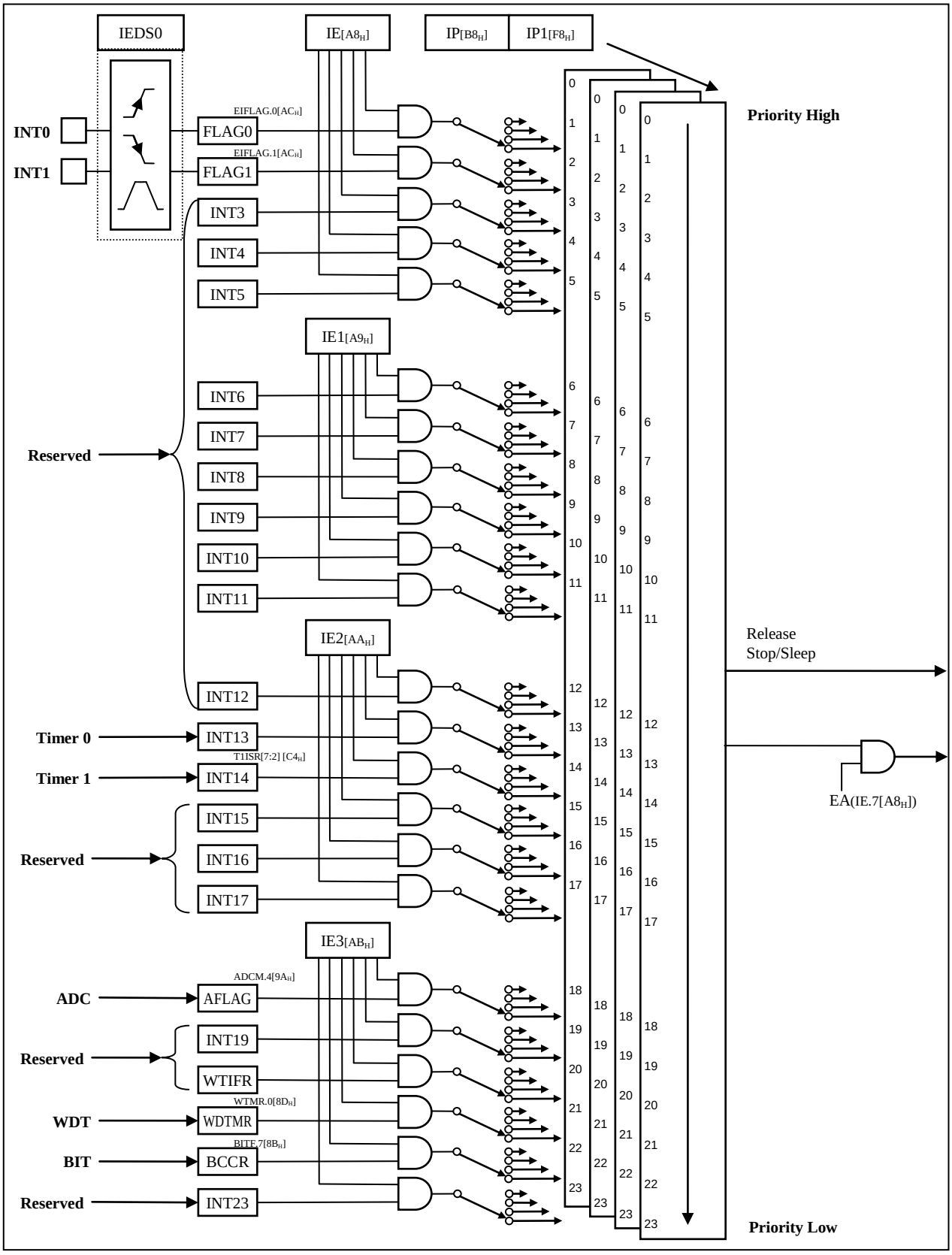


Figure 10.2 Block Diagram of Interrupt

10.4 Interrupt Vector Table

The interrupt controller supports 24 interrupt sources as shown in the Table 10-2 below. When interrupt becomes service, long call instruction (LCALL) is executed in the vector address. Interrupt request 24 has a decided priority order.

Table 10-2 Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Polarity	Mask	Vector Address
Hardware Reset	RESETB	0 0	0	Non-Maskable	0000H
-	INT0	IE0.0	1	Maskable	0003H
External Interrupt 0	INT1	IE0.1	2	Maskable	000BH
External Interrupt 1	INT2	IE0.2	3	Maskable	0013H
-	INT3	IE0.3	4	Maskable	001BH
-	INT4	IE0.4	5	Maskable	0023H
-	INT5	IE0.5	6	Maskable	002BH
-	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
-	INT8	IE1.2	9	Maskable	0043H
-	INT9	IE1.3	10	Maskable	004BH
-	INT10	IE1.4	11	Maskable	0053H
-	INT11	IE1.5	12	Maskable	005BH
-	INT12	IE2.0	13	Maskable	0063H
T0	INT13	IE2.1	14	Maskable	006BH
T1	INT14	IE2.2	15	Maskable	0073H
	INT15	IE2.3	16	Maskable	007BH
	INT16	IE2.4	17	Maskable	0083H
-	INT17	IE2.5	18	Maskable	008BH
ADC	INT18	IE3.0	19	Maskable	0093H
-	INT19	IE3.1	20	Maskable	009BH
-	INT20	IE3.2	21	Maskable	00A3H
WDT	INT21	IE3.3	22	Maskable	00ABH
BIT	INT22	IE3.4	23	Maskable	00B3H
-	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, first EA bit must set ‘1’ and specific interrupt source must set ‘1’ by writing a ‘1’ to associated bit in the IEx. If interrupt request is received, specific interrupt request flag set ‘1’. And it remains ‘1’ until CPU accepts interrupt. After that, interrupt request flag will be cleared automatically.

10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to ‘0’ by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. After finishing the current instruction, at the next instruction to go interrupt service routine needs 3~9 machine cycle and the interrupt service task is terminated upon execution of an interrupt return instruction [RETI]. After generating interrupt, to go to interrupt service routine, the following process is progressed

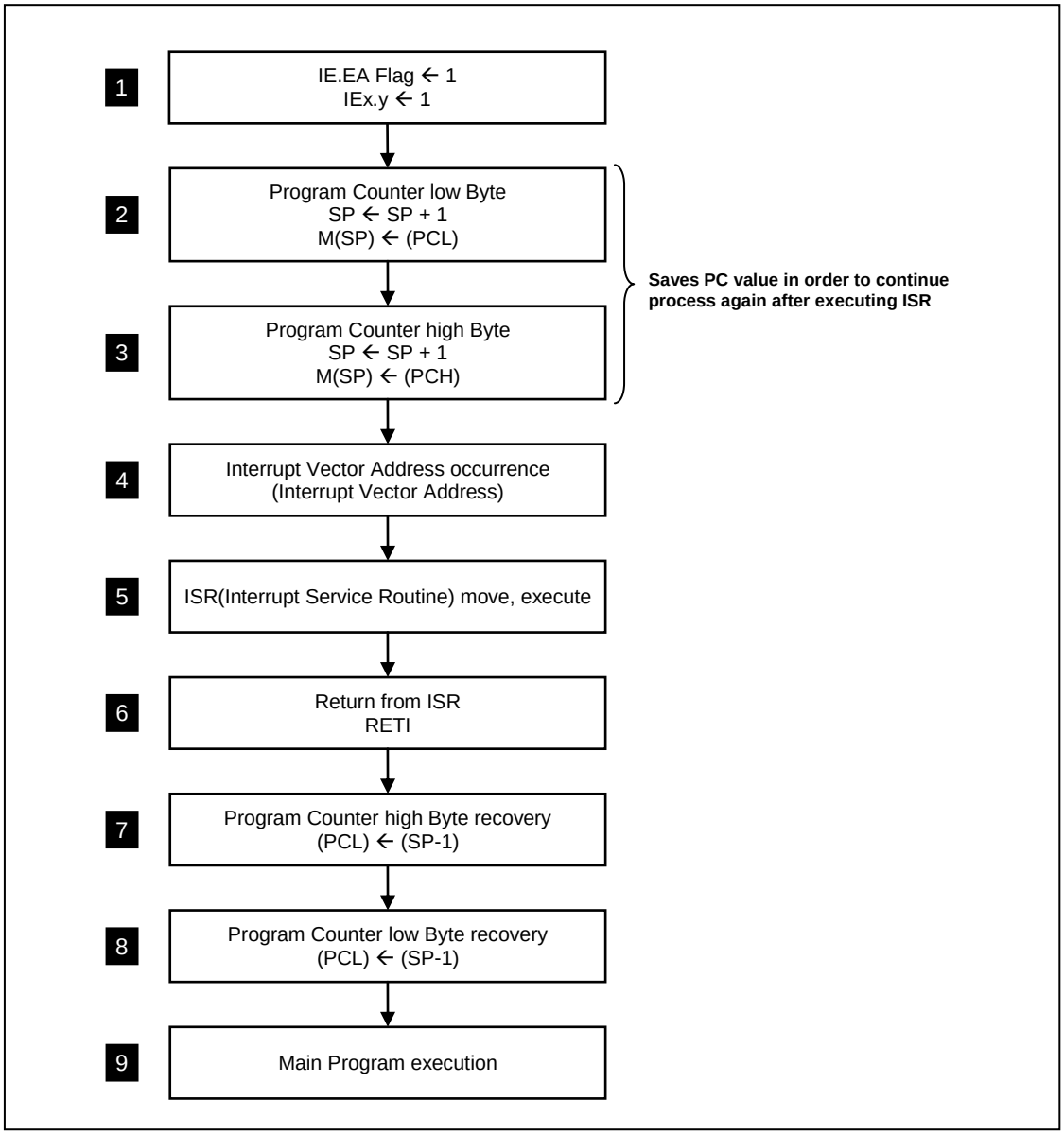


Figure 10.3 Interrupt Vector Address Table

10.6 Effective Timing after Controlling Interrupt bit

Case A) Control Global Interrupt Mask Enable Flag (EA bit).

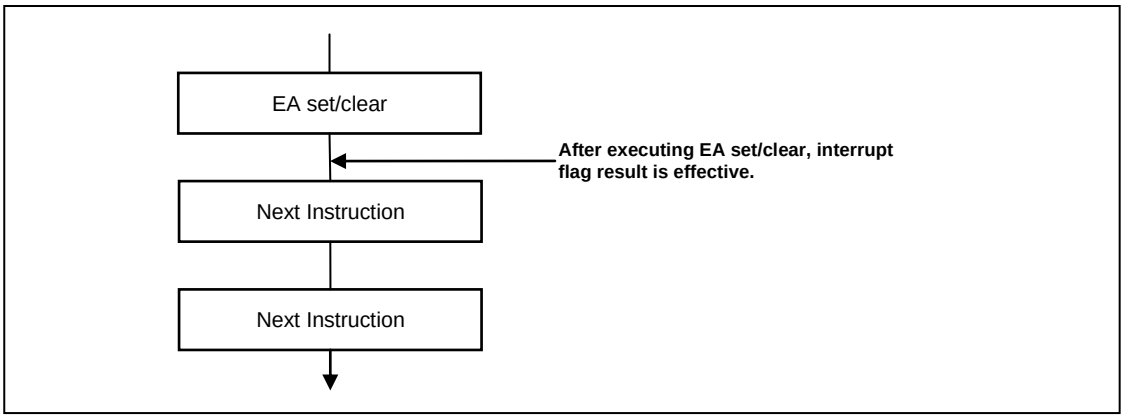


Figure 10.4 Interrupt flag result effective Timing

Case B) Control Interrupt Enable Register (IE, IE1, IE2, IE3)

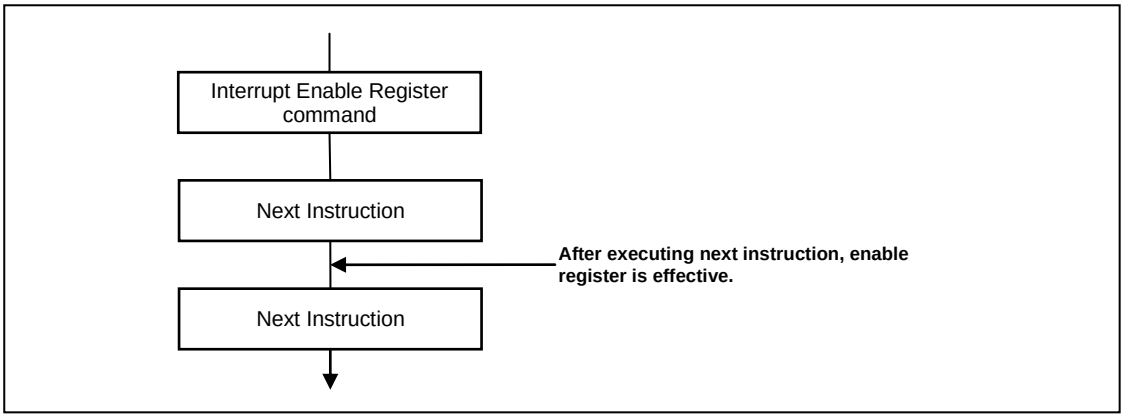


Figure 10.5 Interrupt Enable Register effective Timing

10.7 Multi Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the interrupt are received at the same time simultaneously, an interrupt polling sequence determines by hardware which request is serviced. However, multiple processing through software for special features is possible.

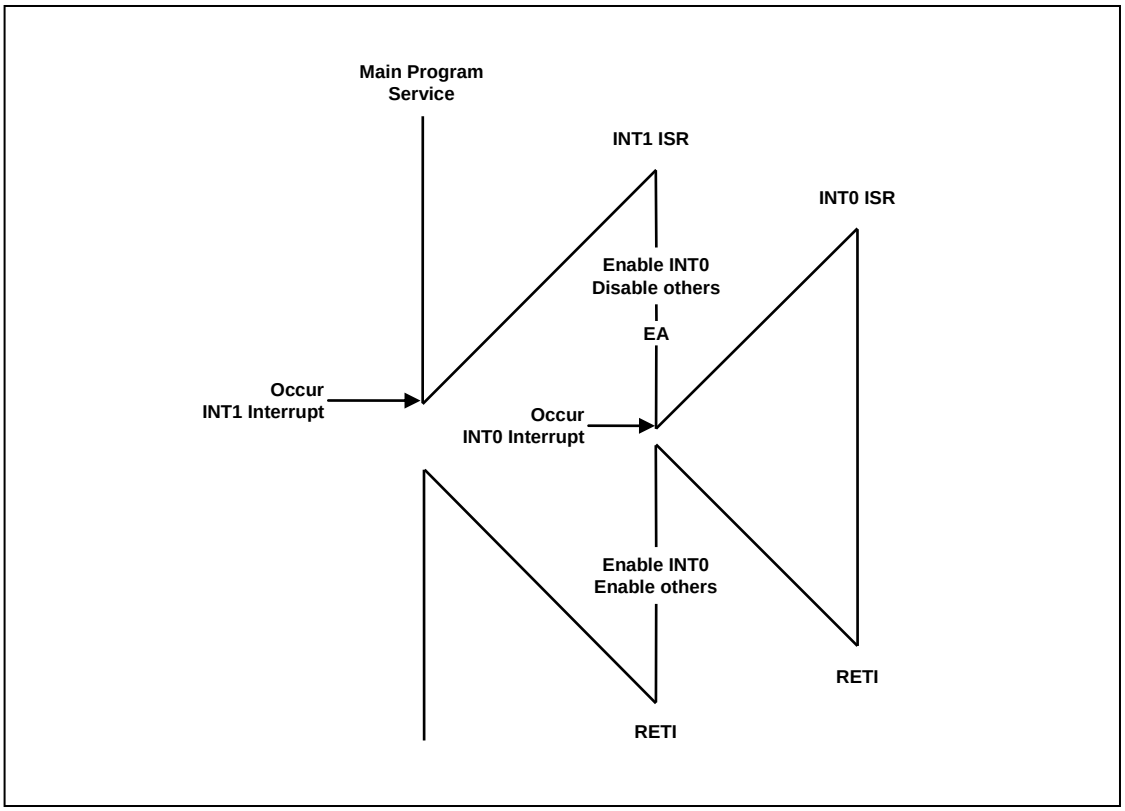


Figure 10.6 Execution of Multi Interrupt

Following example is shown to service INT0 routine during INT1 routine in Figure 10.6. In this example, INT0 interrupt priority is higher than INT1 interrupt priority using IP0, IP1 registers. If some interrupt is lower than INT1 priority, it can't service its interrupt routine.

An interrupt service routine may only be interrupted by an interrupt of higher priority and, if two interrupts of different priority occur at the same time, the higher level interrupt will be serviced first. An interrupt cannot be interrupted by another interrupt of the same or a lower priority level. If two interrupts of the same priority level occur simultaneously, the order in which the interrupts are serviced is determined by the scan order

Example) Software Multi Interrupt:

```
INT1:   MOV     IE, #81H      ; Enable INT0 only
        MOV     IE1, #00H     ; Disable other
        :
        MOV     IE, #0FFH     ; Enable all Interrupts
        MOV     IE1, #0FFH
```

RETI

10.8 Interrupt Enable Accept Timing

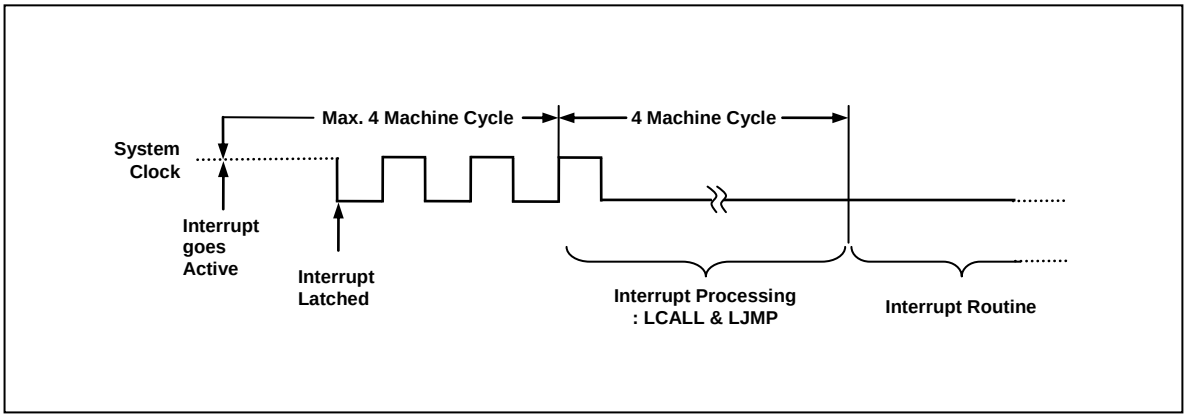


Figure 10.7 Interrupt Response Timing Diagram

10.9 Interrupt Service Routine Address

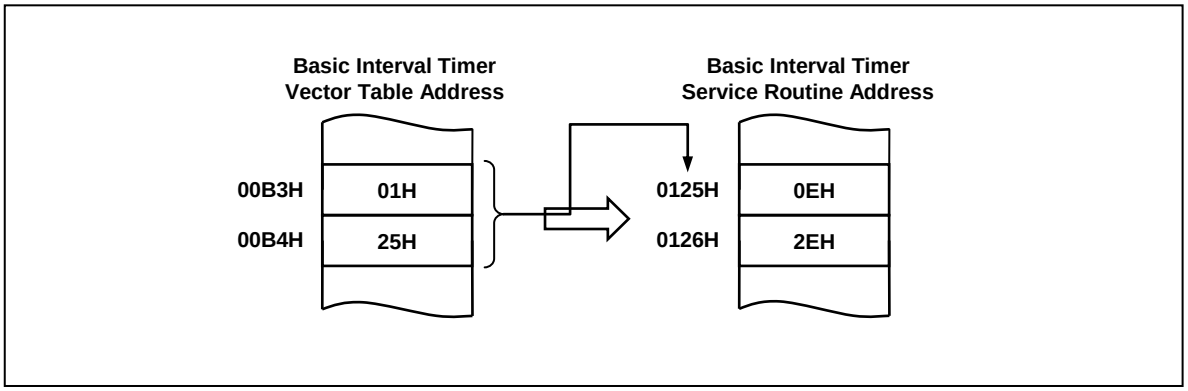


Figure 10.8 Correspondence between vector Table address and the entry address of ISP

10.10 Saving/Restore General-Purpose Registers

```
INTxx : PUSH   PSW
        PUSH   DPL
        PUSH   DPH
        PUSH   B
        PUSH   ACC
        :

Interrupt_Processing:
        :

        POP   ACC
        POP   B
        POP   DPH
        POP   DPL
        POP   PSW
        RETI
```

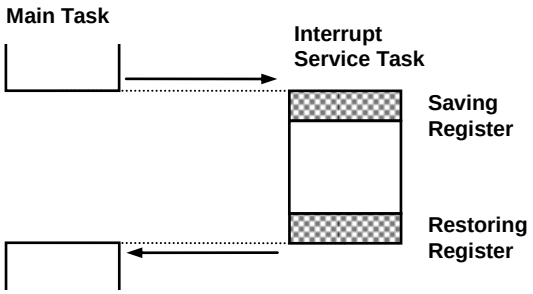


Figure 10.9 Saving/Restore Process Diagram & Sample Source

10.11 Interrupt Timing

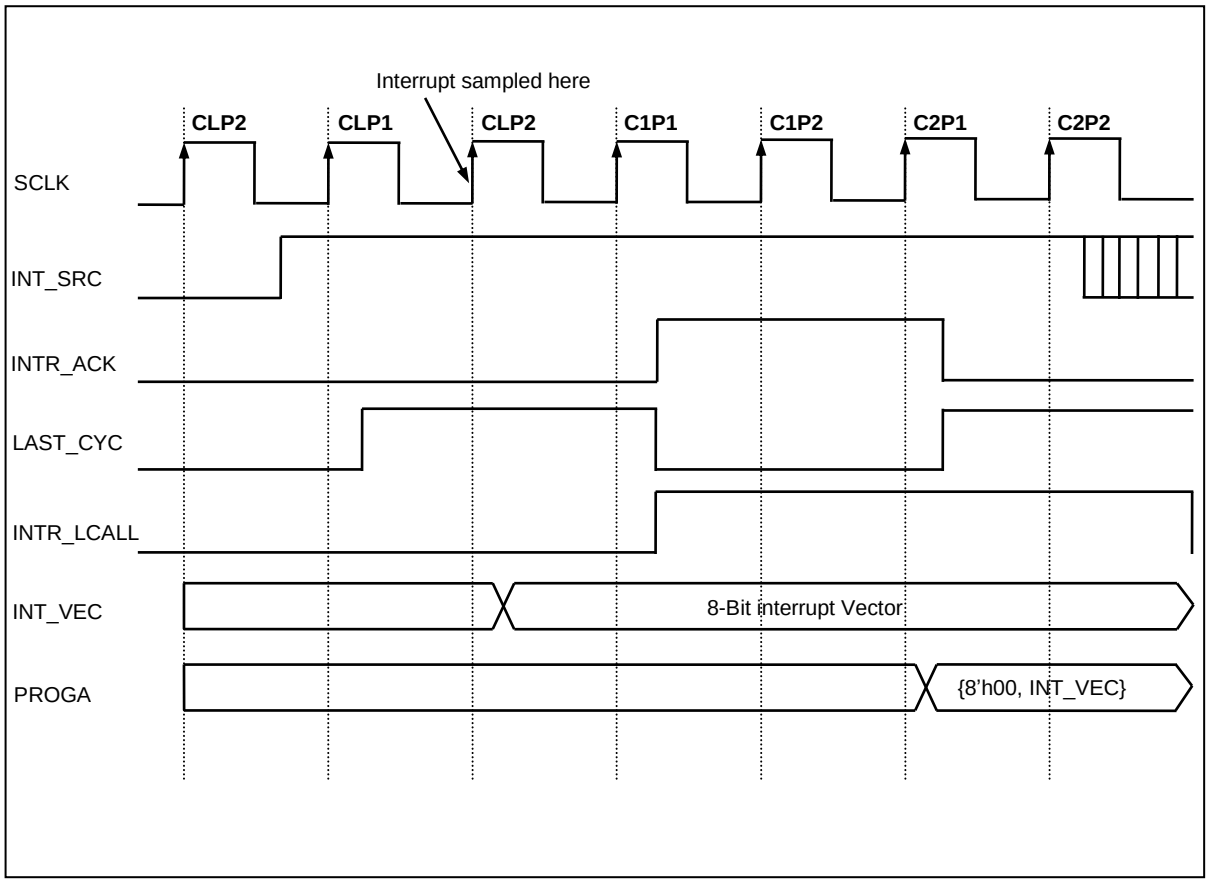


Figure 10.10 Timing chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt source sampled at last cycle of the command. When sampling interrupt source, it is decided to low 8-bit of interrupt vector. M8051W core makes interrupt acknowledge at first cycle of command, executes long call to jump interrupt routine as INT_VEC.

Note) command cycle C?P?: L=Last cycle, 1=1st cycle or 1st phase, 2=2nd cycle or 2nd phase

10.12 Interrupt Register Overview

10.12.1 Interrupt Enable Register (IE, IE1, IE2, IE3)

Interrupt enable register consists of Global interrupt control bit (EA) and peripheral interrupt control bits. Totally 24 peripheral are able to control interrupt.

10.12.2 Interrupt Priority Register (IP, IP1)

The 24 interrupt divides 6 groups which have each 4 interrupt sources. A group can decide 4 levels interrupt priority using interrupt priority register. Level 3 is the high priority, while level 0 is the low priority. Initially, IP, IP1 reset value is '0'. At that initialization, low interrupt number has a higher priority than high interrupt number. If decided the priority, low interrupt number has a higher priority than high interrupt number in that group.

10.12.3 External Interrupt Flag Register (EIFLAG)

The external interrupt flag register is set to '1' when the external interrupt generating condition is satisfied. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a '0' to it.

10.12.4 External Interrupt Edge Register (EIEDGE)

The External interrupt edge register determines which type of edge or level sensitive interrupt. Initially, default value is level. For level, write '0' to related bit. For edge, write '1' to related bit.

10.12.5 External Interrupt Polarity Register (EIPOLA)

According to EIEDGE register, the external interrupt polarity (EIPOLA) register has a different meaning. If EIEDGE is level type, EIPOLA is able to have Low/High level value. If EIEGDE is edge type, EIPOLA is able to have rising/falling edge value.

10.12.6 External Interrupt Enable Register (EIENAB)

When the external interrupt enable register is written to '1', the corresponding external pin interrupt is enabled. The EIEDGE and EIPOLA register defines whether the external interrupt is activated on rising or falling edge or level sensed.

10.12.7 Register Map

Table 10-3 Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1

IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Polarity Register
IP1	F8H	R/W	00H	Interrupt Polarity Register 1
EIFLAG	ACH	R/W	00H	External Interrupt Flag Register
EIEDGE	ADH	R/W	00H	External Interrupt Edge Register
EIPOLA	AEH	R/W	00H	External Interrupt Polarity Register
EIENAB	AFH	R/W	00H	External Interrupt Enable Register

10.13 Interrupt Register Description

The Interrupt Register is used for controlling interrupt functions. Also it has External interrupt control registers. The interrupt register consists of Interrupt Enable Register (IE), Interrupt Enable Register 1 (IE1), Interrupt Enable Register 2 (IE2) and Interrupt Enable Register 3 (IE3). For external interrupt, it consists of External Interrupt Flag Register (EIFLAG), External Interrupt Edge Register (EIEDGE), External Interrupt Polarity Register (EIPOLA) and External Interrupt Enable Register (EIENAB).

10.13.1 Register description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	-	INT5E	INT4E	INT3E	INT2E	INT1E	INT0E
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

EA Enable or disable all interrupt bits
- 0 All Interrupt disable
- 1 All Interrupt enable

INT5E, INT4E, INT3E Reserved

INT2E Enable or disable External Interrupt 1
- 0 disable
- 1 enable

INT1E Enable or disable External Interrupt 0
- 0 disable
- 1 enable

INT0E Reserved

IE1 (Interrupt Enable Register 1) : A9H

7	6	5	4	3	2	1	0
-	-	INT11E	INT10E	INT9E	INT8E	INT7E	INT6E
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

INT11E, Reserved

INT10E, INT8E, INT7E, INT6E

IE2 (Interrupt Enable Register 2) : AAH

7	6	5	4	3	2	1	0
-	-	INT17E	INT16E	INT15E	INT14E	INT13E	INT12E
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

INT17E, INT16E, INT15E Reserved

INT14E Enable or disable Timer 1 Interrupt
- 0 disable
- 1 enable

INT13E Enable or disable Timer 0 Interrupt
- 0 disable
- 1 enable

INT12E Reserved

IE3 (Interrupt Enable Register 3) : ABH

7	6	5	4	3	2	1	0
-	-	INT23E	INT22E	INT21E	INT20E	INT19E	INT18E
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

INT23E Reserved

INT22E Enable or disable BIT Interrupt
- 0 disable
- 1 enable

INT21E Enable or disable WDT Interrupt
- 0 disable
- 1 enable

INT20E, INT19E Reserved

INT18E Enable or disable ADC Interrupt
- 0 disable
- 1 enable

IP (Interrupt Priority Register) : B8H

7	6	5	4	3	2	1	0
-	-	IP5	IP4	IP3	IP2	IP1	IP0

R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP1 (Interrupt Priority Register 1) : F8H

7	6	5	4	3	2	1	0
-	-	IP15	IP14	IP13	IP12	IP11	IP10
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG (External Interrupt Flag Register) : ACH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	FLAG1	FLAG0
R	R	R	R	R	R	R/W	R/W

Initial value : 00H

FLAG[1:0] If External Interrupt is occurred, the flag becomes '1'. The flag can be cleared by writing a '0' to bit

0 External Interrupt not occurred

1 External Interrupt occurred

EIEDGE (External Interrupt Edge Register) : ADH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDGE1	EDGE0
R/W-	R/W-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

EDGE[1:0] Determines which type of edge or level sensitive interrupt may occ ur.

0 Level (default)

1 Edge

EIPOLA (External Interrupt Polarity Register) : AEH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	POLA1	POLA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

POLA[1:0] According to EIEDGE, External interrupt polarity register has a different means. If EIEDGE is level type, external interrupt polarity is able to have Low/High level value. If EIEGDE is edge type, external interrupt polarity is able to have rising/ falling edge value.

Level case:

0 When High level, Interrupt occurred (default)

1 When Low level, Interrupt occurred

Edge case:

0 When Rising edge, Interrupt occurred (default)

1 When Falling edge, Interrupt occurred

EIENAB (External Interrupt Enable Register) : AFH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ENAB1	ENAB0
R/W-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ENAB[1:0] Control External Interrupt

0 disable (default)

1 enable

11. CC/CV Block

CC/CV means “Constant Current/Constant Voltage”. It is used to charge a Li-ion battery what is normally used for mobile phone or digital camera. In order to charge a Li-ion battery, CC/CV power is supplied to the battery.

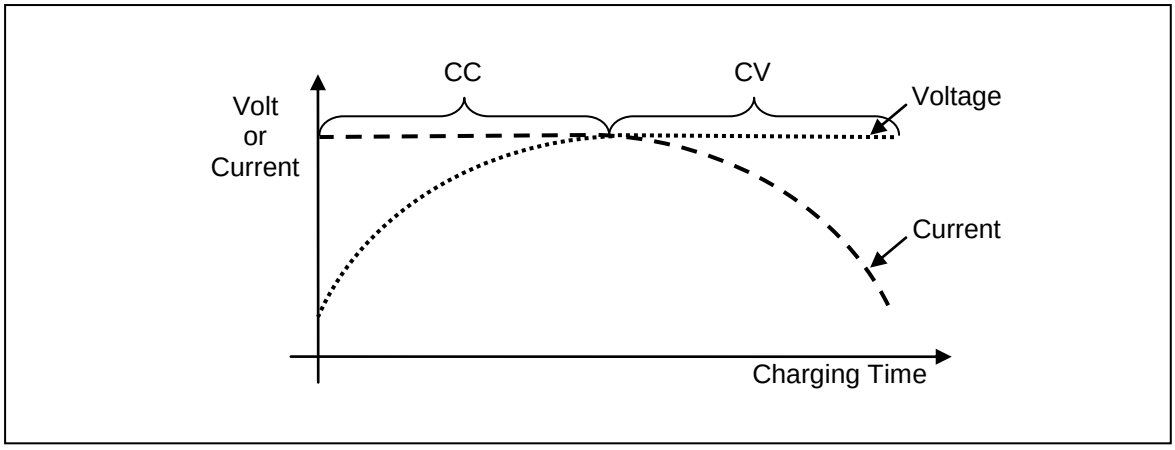


Figure 11.1 CC/CV charging process

At the beginning of charging process, constant current power is supplied to the battery. And the voltage is increased. After supplying voltage is limited by CV circuit, the current is decreased.

When the supplied current is lower than specific level(normally 0.1C), charging process is finished.

That is all, as you can see charging process is very simple when you have CC/CV block. Just enable the CC/CV block to charge and calculate the charging current from the voltage(measured by ADC) at the end of R_{SENSE} resister. And disable the CC/CV block when the current is lower than specific level. See “Measuring the charging current” at next sub-chapter for more information.

11.1 Block Diagram

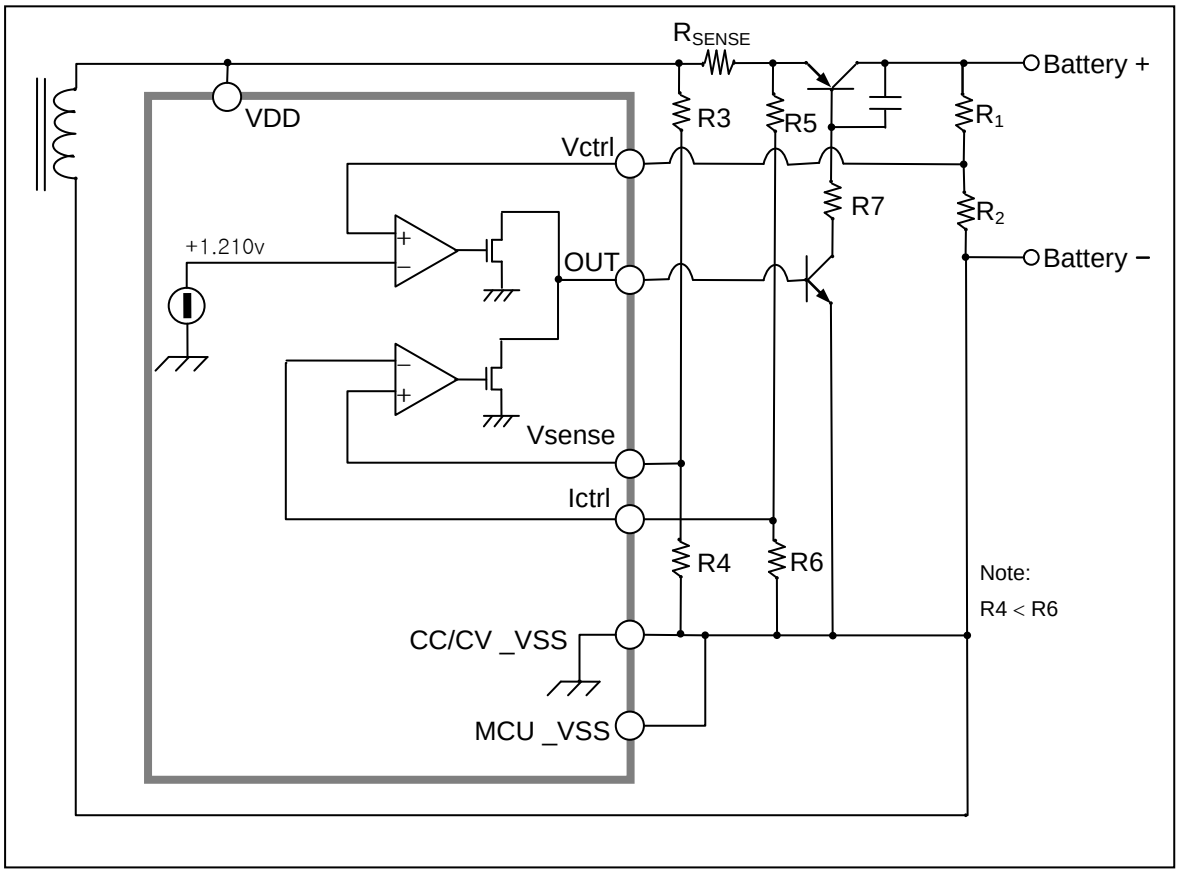


Figure 11.2 CC/CV application block diagram

Figure is a typical application circuit. The CC/CV block is mainly consisted of two OP-AMP circuits.

Voltage Control

The upper side OP-amp in Figure 11.2 controls the constant voltage output. Minus input of the OP-amp is a 1.210v band-gab reference source and plus input is the Vctrl what is the divided voltage of battery charging voltage. So dividing the charging voltage is the key to configure the constant voltage level.

In order to set the CV level, you must set R1 and R2 resister values to satisfy following equation.

$$\mathrm{CV} * \frac{\mathrm{R2}}{\mathrm{R1} + \mathrm{R2}} = 1.210\mathrm{v}$$

, when the CV is the desired constant voltage level for battery charging.

Current Control

The lower side OP-amp in Figure 11.2 controls the constant current output. Minus input of the OP-amp is equal to “Ictrl” and plus input is the “Vsense”. The voltage of R6/(R5+R6) divider is not the voltage of R4/(R3+R4) divider instead, there is a R_{SENSE} resistor between R6/(R5+R6) divider and the voltage of R4/(R3+R4) divider. So, divided voltage level with R6/(R5+R6) is changed based on the current of R_{SENSE}.

When the current of R_{SENSE} is zero, the R6/(R5+R6) divided voltage is higher than the R4/(R3+R4) divided voltage. And it is decreasing until the R4/(R3+R4) divided voltage while the current of R_{SENSE} is increasing.

In order to set the CC level, you must set R_{SENSE} resister value to satisfy following equation.

For example, if the base voltage of R_{SENSE} resister is 200mV, the following equation is completed.

$$CC * R_{SENSE} = 200mV$$

, when the CC is the desired constant current level for battery charging.

Measuring the charging current

To catch the terminating time of charging process it is required to measure the charging current. It is possible to calculate the charging current from the voltage of V_{SENSE} and Ictrl port. And it is possible to measure the V_{SENSE} and Ictrl port's voltage level by ADC. The Vsense and Ictrl port is connected to internal ADC channel. So no more extra circuits are required to measure it.

After get the Vsense and Ictrl voltage level you can easily calculate the charging current by following equation.

Normally, when the current rate is equal or less than 10% compared to maximum current, the CC cut off operation is executed.

$$\text{Charging Current} = \frac{\Delta VR_{SENSE}}{R_{SENSE}} = \left(1 + \frac{R3}{R4}\right) Vsense - (1 + \frac{R5}{R6} Ictrl)$$

11.2 Register Map

CC_CVR(CC/CV Control Register) : 9EH

7	6	5	4	3	2	1	0
-	-	REFOUT_EN	CC_CVEN-	VC_SEL	IC_SEL	VS_SEL	VO_SEL
-	-	-	R/W	R/W	R/W	R/W	R/W

Initial value : 10H

REFOUT_EN Reference voltage(1.8V VDC) output enable
- 0 REFOUT Disable
- 1 REFOUT Enable

CC_CVEN CC/CV block Enable/Disable bit
- 0 CC/CV Disable
- 1 CC/CV Enable

VC_SEL V Control Selection bit
- 0 Disable
- 1 Enable

IC_SEL I Control Selection bit
- 0 Disable
- 1 Enable

VS_SEL V Sense Selection bit
- 0 Disable
- 1 Enable

VO_SEL V Out Selection bit

0	Disable
1	Enable

Note. Before fall in STOP mode, You must disable all CC/CV functions by clear the CC_CVR register with 00_H.

Note. When you use the REFOUT, It is recommendable to put a bypass capacitor at the REFOUT port.

11.3 Reference Voltage Out(1.80V VDC)

11.3.1 How to use Reference Voltage Out

1. Set REFOUT_EN bit of CC_CVR register to 1, and then the 1.80V reference voltage is output to port and ADC channel.
2. Measure the precise voltage level for 1.80V reference voltage by using ADC.
3. Read the option(FUSE_CONF2) byte located in F9H address of SFR area.
4. Find the an exact voltage level as compare with FUSE_CONF2 value

11.3.2 The Contents of FUSE_CONF2 register (SFR address : F9H)

1. The trimmed data for 1.80V reference voltage is written to 7-bits of FUSE_CONF2 register(bit7~bit1) except bit0(PKG information). Be careful not to change bit0.
2. Each step is separated every 5mV unit
3. The structure of "Bit7 to Bit 1" is same as the follows.
   0000000B : the reference voltage is 1.600V
   0000001B : the reference voltage is 1.605V
   0000010B : the reference voltage is 1.610V
   0000011B : the reference voltage is 1.615V
   0000100B : the reference voltage is 1.620V
   …

12. Clock Generator

12.1 Overview

As shown in Figure 12.1, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains main-frequency clock oscillator. The system clock operation can be easily obtained by attaching a crystal between the XIN and XOUT pin, respectively. The system clock can also be obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN pin and open the XOUT pin. The default system clock is INT-RC Oscillator and the default division rate is one. In order to stabilize system internally, use 8 MHz RC oscillator for BIT and WDT.

- Calibrated Internal RC Oscillator (8 MHz / ±8%)
  . INT-RC OSC/1 (Default system clock)
  . INT-RC OSC/2 (4 MHz)
  . INT-RC OSC/4 (2 MHz)
  . INT-RC OSC/8 (1 MHz)
- Crystal Oscillator (1~8 MHz)
- Internal RCWDT Oscillator (1MHz / ±30%)

12.2 Block Diagram

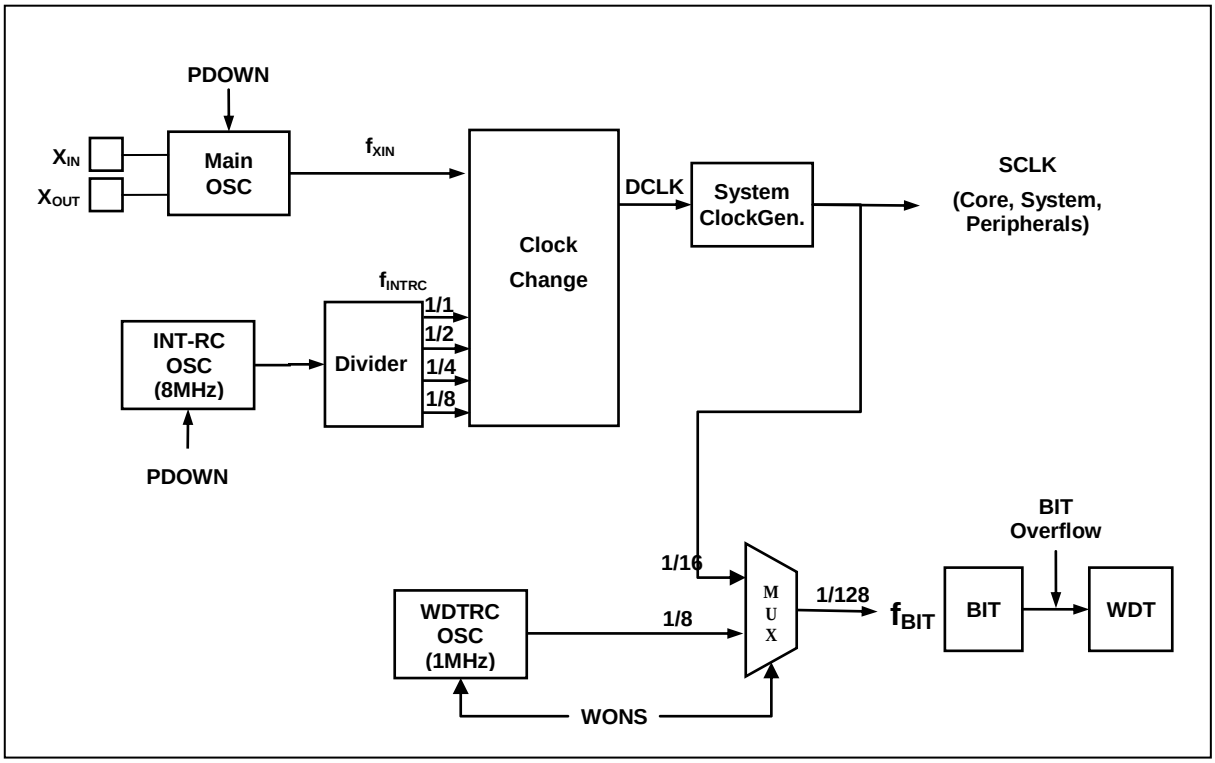


Figure 12.1 Clock Generator Block Diagram

12.3 Register Map

Table 12-1 Register Map

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	04H	System and Clock Control Register

12.4 Clock Generator Register description

The Clock Generation Register uses clock control for system operation. The clock generation consists of System and Clock register.

12.5 Register description for Clock Generator

SCCR (System and Clock Control Register) : 8AH

7	6	5	4	3	2	1	0
WONS	DIV1	DIV0	CBYS	ISTOP	XSTOP	CS1	CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 04H

WONS Control the operation of WDT RC-Oscillation during stop mode

0 WDTRC-Oscillator is disabled at stop mode (=STOP2)

1 WDTRC-Oscillator is enabled at stop mode (=STOP1)

DIV[1:0] When using fINTRC as system clock, determine division rate. Note) when using fINTRC as system clock, only division rate come into effect.

Note) To change by software, CBYS set to '1'

DIV1	DIV0	Description
0	0	fINTRC/1 (8MHz)
0	1	fINTRC/2 (4MHz)
1	0	fINTRC/4 (2MHz)
1	1	fINTRC/8 (1MHz)

CBYS Control the scheme of clock change. If this bit set to '0', clock change is controlled by hardware. But if this set to '1', clock change is controlled by software. Ex) when setting CS[1:0], if CBYS bit set to '0', it is not changed right now, CPU goes to STOP mode and then when wake-up, it applies to clock change.

Note) when clear this bit, keep other bits in SCCR

0 Clock changed by hardware during stop mode (default)

1 Clock changed by software

ISTOP Control the operation of INT-RC Oscillation

Note) when CBYS='1', It is applied

0 RC-Oscillation enable (default)

1 RC-Oscillation disable

XSTOP Control the operation of X-Tal Oscillation

Note1) when CBYS='1', It is applied

Note2) if XINENA bit in FUSE_CONF to '0', XSTOP is fixed to '1'

0 X-Tal Oscillation enable

1 X-Tal Oscillation disable (default)

CS[1:0] Determine System Clock

Note) by CBYS bit, reflection point is decided

CS1	CS0	description
0	0	fINTRC INTRC (8 MHz)
0	1	fXIN External Main Clock (1~8 MHz)
1	0	Not available
1	1	Not available

13. Basic Interval Timer

13.1 Overview

The MC95FB204 has one 8-bit Basic Interval Timer that is free-run and can't stop. Block diagram is shown in Figure 13.1. In addition, the Basic Interval Timer generates the time base for watchdog timer counting. It also provides a Basic Interval Timer interrupt (BITF).

The MC95FB204 has these Basic Interval Timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As clock function, time interrupt occurrence

13.2 Block Diagram

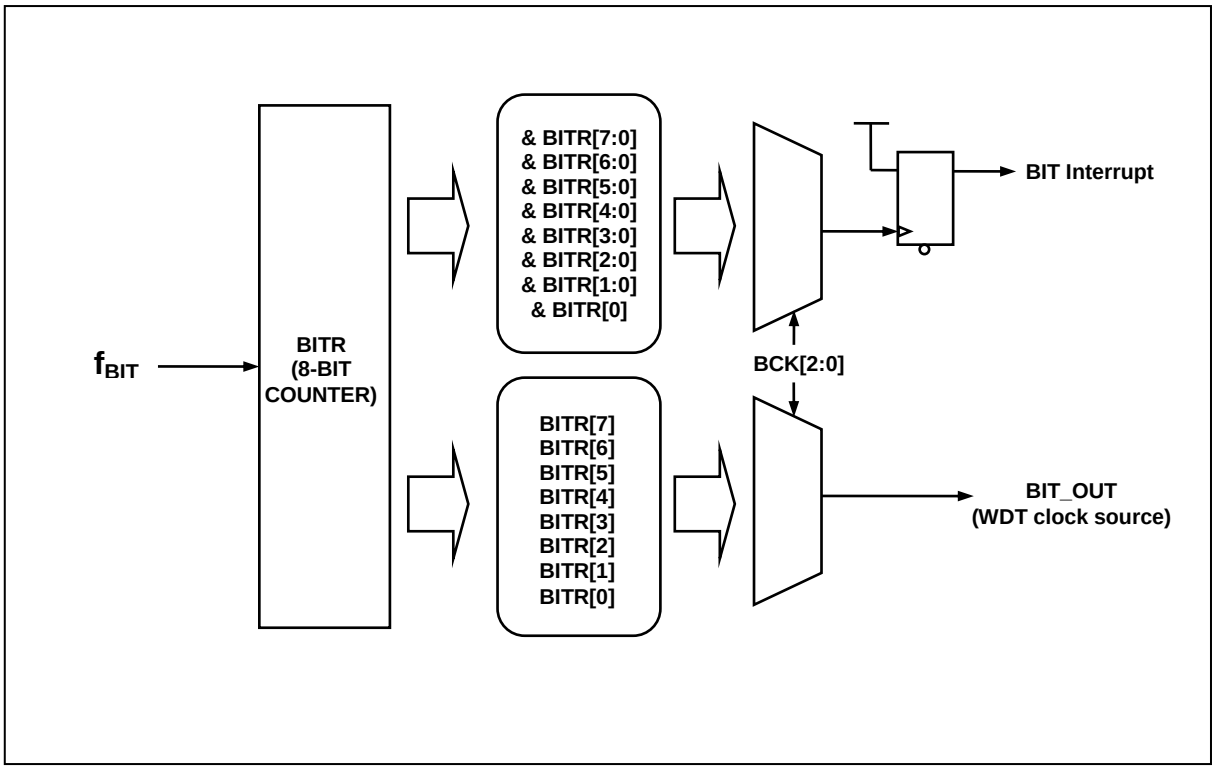


Figure 13.1 BIT Block Diagram

13.3 Register Map

Table 13-1 Register Map

Name	Address	Dir	Default	Description
BCCR	8BH	R/W	05H	BIT Clock Control Register
BITR	8CH	R	00H	Basic Interval Timer Register

13.4 Bit Interval Timer Register description

The Bit Interval Timer Register consists of BIT Clock control register (BCCR) and Basic Interval Timer register (BITR). If BCLR bit set to '1', BITR becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared as '0' automatically.

13.5 Register description for Bit Interval Timer

BCCR (BIT Clock Control Register) : 8BH

7	6	5	4	3	2	1	0
BITF	-	-	-	BCLR	BCK2	BCK1	BCK0
R/W	R	R	R	R/W	R/W	R/W	R/W

Initial value : 05H

BITF When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit.

0 no generation

1 generation

BCLR If BCLK Bit is written to '1', BIT Counter is cleared as '0'

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	
0	0	0	f_{BIT} / 2
0	0	1	f_{BIT} / 4
0	1	0	f_{BIT} / 8
0	1	1	f_{BIT} / 16
1	0	0	f_{BIT} / 32
1	0	1	f_{BIT} / 64 (default)
1	1	0	f_{BIT} / 128
1	1	1	f_{BIT} / 256

BITR (Basic Interval Timer Register) : 8CH

7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R	R	R	R	R	R	R	R

Initial value : 00H

BIT[7:0] BIT Counter

14. WDT

14.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or the like, and resumes the CPU to the normal state. The watchdog timer signal for detecting malfunction can be selected either a reset CPU or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTMR[6] bit. If writing WDTMR[5] to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit has '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTR, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset the CPU in accordance with the bit WDTRSON.

The clock source of Watch Dog Timer is BIT overflow output. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTR set value. The equation is as below

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTR Value+1)

14.2 Block Diagram

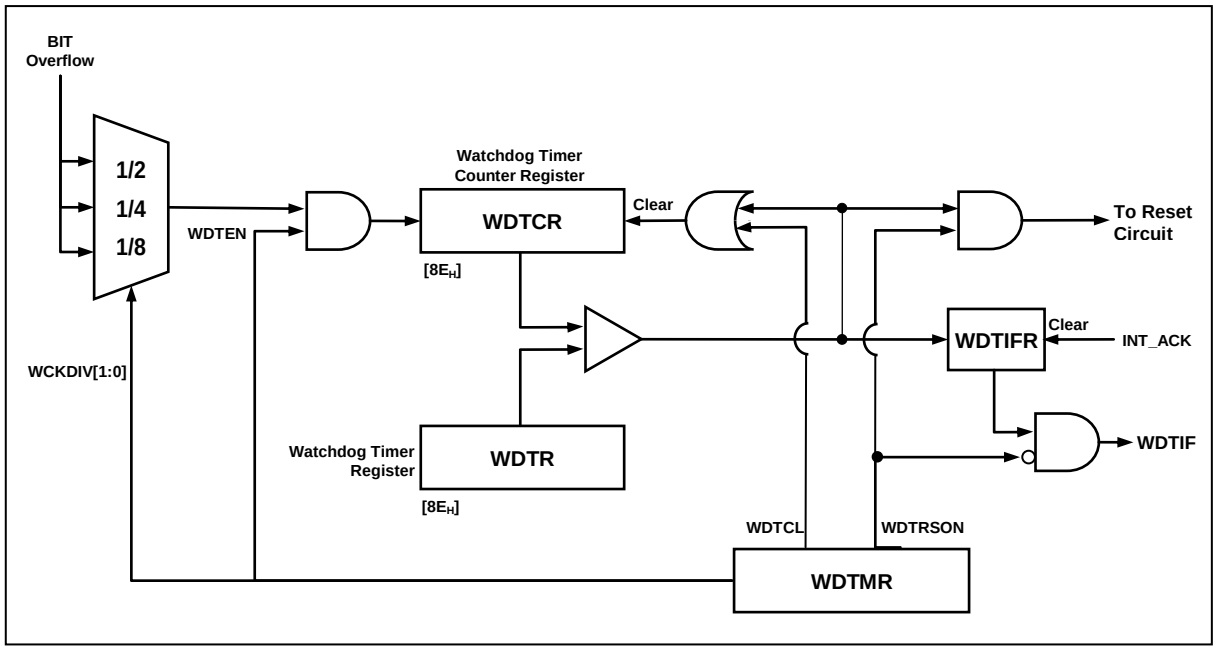


Figure 14.1 WDT Block Diagram

14.3 Register Map

Table 14-1 Register Map

Name	Address	Dir	Default	Description
WDTR	8E	W	FFH	Watch Dog Timer Register
WDTCR	8E	R	00H	Watch Dog Timer Counter Register

WDTMR	8D	R/W	00H	Watch Dog Timer Mode Register

14.4 Watch Dog Timer Register description

The Watch dog timer (WDT) Register consists of Watch Dog Timer Register (WDTR), Watch Dog Timer Counter Register (WDTCR) and Watch Dog Timer Mode Register (WDTMR).

14.5 Register description for Watch Dog Timer

WDTR (Watch Dog Timer Register:Write Case) : 8EH

7	6	5	4	3	2	1	0
WDTR7	WDTR6	WDTR5	WDTR4	WDTR3	WDTR2	WDTR1	WDTR0
W	W	W	W	W	W	W	W

Initial value : FFH

WDTR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTR Value+1)

Note) To guarantee proper operation, the data should be greater than 01H.

WDTCR (Watch Dog Timer Counter Register:Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCR7	WDTCR6	WDTCR5	WDTCR4	WDTCR3	WDTCR2	WDTCR1	WDTCR0
R	R	R	R	R	R	R	R

Initial value : 00H

WDTCR[7:0] WDT Counter

WDTMR (Watch Dog Timer Mode Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	WCKDIV1	WCKDIV0	-	-	WDTIFR
R/W	R/W	R/W	R/W	R/W	-	-	R/W

Initial value : 00H

WDTEN Control WDT operation
0 disable
1 enable

WDTRSON Control WDT Reset operation
0 Free Running 8-bit timer
1 Watch Dog Timer Reset ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WCKDIV[1:0] WDT Clock Division Selection
00 Default No Divided
01 WDT Clock = BIT Clock / 2
10 WDT Clock = BIT Clock / 4
11 WDT Clock = BIT Clock / 8

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write

'0' to this bit or auto clear by INT_ACK signal.

0 WDT Interrupt no generation

1 WDT Interrupt generation

14.6 WDT Interrupt Timing Waveform

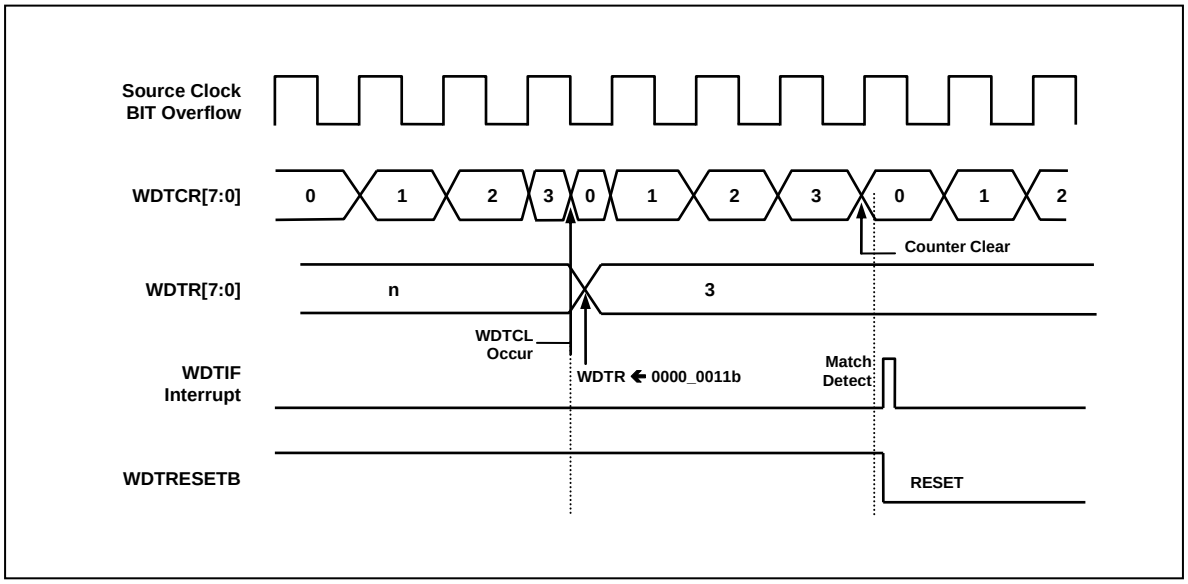


Figure 14.2 WDT Interrupt Timing Waveform

15. Timer/PWM

15.1 Overview

Timer 0 and timer 1 can be used either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, 8-bit timer data register, 8-bit counter register, mode register, input capture register, comparator. For PWM, it has PWM register (PWM1PR, PWM1DR, PWM1HR).

It has seven operating modes:

- 8 Bit Timer/Counter Mode
- 8 Bit Capture Mode
- 8 Bit Compare Output Mode
- 16 Bit Timer/Counter Mode
- 16 Bit Capture Mode
- 16 Bit Compare Output Mode
- PWM Mode

The timer/counter can be clocked by an internal or external clock source (external EC0). The clock source is selected by clock select logic which is controlled by the clock select (T0CK[2:0], T1CK[1:0]).

- TIMER0 clock source : fX/2, 4, 16, 64, 256, 1024, 4096, EC0
- TIMER1 clock source : fX/1, 2, 16, T0CK

In the capture mode, by INT0, INT1, the data is captured into Input Capture Register. The Timer 0 outputs the compare result to T0 port in 8/16-bit mode. Also the timer 1 outputs the result T1 port in the timer mode and the PWM wave form to PWM1 in the PWM mode.

Table 15.1 Operating Modes of Timer

16 Bit	CAP0	CAP1	PWM1E	T0CK[2:0]	T1CK[1:0]	T0/1_PE	Timer 0	Timer 1
0	0	0	0	XXX	XX	00	8 Bit Timer	8 Bit Timer
0	0	1	0	111	XX	00	8 Bit Event Counter	8 Bit Capture
0	1	0	0	XXX	XX	01	8 Bit Capture	8 Bit Compare Output
0	0	0	1	XXX	XX	11	8 Bit Timer/Counter	10 Bit PWM
1	0	0	0	XXX	11	00	16 Bit Timer	
1	0	0	0	111	11	00	16 Bit Event Counter	
1	1	1	0	XXX	11	00	16 Bit Capture	
1	0	0	0	XXX	11	01	16 Bit Compare Output	

15.2 8-Bit Timer/Counter Mode

The 8-bit Timer/Counter Mode is selected by control registers as shown in Figure 15.1.

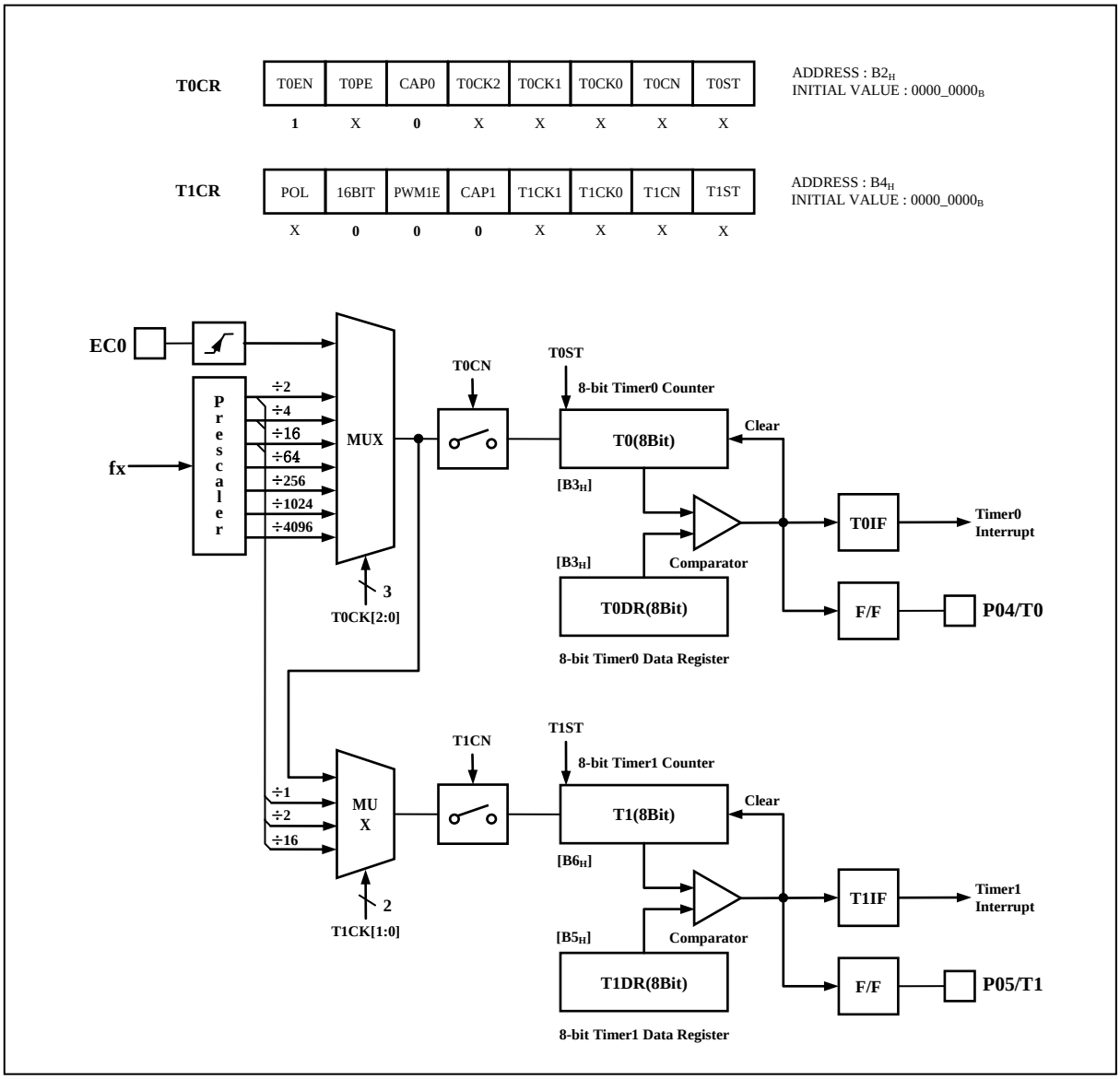


Figure 15.1 8 Bit Timer/Event Counter0, 1 Block Diagram

The two 8-bit timers have each counter and data register. The counter register is increased by internal or external clock input. The timer 0 can use the input clock with 2, 4, 16, 64, 256, 1024, 4096 prescaler division rates (T0CK[2:0]). The timer 1 can use the input clock with 1, 2, 16 and timer 0 overflow clock (T1CK[1:0]). When the value of T0, 1 value and the value of T0DR, T1DR are respectively identical in Timer 0, 1, the interrupt of timer 0, 1 occurs. The external clock (EC0) counts up the timer at the rising edge. If EC0 is selected from T0CK[2:0], EC0 port becomes input port. The timer 1 can't use the external EC0 clock.

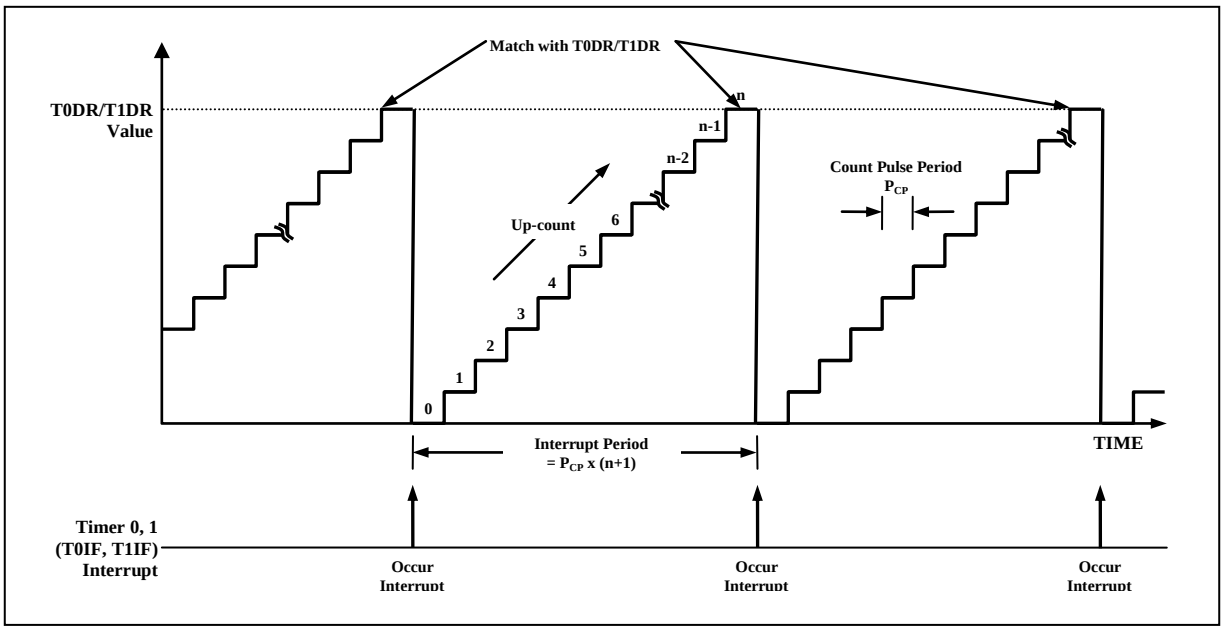


Figure 15.2 Timer/Event Counter0, 1 Example

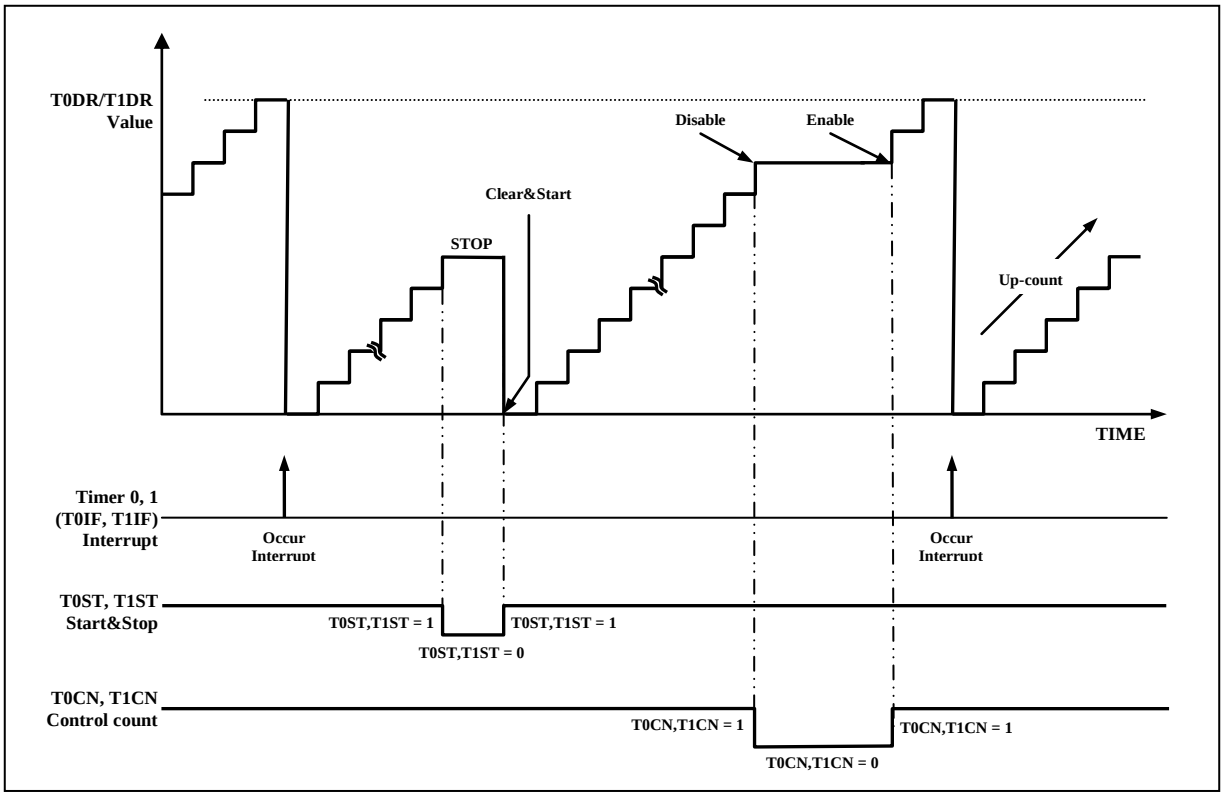


Figure 15.3 Operation Example of Timer/Event Counter0, 1

15.3 16-Bit Timer/Counter Mode

The timer register is being run with all 16bits. A 16-bit timer/counter register T0, T1 are incremented from 0000H to FFFFH until it matches T0DR, T1DR and then resets to 0000H. the match output generates the Timer 0 interrupt (no timer 1 interrupt). The clock source is selected from T0CK[2:0] and T1CK[1:0] must set 11b

and 16BIT bit must set to '1'. The timer 0 is LSB 8-bit, the timer 1 is MSB 8-bit. The 16-bit mode setting is shown as Figure 15.4.

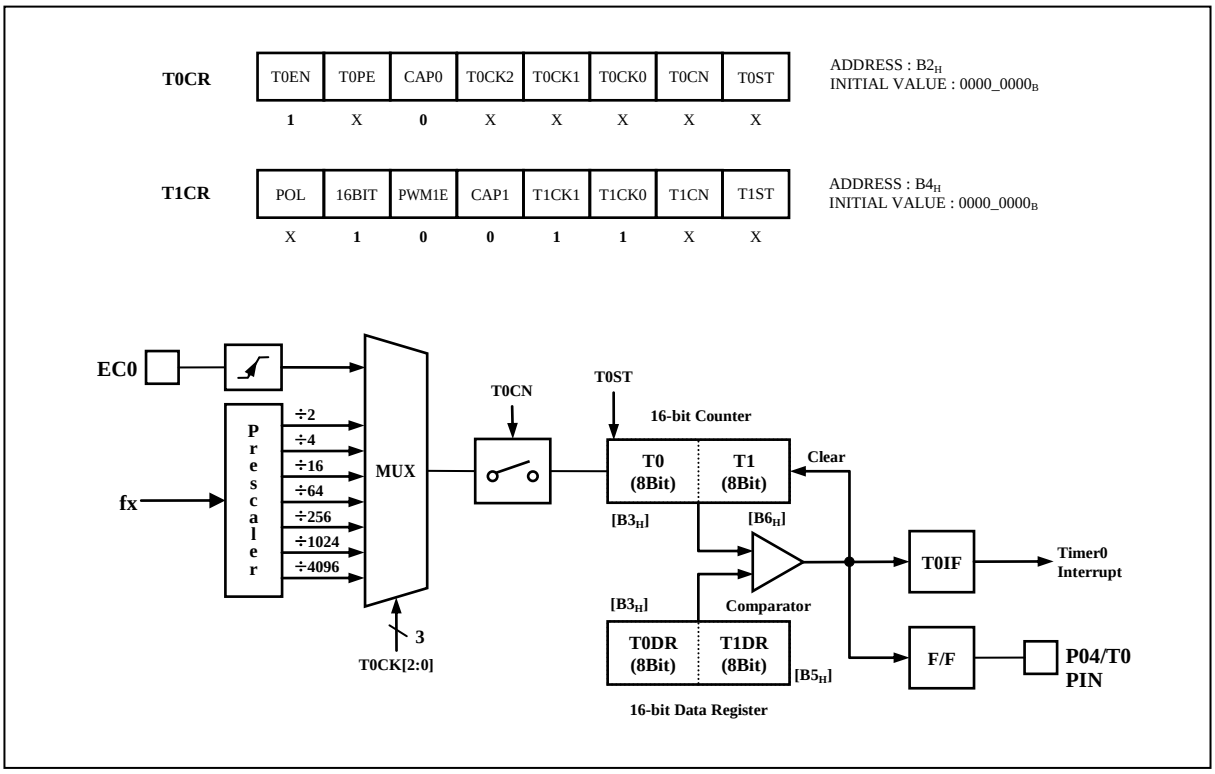


Figure 15.4 16 Bit Timer/Event Counter0, 1 Block Diagram

15.4 8-Bit Capture Mode

The timer 0, 1 capture mode is set by CAP0, CAP1 as '1'. The clock source can use the internal/external clock. Basically, it has the same function of the 8-bit timer/counter mode and the interrupt occurs at T0, T1 and T0DR, T1DR matching time, respectively. The capture result is loaded into CDR0, CDR1. The T0, T1 value is automatically cleared by hardware and restarts counter.

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

As the EIEDGE and EIPOLA register setting, the external interrupt INT0, INT1 function is chosen.

The CDR0, T0 and T0DR are in same address. In the capture mode, reading operation is read the CDR0, not T0DR because path is opened to the CDR0. The CDR1 has the same function.

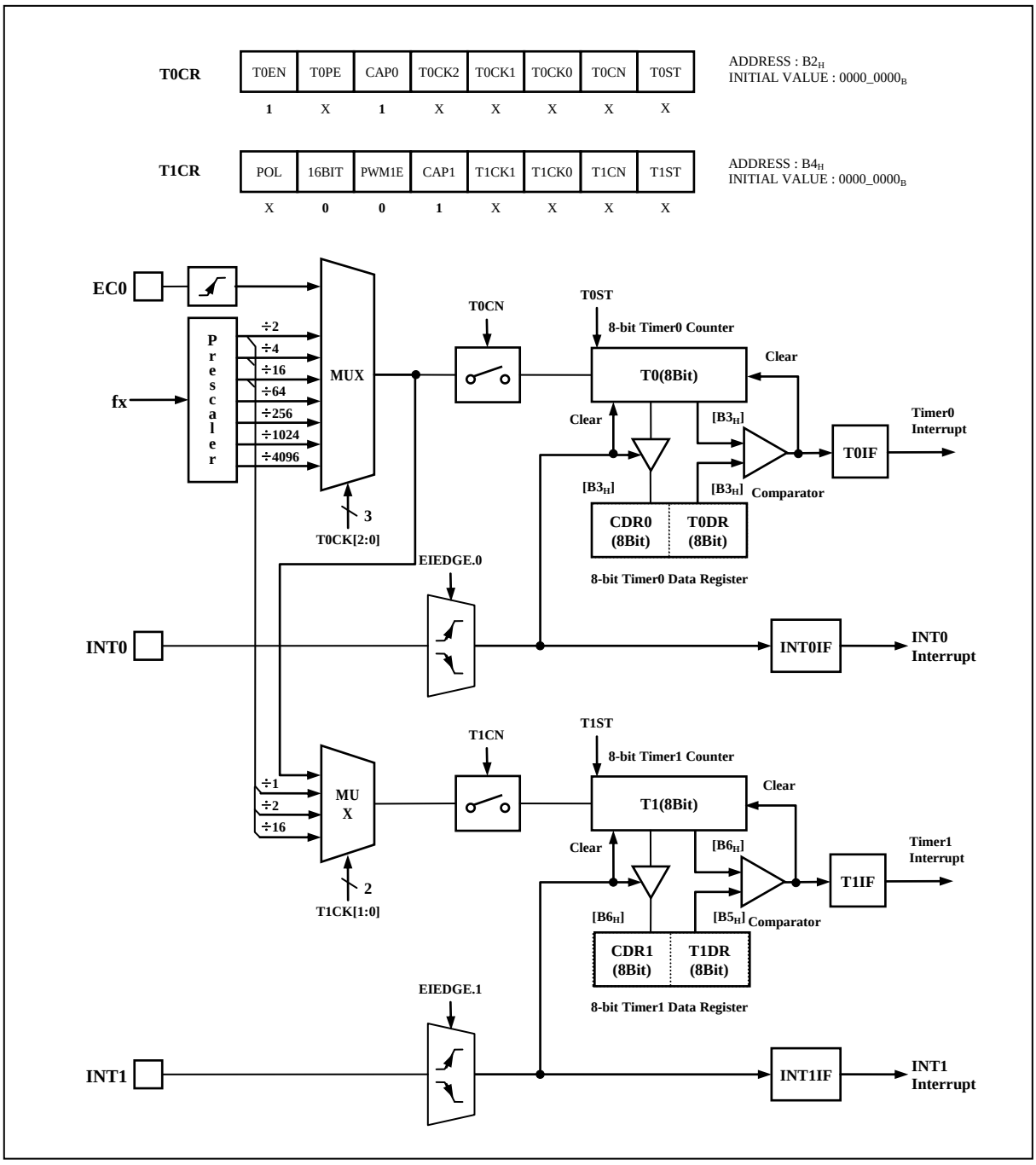


Figure 15.5 8-bit Capture Mode for Timer0, 1

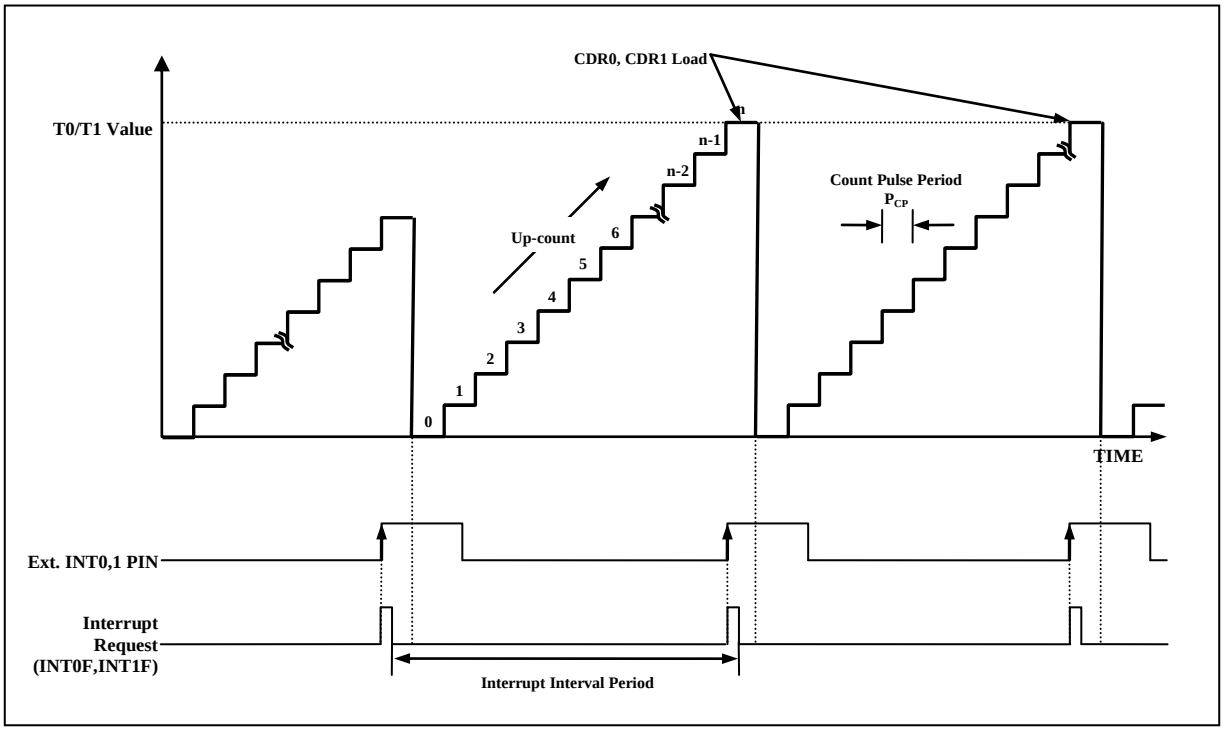


Figure 15.6 Input Capture Mode Operation of Timer 0, 1

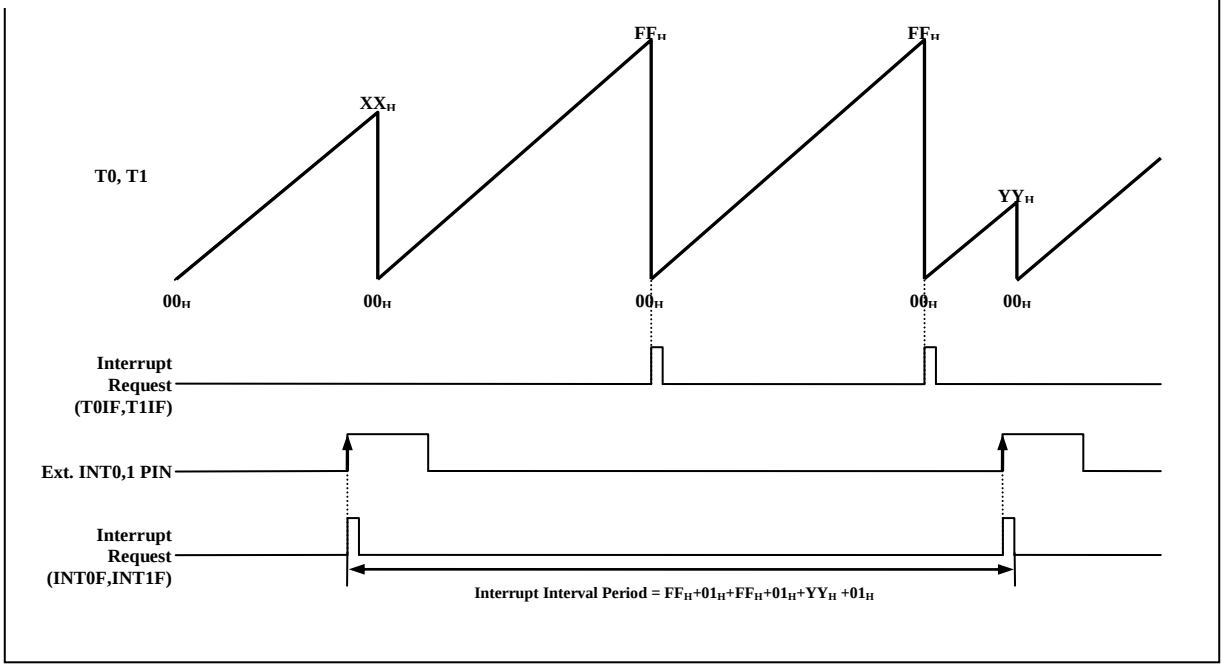


Figure 15.7 Express Timer Overflow in Capture Mode

15.5 16-Bit Capture Mode

The 16-bit capture mode is the same operation as 8-bit capture mode, except that the timer register uses 16 bits.

The clock source is selected from T0CK[2:0] and T1CK[1:0] must set 11b and 16BIT0 bit must set to '1'. The 16-bit mode setting is shown as Figure 15.8.

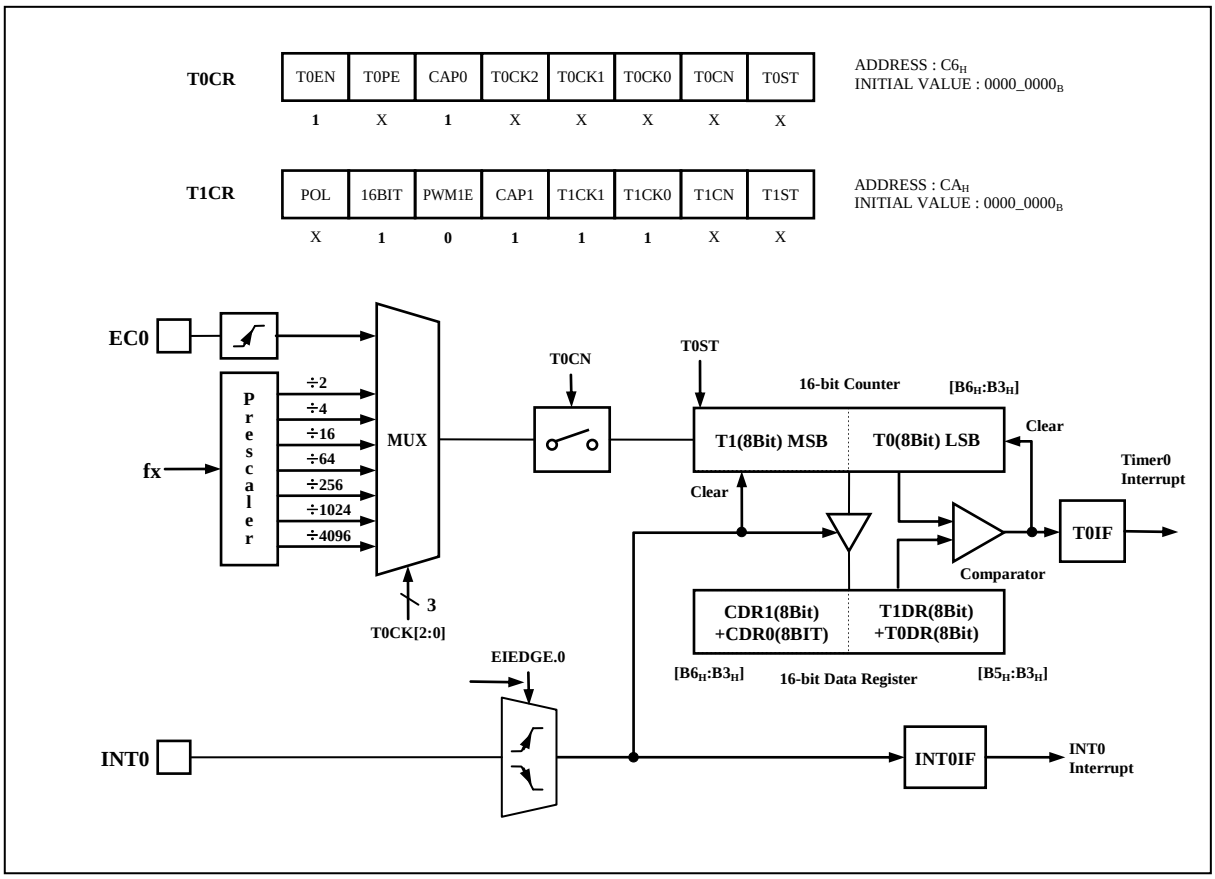


Figure 15.8 16-bit Capture Mode of Timer 0, 1

15.6 PWM Mode

The timer 1 has a PWM (pulse Width Modulation) function. In PWM mode, the T1/PWM1 output pin outputs up to 10-bit resolution PWM output. This pin should be configured as a PWM output by set T1_PE to '1'. The period of the PWM output is determined by the PWM1PR (PWM period register) + PWM1HR[3:2] + PWM1HR[1:0]

PWM Period = [PWM1HR[3:2]PWM1PR] X Source Clock

PWM Duty = [PWM1HR[1:0] PWM1DR] X Source Clock

Table 15.2 PWM Frequency vs. Resolution at 8 Mhz

Resolution	Frequency		
	T1CK[1:0]=00 (125ns)	T1CK[1:0]=01 (250ns)	T1CK[1:0]=10 (2us)
10 Bit	7.8KHz	3.9KHz	0.49KHz
9 Bit	15.6KHz	7.8KHz	0.98KHz
8 Bit	31.2KHz	15.6KHz	1.95KHz
7 Bit	62.4KHz	31.2KHz	3.91KHz

The POL bit of T1CR register decides the polarity of duty cycle. If the duty value is set same to the period value, the PWM output is determined by the bit POL (1: High, 0: Low). And if the duty value is set to "00H", the PWM output is determined by the bit POL (1: Low, 0: High).

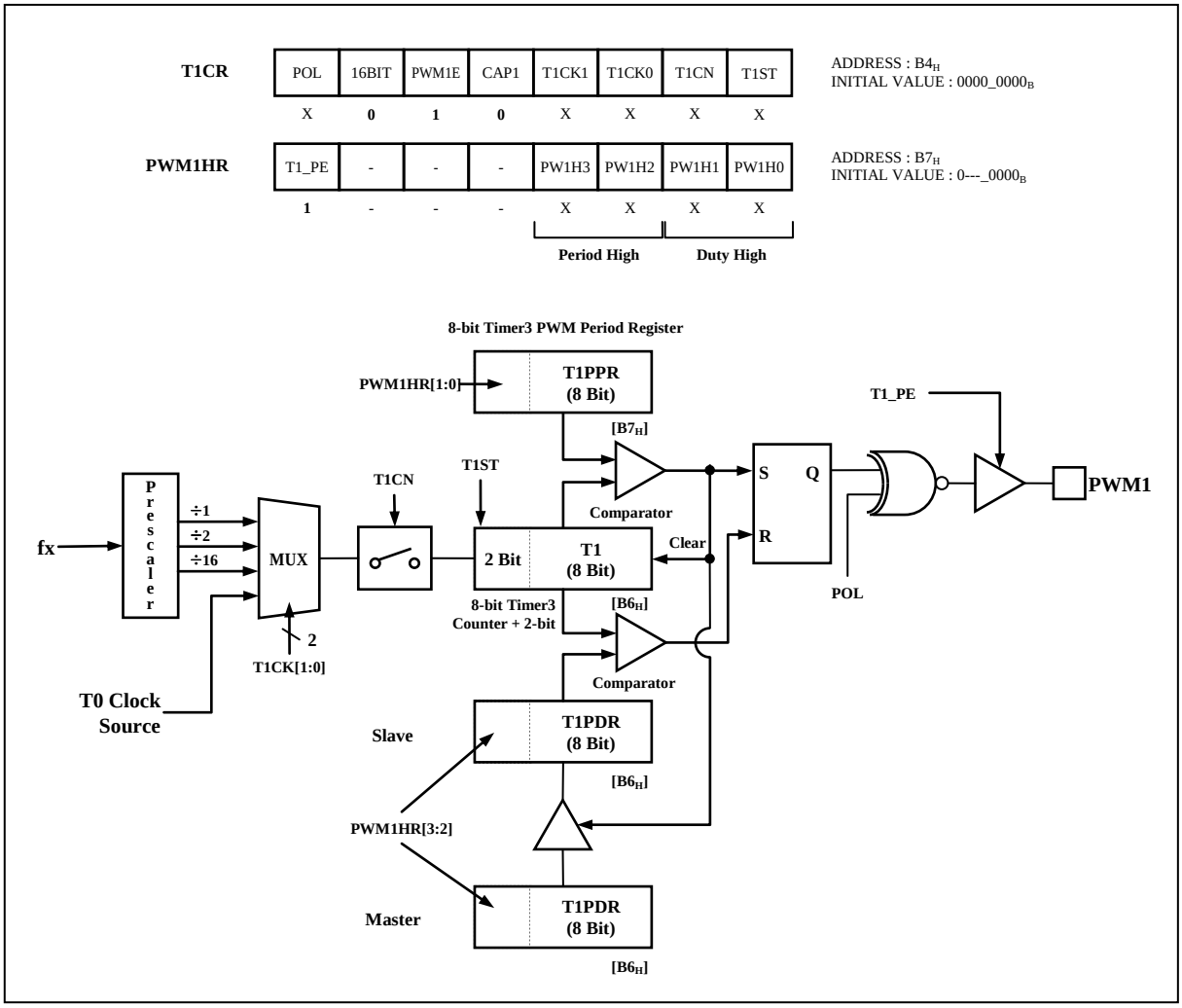


Figure 15.9 PWM Mode

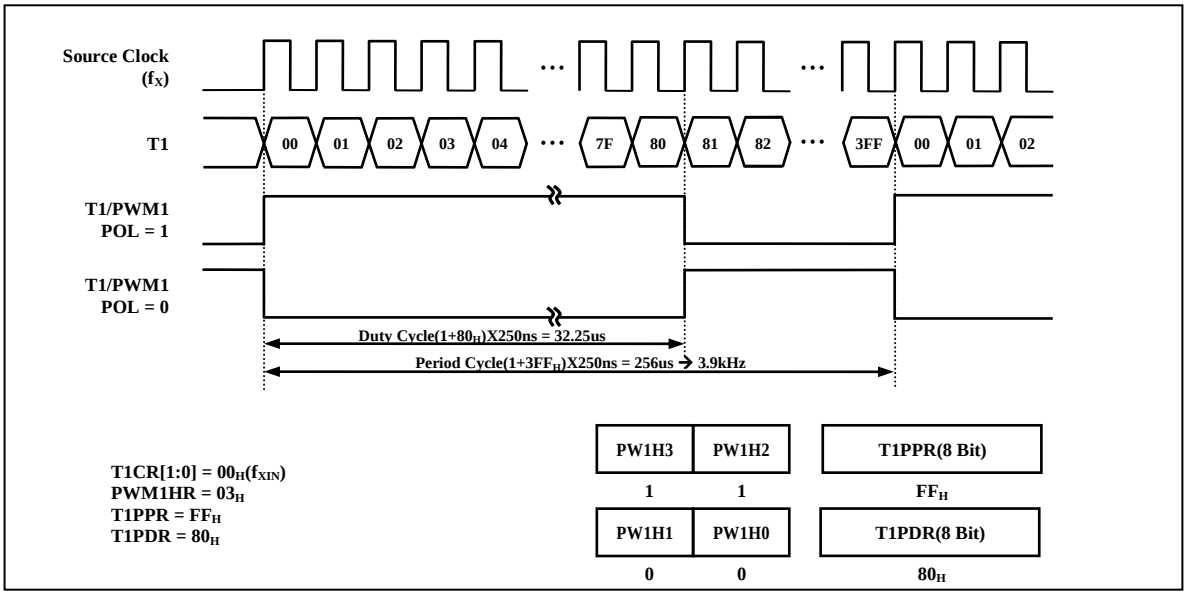


Figure 15.10 Example of PWM at 4MHz

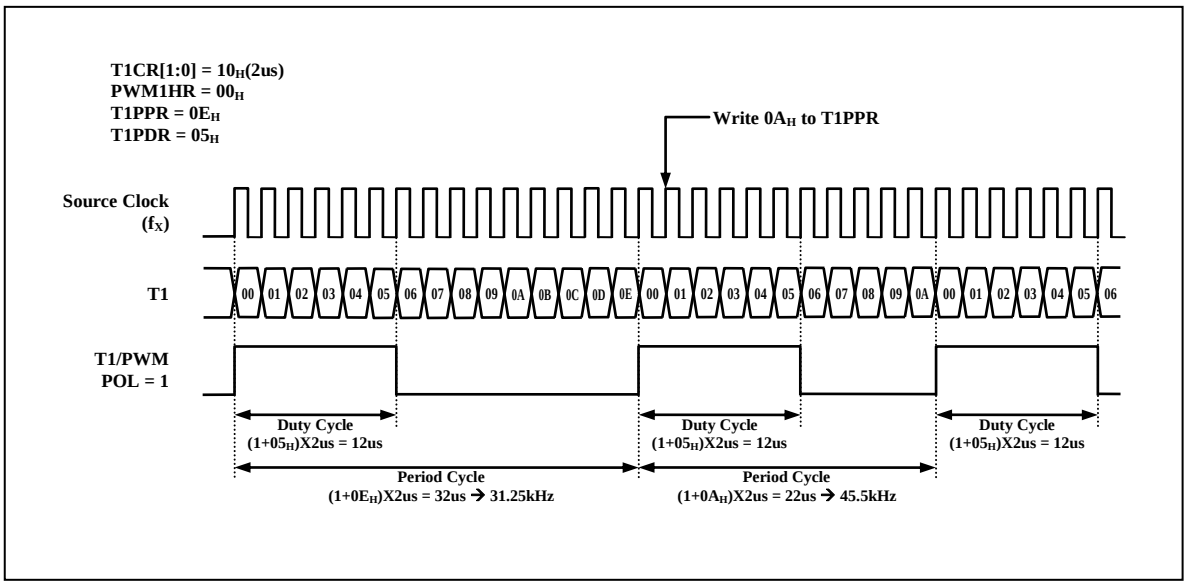


Figure 15.11 Example of Changing the Period in Absolute Duty Cycle at 4Mhz

15.7 8-Bit (16-Bit) Compare Output Mode

If the T1 (T0+T1) value and the T1DR (T0DR+T1DR) value are matched, T1/PWM1 port outputs. The output is 50:50 of duty square wave, the frequency is following

$$f_{COMP} = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Value} \times (TDR + 1)}$$

To export the compare output as T1/PWM1, the T1_PE bit in the PWM1HR register must set to '1'.

15.8 Register Map

Table 15.3 Timer Register Map

Name	Address	Dir	Default	Description
T0CR	B2H	R/W	00H	Timer 0 Mode Control Register
T0	B3H	R	00H	Timer 0 Register
T0DR	B3H	W	FFH	Timer 0 Data Register
CDR0	B3H	R	00H	Capture 0 Data Register
T1CR	B4H	R/W	00H	Timer 1 Mode Control Register
T1DR	B5H	W	FFH	Timer 1 Data Register
PWM1PR	B5H	W	FFH	Timer 1 PWM Period Register
T1	B6H	R	00H	Timer 1 Register
PWM1DR	B6H	R/W	00H	Timer 1 PWM Duty Register
CDR1	B6H	R	00H	Capture 1 Data Register
PWM1HR	B7H	W	00H	Timer 1 PWM High Register

15.9 Timer/Counter 0, 1 Register description

The Timer/Counter 0, 1 Register consists of Timer 0 Mode Control Register (T0CR), Timer 0 Register (T0), Timer 0 Data Register (T0DR), Capture 0 Data Register (CDR0), Timer 1 Mode Control Register (T1CR),

Timer 1 Data Register (T1DR), Timer 1 PWM Period Register (PWM1PR), Timer 1 Register (T1), Timer 1 PWM Duty Register (PWM1PR), Capture 1 Data Register (CDR1) and Timer 1 PWM High Register (PWM1HR).

15.10 Register description for Timer/Counter 0, 1

T0CR (Timer 0 Mode Control Register) : B2H

7	6	5	4	3	2	1	0
T0EN	T0_PE	CAP0	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T0EN Control Timer 0

0 Timer 0 disable

1 Timer 0 enable

T0_PE Control Timer 0 Output port

0 Timer 0 Output disable

1 Timer 0 Output enable

CAP0 Control Timer 0 operation mode

0 Timer/Counter mode

1 Capture mode

T0CK[2:0] Select Timer 0 clock source. Fx is main system clock frequency

T0CK2	T0CK1	T0CK0	Description
0	0	0	fx/2
0	0	1	fx/2^2
0	1	0	fx/2^4
0	1	1	fx/2^6
1	0	0	fx/2^8
1	0	1	fx/2^10
1	1	0	fx/2^12
1	1	1	External Clock (EC0)

T0CN Control Timer 0 Count pause/continue

0 Temporary count stop

1 Continue count

T0ST Control Timer 0 start/stop

0 Counter stop

1 Clear counter and start

T0 (Timer 0 Register: Read Case) : B3H

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00
R	R	R	R	R	R	R	R

Initial value : 00H

T0[7:0] T0 Counter data

T0DR (Timer 0 Data Register: Write Case) : B3H

7	6	5	4	3	2	1	0
T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
W	W	W	W	W	W	W	W

Initial value : FFH

T0D[7:0] T0 Compare data

CDR0 (Capture 0 Data Register: Read Case) : B3H

7	6	5	4	3	2	1	0
CDR07	CDR06	CDR05	CDR04	CDR03	CDR02	CDR01	CDR00
R	R	R	R	R	R	R	R

Initial value : 00H

CDR0[7:0] T0 Capture data

T1CR (Timer 1 Mode Count Register) : B4H

7	6	5	4	3	2	1	0
POL	16BIT	PWM1E	CAP1	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

POL Configure PWM polarity

0 Negative (Duty Match: Clear)

1 Positive (Duty Match: Set)

16BIT Select Timer 1 8/16Bit

0 8 Bit

1 16 Bit

PWM1E Control PWM enable

0 PWM disable

1 PWM enable

CAP1 Control Timer 1 mode

0 Timer/Counter mode

1 Capture mode

T1CK[1:0] Select clock source of Timer 1. Fx is the frequency of main system.

T1CK1	T1CK0	description
0	0	fx
0	1	fx/2

	1	0	fx/2^4
	1	1	Use Timer 0 Clock

T1CN Control Timer 1 Count pause/continue

0	Temporary count stop
1	Continue count

T1ST Control Timer 1 start/stop

0	Counter stop
1	Clear counter and start

T1DR (Timer 1 Data Register: Write Case) : B5H

7	6	5	4	3	2	1	0
T1D7	T1D6	T1D5	T1D4	T1D3	T1D2	T1D1	T1D0
W	W	W	W	W	W	W	W

Initial value : FFH

T1D[7:0] T1 Compare data

PWM1PR (Timer 1 PWM Period Register: Write Case) : B5H

7	6	5	4	3	2	1	0
T1PP7	T1PP6	T1PP5	T1PP4	T1PP3	T1PP2	T1PP1	T1PP0
W	W	W	W	W	W	W	W

Initial value : FFH

T1PP[7:0] T1 PWM Period data

T1 (Timer 1 Register: Read Case) : B6H

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10
R	R	R	R	R	R	R	R

Initial value : 00H

T1[7:0] T1 Counter Period data

PWM1DR (Timer 1 PWM Duty Register) : B6H

7	6	5	4	3	2	1	0
T1PD7	T1PD6	T1PD5	T1PD4	T1PD3	T1PD2	T1PD1	T1PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T1PD[7:0] T1 PWM Duty data
Note) only write, when PWM1E '1'

CDR1 (Capture 1 Data Register: Read Case) : B6H

7	6	5	4	3	2	1	0
CDR17	CDR16	CDR15	CDR14	CDR13	CDR12	CDR11	CDR10
R	R	R	R	R	R	R	R

Initial value : 00H

CDR1[7:0] T1 Capture data

PWM1HR (Timer 1 PWM High Register) : B7H

7	6	5	4	3	2	1	0
T1_PE	-	-	-	PW1H3	PW1H2	PW1H1	PW1H0
W	-	-	-	W	W	W	W

Initial value : 00H

T1_PE Control Timer 1 Output port operation
Note) only writable Bit. Be careful
0 Timer 1 Output disable
1 Timer 1 Output enable

PW1H[3:2] PWM period High value (Bit [9:8])

PW1H[1:0] PWM duty High value (Bit [9:8])

PERIOD:	PW1H3	PW1H2	PWM1PR[7:0]
DUTY:	PW1H1	PW1H0	PWM1DR[7:0]

16. 12-Bit A/D Converter

16.1 Overview

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 12-bit digital value. The A/D module has tenth analog inputs. The output of the multiplex is the input into the converter, which generates the result via successive approximation. The A/D module has four registers which are the control register ADCM (A/D Converter Mode Register), ADCM2 (A/D Converter Mode Register 2) and A/D result register ADCHR (A/D Converter Result High Register) and ADCLR (A/D Converter Result Low Register). It is selected for the corresponding channel to be converted by setting ADSEL[3:0]. To executing A/D conversion, ADST bit sets to '1'. The register ADCHR and ADCLR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCHR and ADCLR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. For processing A/D conversion, AFLAG bit is read as '0'. If using STBY (power down) bit, the ADC is disabled. Also internal timer, external generating event, comparator, the trigger of timer1pwm and etc. can start ADC regardless of interrupt occurrence.

ADC Conversion Time = ADCLK * 60 cycles

After STBY bit is reset (ADC power enable) and it is restarted, during some cycle, ADC conversion value may have an inaccurate value.

16.2 Block Diagram

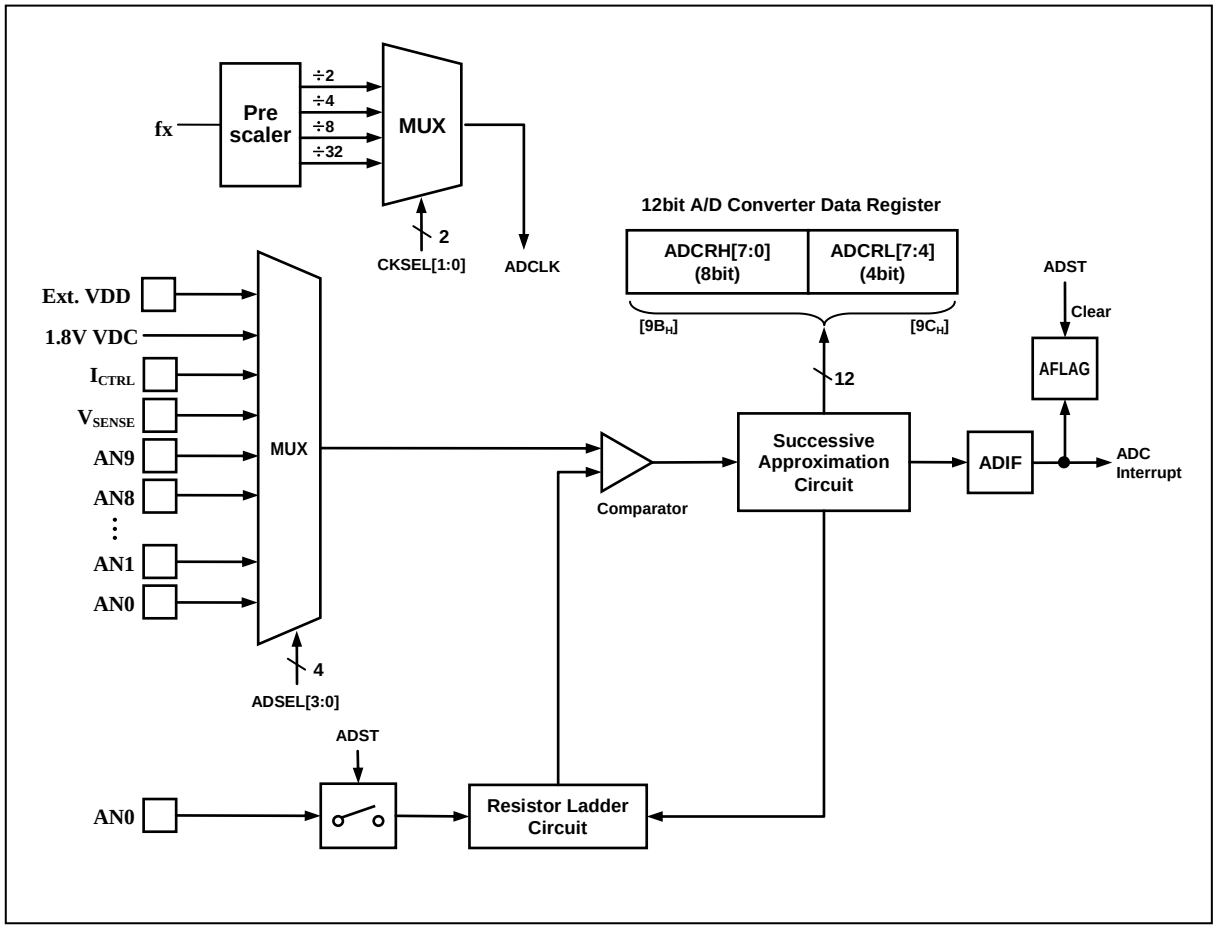


Figure 16.1 ADC Block Diagram

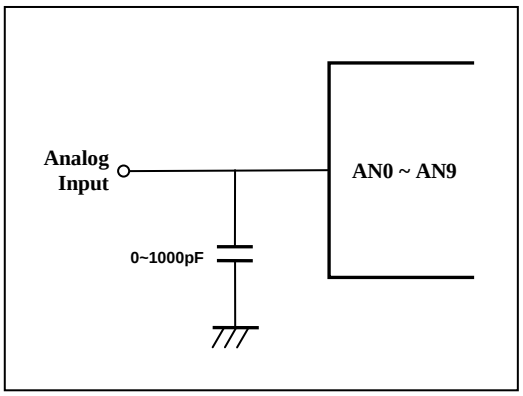


Figure 16.2 A/D Analog Input Pin Connecting Capacitor

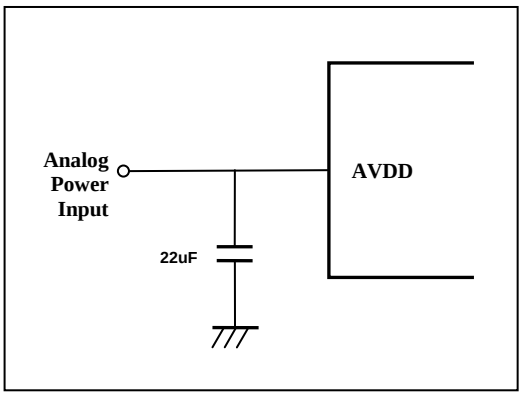


Figure 16.3 A/D Power(AVDD) Pin Connecting Capacitor

16.3 ADC Operation

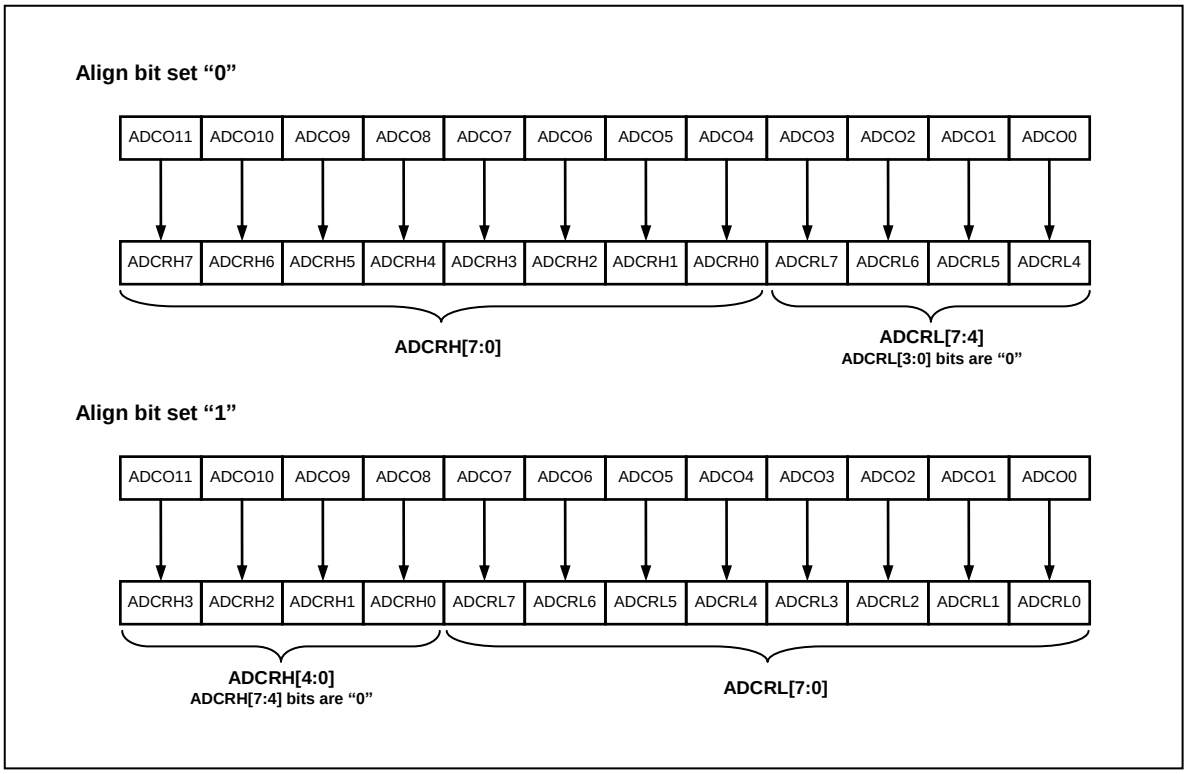


Figure 16.4 ADC Operation for Align bit

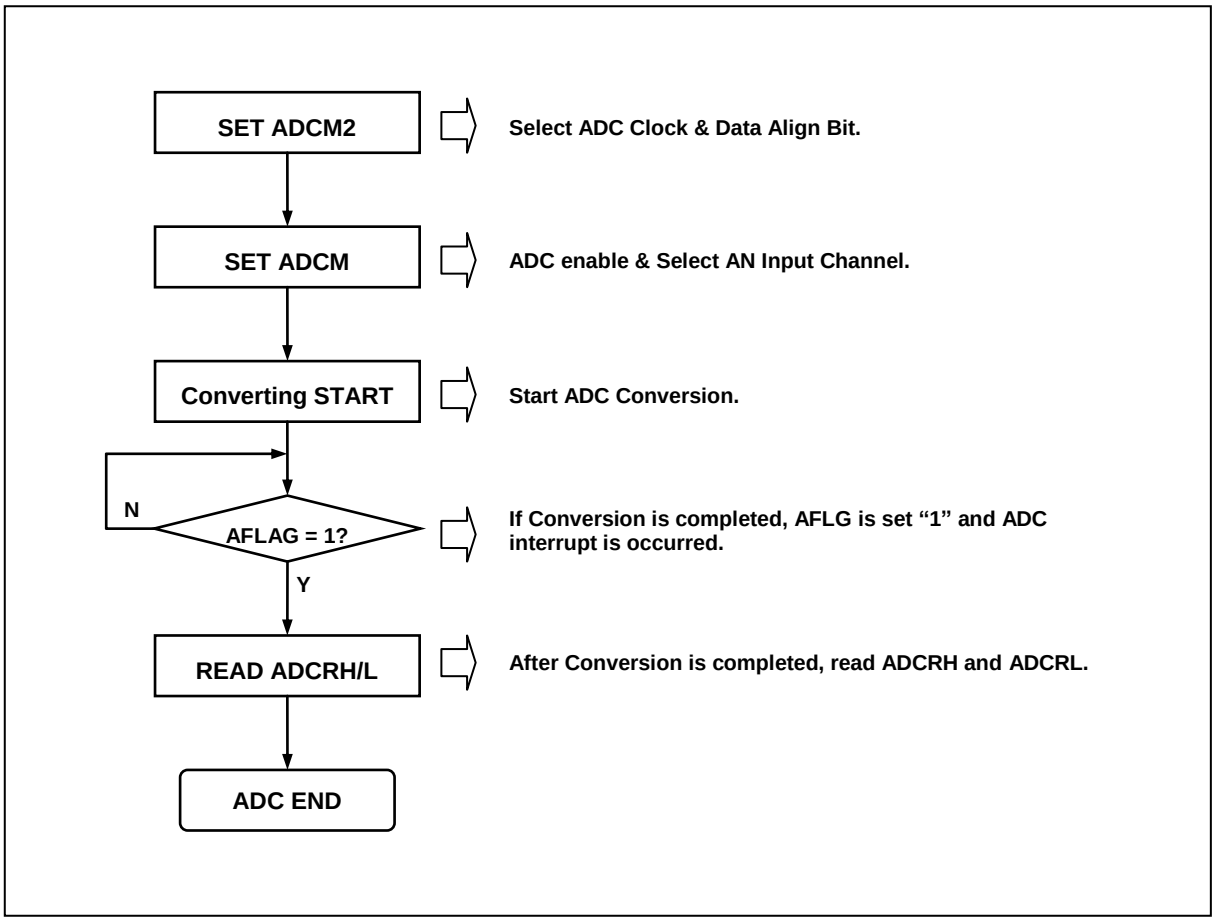


Figure 16.5 A/D Converter Operation Flow

16.4 Register Map

Table 16-1 Register Map

Name	Address	Dir	Default	Description
ADCM	9AH	R/W	8FH	A/D Converter Mode Register
ADCRH	9BH	R	-	A/D Converter Result High Register
ADCRL	9CH	R	-	A/D Converter Result Low Register
ADCM2	9BH	R/W	01H	A/D Converter Mode 2 Register
ALCPR0	92H	R/W	00H	ADC Leakage Current Protection Register 0
ALCPR1	93H	R/W	00H	ADC Leakage Current Protection Register 1

16.5 ADC Register description

The ADC Register consists of A/D Converter Mode Register (ADCM), A/D Converter Result High Register (ADCRH), A/D Converter Result Low Register (ADCRL), A/D Converter Mode 2 Register (ADCM2).

Note1: In case of ADCRH & ADCM2 reading, if STBY bit is set to '0' ADCRH can be read but if STBY bit is reset to '1' ADCM2 will be read.
In case of ADCM2 writing, always ADCM2 is written regardless of STBY bit.

16.6 Register description for ADC

ADCM (A/D Converter Mode Register) : 9AH

7	6	5	4	3	2	1	0
STBY	ADST	REFSEL	AFLAG	ADSEL3	ADSEL2	ADSEL1	ADSEL0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Initial value : 8FH

STBY Control operation of A/D standby (power down)
0 ADC module enable & ADCRH(R) selection
1 ADC module disable (power down) & ADCM2(R) selection

ADST Control A/D Conversion stop/start.
0 ADC Conversion Stop
1 ADC Conversion Start

REFSEL A/D Converter reference selection
0 Internal Reference (VDD)
1 External Reference(AVREF, AN0 disable)

AFLAG A/D Converter operation state
0 During A/D Conversion
1 A/D Conversion finished

ADSEL[3:0] A/D Converter input selection

ADSEL3	ADSEL2	ADSEL1	ADSEL0	Description
0	0	0	0	Channel0(AN0)
0	0	0	1	Channel1(AN1)
0	0	1	0	Channel2(AN2)
0	0	1	1	Channel3(AN3)
0	1	0	0	Channel4(AN4)
0	1	0	1	Channel5(AN5)
0	1	1	0	Channel6(AN6)
0	1	1	1	Channel7(AN7)
1	0	0	0	Channel8(AN8)
1	0	0	1	Channel9(AN9)
1	0	1	0	Channel10(V_{SENSE})
1	0	1	1	Channel11(N/A)
1	1	0	0	Channel12(1.8V VDC)
1	1	0	1	Channel13(Ext. VDD)
1	1	1	0	Channel14(I_{CTRL})
1	1	1	1	Channel15(N/A)

ADCRH (A/D Converter Result High Register) : 9BH

7	6	5	4	3	2	1	0

ADDM11	ADDM10	ADDM9	ADDM8	ADDM7 ADDL11	ADDM6 ADDL10	ADDM5 ADDL9	ADDM4 ADDL8
R	R	R	R	R	R	R	R

Initial value : xxH

ADDM[11:4] MSB align, A/D Converter High result (8-bit)

ADDL[11:8] LSB align, A/D Converter High result (4-bit)

ADCRL (A/D Converter Result Low Register) : 9CH

7	6	5	4	3	2	1	0
ADDM3 ADDL7	ADDM2 ADDL6	ADDM1 ADDL5	ADDM0 ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R-	R	R	R

Initial value : xxH

ADDM[3:0] MSB align, A/D Converter Low result (4-bit)

ADDL[7:0] LSB align, A/D Converter Low result (8-bit)

ADCM2 (A/D Converter Mode Register) : 9BH

7	6	5	4	3	2	1	0
					ALIGN	CKSEL1	CKSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 01H

ALIGN A/D Converter data align selection.

0 MSB align (ADCRH[7:0], ADCRL[7:4])

1 LSB align (ADCRH[3:0], ADCRL[7:0])

CKSEL[1:0] A/D Converter Clock selection

CKSEL1	CKSEL0	ADC Clock	ADC VDD
0	0	fx/2=4Mhz	Test Only
0	1	fx/4=2Mhz	3V~5V
1	0	fx/8=1Mhz	2.7V~3V
1	1	fx/32=0.25Mhz	2.4V~2.7V

ALCPR0 (ADC Leakage Current Protection Register 0) : 92H

7	6	5	4	3	2	1	0
ALCPR07	ALCPR06	ALCPR05	ALCPR04	ALCPR03	ALCPR02	ALCPR01	ALCPR00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ALCPR0[7:0] AN7~AN0 ADC leakage current protection register 0

0 Disable analog channel AN[7:0].

1 Enable analog channel AN[7:0].

ALCPR1 (ADC Leakage Current Protection Register 1) : 93H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ALCPR09	ALCPR08
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

ALCPR09	P15/AN9	ADC leakage current protection register
	0	Disable analog channel AIN9.
	1	Enable analog channel AIN9.
ALCPR08	P14/AN8	ADC leakage current protection register
	0	Disable analog channel AN8.
	1	Enable analog channel AN8.

17. Power Down Operation

17.1 Overview

The MC95FB204 has three power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, IDLE, STOP1 and STOP2 mode. In three modes, program is stopped.

17.2 Peripheral Operation In IDLE/STOP Mode

Table 17-1 Peripheral Operation during Power Down Mode

Peripheral	IDLE Mode	STOP1 Mode	STOP2 Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain	Retain
Basic Interval Timer	Operates Continuously	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Operates Continuously	Stop
TimerP0~1	Operates Continuously	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)
ADC	Operates Continuously	Stop	Stop
Internal OSC (8MHz)	Oscillation	Stop	Stop
Main OSC (1~8MHz)	Oscillation	Stop	Stop
Internal RCOSC (1MHz)	Oscillation	Oscillation	Stop
I/O Port	Retain	Retain	Retain
Control Register	Retain	Retain	Retain
Address Data Bus	Retain	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0), External Interrupt, WDT, BIT	By RESET, Timer Interrupt (EC0), External Interrupt

17.3 IDLE mode

The power control register is set to ‘01h’ to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

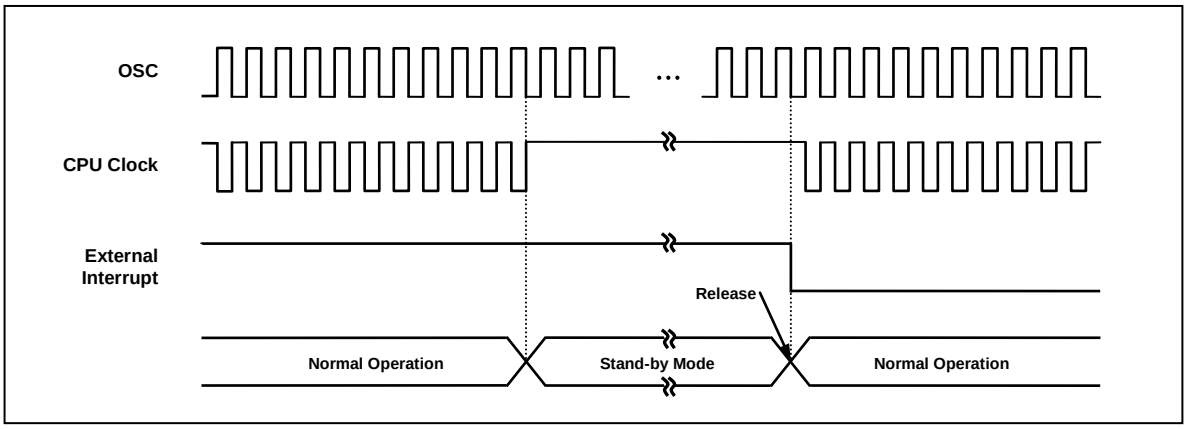


Figure 17.1 IDLE Mode Release Timing by External Interrupt

17.4 STOP mode

The power control register is set to '03h' to enter the STOP Mode. In the stop mode, the main oscillator, system clock and peripheral clock is stopped, but watch timer continue to operate. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers.

When exit from STOP mode, enough oscillation stabilization time is required to normal operation. Figure 17.2 shows the timing diagram. When released from STOP mode, the Basic interval timer is activated on wake-up. Therefore, before STOP instruction, user must be set its relevant prescale divide ratio to have long enough time. This guarantees that oscillator has started and stabilized.

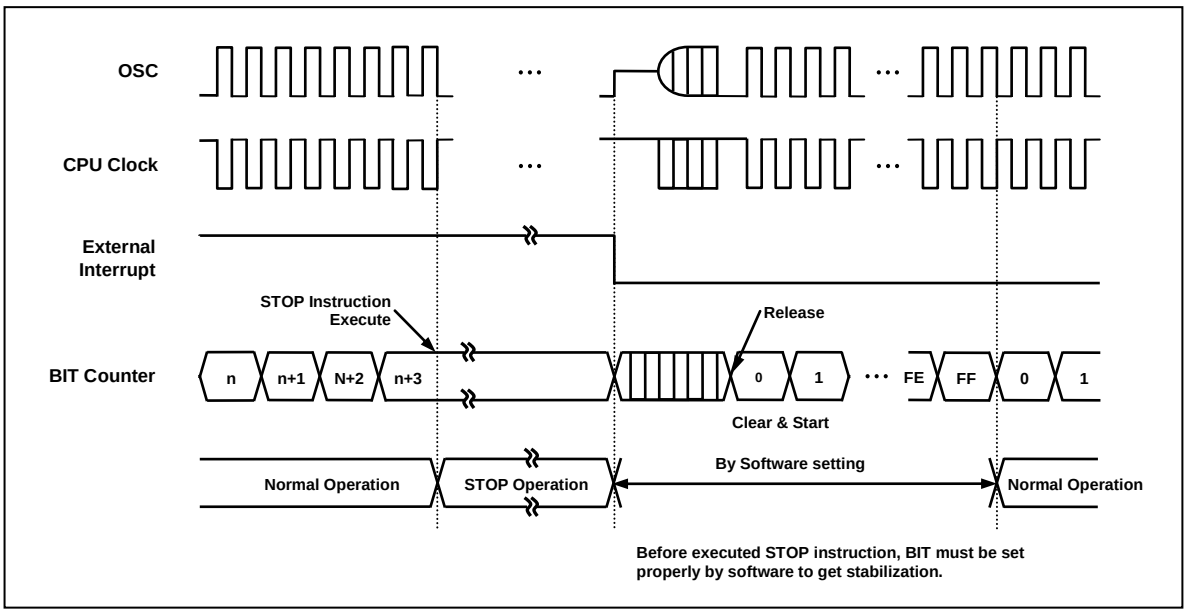


Figure 17.2 STOP Mode Release Timing by External Interrupt

17.5 Release Operation of STOP1, 2 Mode

After STOP1, 2 mode is released, the operation begins according to content of related interrupt register just before STOP1, 2 mode start (Figure 17.3). Interrupt Enable Flag of All (EA) of IE should be set to `1`. Released by only interrupt which each interrupt enable flag = `1`, and jump to the relevant interrupt service routine.

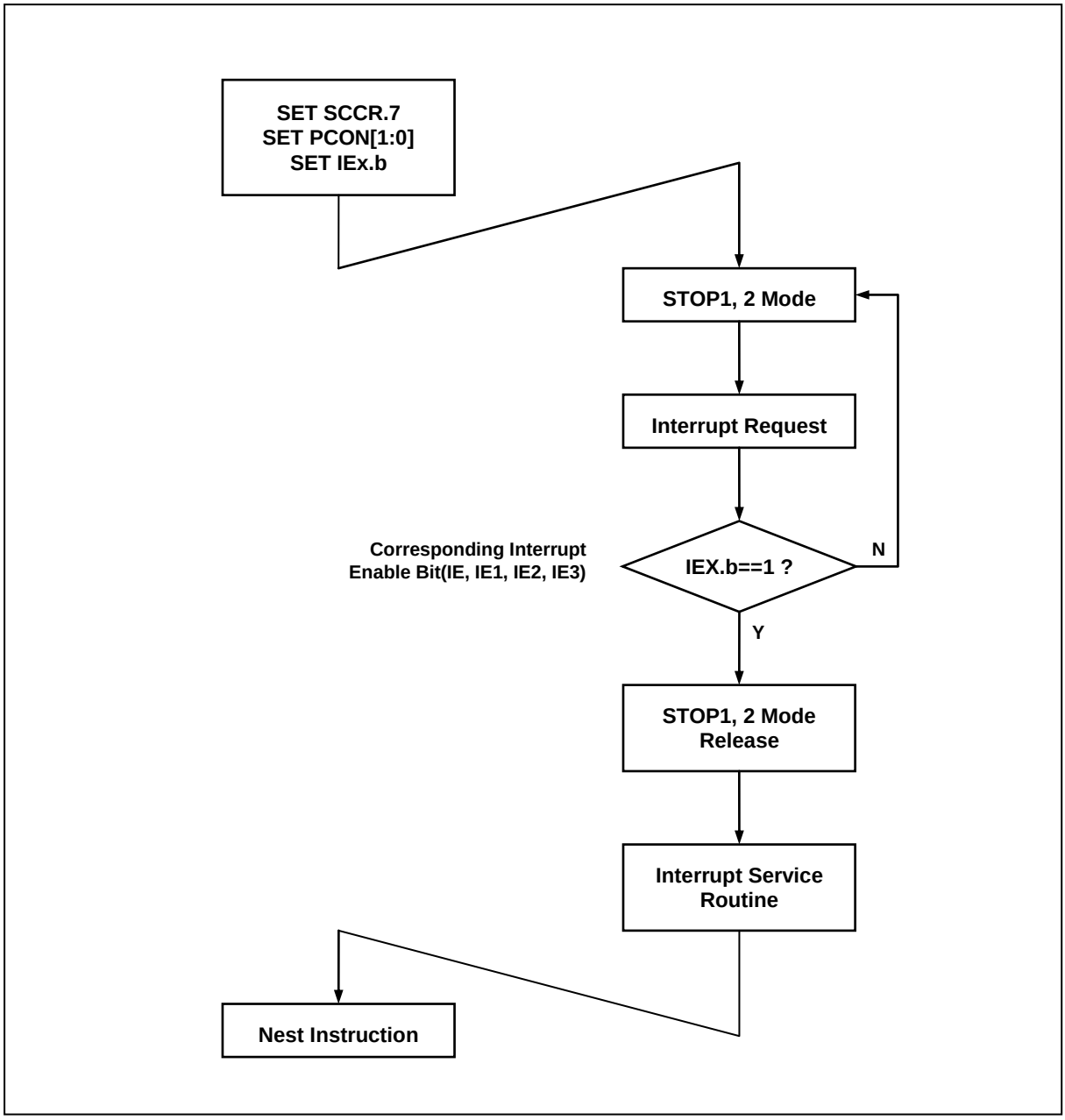


Figure 17.3 STOP1, 2 Mode Release Flow

17.5.1 Register Map

Table 17-2 Register Map

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register

17.5.2 Power Down Operation Register description

The Power Down Operation Register consists of the Power Control Register (PCON).

17.5.3 Register description for Power Down Operation

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IDLE Mode

01H IDLE mode enable

STOP1, 2 Mode

03H STOP1, 2 mode enable

Note)

1. To enter IDLE mode, PCON must be set to ‘01H’.
2. To STOP1,2 mode, PCON must be set to ‘03H’.
   (In STOP1,2 mode, PCON register is cleared automatically by interrupt or reset)
3. When PCON is set to ‘03H’, if SCCR[7] is set to ‘1’, it enters the STOP1 mode. if SCCR[7] is cleared to ‘0’, it enters the STOP2 mode
4. The different thing in STOP 1,2 is only clock operation of internal 1MHz-OSC during STOP mode operating.

18. RESET

18.1 Overview

The MC95FB204 has reset by external RESETB pin. The following is the hardware setting value.

Table 18-1 Reset state

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Peripheral Registers refer
CC/CV	Disable

18.2 Reset source

The MC95FB204 has four types of reset generation procedures. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- OCD Reset

18.3 Block Diagram

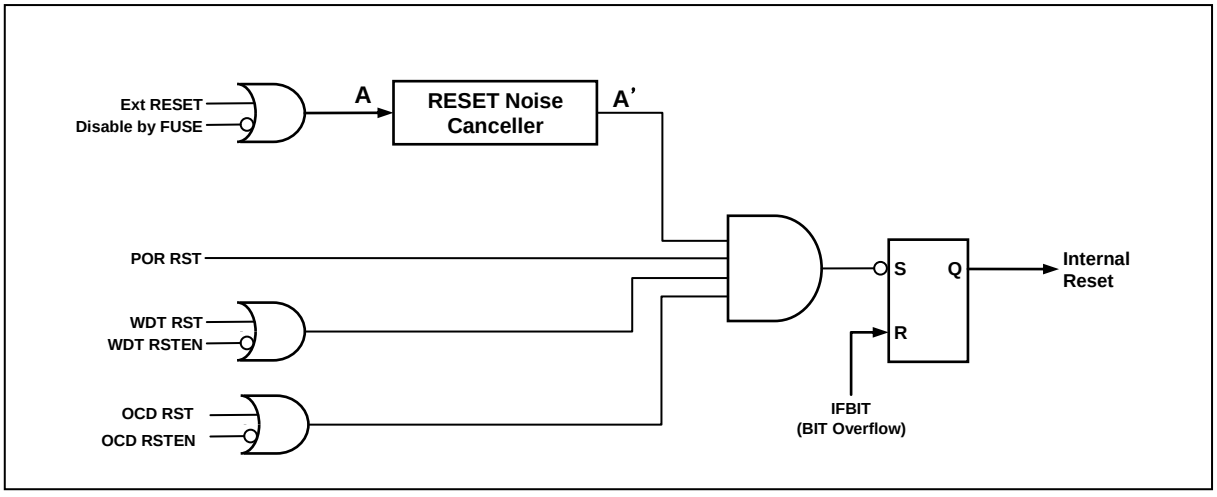


Figure 18.1 RESET Block Diagram

18.4 RESET Noise Canceller

The Figure 18.2 is the Noise Canceller diagram for noise cancel of RESET. It has the noise cancel value of about 7us (@V_{DD}=2.2~5.5V) to the low input of System Reset.

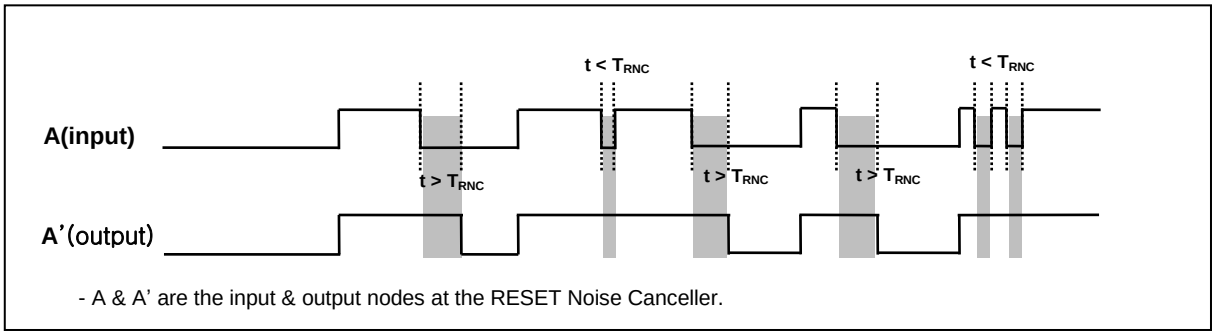


Figure 18.2 Reset noise canceller time diagram

18.5 Power On RESET

When rising device power, the POR (Power On Reset) have a function to reset the device. If using POR, it executes the device RESET function instead of the RESET IC or the RESET circuits. And External RESET PIN is able to use as a normal input pin.

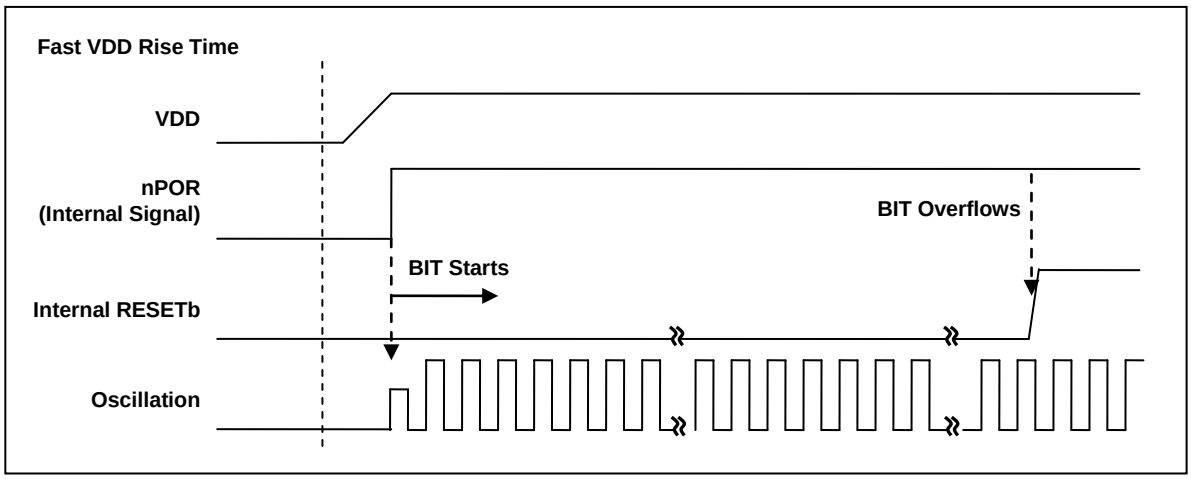


Figure 18.3 Fast VDD rising time

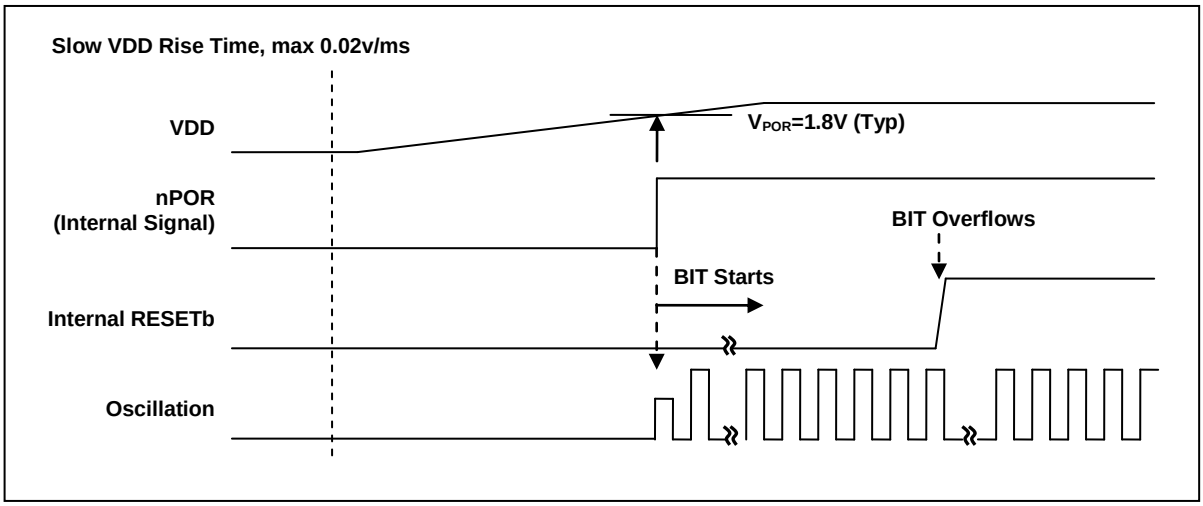


Figure 18.4 Internal RESET Release Timing On Power-Up

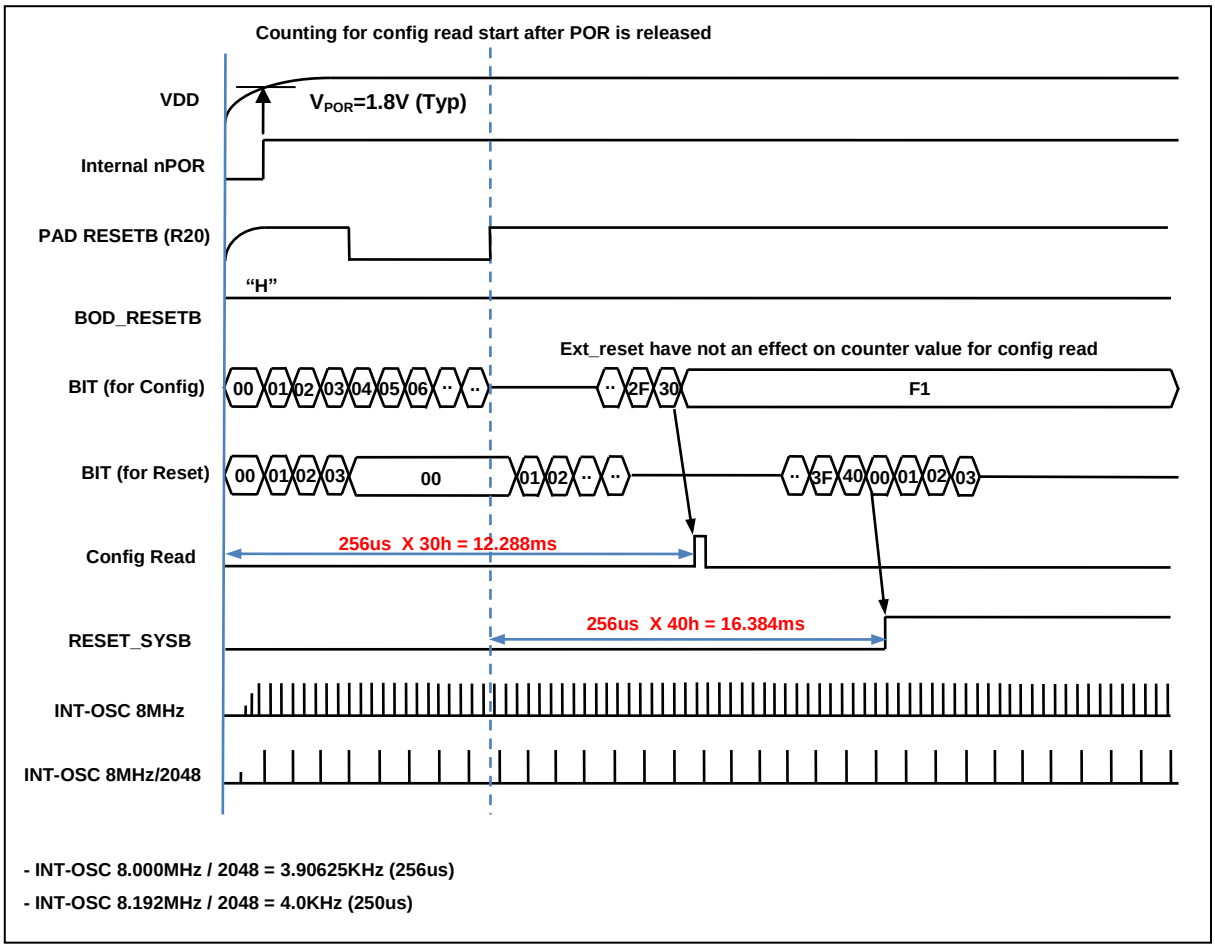


Figure 18.5 Configuration timing when Power-on

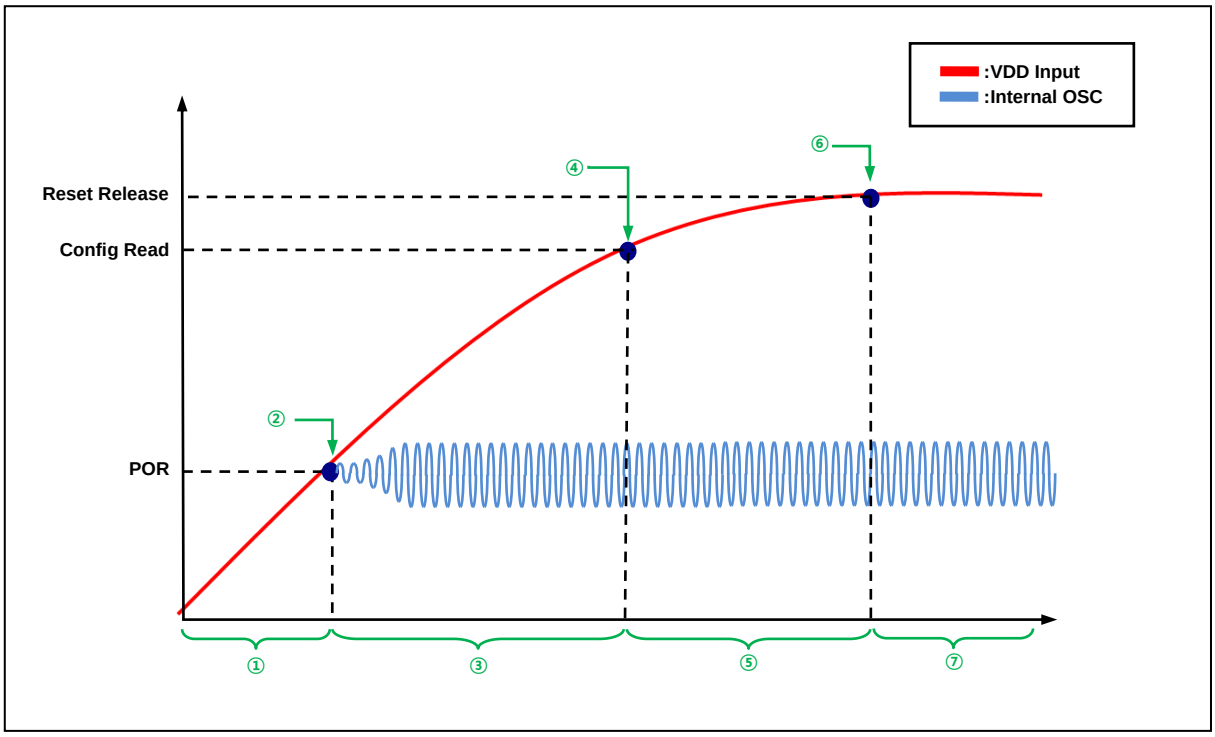


Figure 18.6 Boot Process Wave Form

Table 18-2 Boot Process Description

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection -Internal OSC 8MHz ON	-about 1.7V ~ 1.9V
③	- (INT-OSC 8MHz/2048)x30h Delay section (=12.288ms) -VDD input voltage must rise over than flash operating voltage for Config read	-Slew Rate >= 0.025V/ms
④	- Config read point	-about 1.8V ~ 2.0V -Config Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR or Ext_reset release
⑥	- Reset Release section (BIT overflow) i) after16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

18.6 External RESETB Input

The External RESETB is the input to a Schmitt trigger. A reset is accomplished by holding the reset pin low for at least 7us over, within the operating voltage range and oscillation stable, it is applied, and the internal state is initialized. After reset state becomes '1', it needs the stabilization time with 16ms and after the stable state, the internal RESET becomes '1'. The Reset process step needs 5 oscillator clocks. And the program execution starts at the vector address stored at address 0000H.

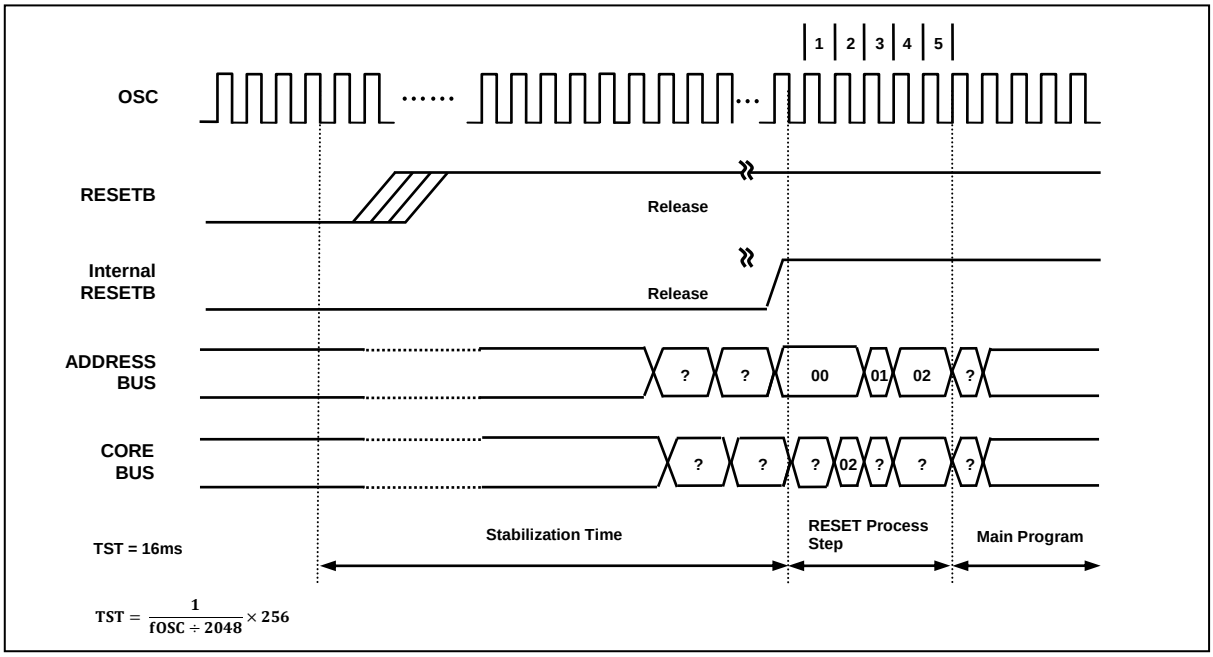


Figure 18.7 Timing Diagram after RESET

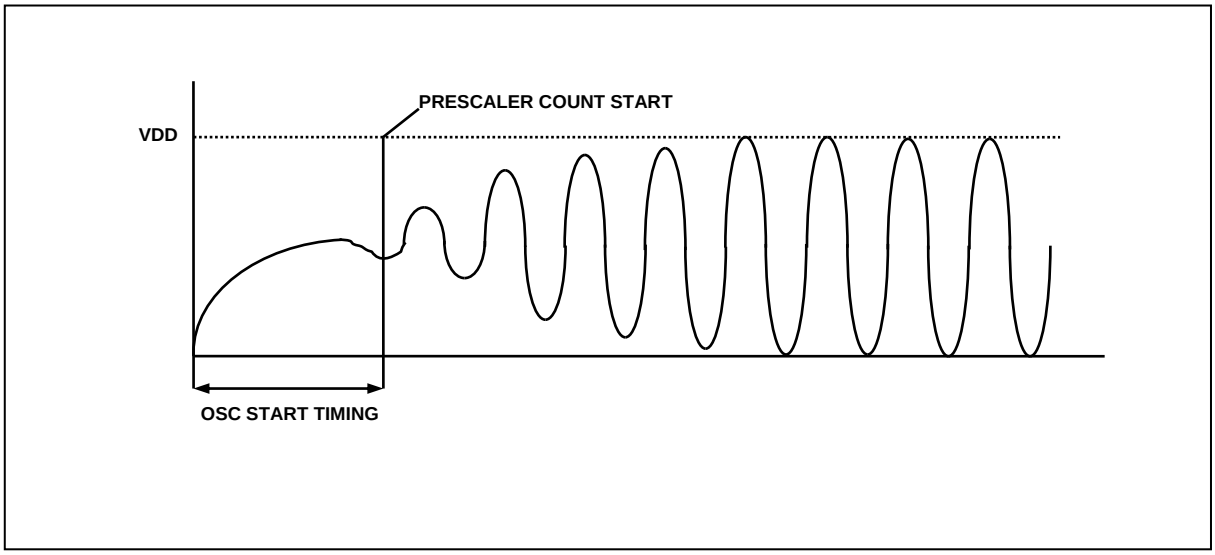


Figure 18.8 Oscillator generating waveform example

Note) as shown Figure 18.8, the stable generating time is not included in the start-up time.

19. On-chip Debug System

19.1 Overview

19.1.1 Description

On-chip debug System (OCD) of MC95FB204 can be used for programming the non-volatile memories and on-chip debugging. Detailed descriptions for programming via the OCD interface can be found in the following chapter.

Figure 19.1shows a block diagram of the OCD interface and the On-chip Debug system.

19.1.2 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Flash and Data EEPROM Memories
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the two-wire Interface
  - On-chip Debugging Supported by Dr.Choice®
- Operating frequency

  Supports the maximum frequency of the target MCU

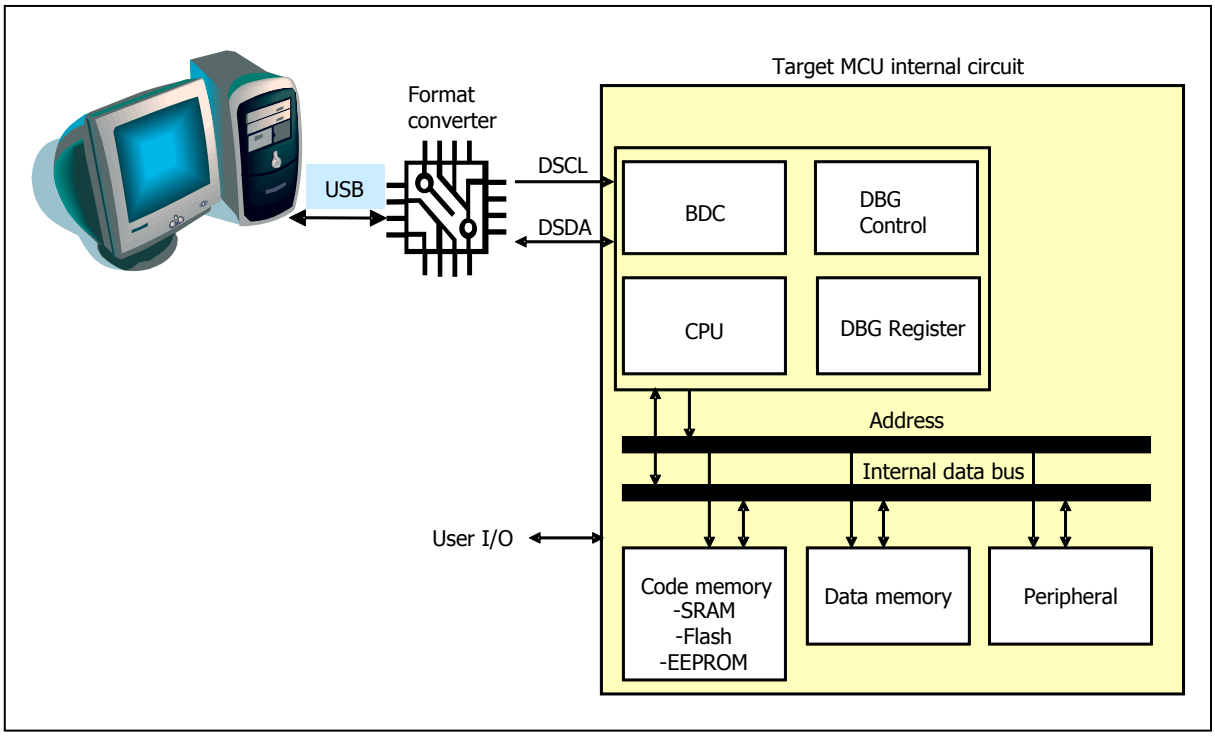


Figure 19.1 Block Diagram of On-chip Debug System

19.2 Two-pin external interface

19.2.1 Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Star condition and stop condition notify the start and the stop of background debugger command respectively.

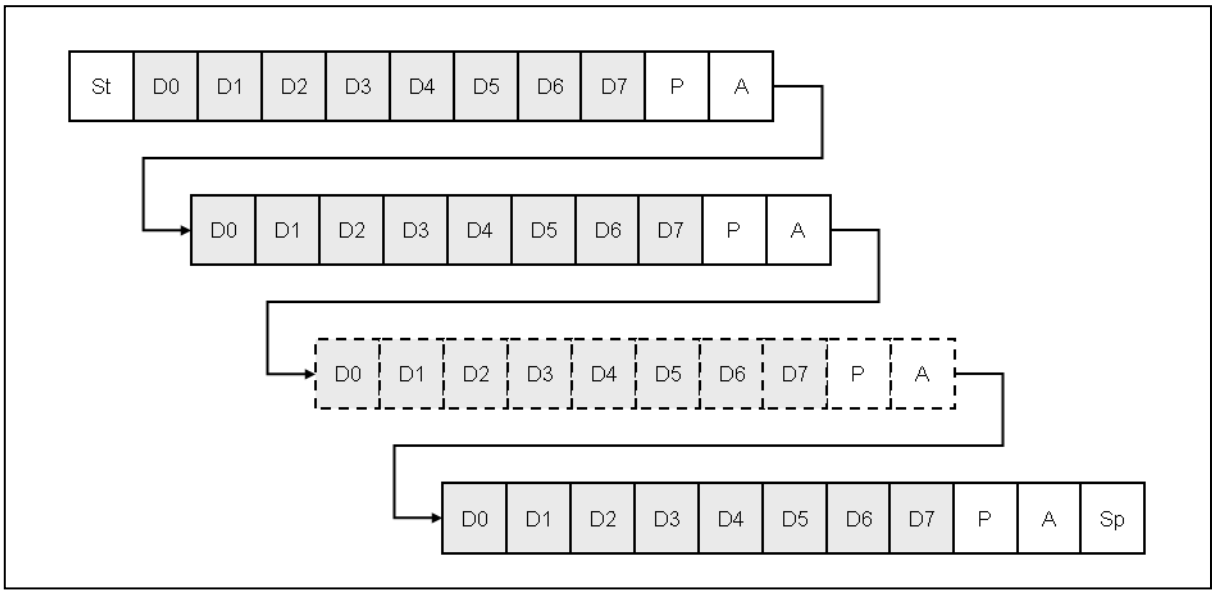


Figure 19.2 10-bit transmission packet

19.2.2 Packet transmission timing

19.2.2.1 Data transfer

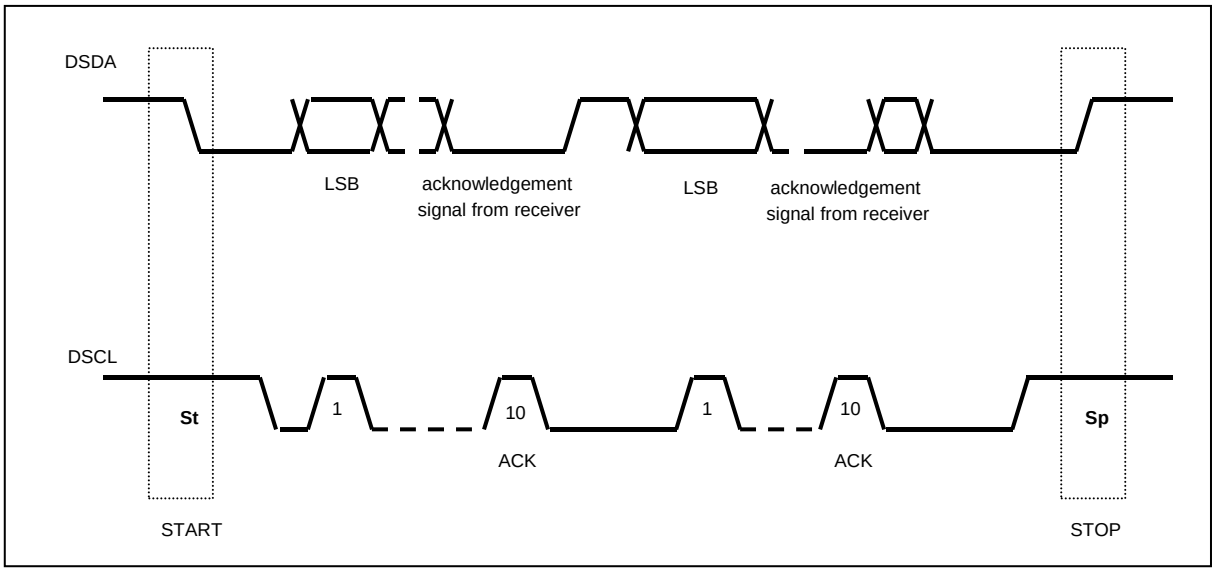


Figure 19.3 Data transfer on the twin bus

19.2.2.2 Bit transfer

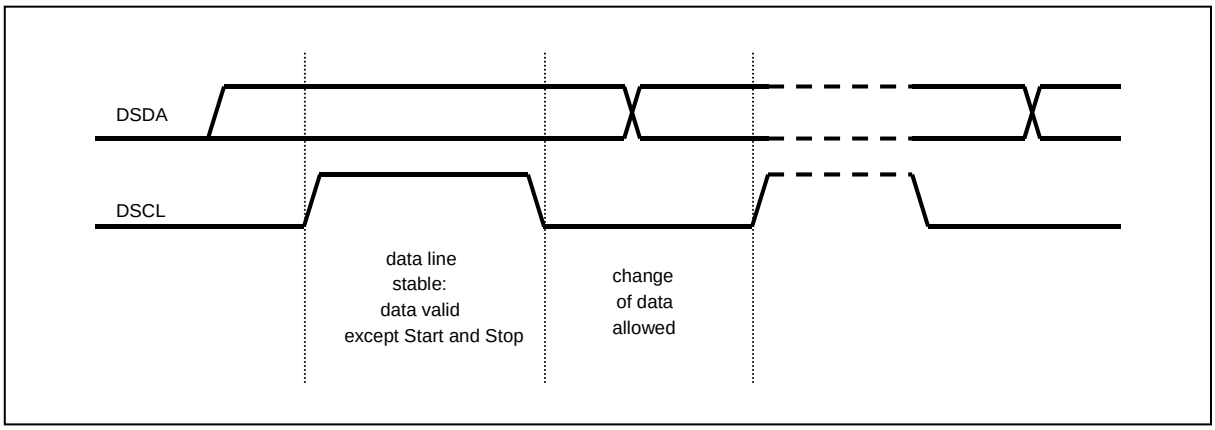


Figure 19.4 Bit transfer on the serial bus

19.2.2.3 Start and stop condition

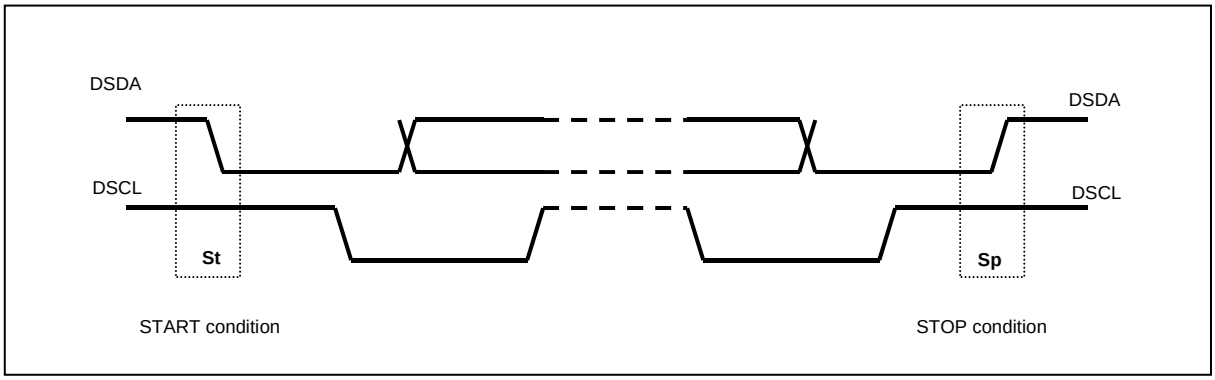


Figure 19.5 Start and stop condition

19.2.2.4 Acknowledge bit

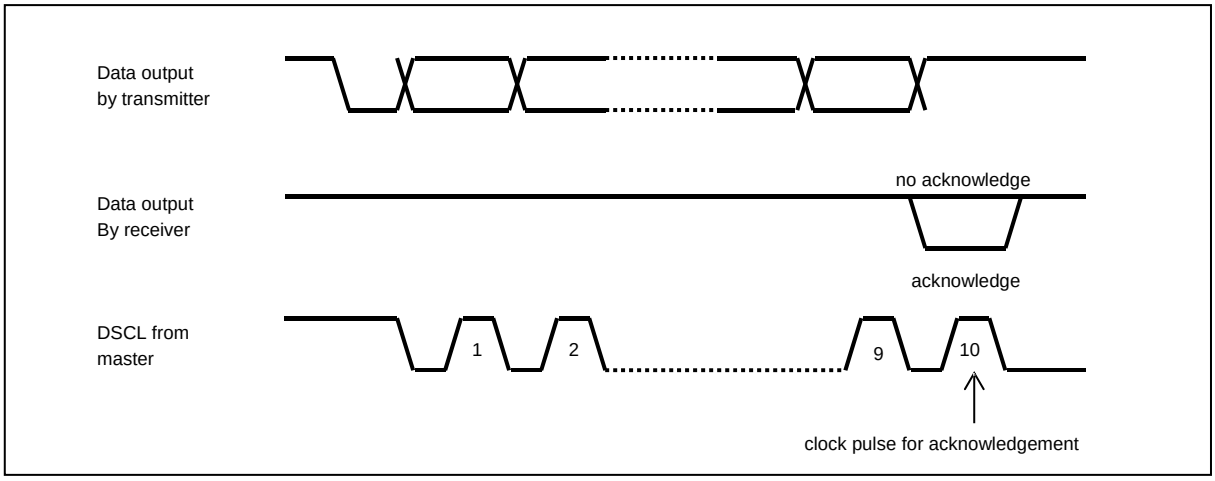


Figure 19.6 Acknowledge on the serial bus

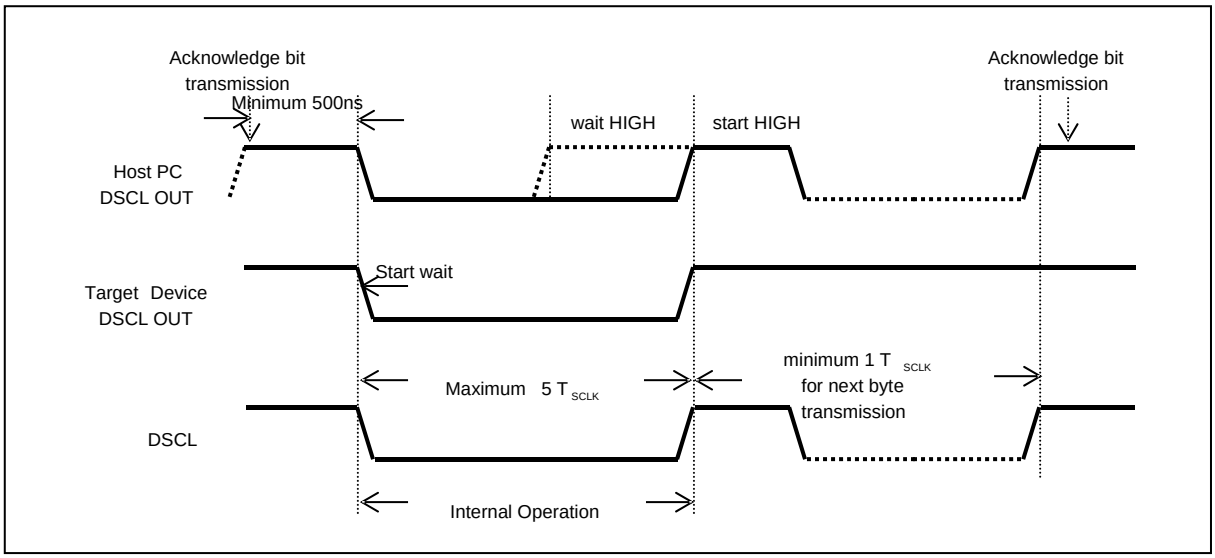


Figure 19.7 Clock synchronization during wait procedure

19.2.3 Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

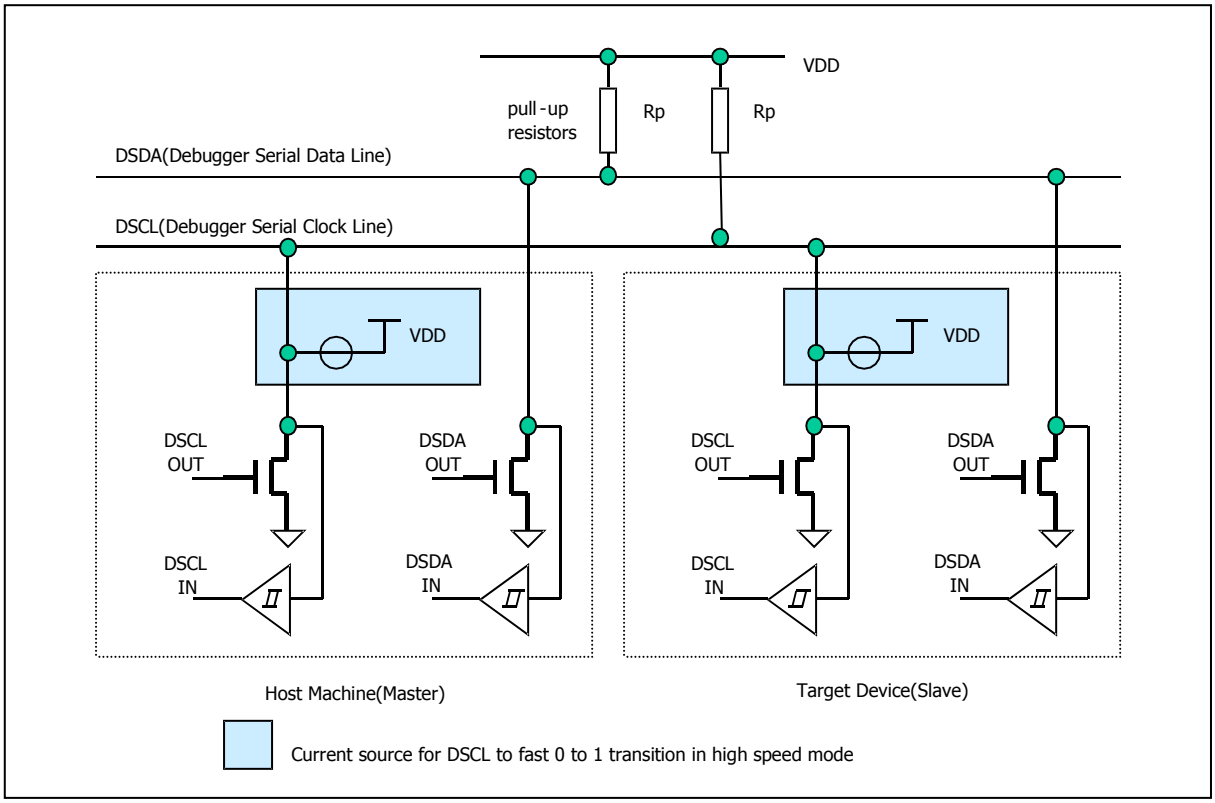


Figure 19.8 Connection of transmission

20. Memory Programming

20.1 Overview

20.1.1 Description

MC95FB204 incorporates flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP modes and byte-parallel ROM writer mode are supported.

Note that this “Memory Programming” feature is not used in user program. All flash control and status registers are used for MDS tools.

20.1.2 Features

- Flash Size : 4Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

20.2 Flash Control and status register

Registers to control Flash are Mode Register (FMR), Control Register (FCR), Status Register (FSR), Time Control Register (FTCR), Address Low Register (FARL), Address Middle Register (FARM), address High Register (FARH) and Data Register (FDR). They are mapped to SFR area and can be accessed only in programming mode.

20.2.1 Register Map

Table 20-1 Register Map

Name	Address	Dir	Default	Description
FMR	EAH	R/W	00H	Flash Mode Register
FCR	EBH	R/W	03H	Flash Control Register
FSR	ECH	R/W	80H	Flash Status Register
FTCR	EDH	R/W	00H	Flash Time Control Register
FARL	F2H	R/W	00H	Flash Address Low Register
FARM	F3H	R/W	00H	Flash Address Middle Register
FARH	F4H	R/W	00H	Flash Address High Register
FDR	F5H	R/W	00H	Flash Data Register

20.2.2 Register description for Flash and EEPROM

FMR (Flash Mode Register) : EAH

7	6	5	4	3	2	1	0
FSEL	ESEL	PGM	ERASE	PBUFF	OTPE	VFY	FEEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

FSEL Select flash memory.
- 0 Deselect flash memory
- 1 Select flash memory

PGM Enable program or program verify mode with VFY
- 0 Disable program or program verify mode
- 1 Enable program or program verify mode

ERASE Enable erase or erase verify mode with VFY
- 0 Disable erase or erase verify mode
- 1 Enable erase or erase verify mode

PBUFF Select page buffer
- 0 Deselect page buffer
- 1 Select page buffer

OTPE Select OTP area instead of program memory
- 0 Deselect OTP area
- 1 Select OTP area

VFY Set program or erase verify mode with PGM or ERASE

Program Verify: PGM=1, VFY=1

Erase Verify: ERASE=1, VFY=1

FEEN Enable program and erase of Flash and data EEPROM. When inactive, it is possible to read as normal mode
- 0 Disable program and erase
- 1 Enable program and erase

FCR (Flash Control Register) : EBH

7	6	5	4	3	2	1	0
AEF	AEE	EXIT1	EXIT0	WRITE	READ	nFERST	nPBRST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 03H

AEF Enable flash bulk erase mode
- 0 Disable bulk erase mode of Flash memory
- 1 Enable bulk erase mode of Flash memory

EXIT[1:0] Exit from program mode. It is cleared automatically after 1 clock

EXIT1	EXIT0	Description
0	0	Don't exit from program mode
0	1	Don't exit from program mode
1	0	Don't exit from program mode

1	1	Exit from program mode

WRITE Start to program or erase of Flash and data EEPROM. It is cleared automatically after 1 clock

0 No operation

1 Start to program or erase of Flash and data EEPROM

READ Start auto-verify of Flash or data EEPROM. It is cleared automatically after 1 clock

0 No operation

1 Start auto-verify of Flash or data EEPROM

nFERST Reset Flash or data EEPROM control logic. It is cleared automatically after 1 clock

0 No operation

1 Reset Flash or data EEPROM control logic.

nPBRST Reset page buffer with PBUFF. It is cleared automatically after 1 clock

PBUFF	nPBRST	Description
0	0	Page buffer reset
1	0	Write checksum reset

WRITE and READ bits can be used in program, erase and verify mode with FEAR registers. Read or writes for memory cell or page buffer uses read and write enable signals from memory controller. Indirect address mode with FEAR is only allowed to program, erase and verify

FSR (Flash Status Register) : ECH

7	6	5	4	3	2	1	0
PEVBSY	VFYGOOD	-	-	ROMINT	WMODE	EMODE	VMODE
R	R/W	R	R	R/W	R	R	R

Initial value : 80H

PEVBSY Operation status flag. It is cleared automatically when operation starts. Operations are program, erase or verification

0 Busy (Operation processing)

1 Complete Operation

VFYGOOD Auto-verification result flag.

0 Auto-verification fails

1 Auto-verification successes

ROMINT Flash ROM interrupt request flag. Auto-cleared when program/erase/verify starts. Active in program/erase/verify completion

0 No interrupt request.

1 Interrupt request.

WMODE Write mode flag

EMODE Erase mode flag

VMODE Verify mode flag

FARL (Flash address low Register) : F2H

7	6	5	4	3	2	1	0
ARL7	ARL6	ARL5	ARL4	ARL3	ARL2	ARL1	ARL0
W	W	W	W	W	W	W	W

Initial value : 00H

ARL[7:0] Flash address low

FARM (Flash address middle Register) : F3H

7	6	5	4	3	2	1	0
ARM7	ARM6	ARM5	ARM4	ARM3	ARM2	ARM1	ARM0
W	W	W	W	W	W	W	W

Initial value : 00H

ARM[7:0] Flash address middle

FARH (Flash address high Register) : F4H

7	6	5	4	3	2	1	0
ARH7	ARH6	ARH5	ARH4	ARH3	ARH2	ARH1	ARH0
W	W	W	W	W	W	W	W

Initial value : 00H

ARH[7:0] Flash address high

FAR registers are used for program, erase and auto-verify. In program and erase mode, it is page address and ignored the same least significant bits as the number of bits of page address. In auto-verify mode, address increases automatically by one.

FARs are write-only register. Reading these registers returns 24-bit checksum result

FDR (Flash data control Register) : F5H

7	6	5	4	3	2	1	0
FDR7	FDR6	FDR5	FDR4	FDR3	FDR2	FDR1	FDR0
W	W	W	W	W	W	W	W

Initial value : 00H

FDR[7:0] Flash data

Data register. In no program/erase/verify mode, READ/WRITE of FECR read or write data from EEPROM or FLASH to this register or from this register to Flash or EEPROM.

The sequence of writing data to this register is used for EEPROM program entry. The mode entrance sequence is to write 0xA5 and 0x5A to it in order.

FTCR (Flash Time control Register) : EDH

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

TCR[7:0] Flash Time control

Program and erase time is controlled by setting FTCR register. Program and erase timer uses 10-bit counter. It increases by one at each clock of 8MHz/32(=8us) frequency. It is cleared when program or erase starts. Timer stops when 10-bit counter is same to FTCR. PEVBSY is cleared when program, erase or verify starts and set when program, erase or verify stops.

Maximum program/erase time: 8us * 1024 = 8.192 ms

In the case of 10% of error rate of counter source clock, program or erase time is 7.3~9 ms

* Program/erase time calculation

for page write or erase, Tpe = (TCON+1) * 2 * 8us

for bulk erase, Tbe = (TCON+1) * 4 * 8us

※ Recommended program/erase time (FTCR = A0h)

	Min	Typ	Max	Unit
program/erase Time	2.4	2.5	2.6	ms

20.3 Memory map

20.3.1 Flash Memory Map

Program memory uses 4-Kbyte of Flash memory. It is read by byte and written by byte or page. One page is 32-byte

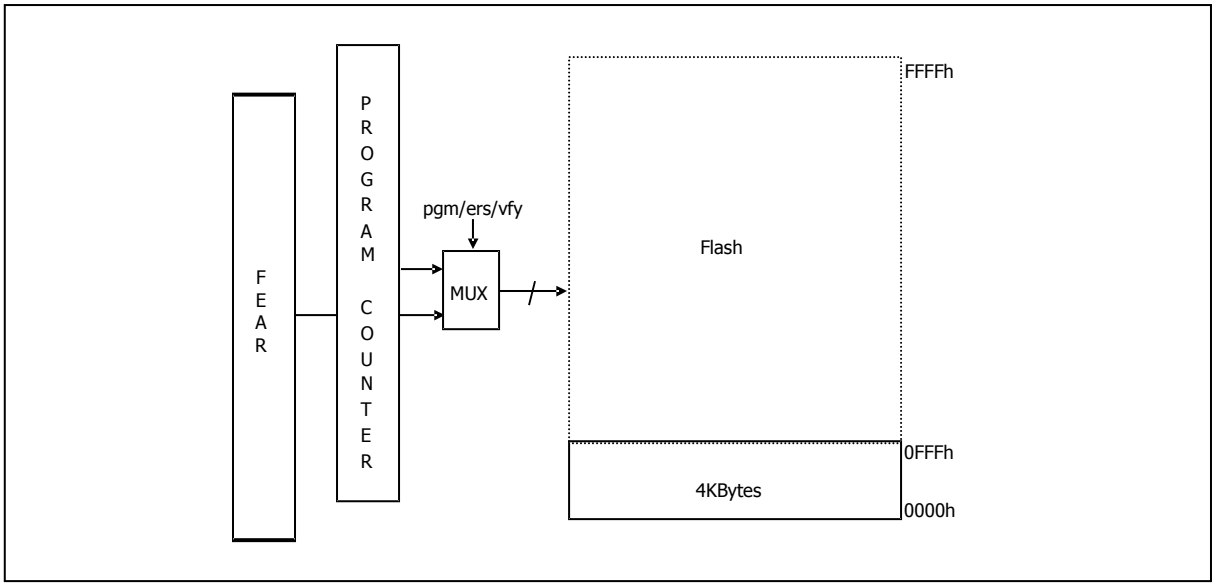


Figure 20.1 Flash Memory Map

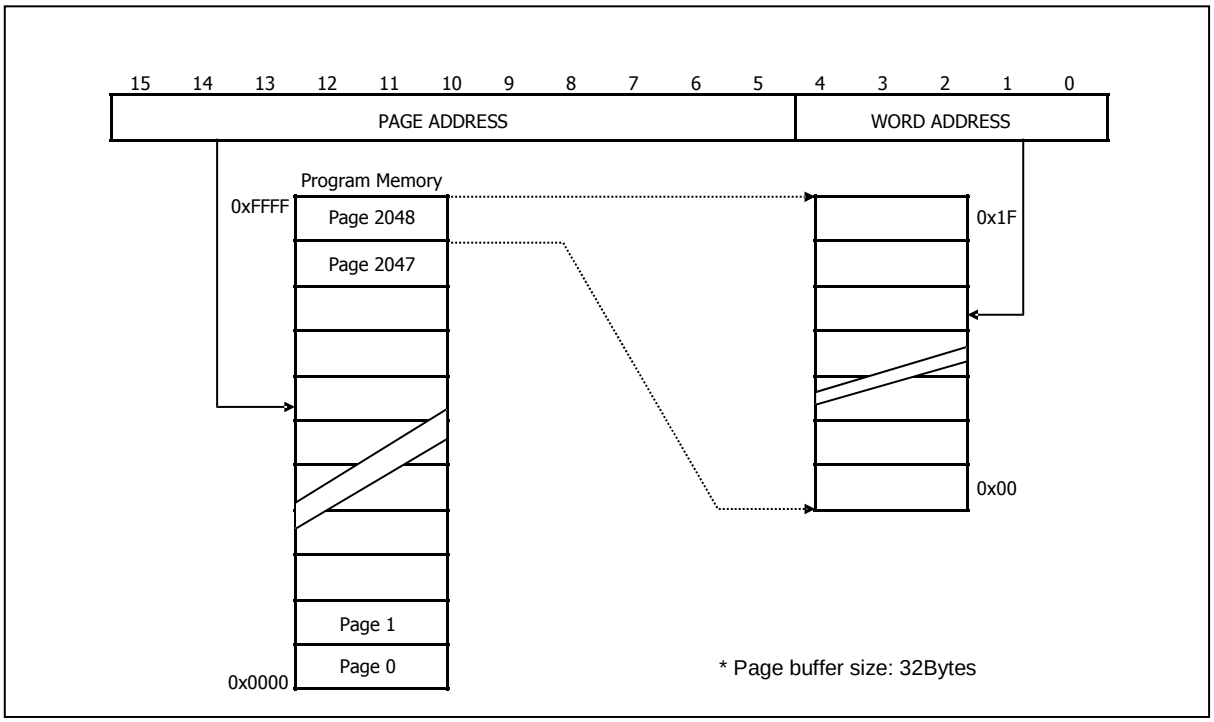


Figure 20.2 Address configuration of Flash memory

20.4 Serial In-System Program Mode

Serial in-system program uses the interface of debugger which uses two wires. Refer to chapter 14 in details about debugger

20.4.1 Flash operation

Configuration(This Configuration is just used for follow description)

7	6	5	4	3	2	1	0
-	FMR[4] & [1]	FMR[5] & [1]	-	-	FMR[2]	FCR[6]	FCR[7]
-	ERASE&VFY	PGM&VFY	-	-	OTPE	AEE	AEF

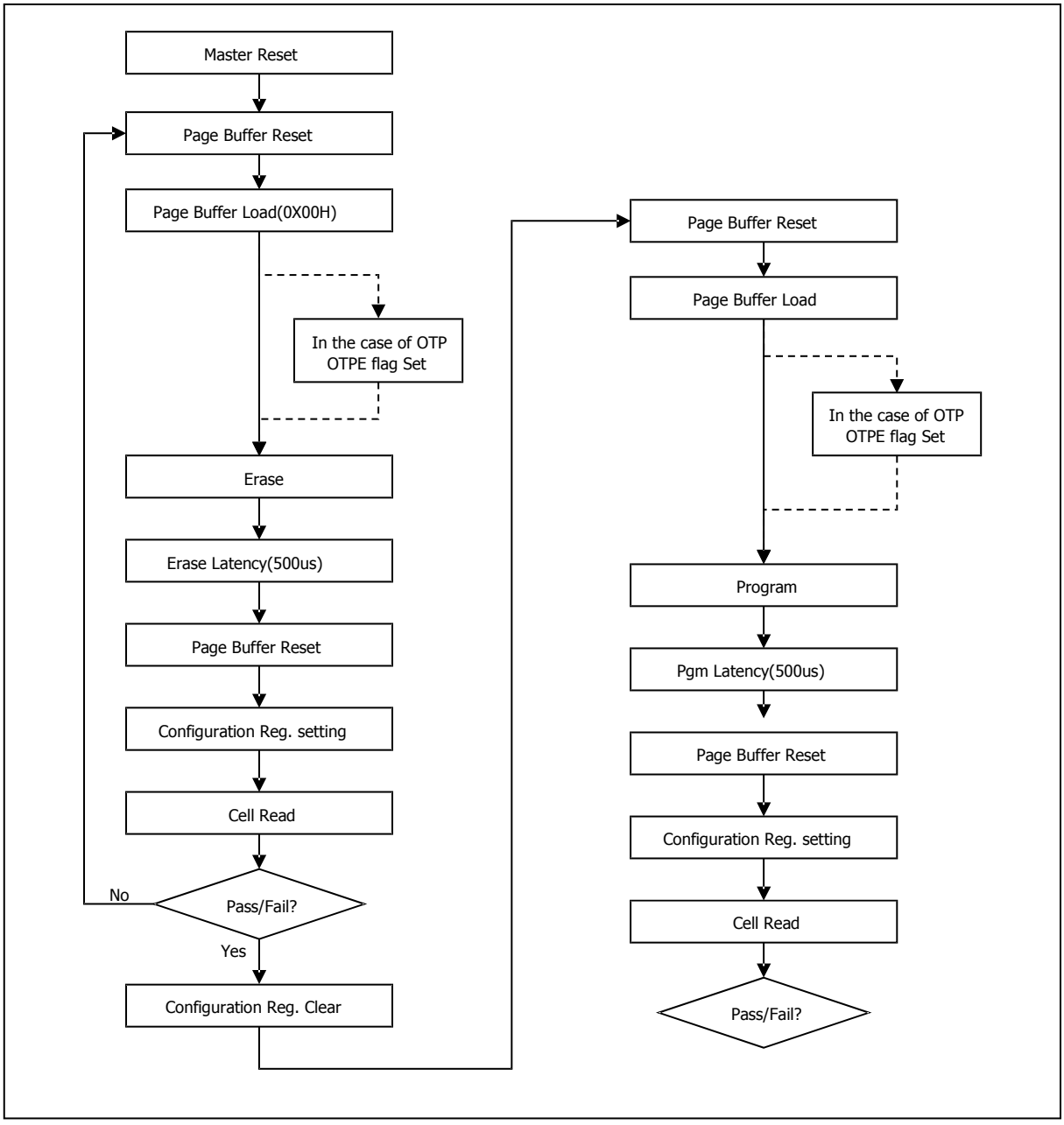


Figure 20.3 The sequence of page program and erase of Flash memory

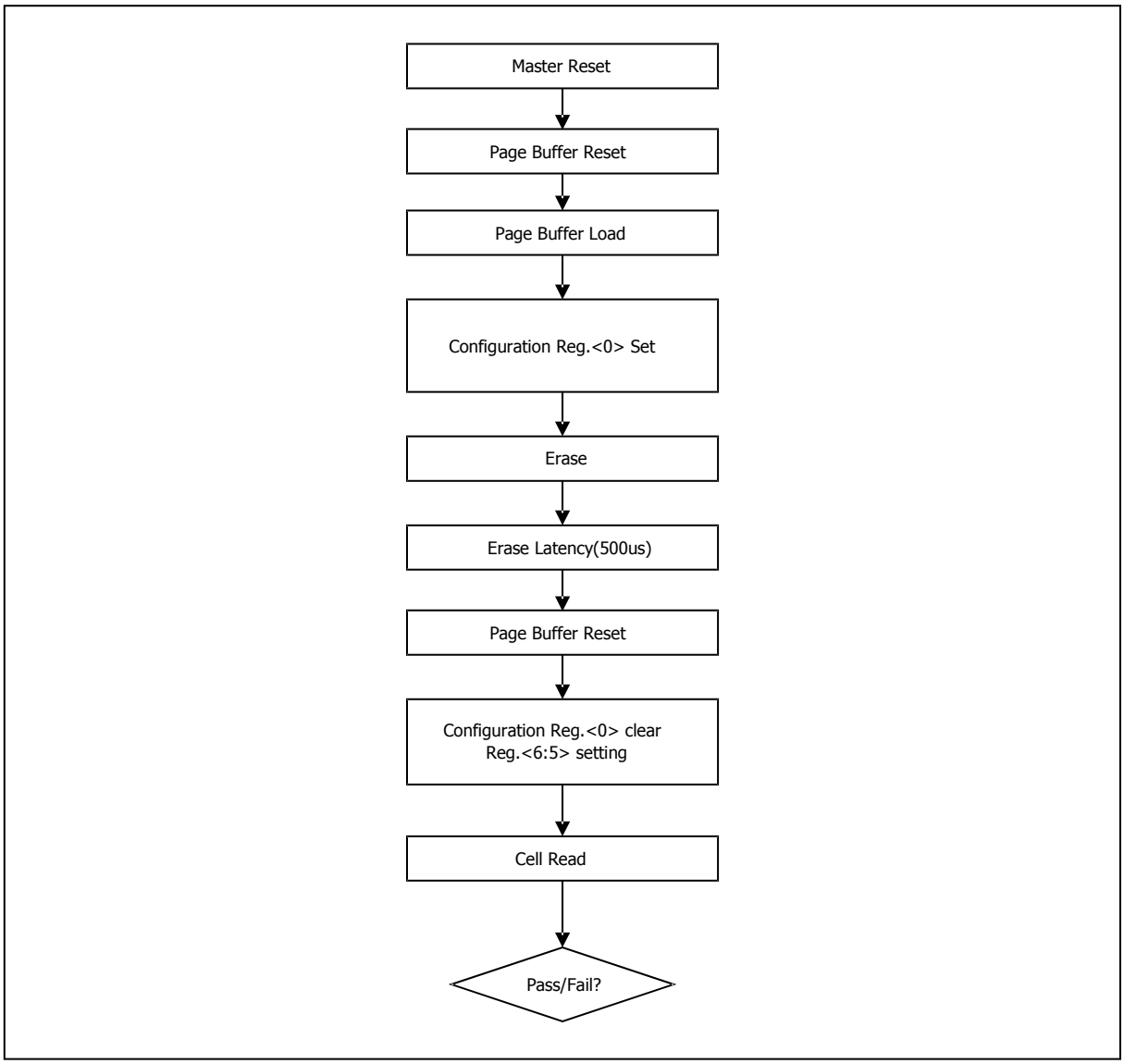


Figure 20.4 The sequence of bulk erase of Flash memory

20.4.1.1 Flash Read

Step 1. Enter OCD(=ISP) mode.
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Read data from Flash.

20.4.1.2 Enable program mode

Step 1. Enter OCD(=ISP) mode.[1]
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Enter program/erase mode sequence.[2]

(1) Write 0xAA to 0xF555.

(2) Write 0x55 to 0xFAAA.

(3) Write 0xA5 to 0xF555.

[1] Refer to how to enter ISP mode..

[2] Command sequence to activate Flash write/erase mode. It is composed of sequentially writing data of Flash memory.

20.4.1.3 Flash write mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FMR: 1000_0001 FCR:0000_0010

Step 3. Select page buffer. FMR:1000_1001

Step 4. Write data to page buffer.(Address automatically increases by twin.)

Step 5. Set write mode. FMR:1010_0001

Step 6. Set page address. FARH:FARM:FARL=20'hx_xxxx

Step 7. Set FTCR.

Step 8. Start program. FCR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FSR until PVBSY is 1.

Step 11. Repeat step2 to step 8 until all pages are written.

20.4.1.4 Flash page erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FMR: 1000_0001 FCR:0000_0010

Step 3. Select page buffer. FMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode. FMR:1001_0001

Step 6. Set page address. FARH:FARM:FARL=20'hx_xxxx

Step 7. Set FTCR.

Step 8. Start erase. FCR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FSR until PVBSY is 1.

Step 11. Repeat step2 to step 8 until all pages are erased.

20.4.1.5 Flash bulk erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FMR: 1000_0001 FCR:0000_0010

Step 3. Select page buffer. FMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode. FMR:1001_0001.

(Only main cell area is erased. For bulk erase including OTP area, select OTP area.(set FMR to 1000_1101.)

Step 6. Set FTCR

Step 7. Start bulk erase. FCR:1000_1011

Step 8. Insert one NOP operation

Step 9. Read FSR until PVBSY is 1.

20.4.1.6 Flash OTP area read mode

Step 1. Enter OCD(=ISP) mode.

Step 2. Set ENBDM bit of BCR.

Step 3. Enable debug and Request debug mode.

Step 4. Select OTP area. FMR:1000_0101

Step 5. Read data from Flash.

20.4.1.7 Flash OTP area write mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FMR: 1000_0001 FCR:0000_0010

Step 3. Select page buffer. FMR:1000_1001

Step 4. Write data to page buffer.(Address automatically increases by twin.)

Step 5. Set write mode and select OTP area. FMR:1010_0101

Step 6. Set page address. FARH:FEARM:FARL=20'hx_xxxx

Step 7. Set FTCR.

Step 8. Start program. FCR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FSR until PVBSY is 1.

20.4.1.8 Flash OTP area erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FMR: 1000_0001 FCR:0000_0010

Step 3. Select page buffer. FMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode and select OTP area. FMR:1001_0101

Step 6. Set page address. FARH:FARM:FARL=20'hx_xxxx

Step 7. Set FTCR.

Step 8. Start erase. FCR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FSR until PVBSY is 1.

20.4.1.9 Flash program verify mode

Step 1. Enable program mode.
Step 2. Set program verify mode. FMR:1010_0011
Step 3. Read data from Flash.

20.4.1.10 OTP program verify mode

Step 1. Enable program mode.
Step 2. Set program verify mode. FMR:1010_0111
Step 3. Read data from Flash.

20.4.1.11 Flash erase verify mode

Step 1. Enable program mode.
Step 2. Set erase verify mode. FMR:1001_0011
Step 3. Read data from Flash.

20.4.1.12 Flash page buffer read

Step 1. Enable program mode.
Step 2. Select page buffer. FMR:1000_1001
Step 3. Read data from Flash.

20.4.1.13 Enable program mode

Step 1. Enter OCD(=ISP) mode.[1]
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Enter program/erase mode sequence.[2]
    (1) Write 0xA5 to FDR.
    (2) Write 0x5A to FDR.

[1] Refer to how to enter ISP mode..
[2] Command sequence to activate data EEPROM write/erase mode. It is composed of sequentially writing to data register(FDR)

20.4.2 Summary of Flash Program/Erase Mode

Table 20-2 Operation Mode

Operation mode		Description
FLASH	Flash read	Read cell by byte.
	Flash write	Write cell by bytes or page.
	Flash page erase	Erase cell by page.
	Flash bulk erase	Erase the whole cells.
	Flash program verify	Read cell in verify mode after programming.
	Flash erase verify	Read cell in verify mode after erase.
	Flash page buffer load	Load data to page buffer.

20.5 Mode entrance method of ISP

20.5.1 Mode entrance method for ISP

TARGET MODE	P07	P06	P07
OCD(ISP)	‘hC	‘hC	‘hC

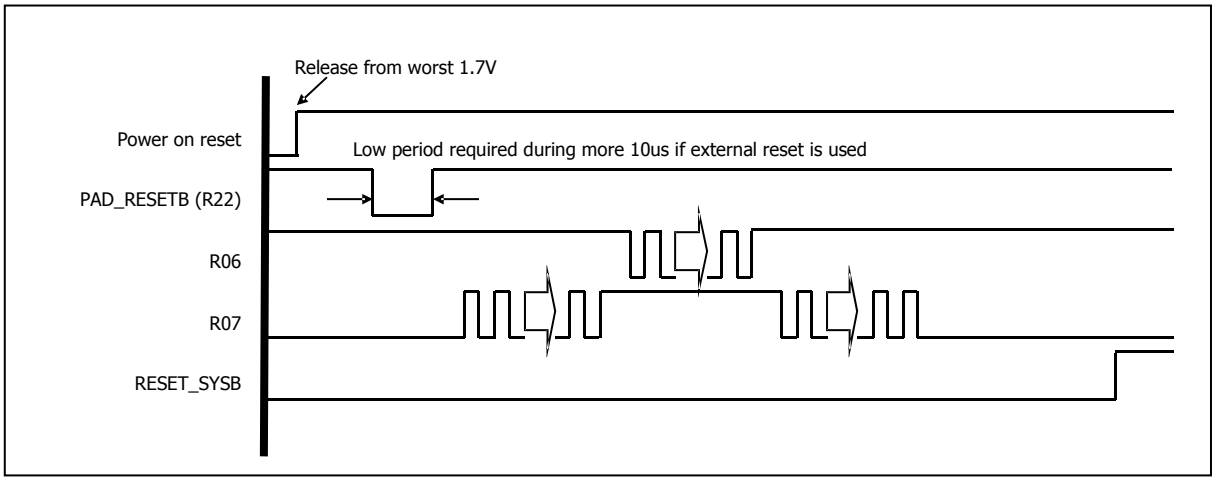


Figure 20.5 ISP mode

20.6 Security

MC95FB204 provides one Lock bit which can be left unprogrammed (“0”) or can be programmed (“1”) to obtain the additional features listed in Table 20-3. The Lock bit can only be erased to “0” with the bulk erase command

Table 20-3 Security policy using lock-bits

LOCK MODE	USER MODE								ISP/OCD MODE							
	FLASH				OTP				FLASH				OTP			
LOCKF	R	W	PE	BE	R	W	PE	BE	R	W	PE	BE	R	W	PE	BE
0	X	X	X	X	X	X	X	X	O	O	O	O	O	O	O	O
1	X	X	X	X	X	X	X	X	X	X	X	O	O	X	X	O

- LOCKF: Lock bit of Flash memory
- R: Read
- W: Write
- PE: Page erase
- BE: Bulk Erase
- O: Operation is possible.
- X: Operation is impossible.

21. Configure option

21.1 Configure option Control Register

FUSE_CONF (Pseudo-Configure Data) : FDH

7	6	5	4	3	2	1	0
-	-	-	XINENA	RSTDIS	-	-	LOCKF
R	R	R	R	R	R	R	R

Initial value : 00H

XINENA External Main Oscillator Enable Bit
- 0 Main OSC disable (default,P20,P21)
- 1 Main OSC Enable(XIN,XOUT)

RSTDIS External RESETB disable Bit
- 0 External RESET enable(RESET)
- 1 External RESET disable(P22)

LOCKF CODE memory LOCK bit
- 0 LOCK Disable
- 1 LOCK Enable

22. APPENDIX

22.1 Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.
Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table.
1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43

XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	F8-FF
MOV Rn,A	Move A to register	1	1	A8-AF
MOV Rn,dir	Move direct byte to register	2	2	78-7F
MOV Rn,#data	Move immediate to register	2	1	F5
MOV dir,A	Move A to direct byte	2	1	88-8F
MOV dir,Rn	Move register to direct byte	2	2	85
MOV dir,dir	Move direct byte to direct byte	3	2	86-87
MOV dir,@Ri	Move indirect memory to direct byte	2	2	75
MOV dir,#data	Move immediate to direct byte	3	2	F6-F7
MOV @Ri,A	Move A to indirect memory	1	1	A6-A7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	76-77
MOV @Ri,#data	Move immediate to indirect memory	2	1	90
MOV DPTR,#data	Move immediate to data pointer	3	2	93
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	83
MOVC A,@A+PC	Move code byte relative PC to A	1	2	E2-E3
MOVX A,@Ri	Move external data(A8) to A	1	2	F2-F3
MOVX A,@DPTR	Move external data(A16) to A	1	2	F0
MOVX @Ri,A	Move A to external data(A8)	1	2	C0
MOVX @DPTR,A	Move A to external data(A16)	1	2	23
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2

SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	3	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the

destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

22.2 Instructions on how to use the input port.

22.2.1 Error occur status

- Using compare jump instructions with input port, it could cause error due to the timing conflict inside the MCU.
- Compare jump Instructions which cause potential errorused with input port condition:

```
JB      bit, rel        ; jump on direct bit=1
JNB     bit, rel        ; jump on direct bit=0
JBC     bit, rel        ; jump on direct bit=1 and clear
CJNE    A, dir, rel     ; compare A, direct jne relative
DJNZ    dir, rel        ; decrement direct byte, jnz relative
```

- It is only related with Input port. Internal parameters, SFRs and output bit ports don't cause an y error by using compare jump instructions.
- If input signal is fixed, there is no error in using compare jump instructions.

22.2.2 Error status example

```
while(1){
if (P00==1){P10=1; }
else{ P10=0; }
  P11^=1;
}
```

```
zzz:   JNB     080.0, xxx  ; it possible to be error
       SETB    088.0
       SJMP    yyy
xxx:   CLR     088.0
yyy:   MOV     C,088.1
       CPL     C
       MOV     088.1,C
       SJMP    zzz
```

```
unsignedchar ret_bit_err(void)
{
return !P00;
}
```

```
       MOV     R7, #000
JB     080.0, xxx  ; it possible to be error
       MOV     R7, #001
xxx:   RET
```

22.2.3 Preventative measures (2 cases)

- Do not use input bit port for bit operation but for byte operation.Using byte operation instead of bit operation will not cause any errorin using compare jump instructions for input port.

```
while(1){
if ((P0&0x01)==0x01){ P10=1; }
  else{ P10=0; }
   P11^=1;
}
```

```
zzz:   MOV     A, 080       ; read as byte
JNB      0E0.0, xxx     ; compare
      SETB      088.0
SJMP     yyy
xxx:   CLR       088.0
yyy:   MOV      C,088.1
       CPL      C
       MOV      088.1,C
       SJMP     zzz
```

- If you use input bit port for compare jump instruction, you have to copy the input port as intern al parameter or carry bit and then use compare jump instruction.

```
bittt;
while(1){
tt=P00;
if (tt==0){P10=1;}
else {     P10=0;}
   P11^=1;
}
```

```
zzz:   MOV      C,080.0  ; input port use internal parameter
  MOV      020.0, C       ; move
JB       020.0, xxx    ; compare
      SETB     088.0
      SJMP     yyy
xxx:   CLR       088.0
yyy:   MOV      C,088.1
  CPL      C
      MOV      088.1,C
      SJMP     zzz
```