CMOS single-chip 8-bit MCU with 12-bit A/D converter

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 16Kbytes Flash Code Memory
  - 768bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator (±1.5%, T_A= 0 ~ +50°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (15 inputs)
  - UART 8-bit x 1-ch
  - SPI 8-bit x 1-ch
  - I2C 8-bit x 1-ch
- **I/O and Packages**
  - Up to 30 Programmable I/O lines with 32-pin package
  - 32/28/20 SOP, 32 LQFP, 24 QFN
  - Pb-free package
- **Operating Conditions**
  - 2.2V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Small Home Appliance

MC96F8316A
MC96F8216A

Data Sheet

V 1.4

Revised 1 August, 2019

Revision history

Version	Date	Revision list
1.0	2016.05.29	Published this book.
1.1	2016.07.06	Remove packages the 32 QFN, 28 TSSOP, 24 SOP and 24 QFN.
1.2	2017.09.22	Add package the 24 QFN
1.3	2018.07.26	Added Figure 1.1 Device Nomenclature.
1.4	2019.08.01	Revised this book. Add package the 24 QFN(Thin). Removed the other bits except PCON[1:0] in Chapter 12.8 Register Description for Power Down Operation. Updated OCD dongle image and writing tool images in Chapter 1.3 Development tools. Fixed typos of I2C Status Register in Chapter 11.12 I2C.

Version 1.4

Published by FAE team

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1 Overview

1.1 Description

The MC96F8316A is an advanced CMOS 8-bit microcontroller with 16 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This offers the following features: 16 Kbytes of FLASH, 256 bytes of IRAM, 512 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F8316A also supports power down modes to reduce power consumption.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96F8316AD	16 Kbytes	512 bytes	256 bytes	15 inputs	30	32 SOP
MC96F8316AL				15 inputs	30	32 LQFP
MC96F8316AM				12 inputs	26	28 SOP
MC96F8216AU				11 inputs	22	24 QFN
MC96F8216AD				8 inputs	18	20 SOP

Table 1.1 Ordering Information of MC96F8316A

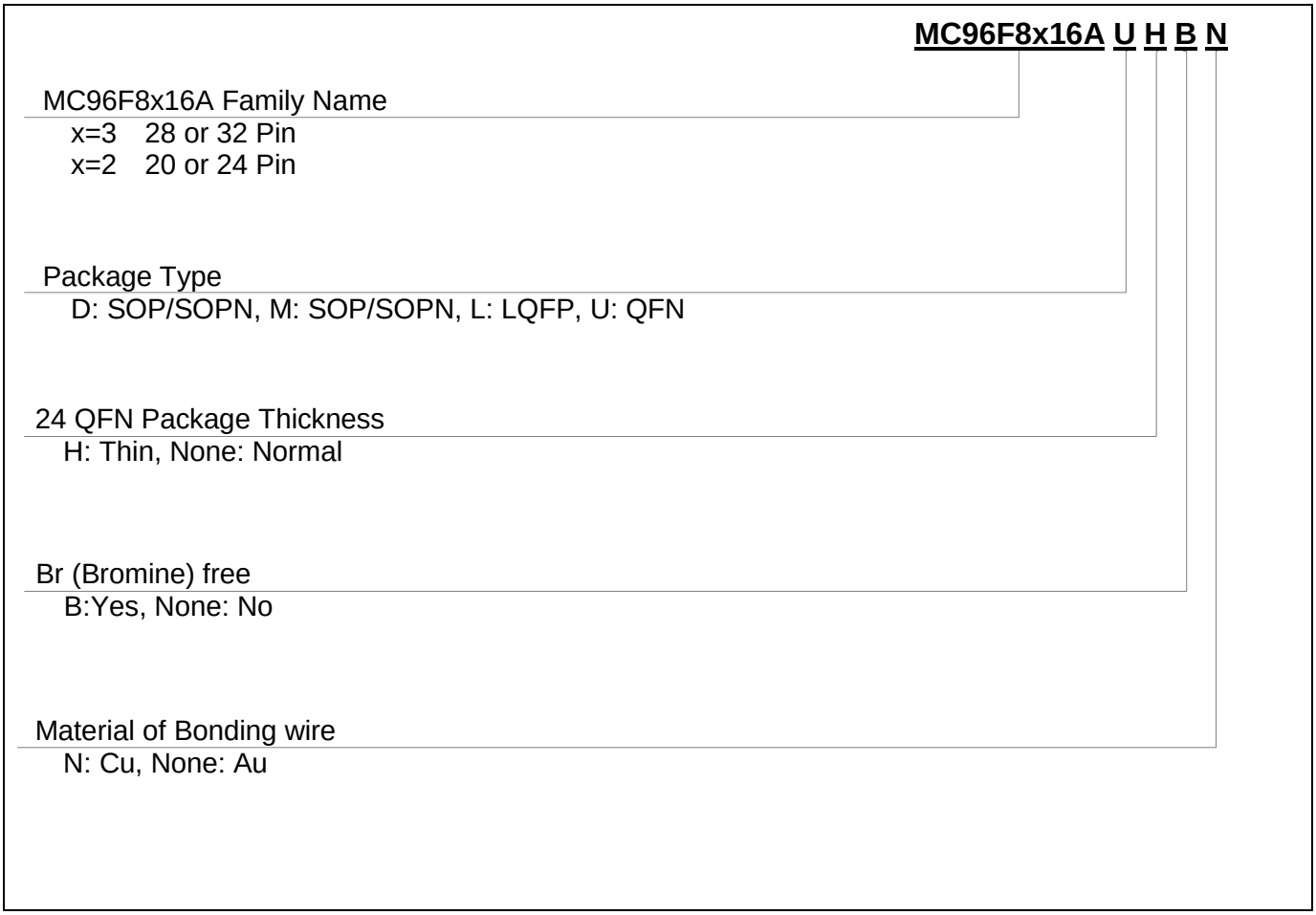


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 16 Kbytes Flash with self read/write capability
  - In-System Programming(ISP)
  - Endurance : 10,000 times (Sector 0~503)
    100,000 times (Sector 504~511)
  - Retention : 10 years
- **256bytes IRAM**
- **512bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 30 Ports
    (P0[6:0], P1[7:0], P2[6:0], P3[7:0])
  - LED display drive capability pins : 30 Ports
    (P0[6:0], P1[7:0], P2[6:0], P3[7:0])
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit× 1-ch
  - Watch Dog Timer (WDT) 8-bit× 1-ch
  - 5kHz internal RC oscillator
  - 8-bit× 1-ch(T0), 16-bit× 2-ch (T1/T2)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
  - 8-Bit PWM (by T0)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s /1 min interval at 32.768kHz
- **Buzzer**
  - 8-bit× 1-ch
- **SPI**
  - 8-bit× 1-ch
- **UART**
  - 8-bit× 1-ch
- **I2C**
  - 8-bit× 1-ch
- **12-bit A/D Converter**
  - 15 Input channels
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 12 level detect (1.85/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Low Voltage Indicator**
  - 11 level detect (2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0~4, EINT5, EINT6, EINT7~A, EINT10, EINT11, EINT12) (7)
  - Timer(0/1/2) (4)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SPI (1)
  - UART (2)
  - I2C (1)
  - ADC (1)
  - ADC Wake-up (1)
- **Internal RC Oscillator**
  - Internal RC frequency:
    16MHz ±1.5% (T_A= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V~ 5.5V (@32~ 38kHz with X-tal)
  - 2.2V~ 5.5V (@0.4~ 4.2MHz with X-tal)
  - 2.7V~ 5.5V (@0.4~ 10.0MHzwith X-tal)
  - 3.0V~ 5.5V (@0.4~ 12.0MHz with X-tal)
  - 2.2V~ 5.5V (@0.5~ 16.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 32 SOP
  - 32 LQFP
  - 28 SOP
  - 24 QFN
  - 20 SOP
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compier provider.
The MC96F8316A core is Mentor 8051 and the ROM size is smaller than 64 Kbytes.Therefore, developer can use the standard 8051 compiler from other providers.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.
The OCD debugger program works on all Microsoft-Windows operating system.If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

- DSCL (MC96F8316 P01 port)
- DSDA (MC96F8316 P00 port)

NOTE)

1. MC96F8316A does not support the OCD function. MC96F8316 should be used for debugging.
2. Do not access to P0, P1, P2, P3, EIFLAG0 and EIFLAG1 registers through the "direct bit test and branch instructions" in the MC96F8316. Refer to the "MC96F8316 User's Manual".

OCD connector diagram: Connect OCD with user system

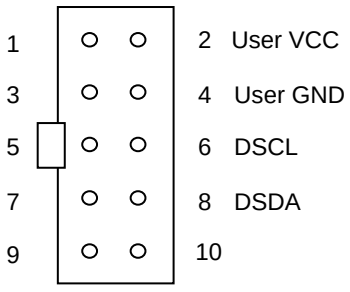


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

Subject	MC96F8316A	MC96F8316S	MC96F8316
On Chip Debugger (OCD)	Not supported	Not supported	Supported
Operating Voltage and Frequency	VDD: 2.2V to 5.5V, Freq.: Up to 16MHz - 2.2V to 5.5V @ 32 to 38kHz with x-tal - 2.2V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 2.2V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC
Supply Current IDD3 (Sub operation)	Typ/Max : 90/180 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃	Typ/Max : 60/90 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃	Typ/Max : 60/90 [uA] - 32.768kHz, VDD=3V±10%, TA=25℃
Power-On Reset Characteristics	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/5.0[V/ms]
IOH of ports (Chapter 7.8 – DC Characteristics)	P0, P1, P26, P3: IOH = -20mA @VDD=4.5V	P0, P1, P26, P3: IOH = -20mA @VDD=4.5V	P1: IOH = -20mA @VDD = 4.5V P0, P26, P3: IOH = -10mA @VDD = 4.5V
Output Low Voltage(VOL1) (Chapter 7.8 – DC Characteristics)	IOL = 15mA @ VDD = 4.5V and VOL1 = 1.2V	IOL = 15mA @ VDD = 4.5V and VOL1 = 1.0V	IOL = 15mA @ VDD = 4.5V and VOL1 = 1.0V
Internal RC frequency (IRC)	Tolerance TA= 0°C to +50°C : ±1.5% TA= -20°C to +85°C : ±2.5% TA= -40°C to +85°C : ±3.5%	Tolerance TA= 0°C to +50°C : ±1.5% TA= -20°C to +85°C : ±2.5% TA= -40°C to +85°C : ±3.5%	Tolerance TA= 0°C to +50°C : ±1.0% TA= -20°C to +85°C : ±2.0% TA= -40°C to +85°C : ±3.0%
x-tal filter selectable (XTFLSR Register)	x-tal filter selection register for noise immunity - 10.5MHz < x-tal ≤ 12MHz - 8.5MHz < x-tal ≤ 10.5MHz - 6.5MHz < x-tal ≤ 8.5MHz - 4.5MHz < x-tal ≤ 6.5MHz - x-tal ≤ 4.5MHz	Not supported	Not supported
LVR/LVI	12 Level Selectable - 1.85V, 2.2V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V
	11 Level Selectable - 2.2V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V
	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 10.0(TYP)/15.0(MAX) uA One: 8.0(TYP)/12.0(MAX) uA
ADC	A/D Converter INL : ±6LSB DNL : ±1 LSB TOE : ±5 LSB ZOE : ±5 LSB	A/D Converter INL: ±6LSB DNL: ±1 LSB TOE: ±5 LSB ZOE: ±5 LSB	A/D Converter INL: ±4LSB DNL: ±1 LSB TOE: ±3 LSB ZOE: ±3 LSB
Vector Area Protection	En/Disable Vector Area(00H – FFH) Protection	Not supported	Not supported
Specific Area for Write Protection	8 kinds of protection size selectable - Address 0100H – 03FFH - Address 0100H – 07FFH - Address 0100H – 0BFFH - Address 0100H – 0FFFH - Address 0100H – 37FFH - Address 0100H – 3BFFH - Address 0100H – 3DFFH - Address 0100H – 3EFFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH
Full-flash Erase Mode Method (Chapter 15 – Flash Memory)	Sector Erase Mode	Sector Erase Mode	Sector and Byte Erase Mode

Table 1.2 Difference among MC96F8316A, MC96F8316S and MC96F8316

1.3.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

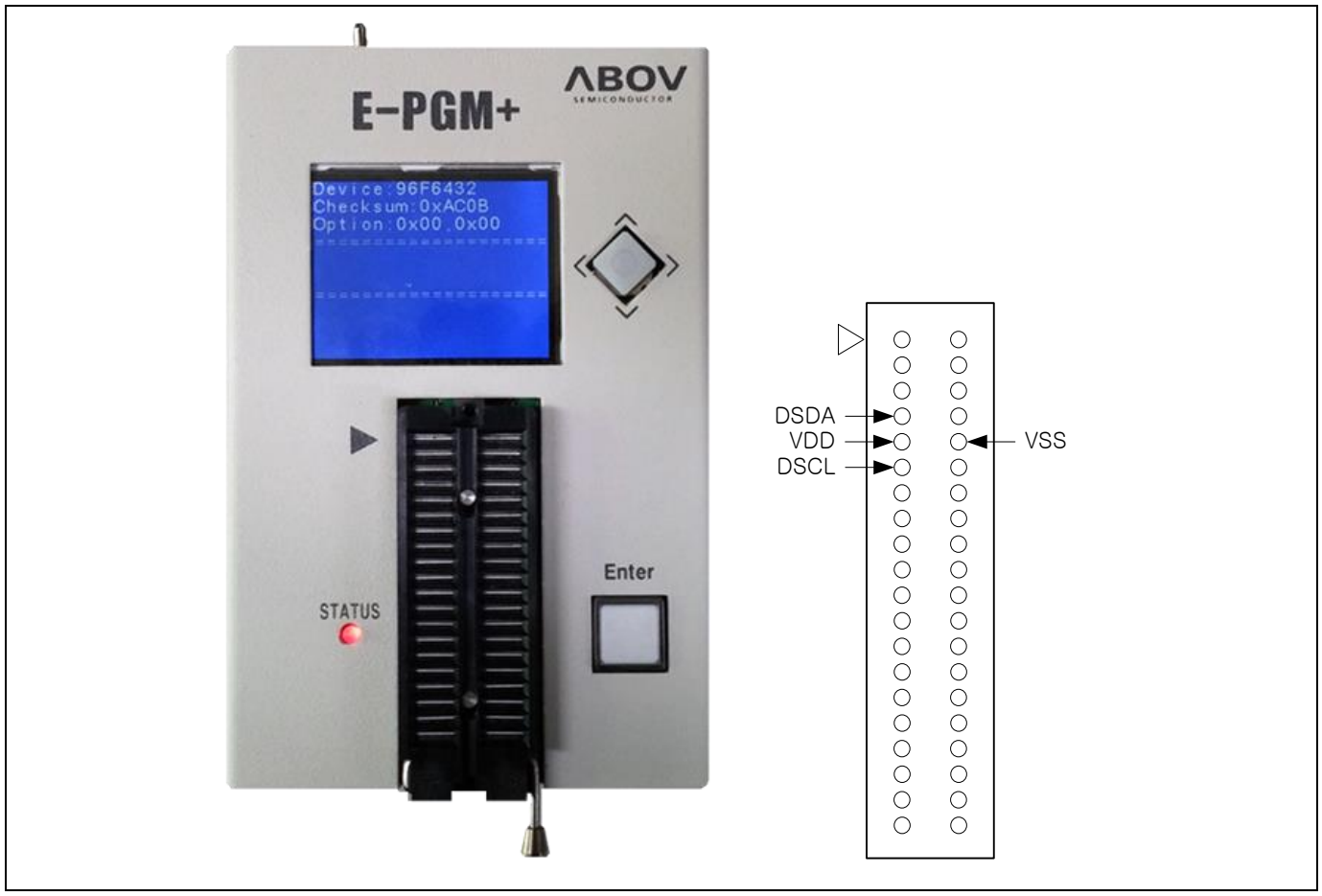


Figure 1.3 E-PGM+(Single writer)

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC96F8316A is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD and VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

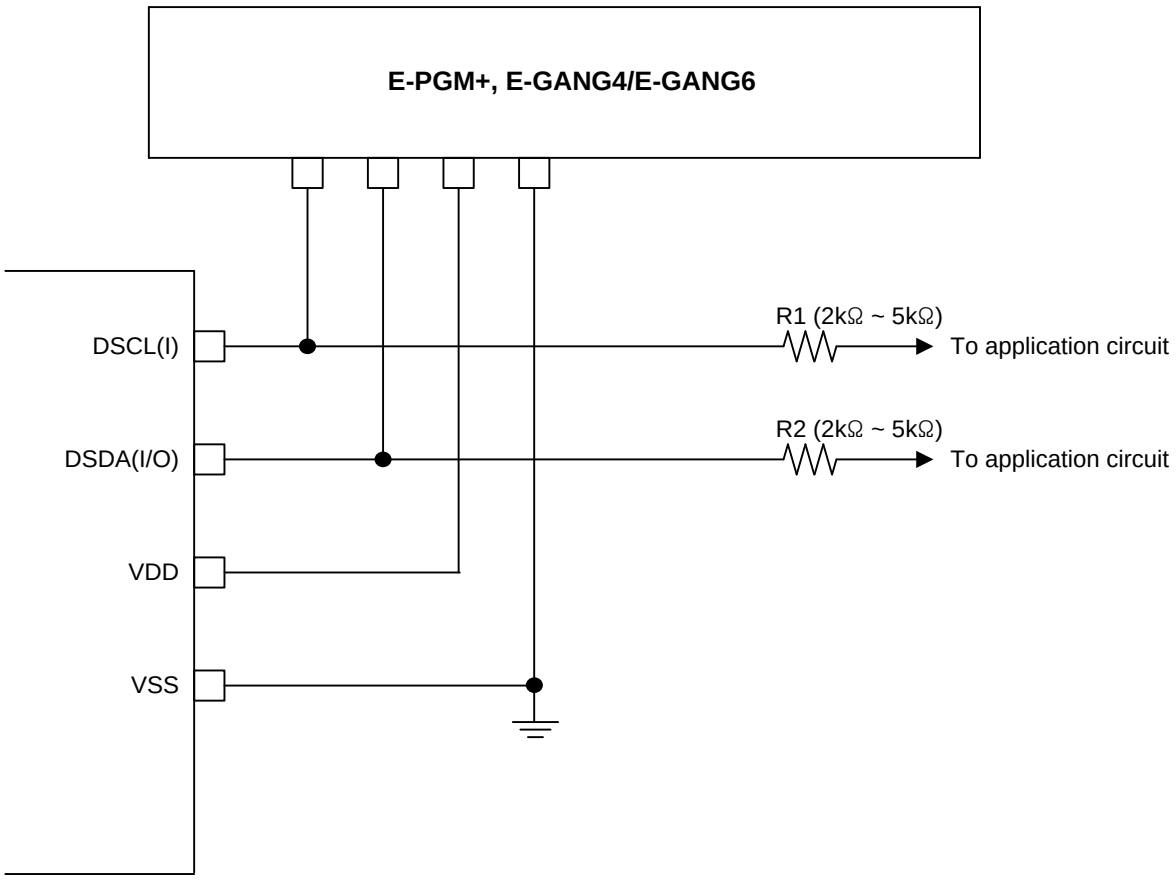
Table 1.3 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The MC96F8316A needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

1.4.2.1 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that areDSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.
Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

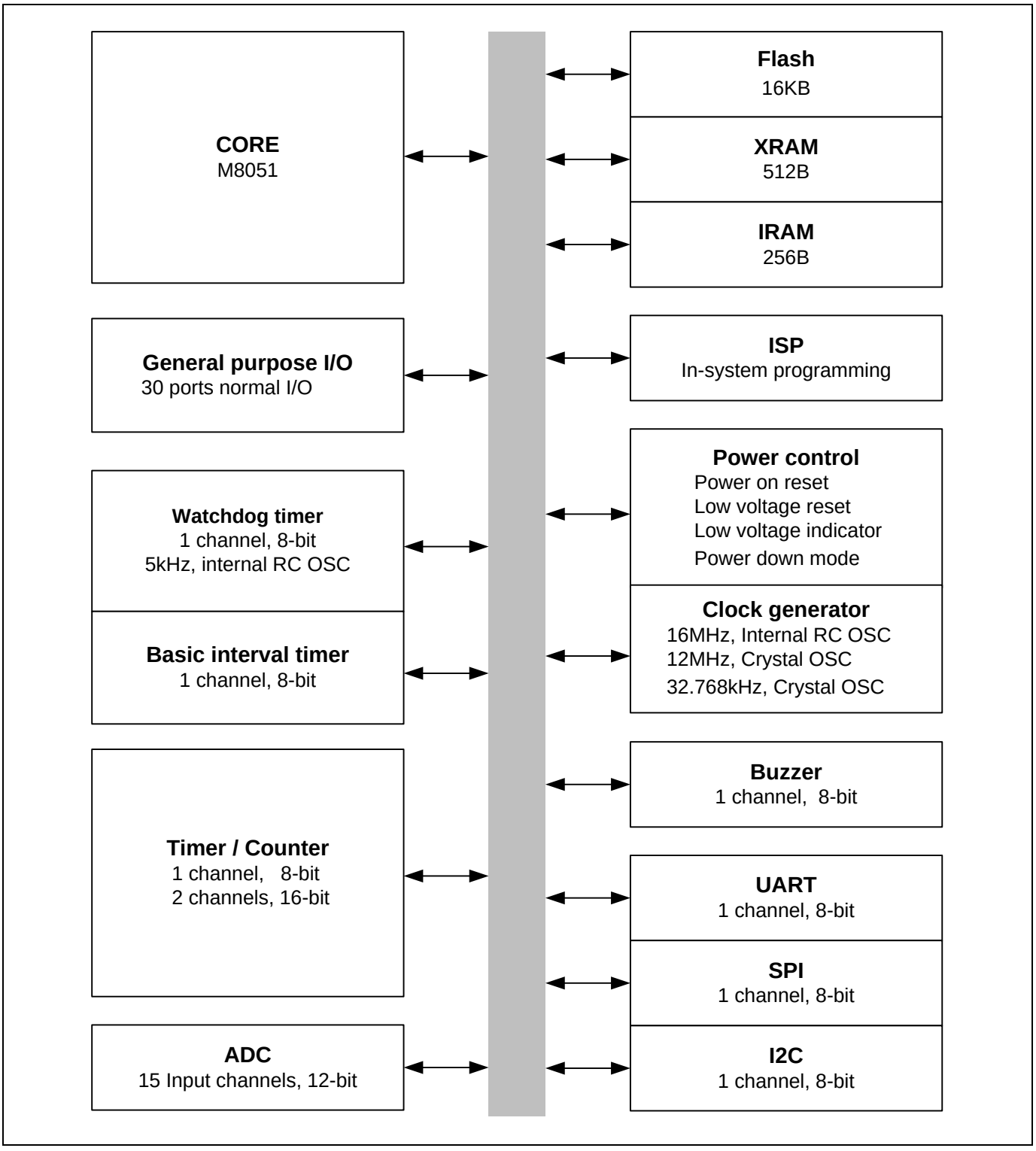
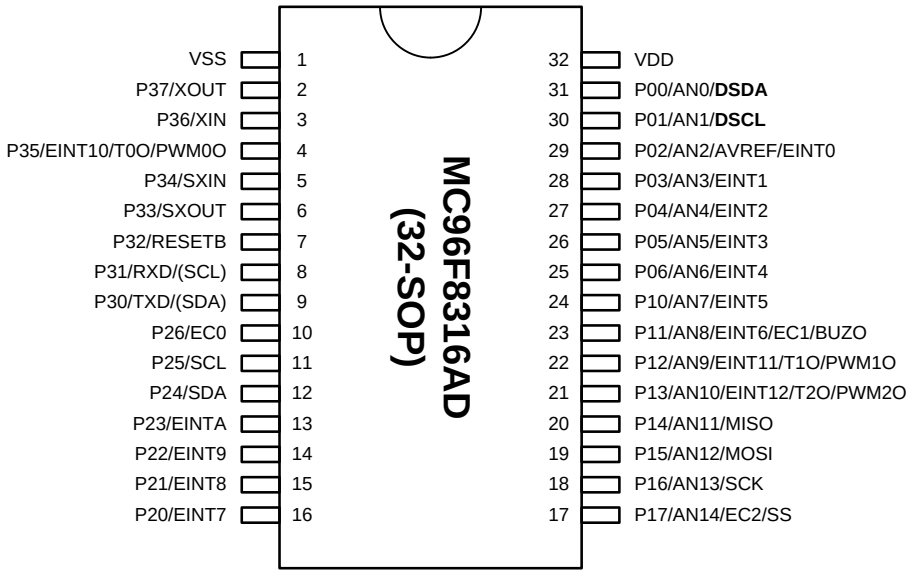


Figure 2.1 Block diagram of MC96F8316A

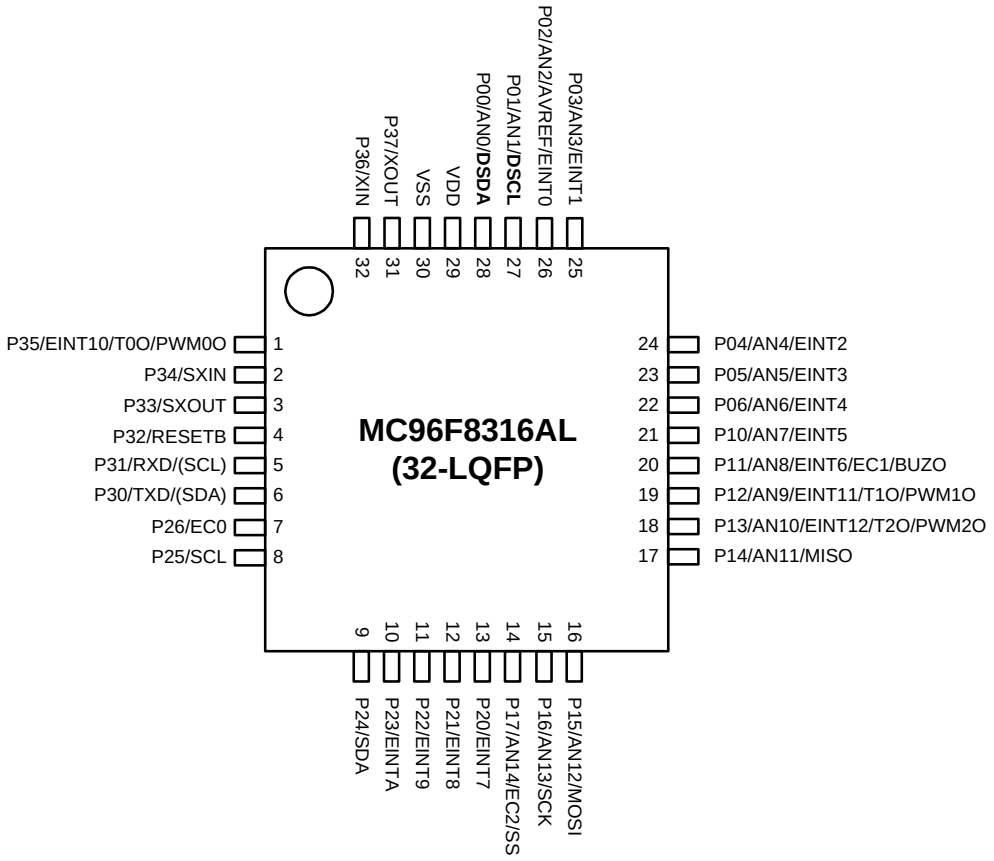
3 Pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

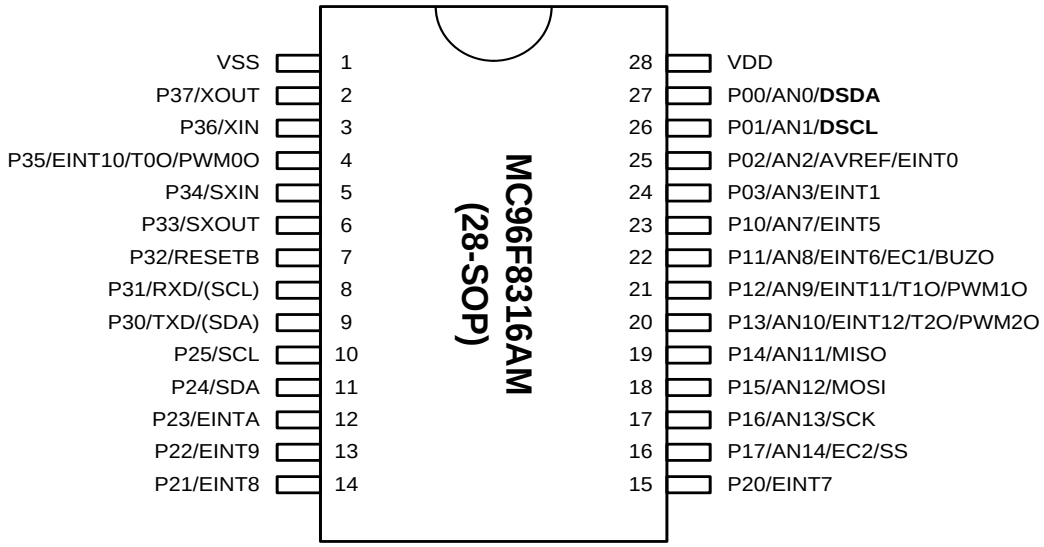
Figure 3.1 MC96F8316AD 32SOP pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

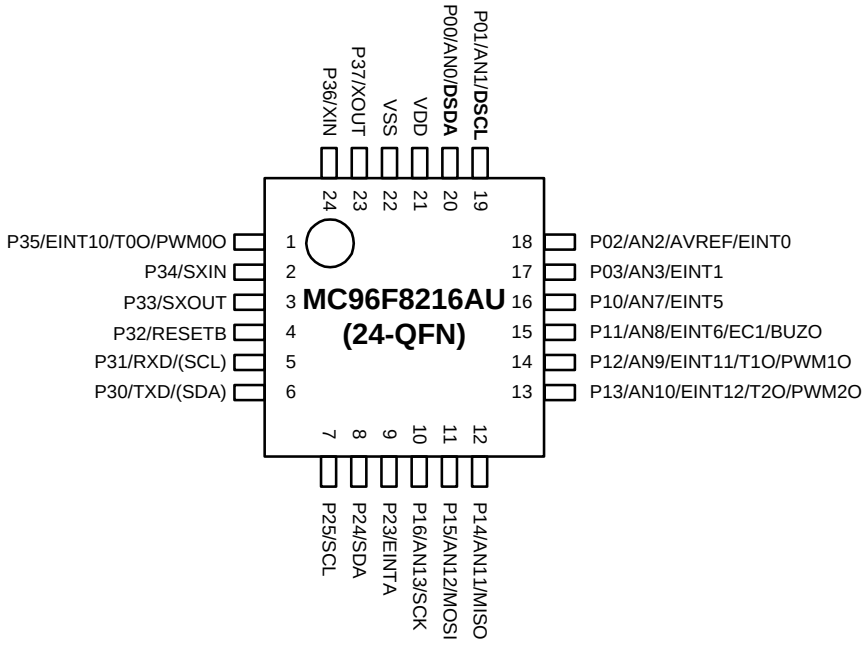
Figure 3.2 MC96F8316AL 32LQFP pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P04-P06 and P26 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 28-pin package is used.
3. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

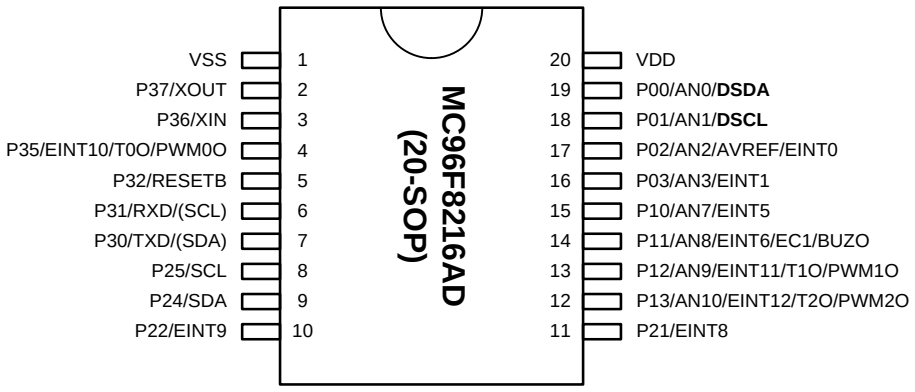
Figure 3.3 MC96F8316AM 28SOP pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P04-P06, P17, P20-P22 and P26 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 24-pin package is used.
3. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

Figure 3.4 MC96F8216AU 24QFN pin assignment



NOTE)

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P04-P06, P14-P17, P20, P23, P26 and P33-P34 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 20-pin package is used.
3. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

Figure 3.5 MC96F8216AD 20SOP pin assignment

4 Package Diagram

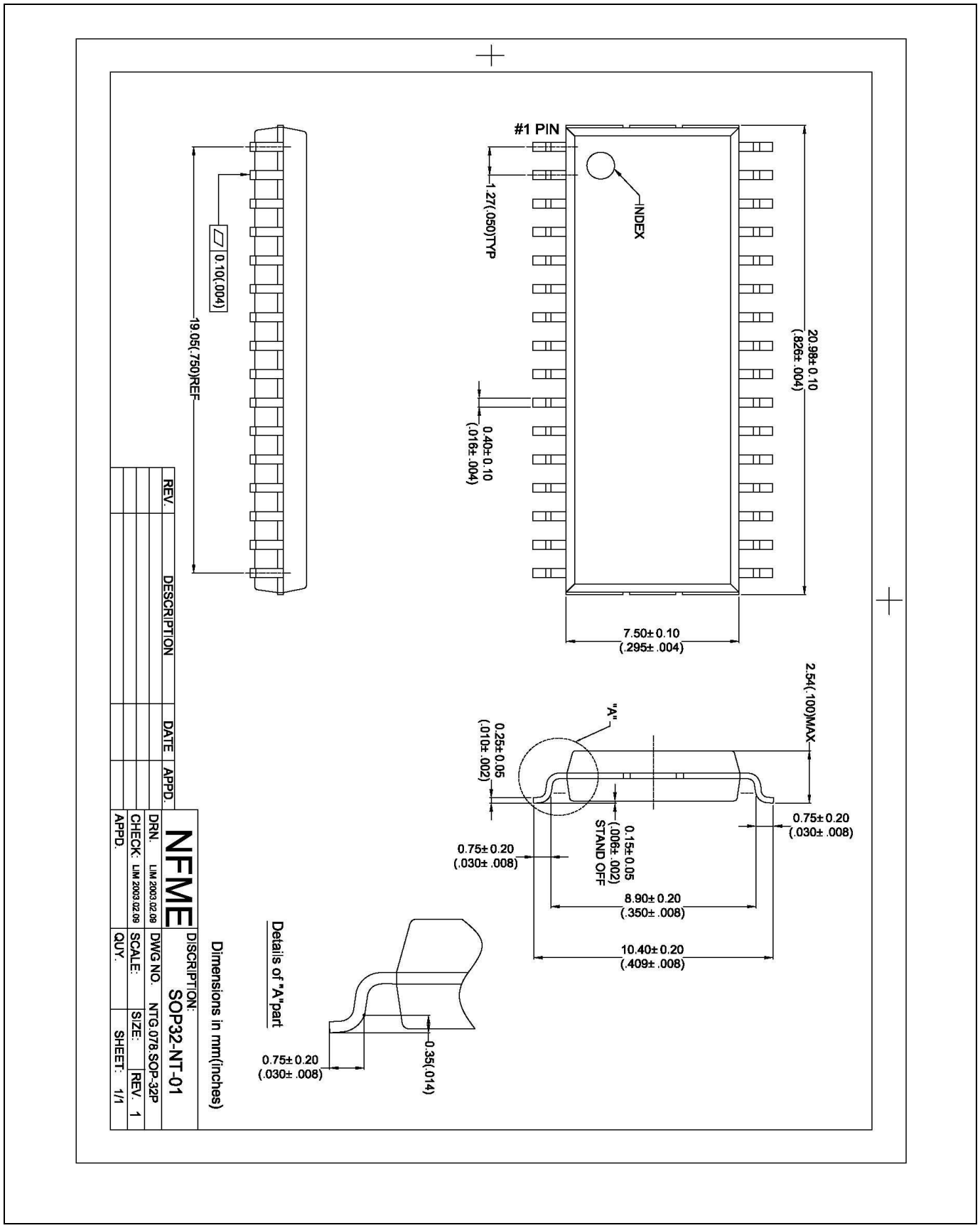
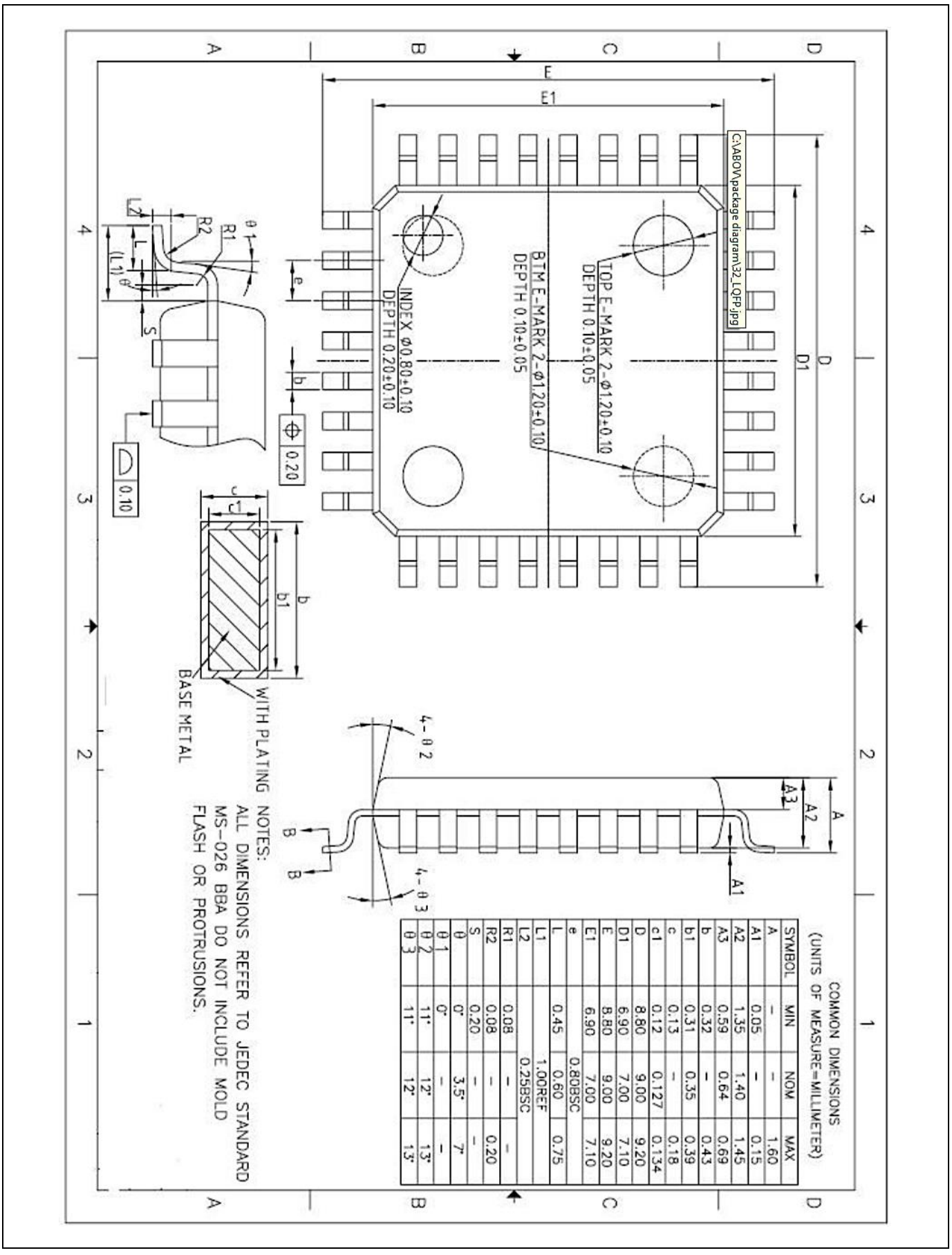


Figure 4.1 32-pin SOP Package



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

Figure 4.2 32-Pin LQFP Package

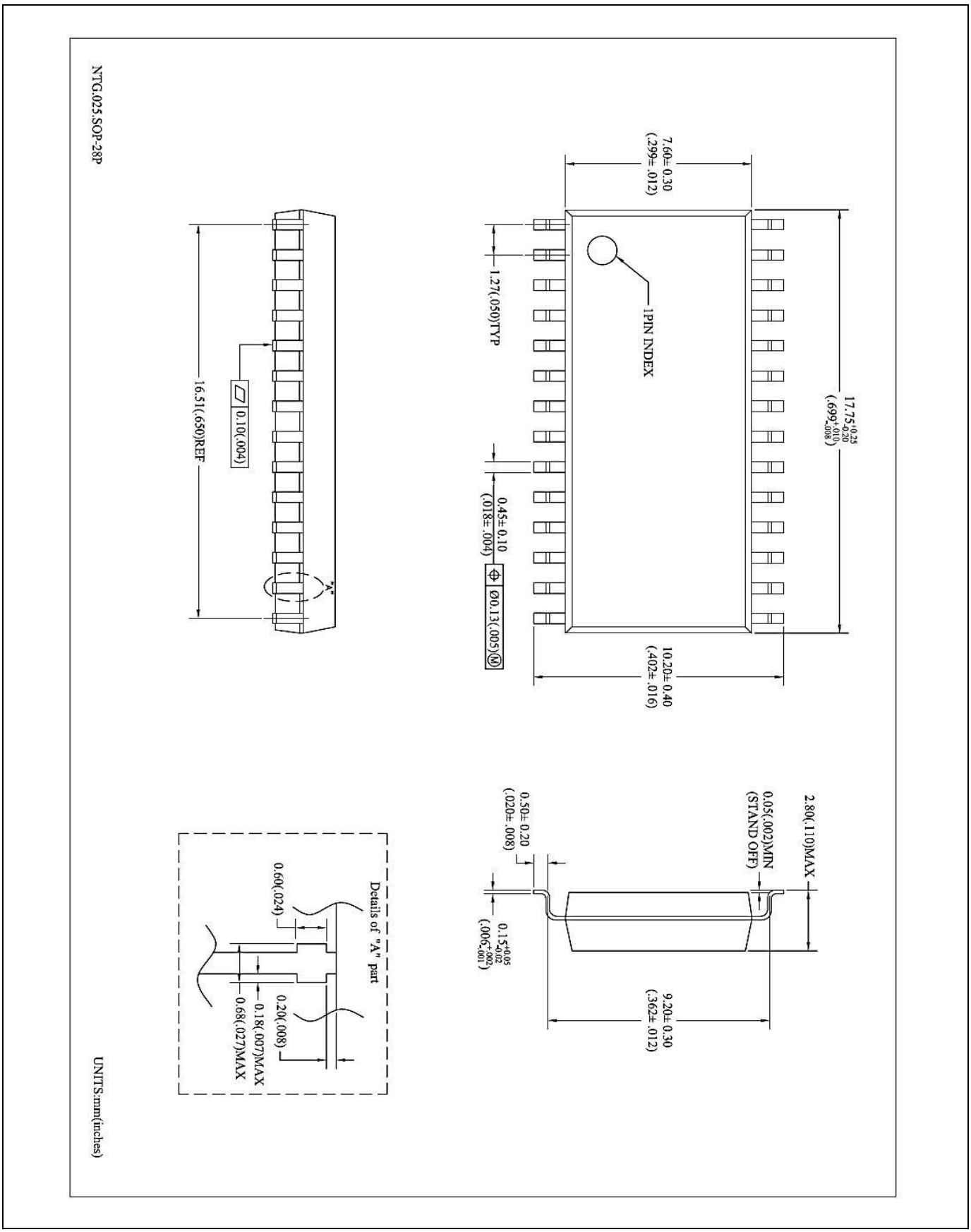


Figure 4.3 28-Pin SOP Package

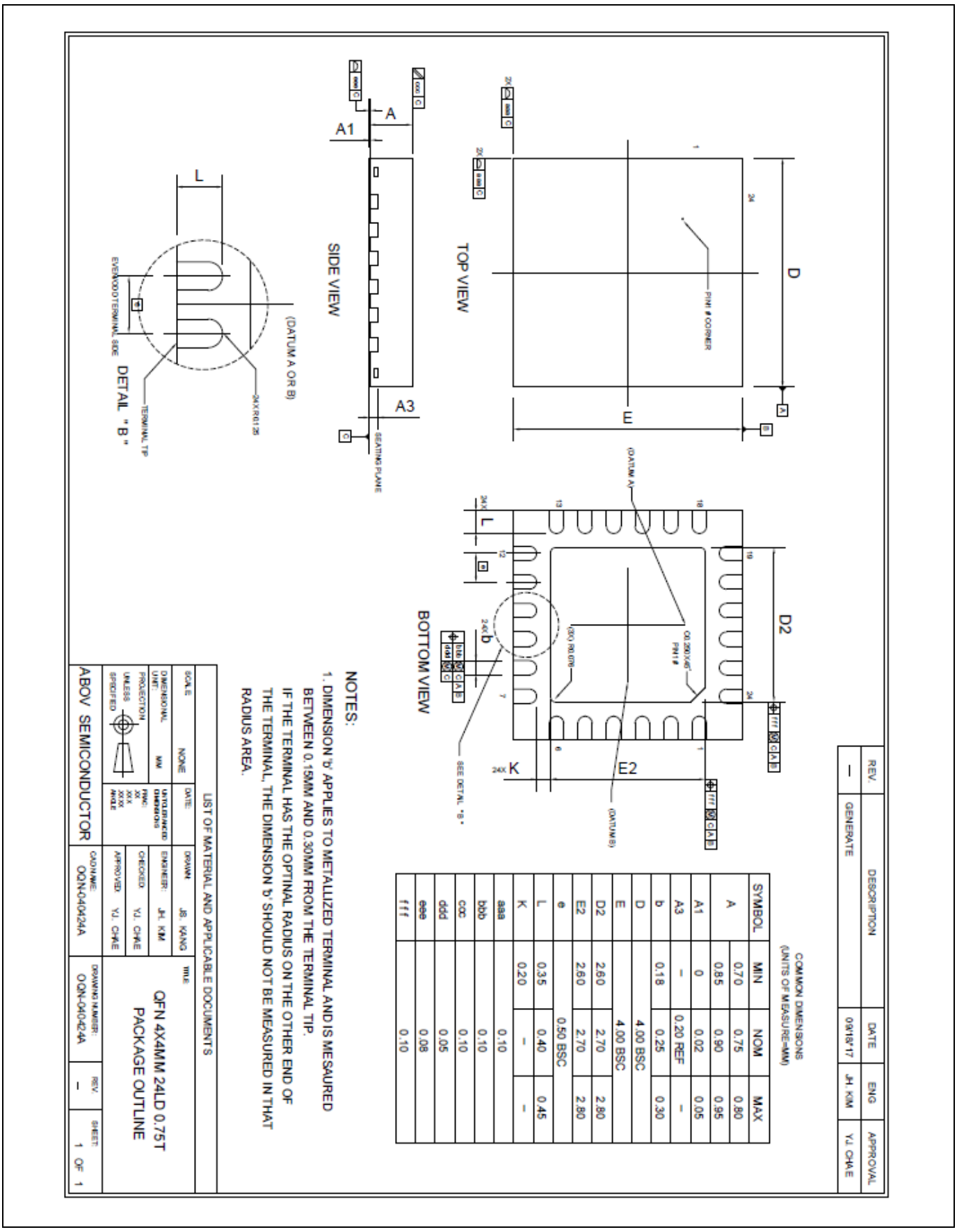


Figure 4.4 24-Pin QFN Package

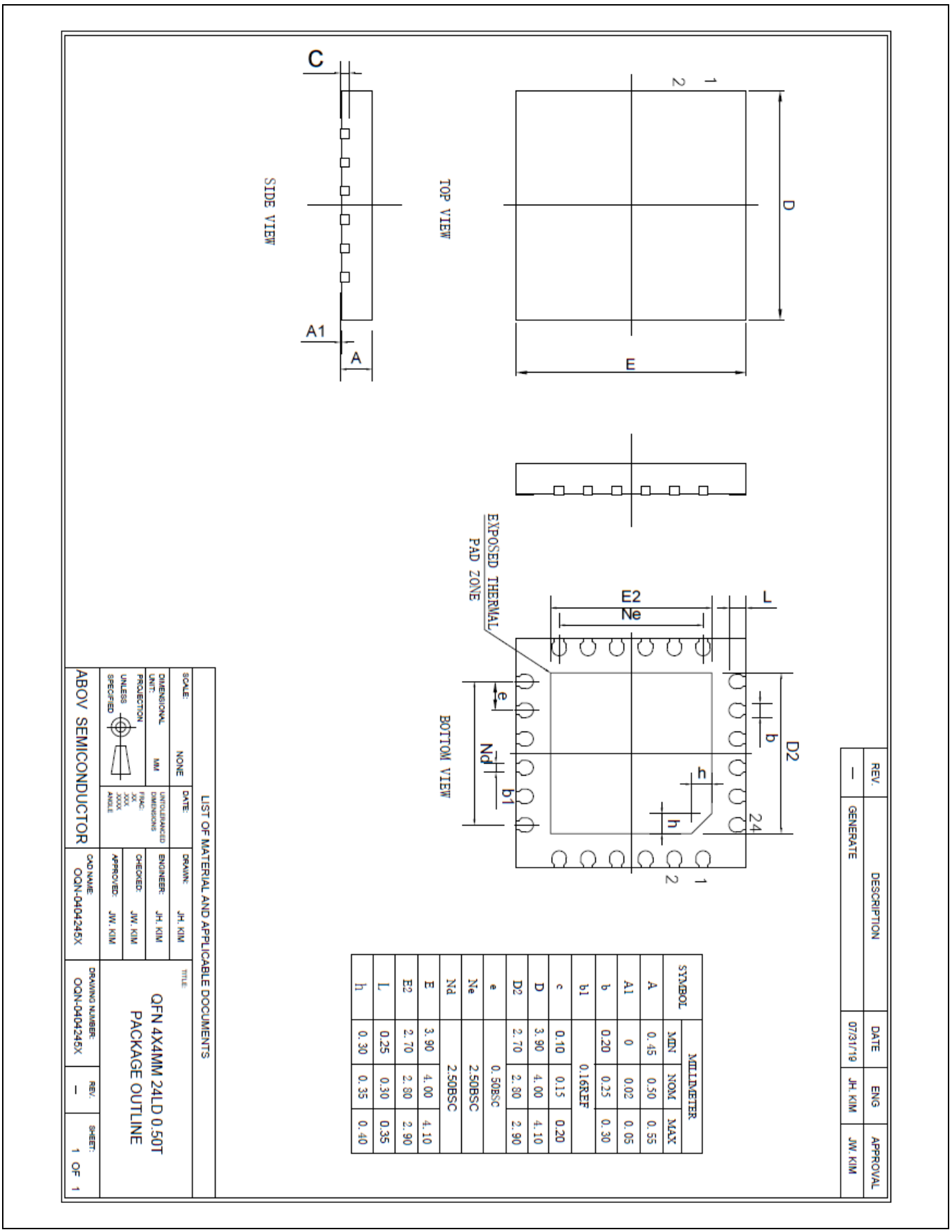
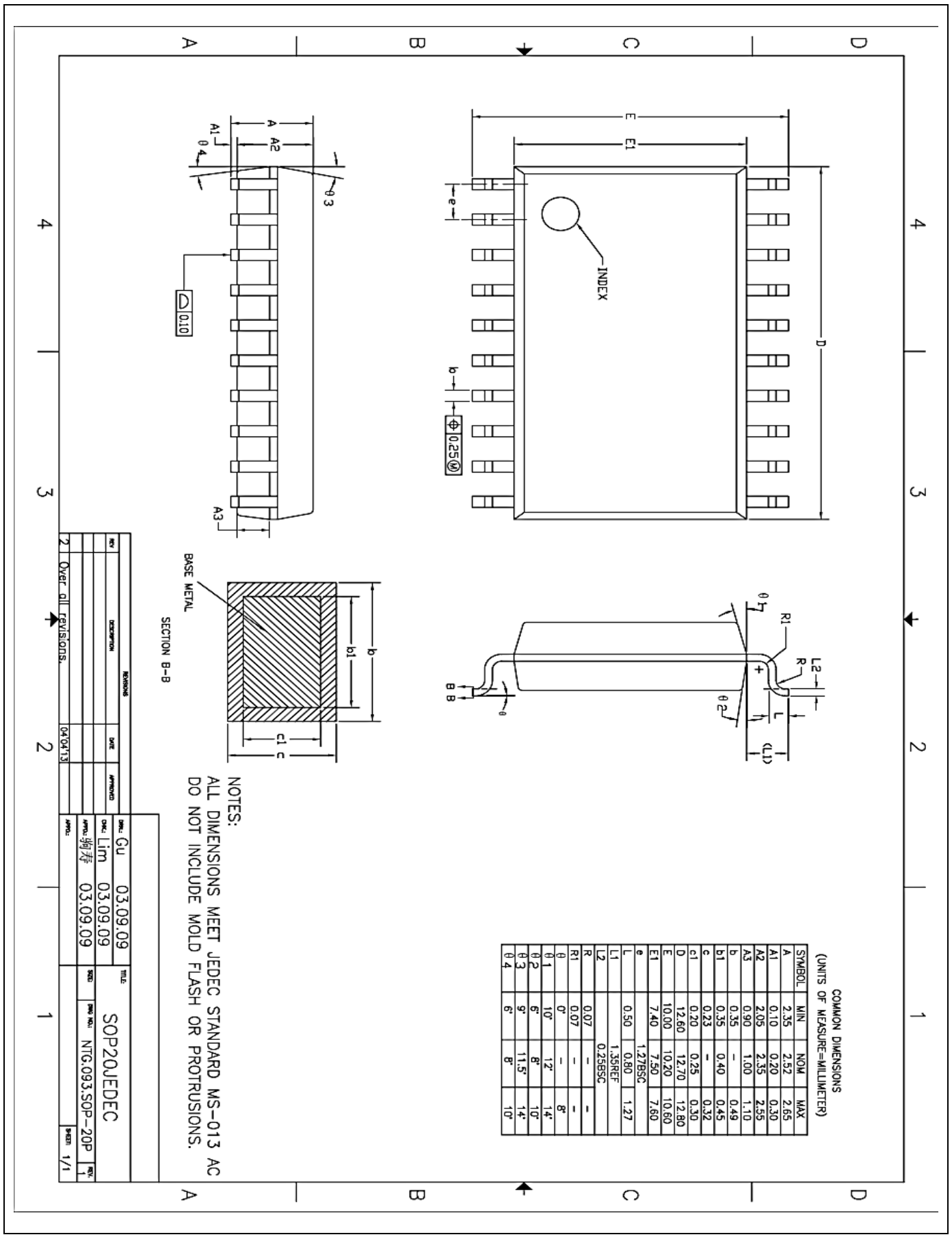


Figure 4.5 24-Pin QFN Package (Thin)



SYMBOL	MIN	NOM	MAX
A	2.35	2.52	2.65
A1	0.10	0.20	0.30
A2	2.05	2.35	2.55
A3	0.90	1.00	1.10
b	0.35	–	0.49
b1	0.35	0.40	0.45
c	0.23	–	0.32
c1	0.20	0.25	0.30
D	12.60	12.70	12.80
E	10.00	10.20	10.60
E1	7.40	7.50	7.60
e		1.27BSC	
L	0.50	0.80	1.27
L1		1.35REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	10°	12°	14°
θ2	6°	8°	10°
θ3	9°	11.5°	14°
θ4	6°	8°	10°

Figure 4.6 20-Pin SOP Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P04 – P06 are only in the 32-Pin package.	Input	AN0/DSDA
P01				AN1/DSCL
P02				AN2/AVREF/EINT0
P03				AN3/EINT1
P04				AN4/EINT2
P05				AN5/EINT3
P06				AN6/EINT4
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P17 is not in the 24-Pin package. The P14 – P17 are not in the 20-Pin package.	Input	AN7/EINT5
P11				AN8/EINT6/EC1/BUZO
P12				AN9/EINT11/T1O/PWM1O
P13				AN10/EINT12/T2O/PWM2O
P14				AN11/MISO
P15				AN12/MOSI
P16				AN13/SCK
P17				AN14/EC2/SS
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20 – P22 are not in the 24-Pin package. The P20 and P23 are not in the 20-Pin package. The P26 is only in the 32-Pin package.	Input	EINT7
P21				EINT8
P22				EINT9
P23				EINTA
P24				SDA
P25				SCL
P26				EC0
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P33 – P34 are not in the 20-Pin package.	Input	TXD
P31				RXD
P32				RESETB
P33				SXOUT
P34				SXIN
P35				EINT10/T0O/PWM0O
P36				XIN
P37				XOUT

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
EINT0	I/O	External interrupt inputs	Input	P02/AN2/AVREF
EINT1				P03/AN3
EINT2				P04/AN4
EINT3				P05/AN5
EINT4				P06/AN6
EINT5				P10/AN7
EINT6				P11/AN8/EC1/BUZO
EINT7				P20
EINT8				P21
EINT9				P22
EINTA				P23
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P35/T0O/PWM0O
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P12/AN9/T1O/PWM1O
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P13/AN10/T2O/PWM2O
T0O	I/O	Timer 0 interval output	Input	P35/EINT10/PWM0O
T1O	I/O	Timer 1 interval output	Input	P12/AN9/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P13/AN10/EINT12/PWM2O
PWM0O	I/O	Timer 0 PWM output	Input	P35/EINT10/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P12/AN9/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P13/AN10/EINT12/T2O
EC0	I/O	Timer 0 event count input	Input	P26
EC1	I/O	Timer 1 event count input	Input	P11/AN8/EINT6/BUZO
EC2	I/O	Timer 2 event count input	Input	P17/AN14/SS
BUZO	I/O	Buzzer signal output	Input	P11/AN8/EINT6/EC1
SCK	I/O	Serial clock input/output	Input	P16/AN13
MISO	I/O	Serial data input/output	Input	P14/AN11
MOSI	I/O	Serial data input/output	Input	P15/AN12
SS	I/O	Slave select input	Input	P17/AN14/EC2
TXD	I/O	UART data output	Input	P30
RXD	I/O	UART data input	Input	P31
SCL	I/O	I2C clock input/output	Input	P25
SDA	I/O	I2C data input/output	Input	P24

Table 5.1 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
AVREF	I/O	A/D converter reference voltage	Input	P02/AN2/EINT0
AN0	I/O	A/D converter analog input channels	Input	P00/DSDA
AN1				P01/DSCL
AN2				P02/AVREF/EINT0
AN3				P03/EINT1
AN4				P04/EINT2
AN5				P05/EINT3
AN6				P06/EINT4
AN7				P10/EINT5
AN8				P11/EINT6/EC1/BUZO
AN9				P12/EINT11/T1O/PWM1O
AN10				P13/EINT12/T2O/PWM2O
AN11				P14/MISO
AN12				P15/MOSI
AN13				P16/SCK
AN14				P17/EC2/SS
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P32
DSDA	I/O	Programmer data input/output (NOTE5,6)	Input	P00
DSCL	I/O	Programmer clock input (NOTE5,6)	Input	P01
XIN	I/O	Main oscillator pins	Input	P36
XOUT				P37
SXIN	I/O	Sub oscillator pins	Input	P34
SXOUT				P33
VDD, VSS	–	Power input pins	–	–

Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P04-P06 and P26 are not in the 28-Pin package.
2. The P04-P06, P17, P20-P22 and P26 are not in the 24-Pin package.
3. The P04-P06, P14-P17, P20, P23, P26 and P33-P34 are not in the 20-Pin package.
4. The P32/RESETB pin is configured as one of the P32 and the RESETB pin by the “CONFIGURE OPTION”.
5. If the P00 and P01 pins are connected to the programmer during the reset or power-on reset, the pins are automatically configured as the programmer pins.
6. The P00 and P01 pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
7. The P37/XOUT, P36/XIN, P34/SXIN and P33/SXOUT pins are configured as a function pin by software control.

6 Port Structures

6.1 General Purpose I/O Port

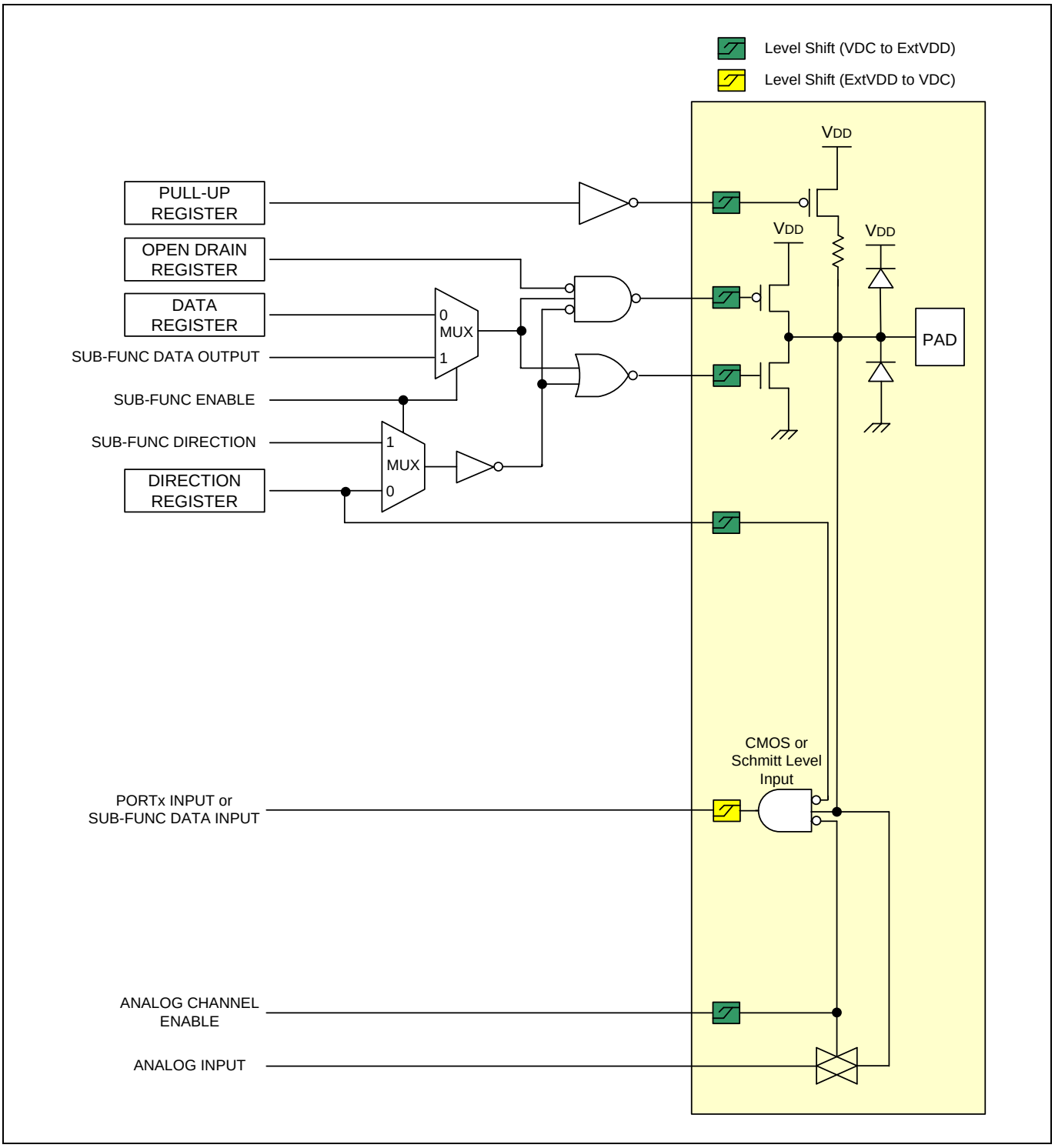


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

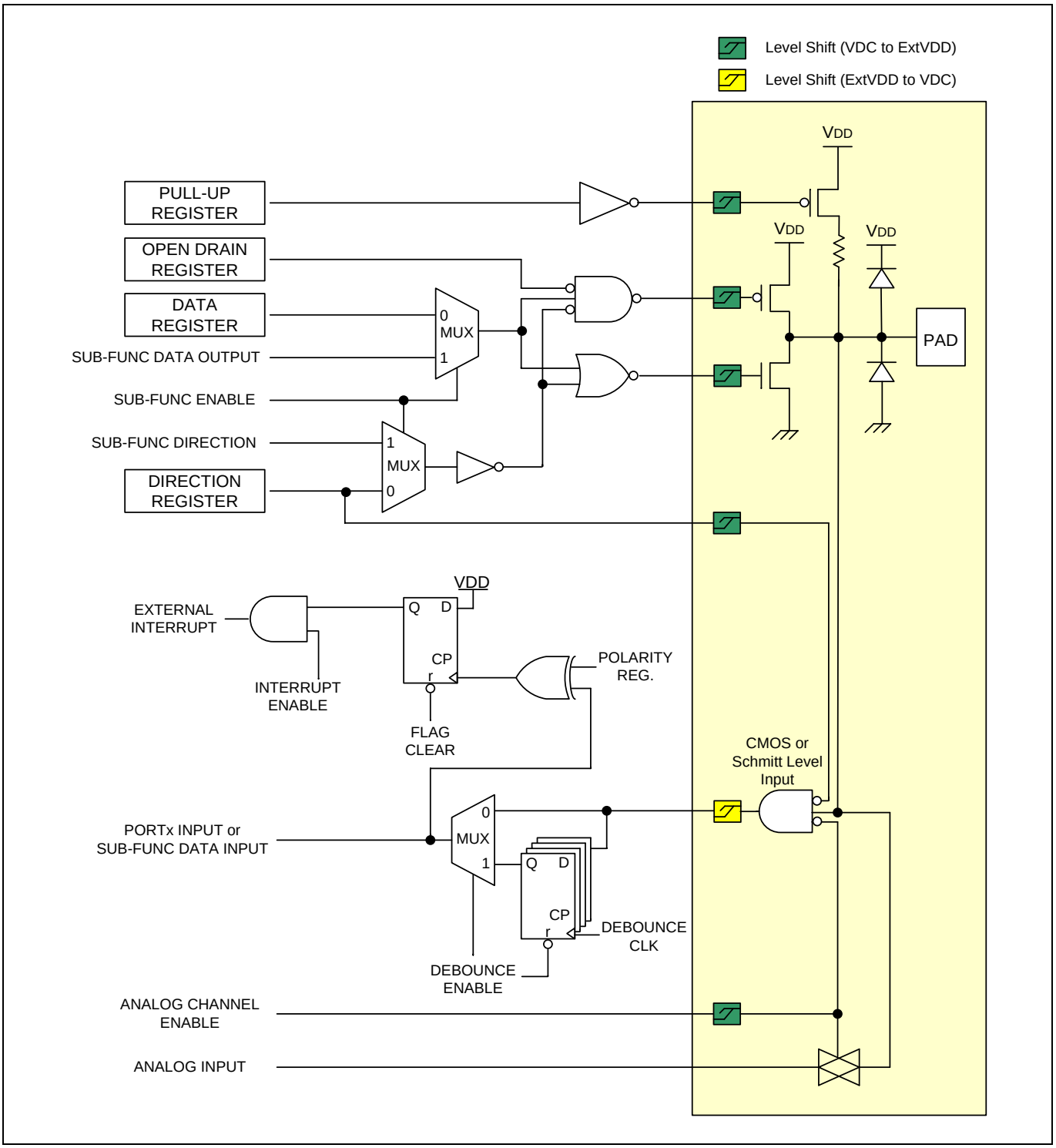


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-25	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-200	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	180	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	200	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	SX-tal	2.2	–	5.5	V
		f_X= 0.4 ~ 4.2MHz	X-tal	2.2	–	5.5	
		f_X= 0.4 ~ 10.0MHz		2.7	–	5.5	
		f_X= 0.4 ~ 12.0MHz		3.0	–	5.5	
		f_X= 0.5 ~ 16.0MHz	Internal RC	2.2	–	5.5	
Operating Temperature	T_{OPR}	VDD= 2.2 ~ 5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	AVREF= 4.0V – 5.5V		20	–	–	us
		AVREF= 3.0V – 5.5V		30	–	–	
		AVREF= 2.7V – 5.5V		60	–	–	
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		2.2	–	VDD	
VDD19	–	–		–	1.95	–	V
Analog Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	0.5V to 2.0V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	μA

Table 7.4 Power-on Reset Characteristics

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.85V		–	1.85	2.15	V
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
LVR Hysteresis	△V	–		–	50	150	mV
LVI Hysteresis	△V	–		–	10	50	
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	–	–	–	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 – 5.5V	–	16	–	MHz
Tolerance	–	T_A = 0°C to +50˚C	–	–	±1.5	%
		T_A = -20°C to +85˚C			±2.5	
		T_A = -40°C to +85˚C			±3.5	
Clock Duty Ratio	TOD	–	40	50	60	%
Stabilization Time	T_{HFS}	–	–	–	100	us
IRC Current	I_{IRC}	Enable	–	0.2	–	mA
		Disable	–	–	0.1	uA

Table 7.6 High Internal RC Oscillator Characteristics

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

7.8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	All input pins, RESETB		0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, RESETB		–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD= 4.5V, I_{OH}= -20mA, All output ports except V_{OH2}		VDD-2.0	–	–	V
	V_{OH2}	VDD= 4.5V, I_{OH}= -10mA, P20-P25		VDD-2.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 15mA, All output ports except V_{OL2}		–	–	1.2	V
	V_{OL2}	VDD= 4.5V, I_{OL}= 160mA, P20-P25		–	1.5	3.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	μA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	μA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
ADC wake-up pull-up resistor	R_{AWPU1}	T_A= 25°C		90	150	200	kΩ
	R_{AWPU2}			180	300	400	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25 °C ,VDD=5V		2500	5000	10000	

Table 7.8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz, VDD= 5V±10%		–	3.0	6.0	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	2.2	4.4	
		f_{IRC}= 16MHz, VDD= 5V±10%		–	3.0	6.0	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz, VDD= 5V±10%		–	1.3	2.6	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	0.7	1.4	
		f_{IRC}= 16MHz, VDD= 5V±10%		–	0.8	1.6	
	I_{DD3}	f_{SUB}=32.768kHz VDD= 3V±10% T_A= 25°C	Sub RUN	–	90.0	180.0	uA
	I_{DD4}		Sub IDLE	–	6.0	12.0	uA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	uA

Table 7.9 DC Characteristics(Continued**)**

NOTE)

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.9 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5V(n= 0, 1, 2)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5V(n= 0, 1, 2)	20	–	–	

Table 7.10 AC Characteristics

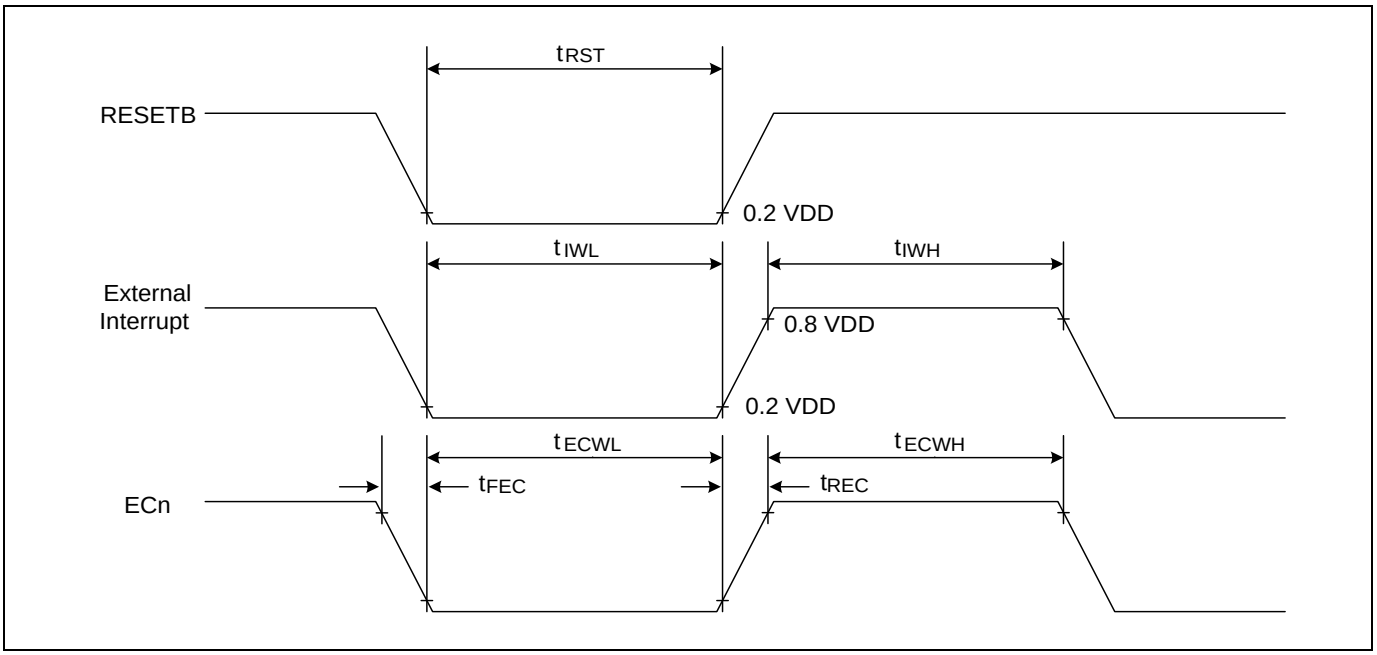


Figure 7.1 AC Timing

7.10 SPI Characteristics

(T_A=-40°C– +85°C, VDD=2.2V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.11 SPI Characteristics

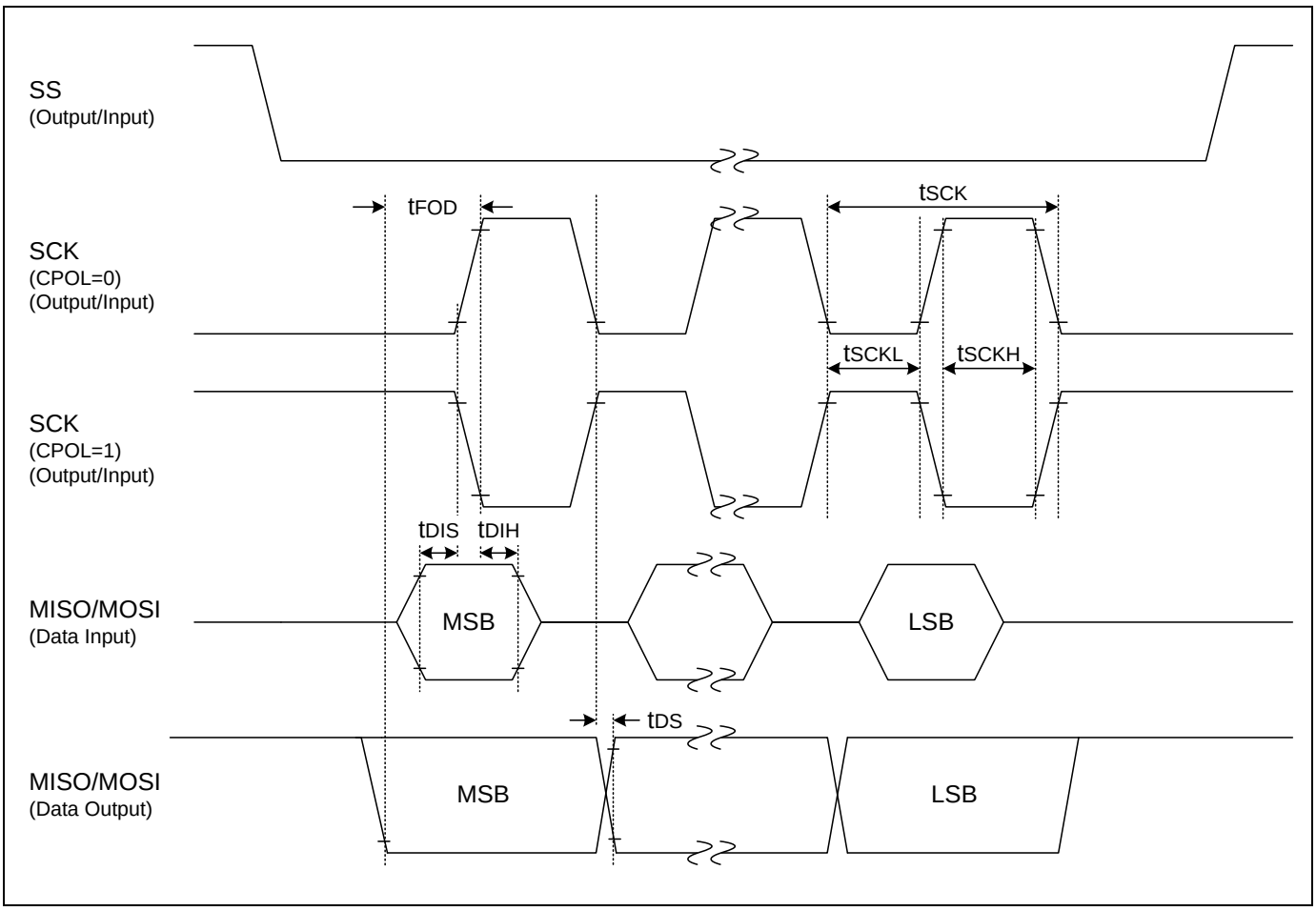


Figure 7.2 SPI Timing

7.11 UART Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	ns

Table 7.12 UART Characteristics

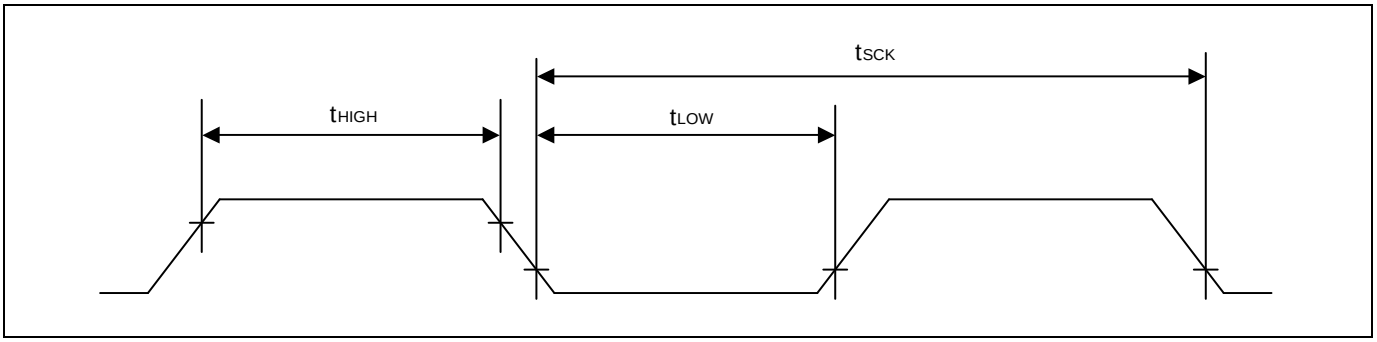


Figure 7.3 Waveform for UART Timing Characteristics

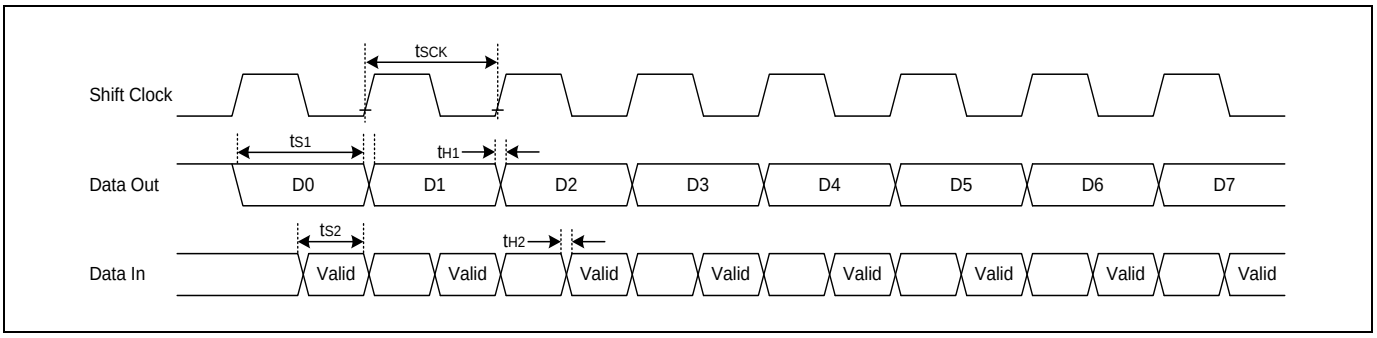


Figure 7.4 Timing Waveform for the UART Module

7.12 I2C Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.13 I2C Characteristics

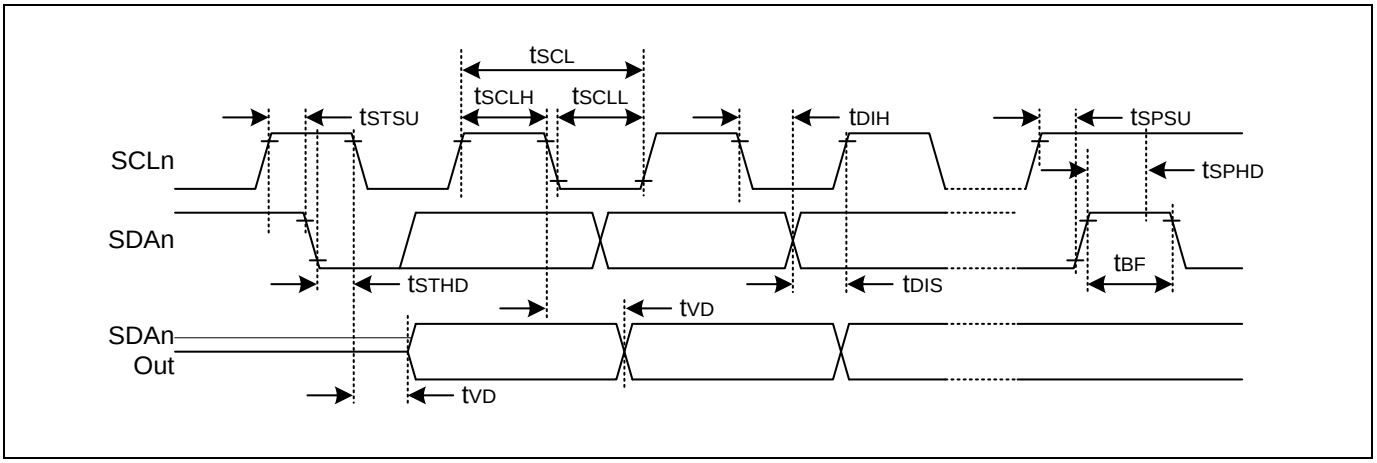


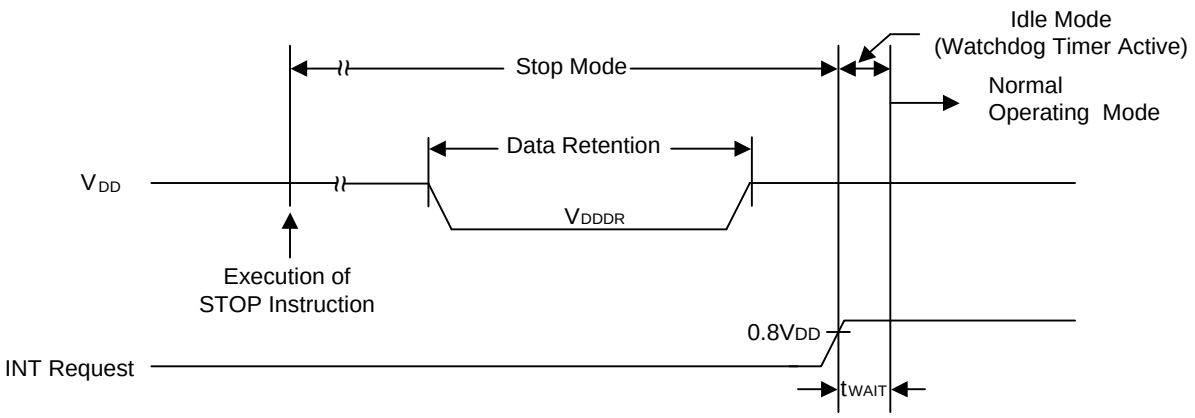
Figure 7.5 I2C Timing

7.13 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

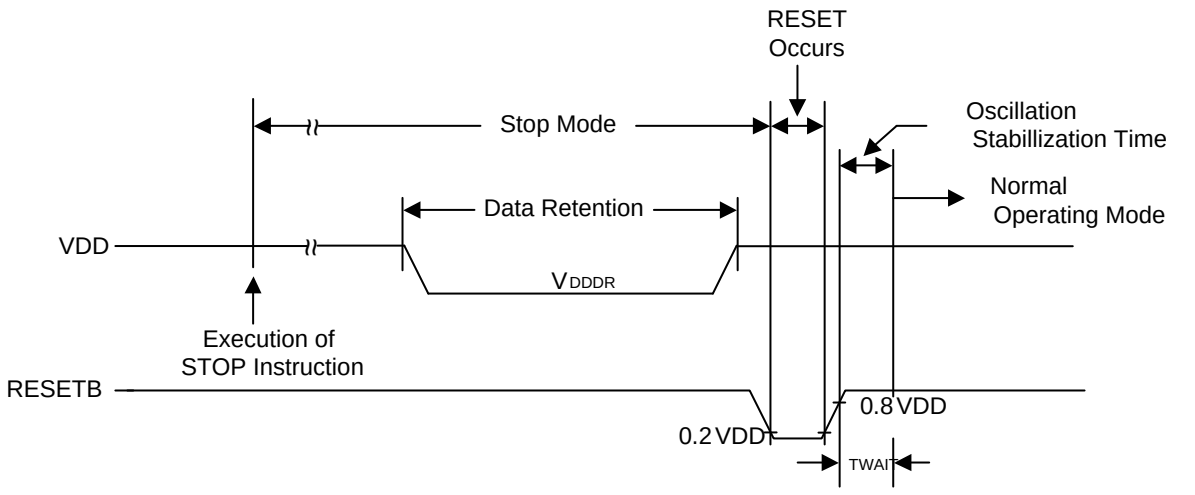
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 2.2V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7.14 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.14 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase (Sector 0~503)	NF_{WE}	–	–	–	10,000	times
Endurance of Write/Erase (Sector 504~511)					100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Table 7.15 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.15 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.16 Input/Output Capacitance

7.16 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	

Table 7.17 Main Clock Oscillator Characteristics

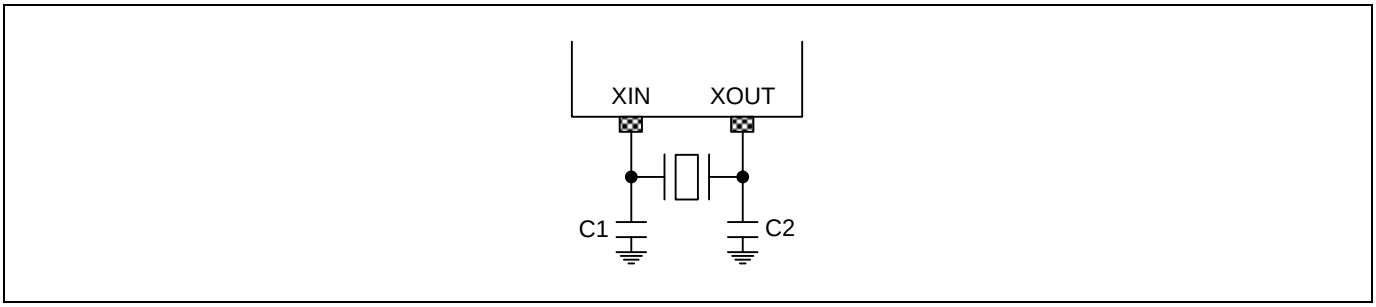


Figure 7.8 Crystal/Ceramic Oscillator

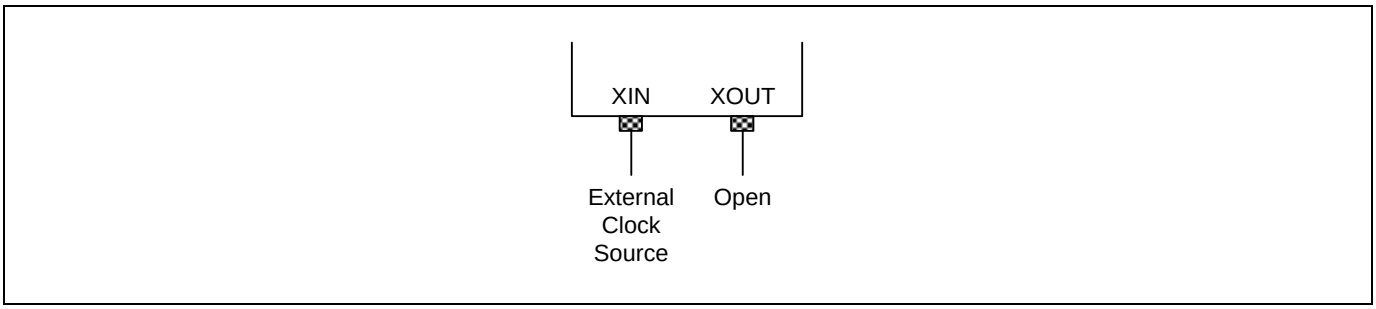


Figure 7.9 External Clock

7.17 Sub Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	2.2V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

Table 7.18 Sub Clock Oscillator Characteristics

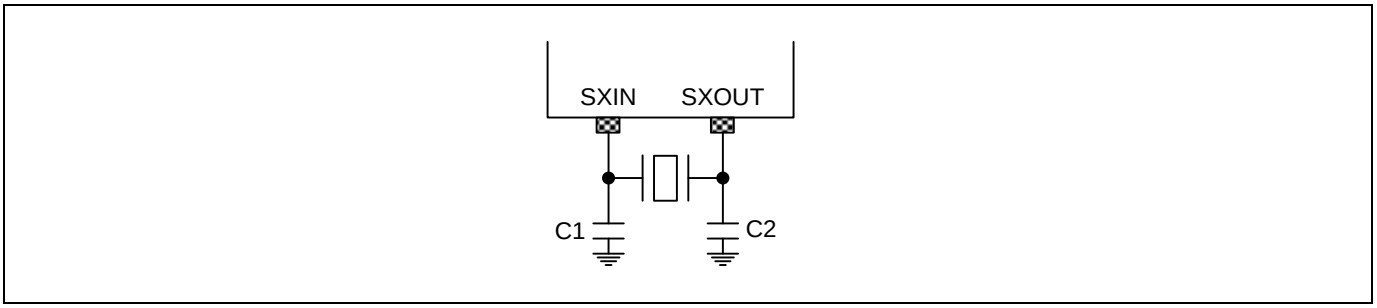


Figure 7.10 Crystal Oscillator

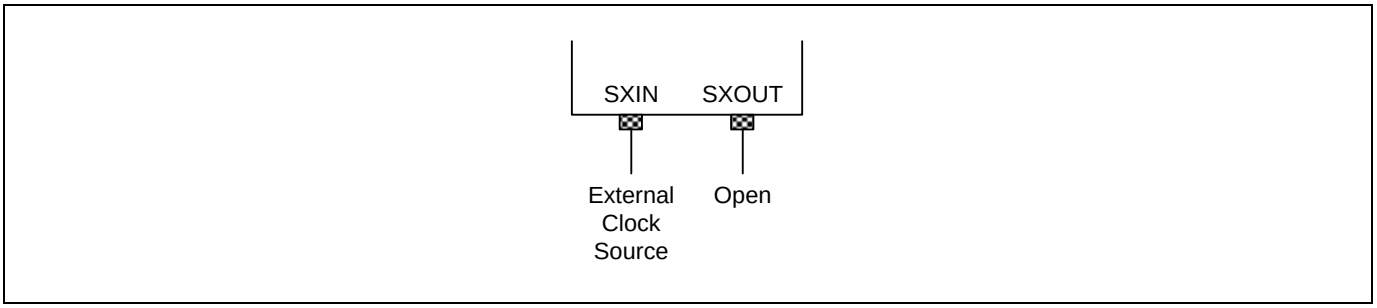


Figure 7.11 External Clock

7.18 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

Table 7.19 Main Oscillation Stabilization Characteristics

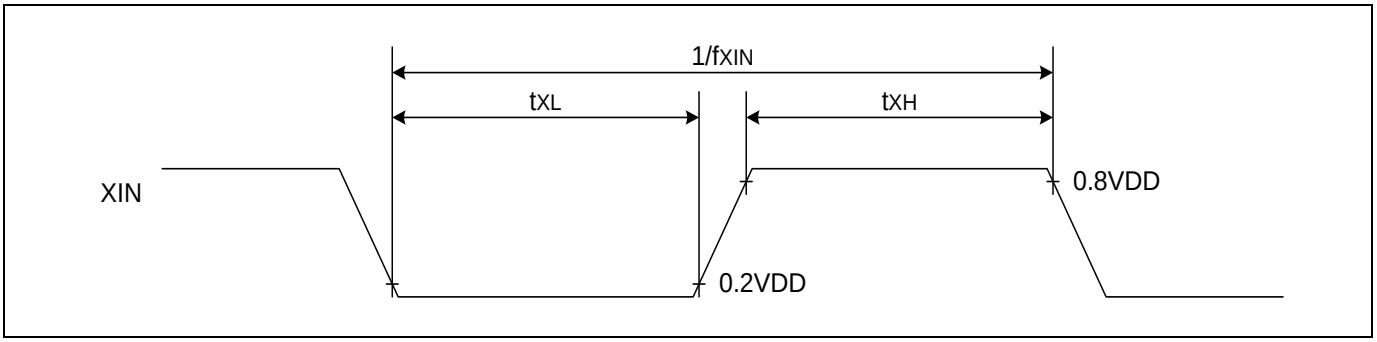


Figure 7.12 Clock Timing Measurement at XIN

7.19 Sub Oscillation Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

Table 7.20 Sub Oscillation Stabilization Characteristics

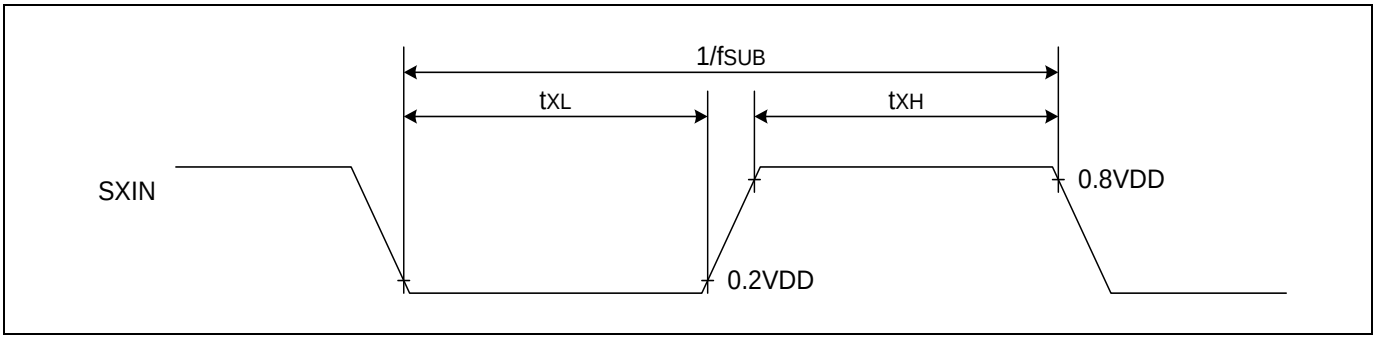


Figure 7.13 Clock Timing Measurement at SXIN

7.20 Operating Voltage Range

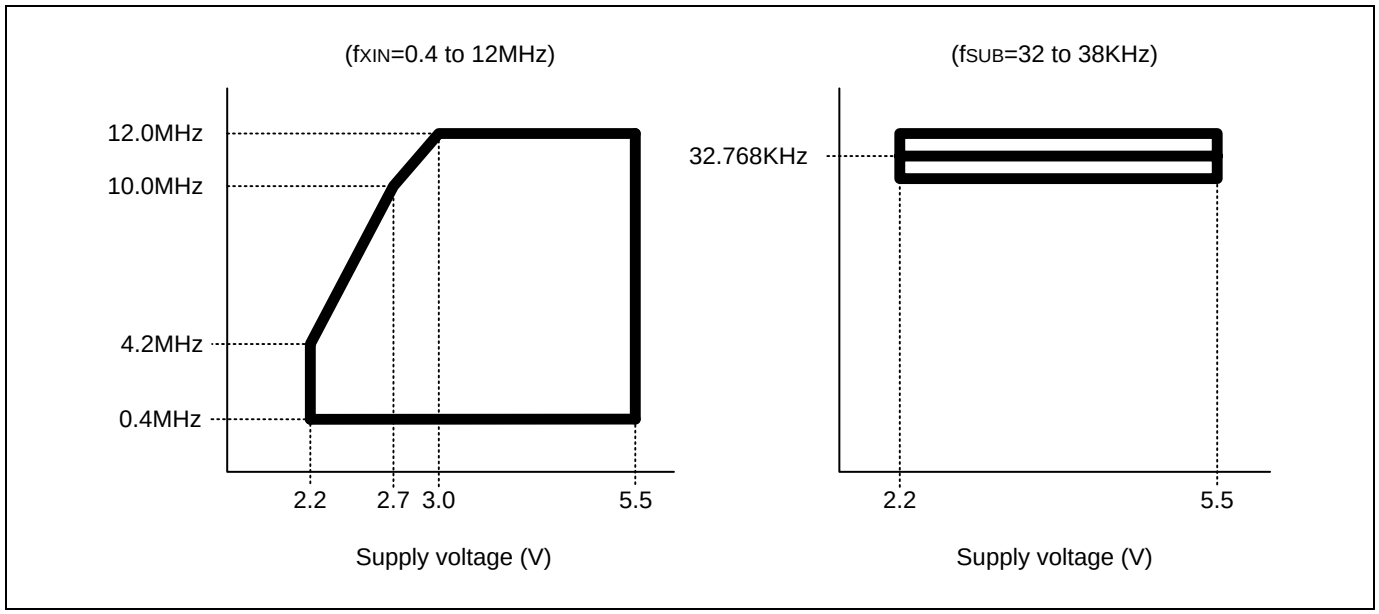


Figure 7.14 Operating Voltage Range

7.21 Recommended Circuit and Layout

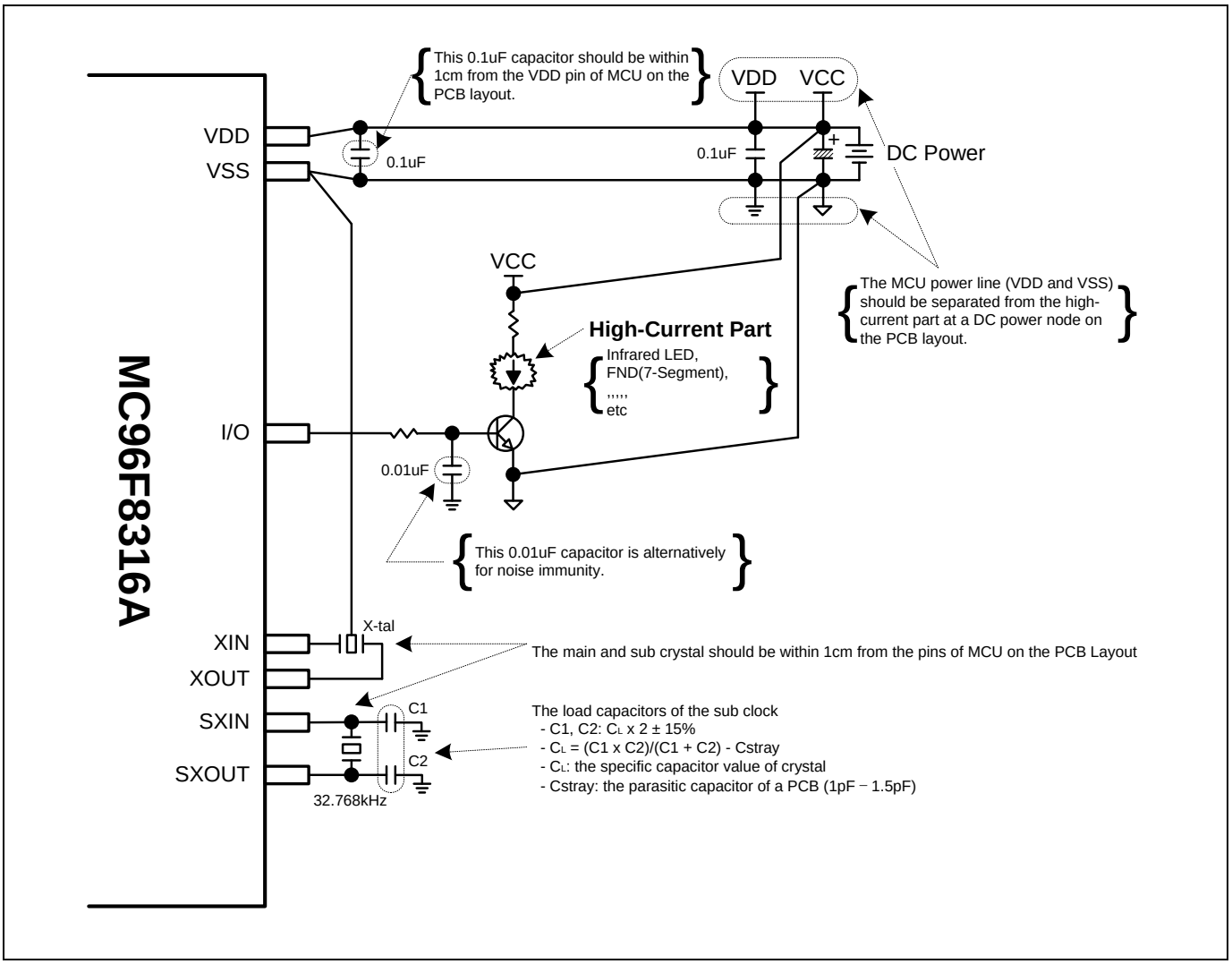
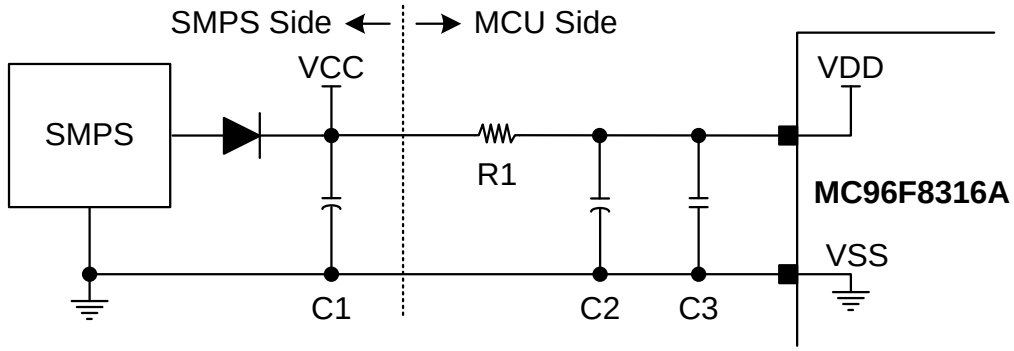


Figure 7.15 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.16 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

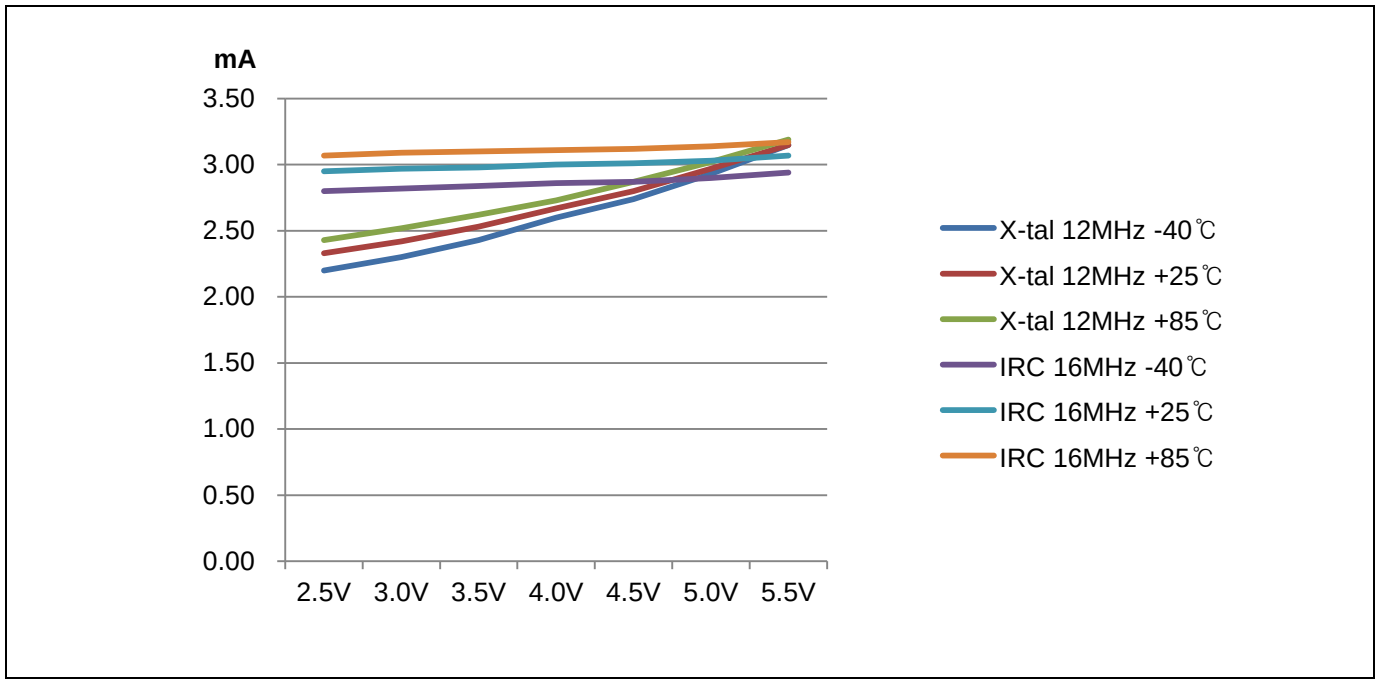


Figure 7.17 RUN (IDD1) Current

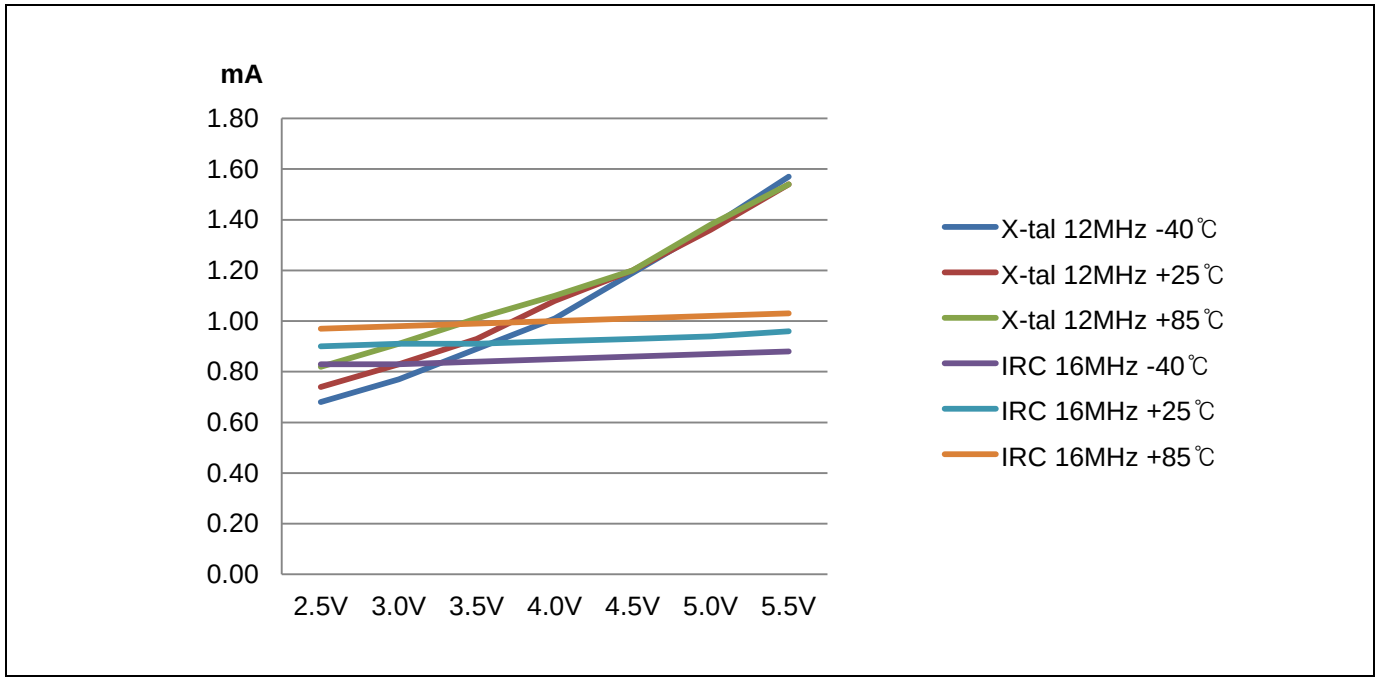


Figure 7.18 IDLE (IDD2) Current

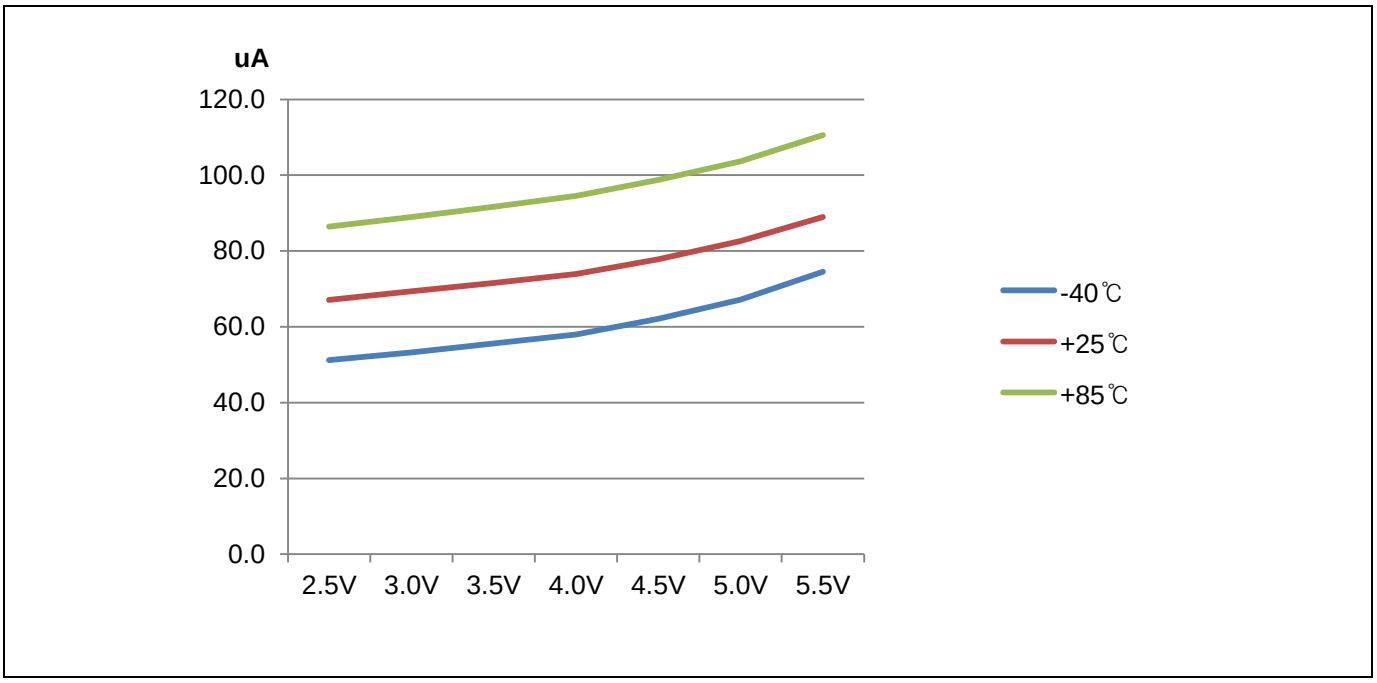


Figure 7.19 SUB RUN (IDD3) Current

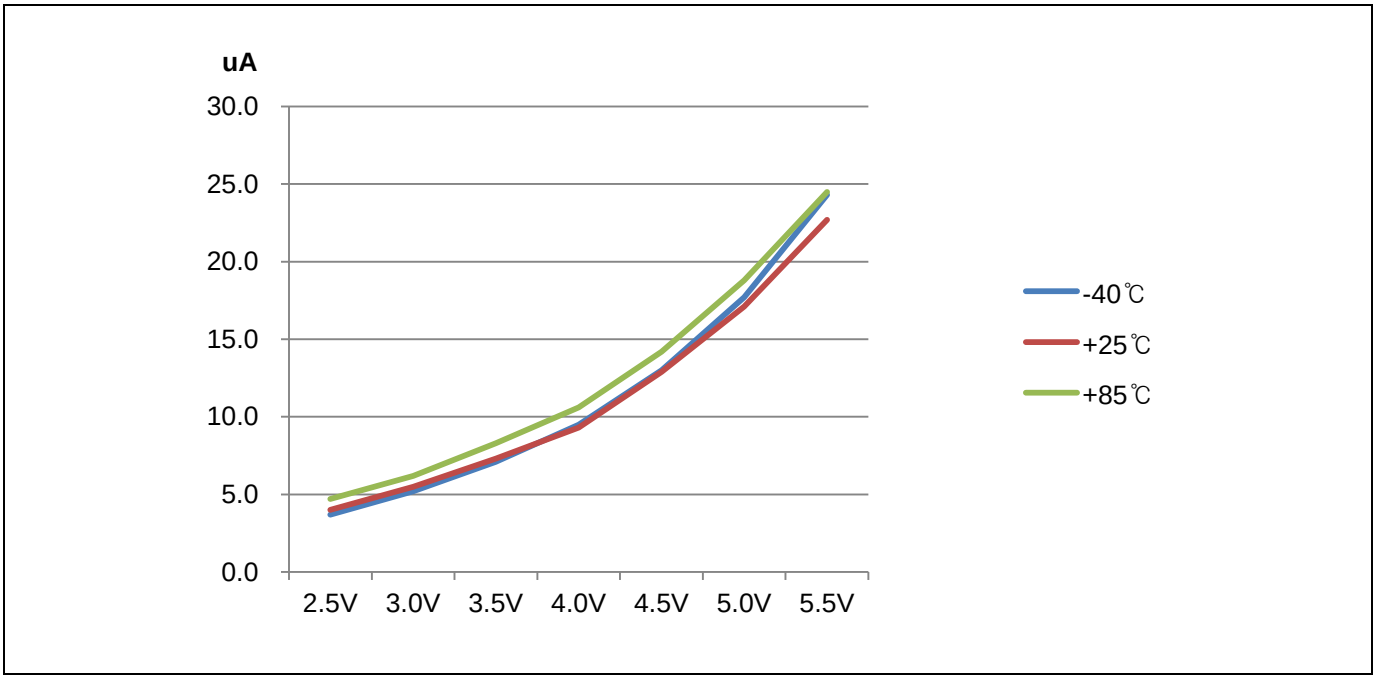


Figure 7.20 SUB IDLE (IDD4) Current

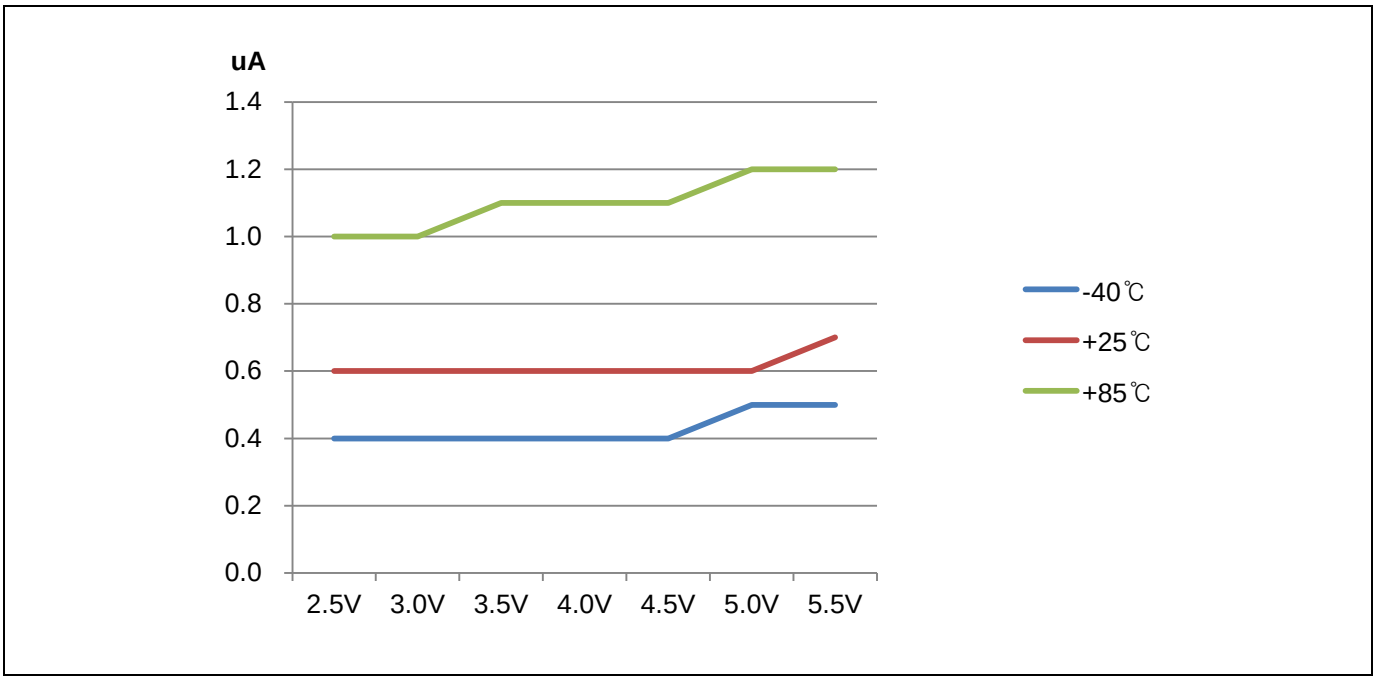


Figure 7.21 STOP (IDD5) Current

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