ABOV SEMICONDUCTOR Co., Ltd.
8-BIT MICROCONTROLLERS

MC96P6608/P6408

User's Manual (Ver. 1.4)

REVISION HISTORY

VERSION 0.0 (September 27, 2010)

VERSION 1.0 (June 20, 2011)

VERSION 1.1 (July 18, 2011)

Added the MC96P6408L-EVA.

VERSION 1.2 (November 23, 2011)

Modified the MC96P6408L and MC96P6408L-EVA pin assignment.

Modified the WDTCR.1 bit name.

Add ‘Instructions on how to use the input port’ descriptions.

VERSION 1.3 (November 13, 2012)

Add a note at ‘TIFR’ Register description’

VERSION 1.4(April 21, 2015) This book

Add a note at P0, P1, P2, P3, P4, P5, P6, P6, KFLAG register description and SFR map.

Change Figure 10.8 and 10.8 in Interrupt.

Version 1.4
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MC96P6608/P6408

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

1. Overview

1.1 Description

The MC96P6608/P6408 is advanced CMOS 8-bit microcontroller with 8k bytes of OTP. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 8k bytes of OTP, 256 bytes of IRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, carrier generation, watch timer, buzzer driving port, SIO, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96P6608/P6408 also supports power saving modes to reduce power consumption.

Device Name	OTP	IRAM	I/O PORT	Package
MC96P6608	8k bytes	256 bytes	59	64 LQFP
MC96P6408			44	48 LQFP

1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible)
- **ROM Capacity**
  - 8k Bytes
- **256 Bytes IRAM**
  - (32 Bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 20 Ports
    (P0[7:0], P1[7:0], P70, P71, P73, P74)
  - Input only : 1 Port
    (P72)
  - LCD shared I/O : 38 Ports
    (P2[7:0], P3[7:0], P4[7:0], P5[7:0], P6[5:0])
- **Basic Interval Timer (BIT)**
  - 8Bit × 1ch
  - **Watch Dog Timer (WDT)**
  - 8Bit × 1ch
  - 60kHz internal RC oscillator
- **Timer / Counter**
  - 8Bit × 4ch (T0/T1/T2/T3), 16Bit x 2ch (T0/T2)
- **Carrier Generation**
  - Carrier Generation (by T1), T2 Clock source
- **Watch Timer (WT)**
  - 3.91mS/0.25S/0.5S/1S interval at 32.768kHz
- **Buzzer**
  - 8Bit × 1ch
- **SIO**
  - 8Bit × 1ch
- **LCD Driver**
  - 26 Segments and 8 Common terminals
  - Internal or external resistor bias
  - 2, 3, 4, 5, 6 and 8 common selectable
  - Bias selectable (1/2, 1/3, 1/4)
- **Power On Reset**
  - Reset release level (2.05V)
- **Low Voltage Reset**
  - 4 level detect (2.4V/ 2.7V/ 3.0V/ 3.9V)
- **Low Voltage Indicator**
  - 4 level detect (2.4V/ 2.8V/ 3.2V/ 3.9V)
- **Interrupt Sources**
  - External Interrupts
    (EINT10, EINT12) (2)
  - Key Interrupts (8)
  - Timer (0/1/2/3) (4)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SIO (1)
- **Internal RC Oscillator**
  - Internal RC frequency: 8MHz ± 20%
    (T_A= -10°C ~ +70°C, V_{DD}=4.5V ~ 5.5V)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V ~ 5.5V (@1.0 ~ 4.2MHz)
  - 2.7V ~ 5.5V (@1.0 ~ 6.0MHz)
  - 3.5V ~ 5.5V (@1.0 ~ 8.0MHz)
  - 4.0V ~ 5.5V (@1.0 ~ 10.0MHz)
  - 4.5V ~ 5.5V (@1.0 ~ 12.0MHz)
- **Minimum Instruction Execution Time**
  - 167nS (@ 12MHz main clock)
  - 61μS (@ 32.768kHz sub clock)
- **Operating Temperature:** – 40 ~ + 85℃
- **Oscillator Type**
  - 1.0-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
  - Frequency Locked Loop (Max. 19.98MHz)
- **Package Type**
  - 64 LQFP-1010
  - 48 LQFP-0707
  - Pellet

1.3 Ordering Information

Table 1-1 Ordering Information of MC96P6608/P6408

Device name	ROM size	IRAM size	Package
MC96P6608L	8k bytes OTP	256 bytes	64 LQFP
MC96P6408L	8k bytes OTP	256 bytes	48 LQFP

1.4 Development Tools

1.4.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96P6608/P6408 are Mentor 8051. And, device ROM size is smaller than 8k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.4.2 OCD emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- SCLK (MC96P6608L-EVA pin 5), (MC96P6408L-EVA pin 4)
- SDATA (MC96P6608L-EVA pin 6), (MC96P6408L-EVA pin 5)

OCD connector diagram: Connect OCD with user system

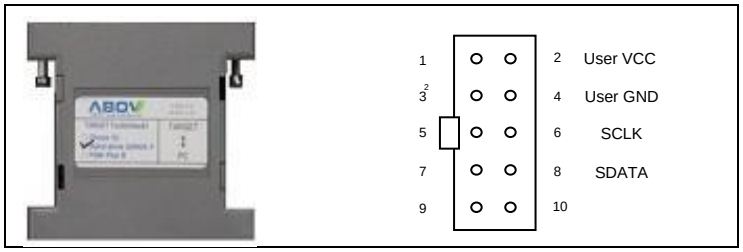


Figure 1.1 OCD Debugger and Pin Description

NOTE) When OCD(On Chip Debug) mode, the OCD interface is detached to user's system if the POR is changed disable to enable during the LVR is selected as disable by configure option.

1.4.3 Programmer

Single programmer:

PGMplus USB: It programs MCU device directly.

Figure 1.2 PGMplusUSB (Single Writer)

StandAlone PGMplus: It programs MCU device directly.

Figure 1.3 StandAlone PGMplus (Single Writer)

OCD emulator: It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer:

It programs 8 MCU devices at once.

So, it is mainly used in mass production line.

Gang programmer is standalone type, it means it does not require host PC, after a program is downloaded from host PC to Gang programmer.

Figure 1.4 StandAlone Gang8 (for Mass Production)

1.5 OTP Programming

1.5.1 Overview

The program memory of MC96P6608/P6408 are OTP Type. This EPROM is accessed by serial data format. There are five pins(SCLK, SDAT, VPP, VDD, VSS) for programming/reading the EPROM.

Table 1-2 Discriptions of Pins used to Programming/Reading the EPROM

Pin name	Pin number	During programming		Main chip pin name
		I/O	Description	
SCLK	5 (4)	I	Serial clock pin. Input only pin.	SCLK
SDAT	6 (5)	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as a input/push-pull output port.	SDAT
VPP	11 (10)	I	Power supply pin for EPROM cell programming (indicates that OTP enters into the programming mode). This pin is always applied with +11.5 V.	P72/RESETB
VDD, VSS	7, 8 (6, 7)	-	Logic power supply pin. VDD should be tied to +5 V during programming.	VDD, VSS

NOTE) Parentheses indicate pin number for 48-LQFP-0707 package.

1.5.2 On Board Programming

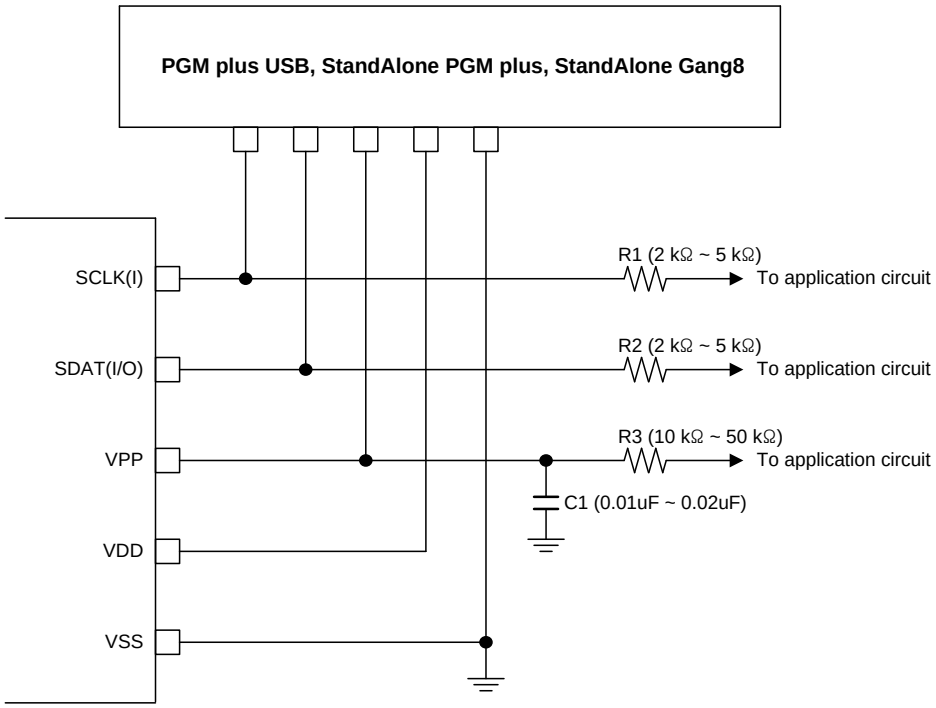
The MC96P6608/P6408 needs only five signal lines including VDD and VSS pins for programming EPROM with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.5.2.1 Circuit Design Guide

At the EPROM programming, the programming tool needs 5 signal lines that are SCLK, SDAT, VPP, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

In case of VPP pin when programming mode, a resistor should be inserted between the VPP pin and VSS. The SDAT and SCLK should be treated under the same consideration.

Please be careful to design the related circuit of these signal pins because rising/falling timing of VPP, SCLK and SDAT is very important for proper programming.



NOTES) 1. In on-board programming mode, very high-speed signal will be provided to pin SCLK and SDAT. And it will cause some damages to the application circuits connected to SCLK or SDAT port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of SDAT, SCLK pins had better be set to input mode.

2. C1 is used to improve the noise effect.

3. The value of R1~R3 and C is recommended value. It varies with circuit of system.

Figure 1.5 PCB Design Guide for On Board Programming

2. Block Diagram

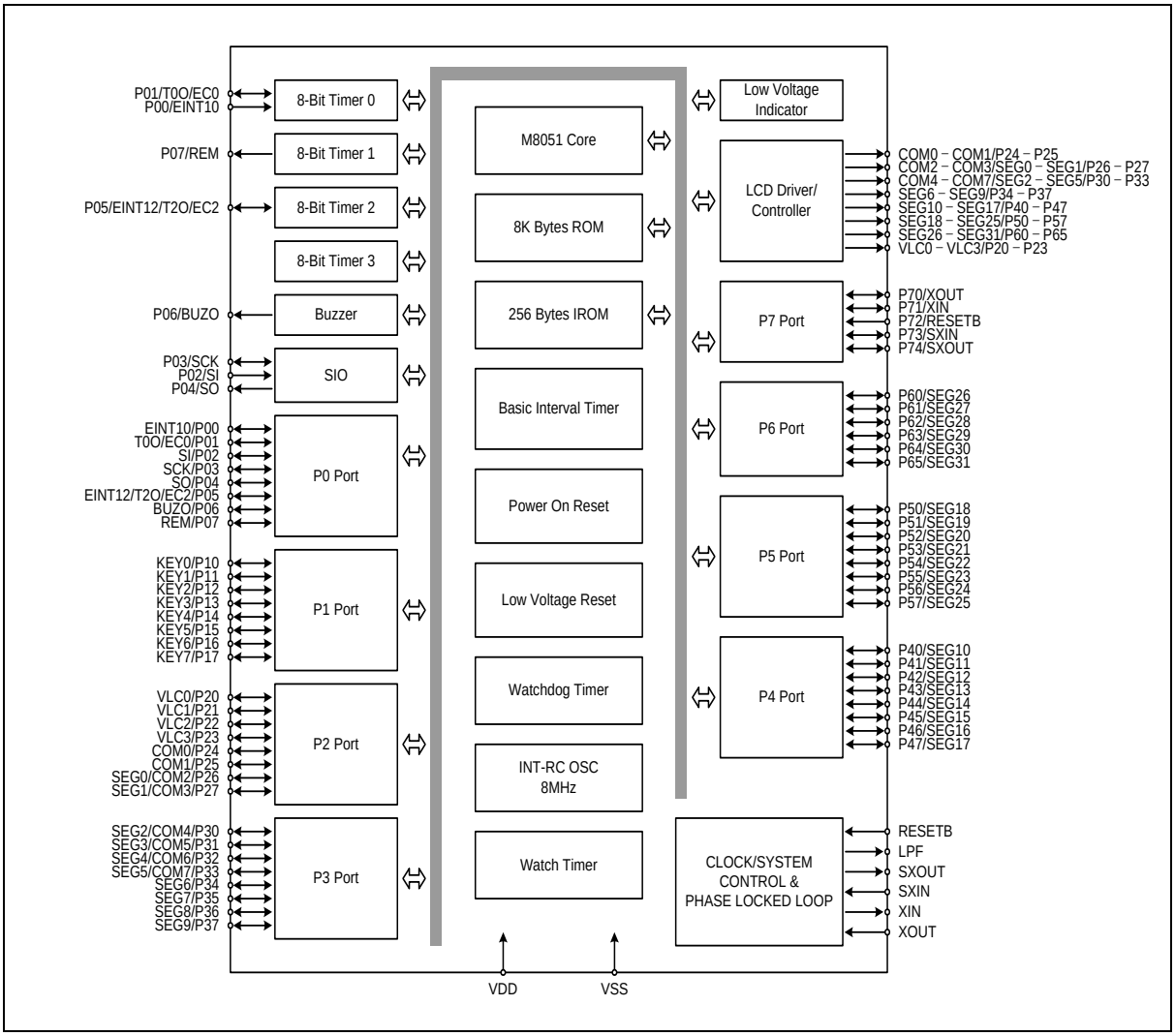


Figure 2.1 Block Diagram

3. Pin Assignment

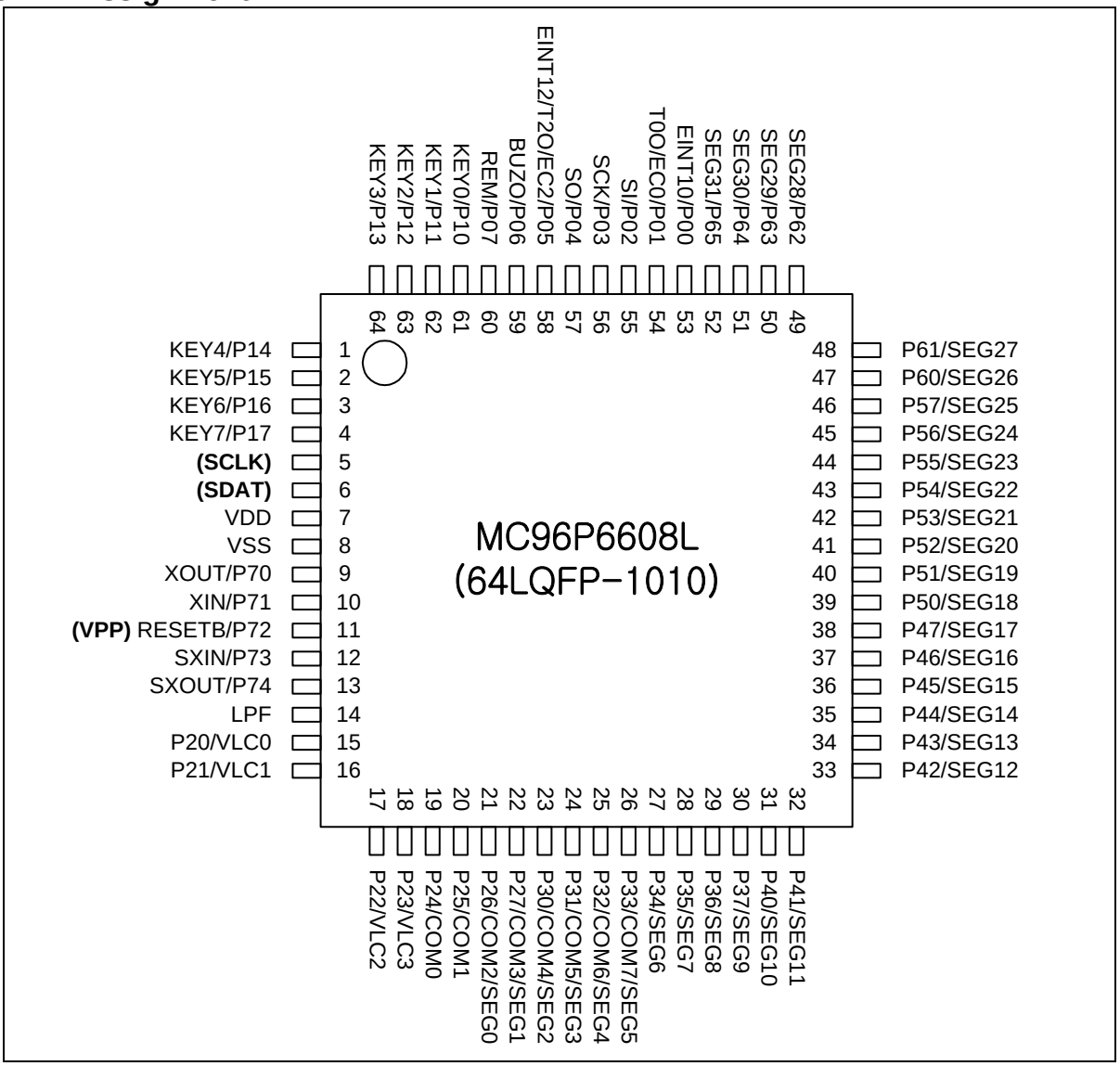


Figure 3.1 MC96P6608 64LQFP-1010 Pin Assignment

NOTES) 1. The OTP programming uses SCLK, SDAT, and RESETB/P72 pin as SCLK, SDAT, and VPP, refer to the chapter 1.5 OTP Programming.

2. There is EVA Chip(MC96P6608L-EVA) for On-Chip Debugging, refer to the chapter 14. On-chip Debug System.

3. The RESETB/P72 pin is configured as an input and P72 should be connected external pull-up or pull-down resistor when the LVR enable.

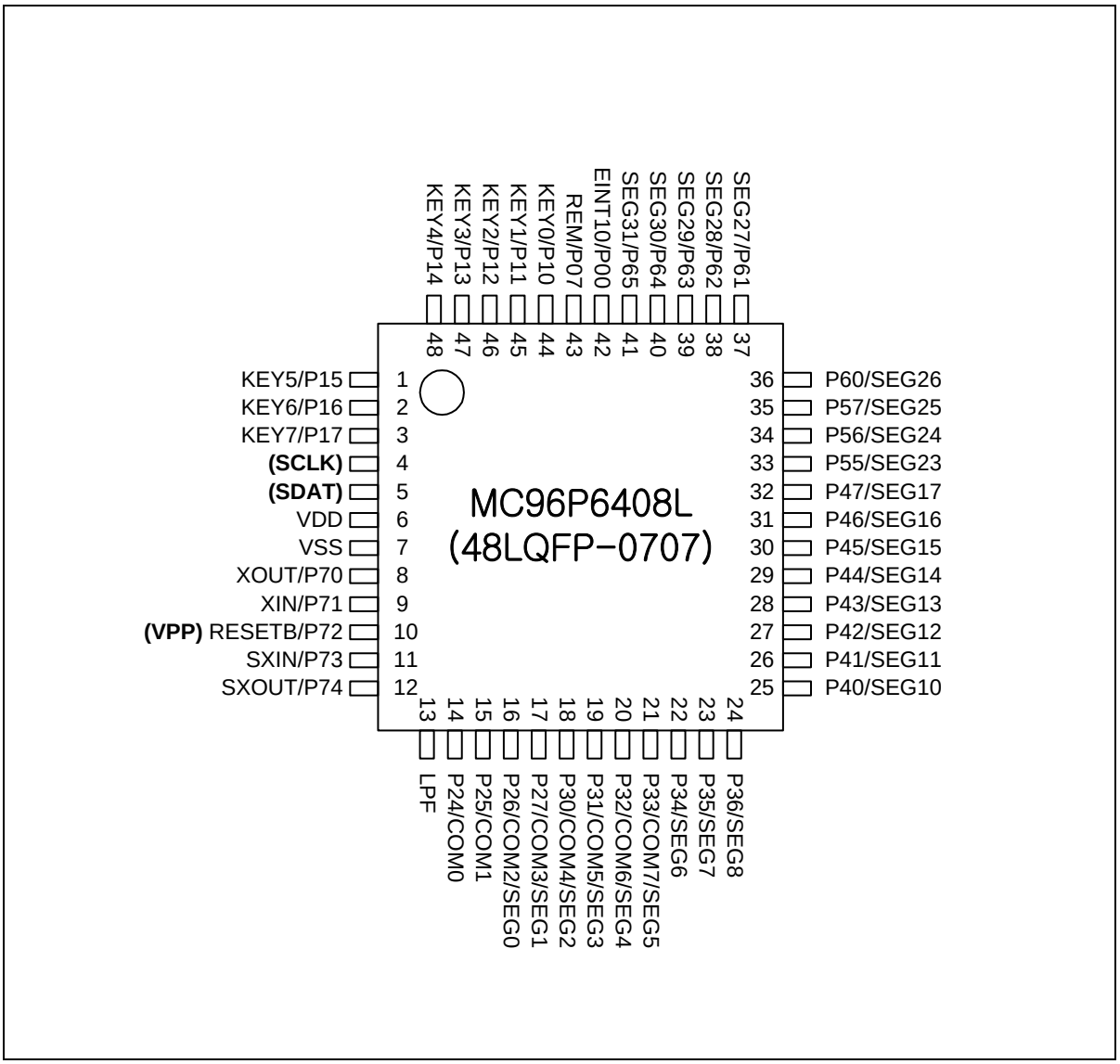


Figure 3.2 MC96P6408 48LQFP-0707 Pin Assignment

NOTES) 1. The OTP programming uses SCLK, SDAT, and RESETB/P72 pin as SCLK, SDAT, and VPP, refer to the chapter 1.5 OTP Programming.

2. There is EVA Chip(MC96P6408L-EVA) for On-Chip Debugging, refer to the chapter 14. On-chip Debug System.
3. The RESETB/P72 pin is configured as an input and P72 should be connected external pull-up or pull-down resistor when the LVR enable.
4. The P01-P06, P20-P23, P50-P54 and P37 are only in the 64-pin package.
5. The P01-P06, P20-P23, P50-P54 and P37 should be selected as push-pull or open-drain output by software control when the 48-pin packaged is used.

4. Package Diagram

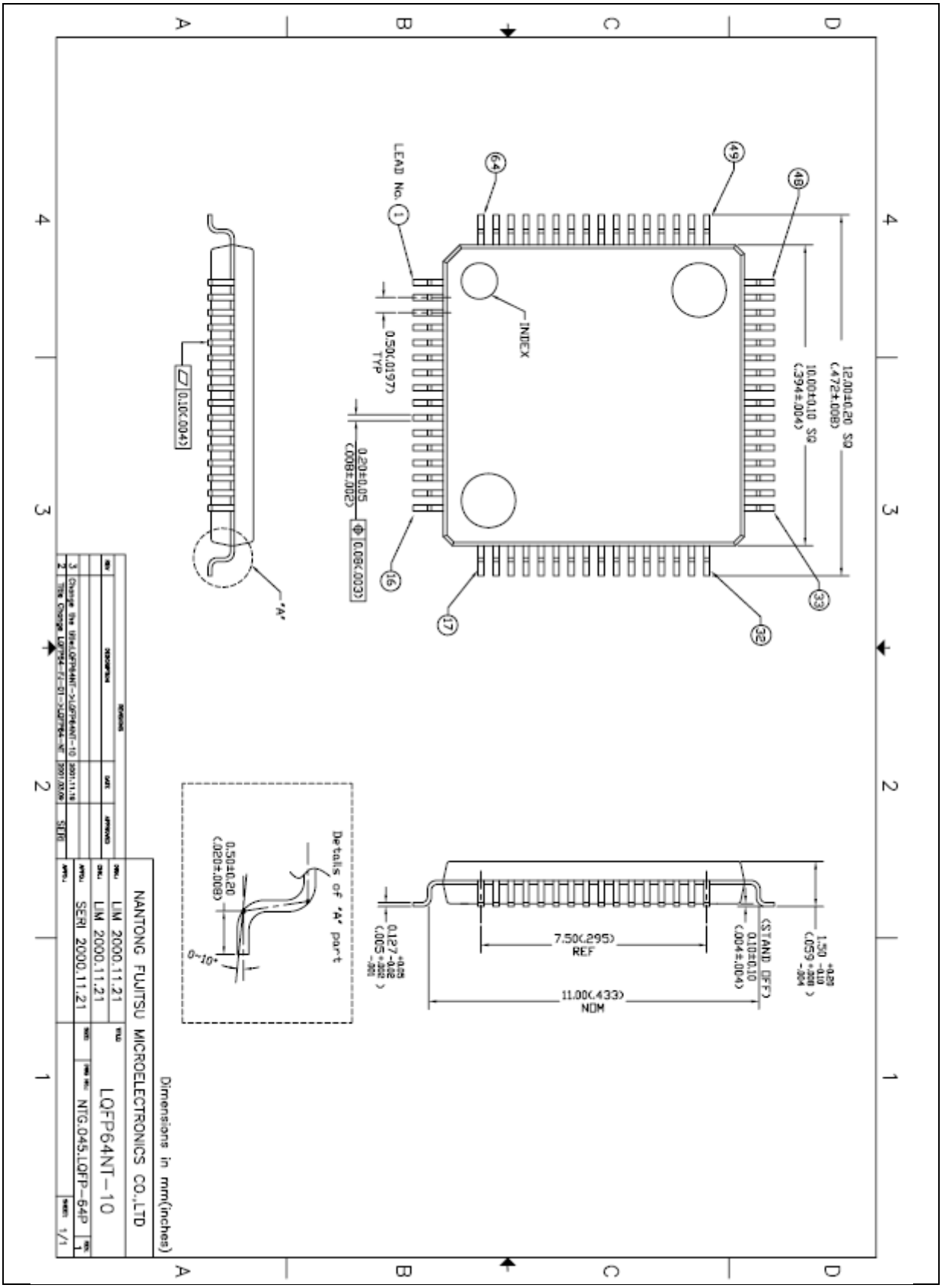
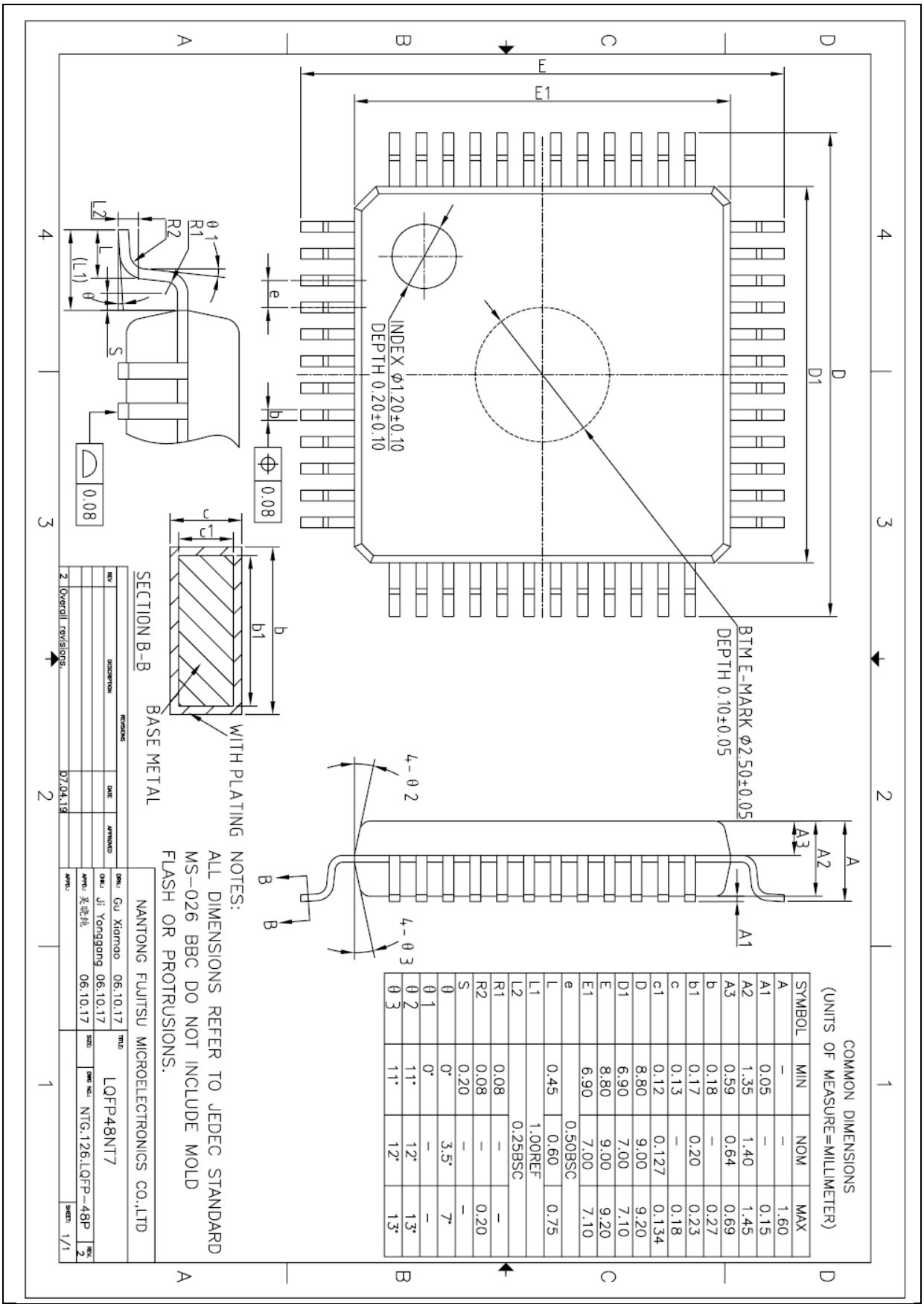


Figure 4.1 64-Pin LQFP Package



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 4.2 48-Pin LQFP Package

5. Pin Description

Table 5-1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	The P00 and P05 are a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT0
P05				EINT12/T2O/EC2
P01	I/O	The P01- P04, P06 and P07 are a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P01-P06 are only in the 64-pin package.	Input	T0O/EC0
P02				SI
P03				SCK
P04				SO
P06				BUZO
P07				REM
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	KEY0
P11				KEY1
P12				KEY2
P13				KEY3
P14				KEY4
P15				KEY5
P16				KEY6
P17				KEY7
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20-P23 are only in the 64-pin package.	Input	VLC0
P21				VLC1
P22				VLC2
P23				VLC3
P24				COM0
P25				COM1
P26				COM2/SEG0
P27				COM3/SEG1
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	COM4/SEG2
P31				COM5/SEG3
P32				COM6/SEG4
P33				COM7/SEG5
P34				SEG6
P35				SEG7
P36				SEG8
P37				SEG9

Table 5-1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG10
P41				SEG11
P42				SEG12
P43				SEG13
P44				SEG14
P45				SEG15
P46				SEG16
P47				SEG17
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P50-P54 are only in the 64-pin package.	Input	SEG18
P51				SEG19
P52				SEG20
P53				SEG21
P54				SEG22
P55				SEG23
P56				SEG24
P57				SEG25
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG26
P61				SEG27
P62				SEG28
P63				SEG29
P64				SEG30
P65				SEG31
P70	I/O	The P70 – P71 are a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT
P71				XIN
P72	I	The P72 is only schmitt-trigger input pin.	Input	RESETB
P73	I/O	The P73 – P74 are a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SXIN
P74				SXOUT
EINT10	I/O	External interrupt input/Timer 0 capture input	Input	P00
EINT12	I/O	External interrupt input/Timer 2 capture input	Input	P05/T2O/EC2
KEY0	I/O	External Key interrupt input	Input	P10
KEY1				P11
KEY2				P12
KEY3				P13
KEY4				P14
KEY5				P15
KEY6				P16
KEY7				P17
T0O	I/O	Timer 0 interval output	Input	P01/EC0
EC0	I/O	Timer 0 event count input	Input	P01/T0O

Table 5-1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
REM	I/O	Carrier generation output	Input	P07
T2O	I/O	Timer 2 interval output	Input	P05/EINT12/EC2
EC2	I/O	Timer 2 event count input	Input	P05/EINT12/T2O
BUZO	I/O	Buzzer signal output	Input	P06
SCK	I/O	Serial clock input	Input	P03
SI	I/O	Serial data input	Input	P02
SO	I/O	Serial data output	Input	P04
VLC0–VLC3	I/O	LCD bias voltage pins	Input	P20–P23
COM0–COM1	I/O	LCD common signal output	Input	P24–P25
COM2–COM7				P26/SEG0–P33/SEG5
SEG0	I/O	LCD segment signal output	Input	P26/COM2
SEG1				P27/COM3
SEG2				P30/COM4
SEG3				P31/COM5
SEG4				P32/COM6
SEG5				P33/COM7
SEG6–SEG9				P34–P37
SEG10–SEG17				P40–P47
SEG18–SEG25				P50–P57
SEG26–SEG31				P60–P65
SDAT	I/O	Serial data pin. Output port when reading and input port when writing.	Input	–
SCLK	I	Serial clock pin. Input only pin.	Input	–
RESETB	I	System reset pin. Input only pin.	Input	P72
XIN, XOUT	I/O	Main oscillator pins	Input	P70, P71
SXIN, SXOUT	I/O	Sub oscillator pins	Input	P73, P74
LPF	–	Loop filter pump output of PLL. The LPF is only in the 64-pin package.	–	–
VDD, VSS	–	Power input pins	–	–

NOTES) 1. The OTP programming uses SCLK, SDAT, and RESETB/P72 pin as SCLK, SDAT, and VPP, refer to the chapter 1.5 OTP Programming.

2. There is EVA Chip(MC96P6608L-EVA) for On-Chip Debugging, refer to the chapter 14. On-chip Debug System

3. The RESETB/P72 pin is configured as an input and P72 should be connected external pull-up or pull-down resistor when the LVR enable.

4. The P01-P06, P20-P23, P50-P54 and P37 are only in the 64-pin package.

5. The P01-P06, P20-P23, P50-P54 and P37 should be selected as push-pull or open-drain output by software control when the 48-pin packaged is used.

6. Port Structures

6.1 General Purpose I/O Port

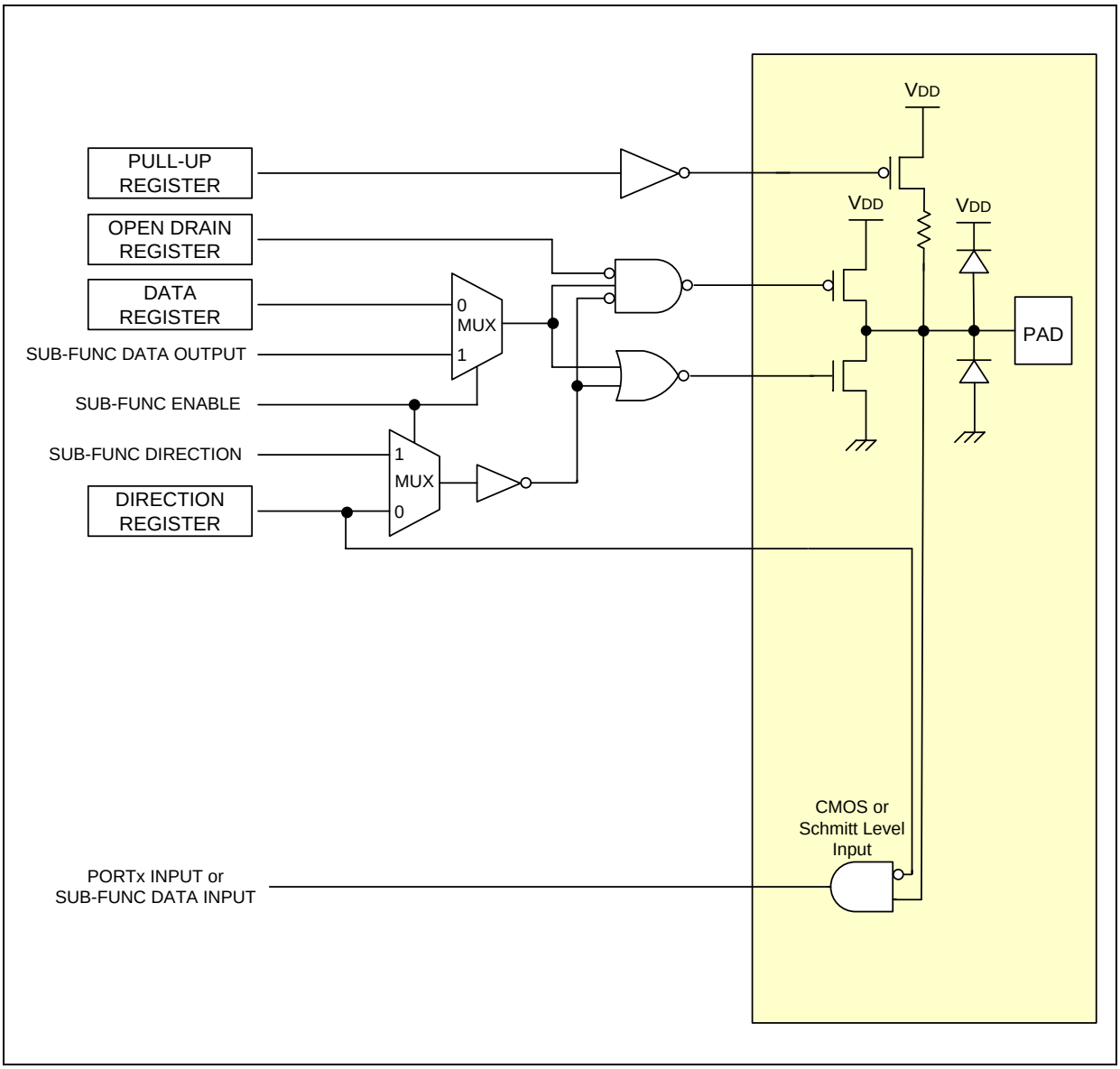


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

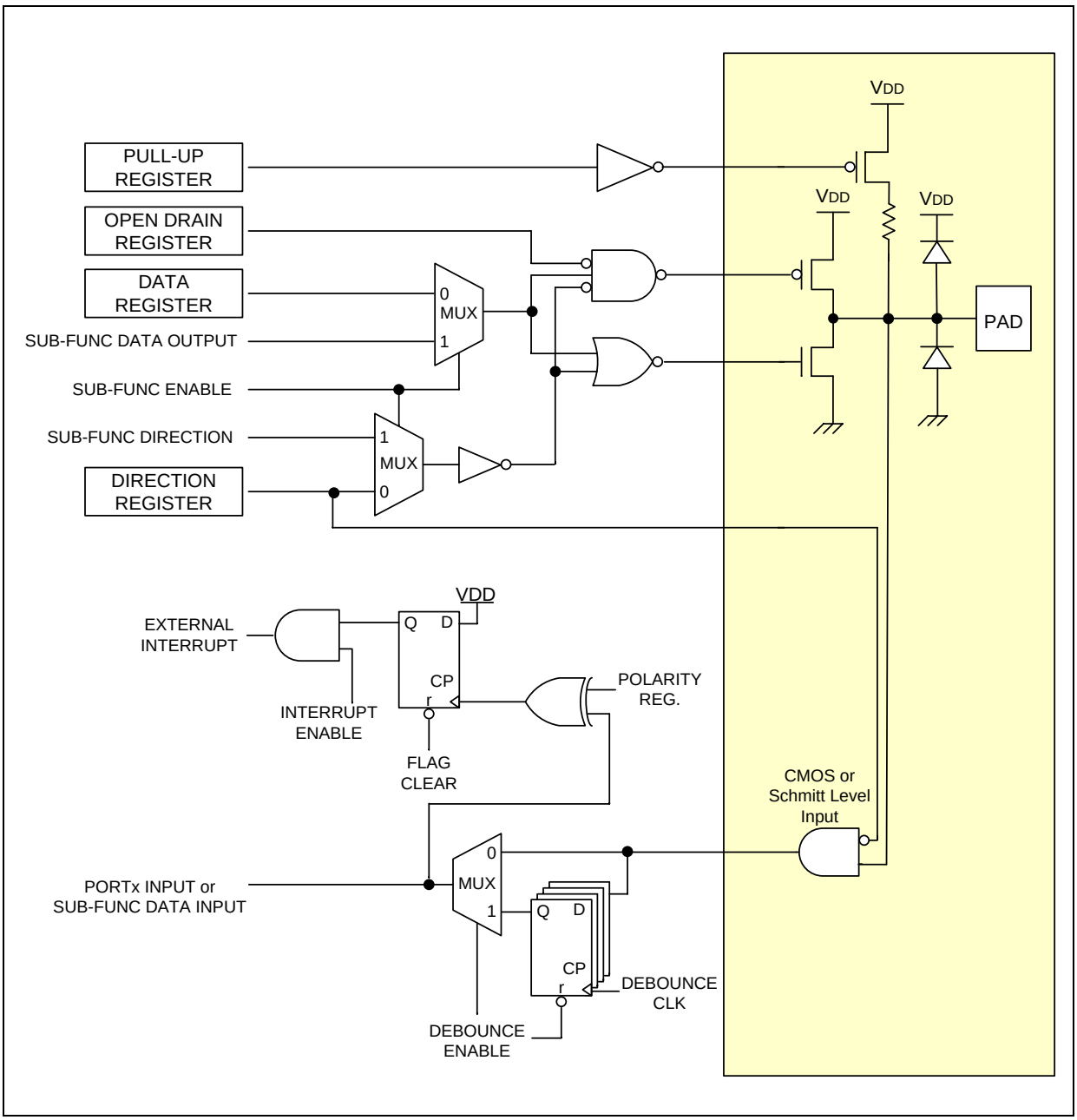


Figure 6.2 External Interrupt I/O Port

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.0	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

NOTE) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Conditions

(T_A= -40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Supply Voltage	VDD	f_X= 32 ~ 35kHz	SX-tal	2.2	–	5.5	V
		f_X= 1.0 ~ 4.2MHz	X-tal	2.2	–	5.5	
		f_X= 1.0 ~ 6.0MHz		2.7	–	5.5	
		f_X= 1.0 ~ 8.0MHz		3.5	–	5.5	
		f_X= 1.0 ~ 10.0MHz		4.0	–	5.5	
		f_X= 1.0 ~ 12.0MHz		4.5	–	5.5	
		f_X= 1.0 ~ 8.0MHz	Internal RC	2.2	–	5.5	
Operating Temperature	T_{OPR}	VDD= 2.2 ~ 5.5V		-40	–	85	°C

7.3 Power-On Reset Characteristics

Table 7-3 Power-On Reset Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	T_A= 25°C	–	2.05	–	V
VDD Voltage Rising Time	t_R	–	0.02	–	–	V/mS
POR Current	I_{POR}	T_A= 25°C	–	2.5	5.0	μA

7.4 Low Voltage Reset Characteristics

Table 7-4 LVR Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR}	T_A= 25°C		2.2	2.4	2.6	V
				2.5	2.7	2.9	
				2.7	3.0	3.3	
				3.5	3.9	4.3	
Hysteresis	△V	T_A= 25°C		-	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	μS
LVR Consumption	I_{LVR}	Enable	T_A= 25°C,	–	2.5	5.0	μA
		Disable	VDD= 5V	–	–	0.1	

7.5 Low Voltage Indicator Characteristics

Table 7-5 LVI Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVI}	T_A= 25°C		2.2	2.4	2.6	V
				2.5	2.8	3.1	
				2.9	3.2	3.5	
				3.5	3.9	4.3	
Hysteresis	△V	T_A= 25°C		–	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	μS
LVI Consumption	I_{LVI}	Enable	T_A= 25°C,	–	2.5	5.0	μA
		Disable	VDD= 5V	–	–	0.1	

7.6 Internal RC Oscillator Characteristics

Table 7-6 Internal RC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	T_A= 25°C, VDD=5.0V		–	8.0	–	MHz
Tolerance	–	T_A= 25°C, VDD=5.0V		-4	–	+4	%
		T_A = -10°C to +70°C	VDD=5.0V	-10	–	+10	
			VDD=4.5V~5.5V	-20	–	+20	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{IRCS}	T_A= 25°C		–	–	100	μS
IRC Current	I_{IRC}	Enable	VDD=5.0V	–	1.0	2.0	mA
		Disable		–	–	0.1	μA

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

Table 7-7 Internal WDTRC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	T_A = 25°C, VDD=5.0V	30	60	90	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	mS
WDTRC Current	I_{WDTRC}	Enable	–	–	10	μA
		Disable	–	–	0.1	

7.8 DC Characteristics

Table 7-8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P00, P05, P1, P70–P74		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P00, P05, P1, P70–P74		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	V
Output High Voltage	V_{OH}	All output ports; I_{OH}= -2mA, VDD= 4.5V		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	All output ports; I_{OL}= 15mA, VDD= 4.5V		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	µA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	µA
Pull-Up Resistor	R_{PU}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		350	700	1500	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25 °C ,VDD=5V		1800	3600	7200	
LCD Voltage Dividing Resistor	R_{LCD}	T_A= 25 °C		40	80	120	kΩ
LCD Driver Output Impedance	R_{LO}	VLCD=3V, ILOAD = ±10µA		–	5	10	kΩ
Middle Output Voltage (NOTE)	V_{LC1}	VDD= 2.7V to 5.5V, 1/4 bias LCD clock= 0Hz, VLC0=VDD		0.75VDD -0.2	0.75VDD	0.75VDD +0.2	V
	V_{LC2}			0.50VDD -0.2	0.50VDD	0.50VDD +0.2	
	V_{LC3}			0.25VDD - 0.2	0.25VDD	0.25VDD +0.2	

NOTE) It is middle output voltage when the VDD and the V_{LC0} node are connected.

Table 7-8 DC Characteristics (Continued)

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz, VDD= 5V±10%		–	13.0	20.0	mA
		f_{XIN}= 8.0MHz, VDD= 3V±10%		–	5.0	10.0	
		f_{XIN}= 4.2MHz, VDD= 3V±10%		–	3.0	6.0	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz, VDD= 5V±10%		–	5.0	10.0	mA
		f_{XIN}= 8.0MHz, VDD= 3V±10%		–	2.0	4.0	
		f_{XIN}= 4.2MHz, VDD= 3V±10%		–	1.0	2.0	
	I_{DD3}	f_{SUB}= 32.768kHz VDD= 3V±10% Crystal oscillator T_A= 25°C	Sub RUN	–	30.0	60.0	µA
	I_{DD4}		Sub IDLE	–	14.0	24.0	µA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	5.0	µA

.

7.9 Serial I/O Characteristics

Table 7-9 Serial I/O Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCK cycle time	t_{KCY}	External SCK source	1,000	–	–	nS
		Internal SCK source	1,000			
SCK high, low width	t_{KH}, t_{KL}	External SCK source	500			nS
		Internal SCK source	t_{KCY}/2-50			
SI setup time to SCK high	t_{SIK}	External SCK source	250			nS
		Internal SCK source	250			
SI hold time to SCK high	t_{KSI}	External SCK source	400			nS
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	nS
		Internal SCK source			250	
Interrupt input high, low width	t_{INTH}, t_{INTL}	All interrupt, VDD= 5V	200	–	–	nS
RESETB input low width	t_{RSL}	Input, VDD= 5V	10	–	–	μS

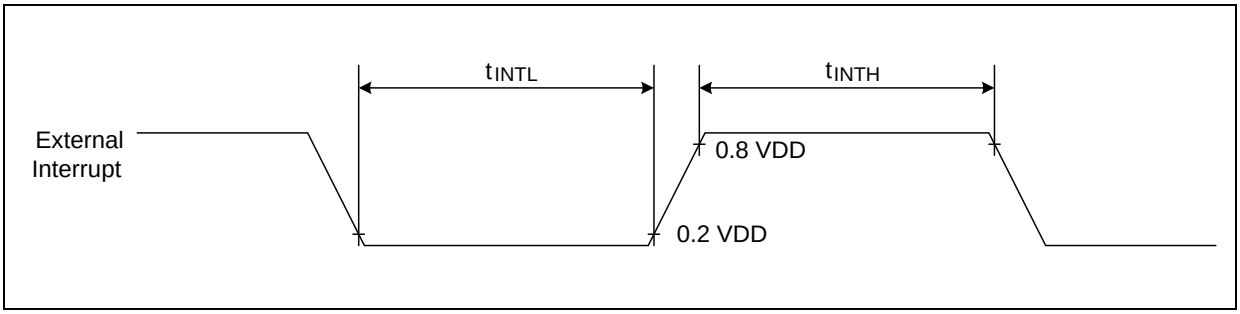


Figure 7.1 Input Timing for External Interrupts

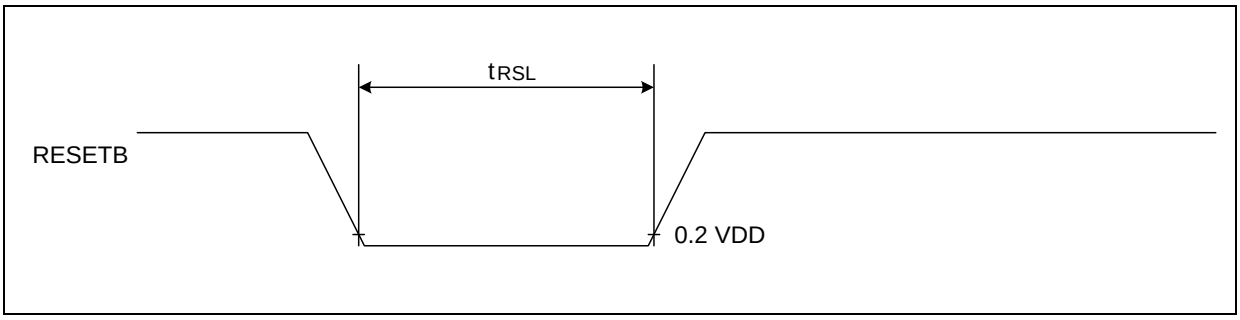


Figure 7.2 Input Timing for RESETB

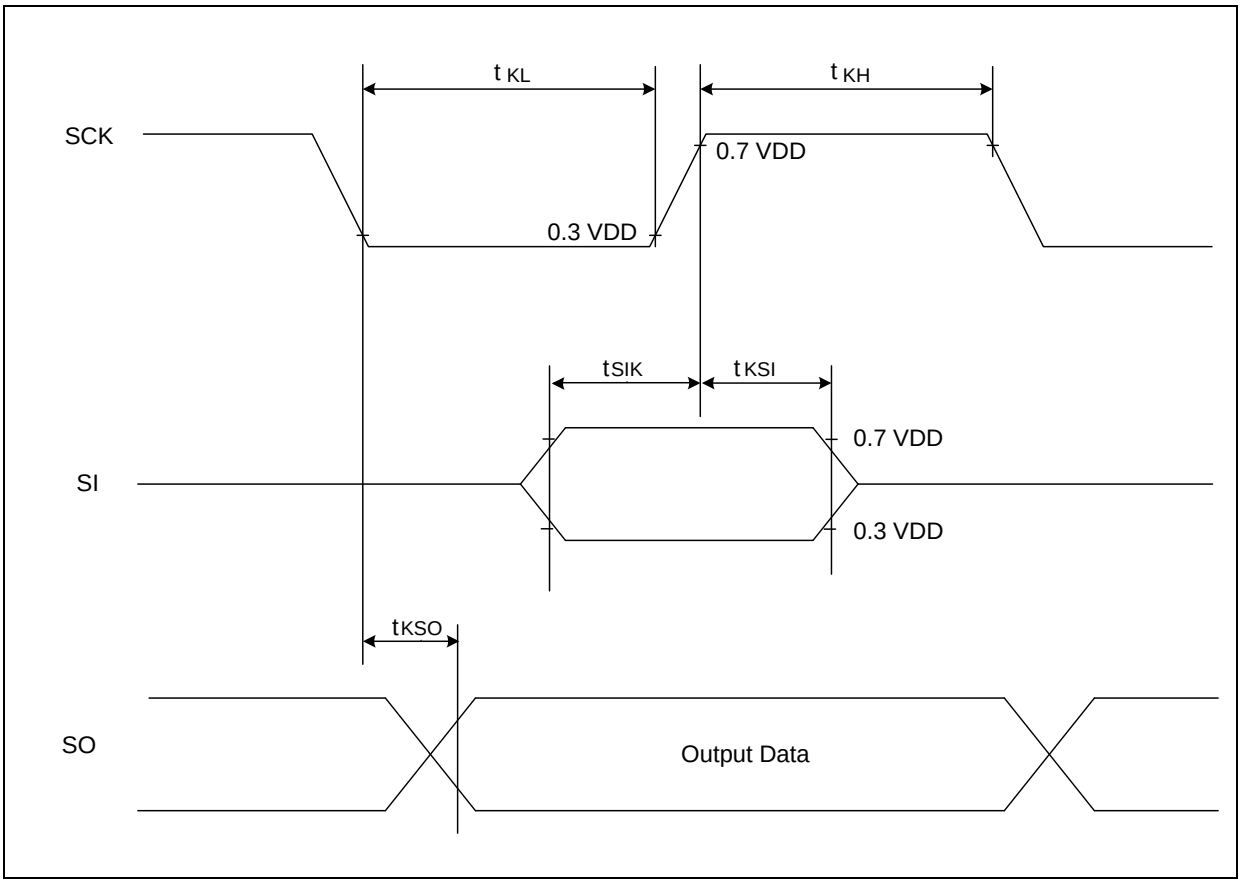


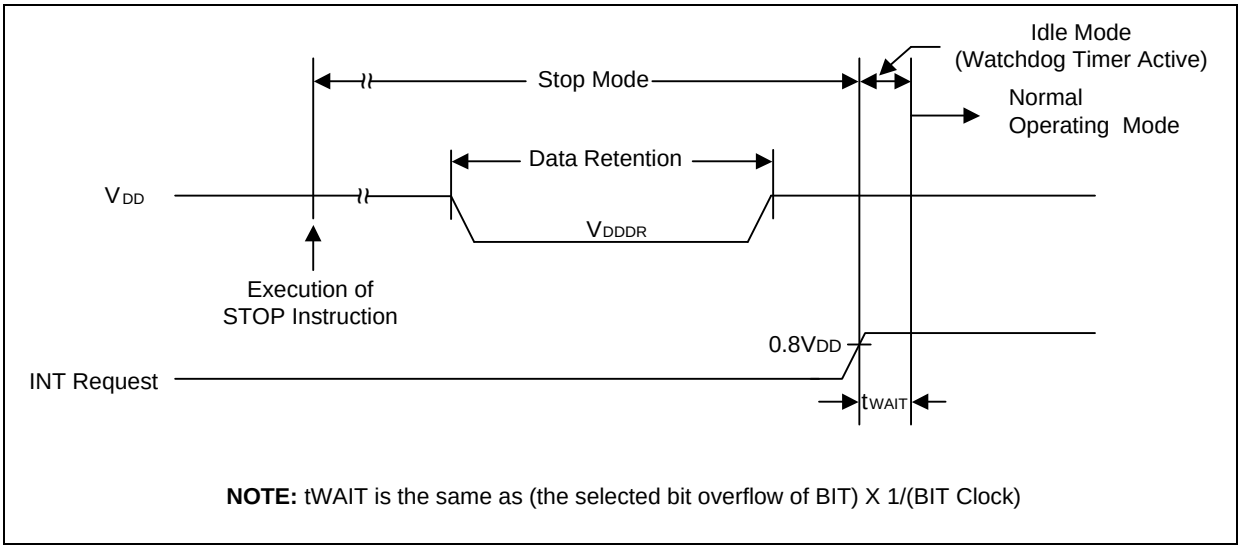
Figure 7.3 Serial Interface Data Transfer Timing

7.10 Data Retention Voltage in Stop Mode

Table 7-10 Data Retention Voltage in Stop Mode

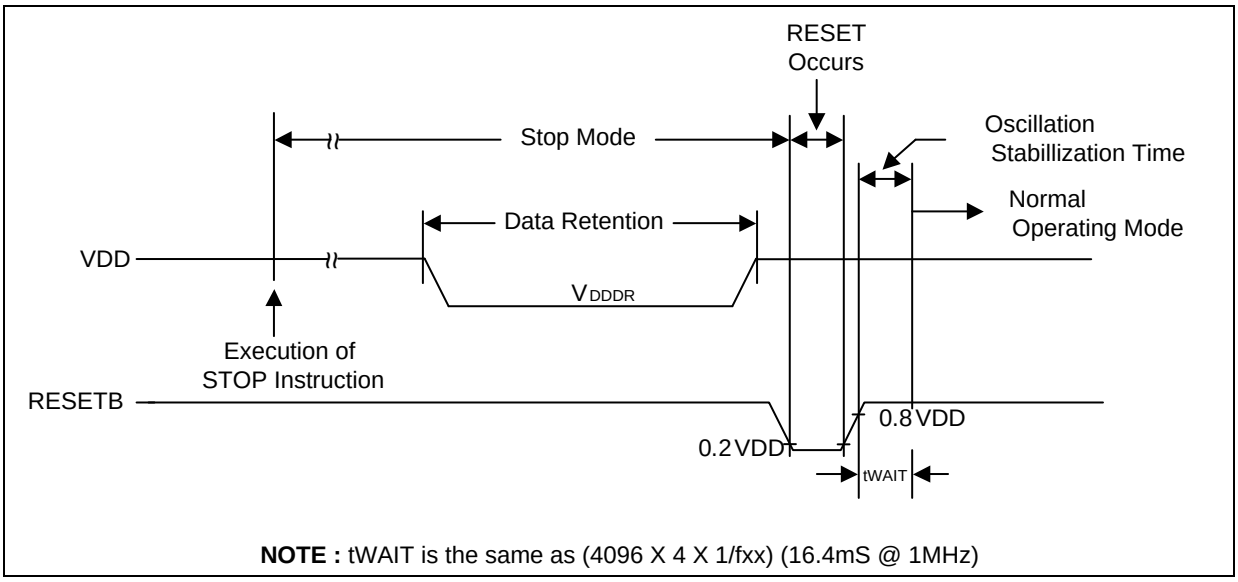
(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	VDDDR= 2.2V, (T_A= 25°C), Stop mode	–	–	1	μA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.4 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fxx) (16.4mS @ 1MHz)

Figure 7.5 Stop Mode Release Timing when Initiated by RESETB

7.11 Input/Output Capacitance

Table 7-11 Input/Output Capacitance

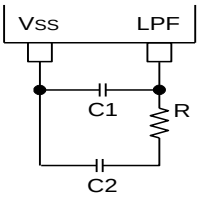
(T_A= -40°C ~ +85°C, VDD= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

7.12 Phase Locked Loop Characteristics

Table 7-12 Phase Locked Loop Characteristics

(T_A= -40°C ~ +85°C, VDD= 4.5V ~ 5.5V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
PLL Current	I_{PLL}	VDD= 5V	–	4.0	8.0	mA
Input clock frequency	f_{SUB}		–	32.768	–	kHz
Output clock frequency	f_{VCO}		11.99	–	19.98	MHz
Output Clock duty	–		40	–	60	%
Setting time	t_D		–	50	100	mS
Accuracy	–		–	2	4	%
PLL operating voltage	V_{OPR}	f_{PLL} = 11.9 MHz	4.5	–	5.5	V
		f_{PLL}= 1.49-9.99MHz	4.0	–	5.5	V

NOTE) Where R= 51kΩ, C1=6.8nF, C2= 6.8nF.

7.13 Main Clock Oscillator Characteristics

Table 7-13 Main Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.2V – 5.5V	1.0	–	4.2	MHz
		2.7V – 5.5V	1.0	–	6.0	
		3.5V – 5.5V	1.0	–	8.0	
		4.0V – 5.5V	1.0	–	10.0	
		4.5V – 5.5V	1.0	–	12.0	
Ceramic Oscillator	Main oscillation frequency	2.2V – 5.5V	1.0	–	4.2	MHz
		2.7V – 5.5V	1.0	–	6.0	
		3.5V – 5.5V	1.0	–	8.0	
		4.0V – 5.5V	1.0	–	10.0	
		4.5V – 5.5V	1.0	–	12.0	
External Clock	XIN input frequency	2.2V – 5.5V	1.0	–	4.2	MHz
		2.7V – 5.5V	1.0	–	6.0	
		3.5V – 5.5V	1.0	–	8.0	
		4.0V – 5.5V	1.0	–	10.0	
		4.5V – 5.5V	1.0	–	12.0	

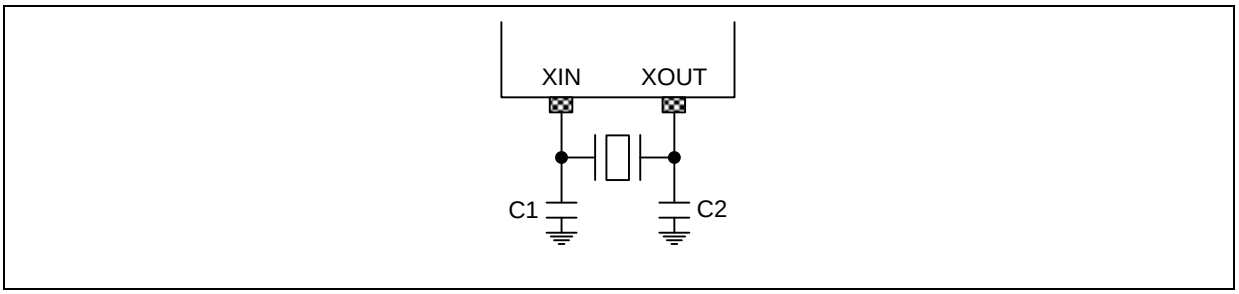


Figure 7.6 Crystal/Ceramic Oscillator

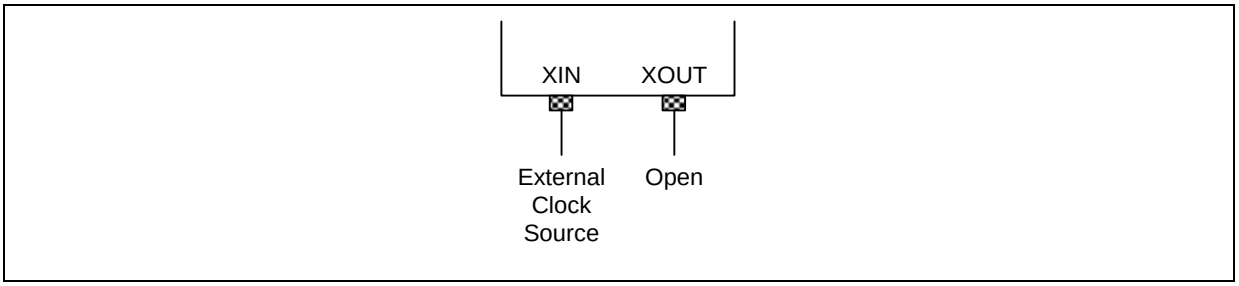


Figure 7.7 External Clock

7.14 Sub Clock Oscillator Characteristics

Table 7-14 Sub Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	2.2V – 5.5V	32	32.768	35	kHz
External Clock	SXIN input frequency		32	–	100	kHz

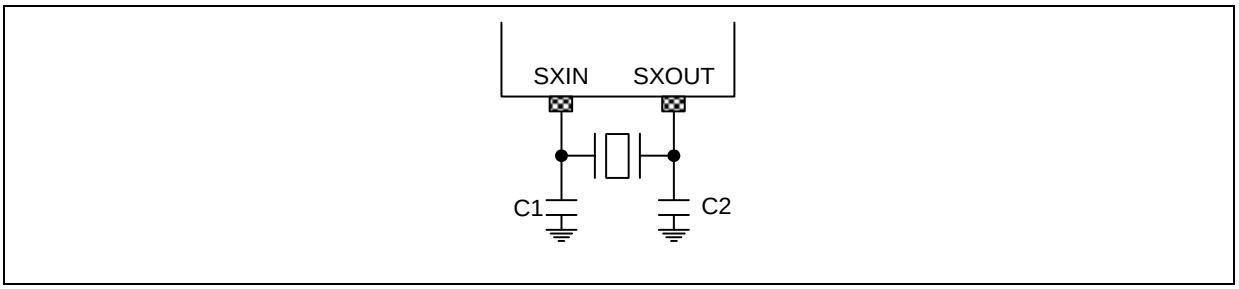


Figure 7.8 Crystal Oscillator

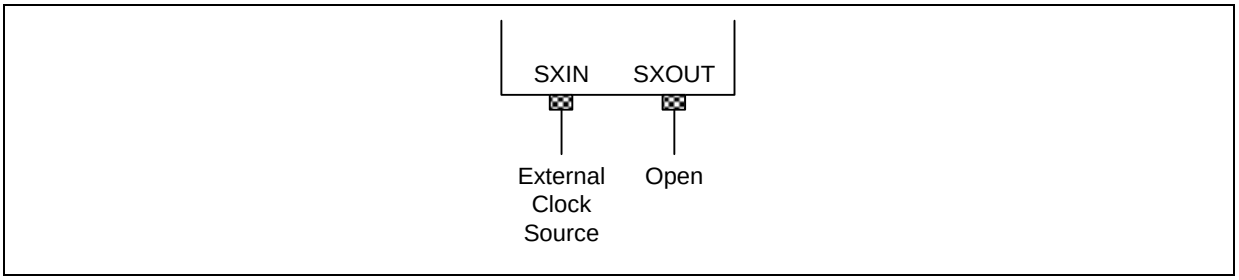


Figure 7.9 External Clock

7.15 Main Oscillation Stabilization Characteristics

Table 7-15 Main Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	mS
Ceramic		–	–	10	mS
External Clock	XIN input high and low width (t_{XH}, t_{XL})	41.6	–	500	nS

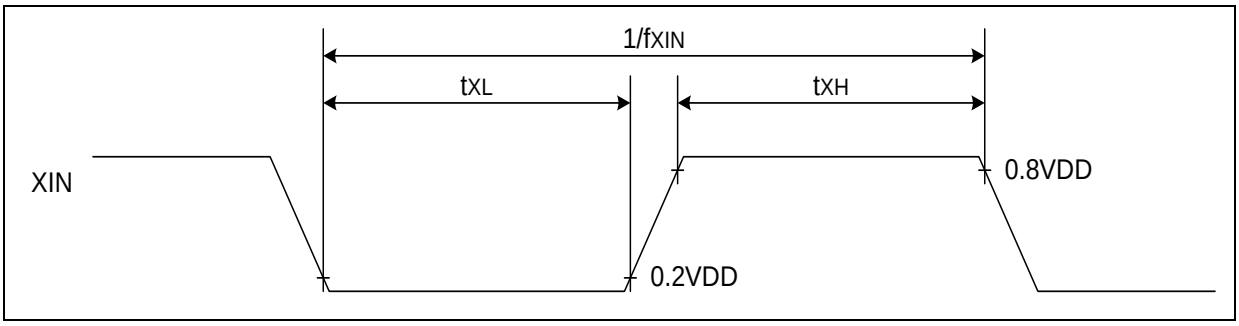


Figure 7.10 Clock Timing Measurement at XIN

7.16 Sub Oscillation Characteristics

Table 7-16 Sub Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	S
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	μS

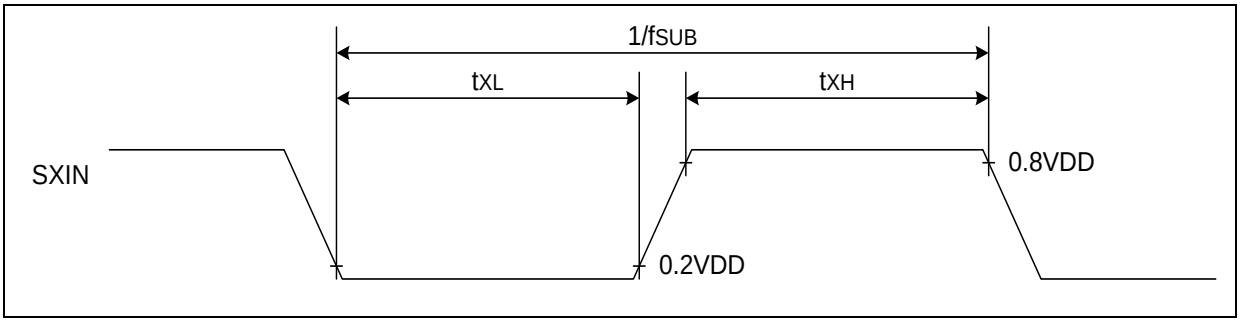


Figure 7.11 Clock Timing Measurement at SXIN

7.17 Operating Voltage Range

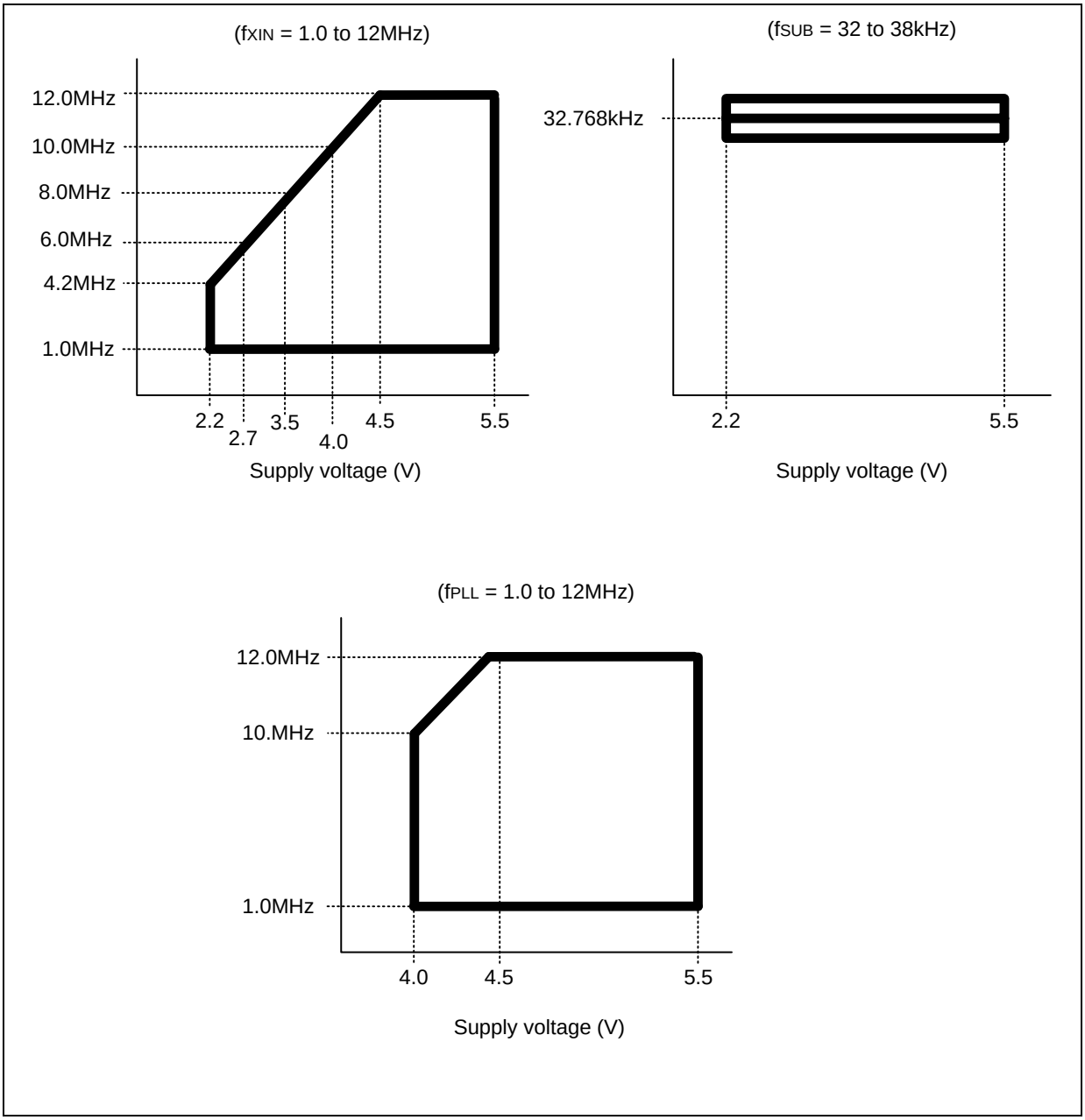


Figure 7.12 Operating Voltage Range

7.18 Recommended Circuit and Layout

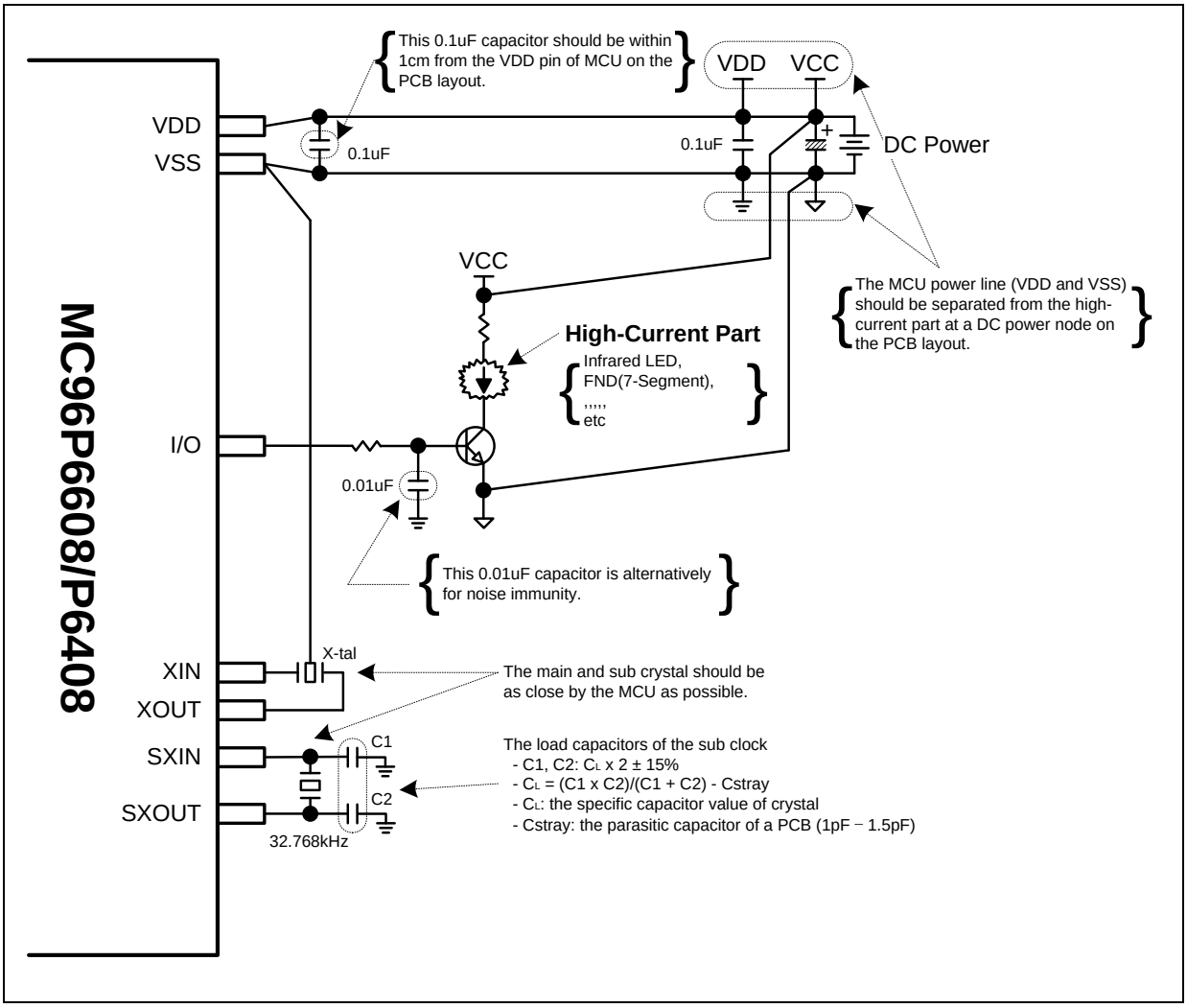


Figure 7.13 Recommended Circuit and Layout

7.19 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

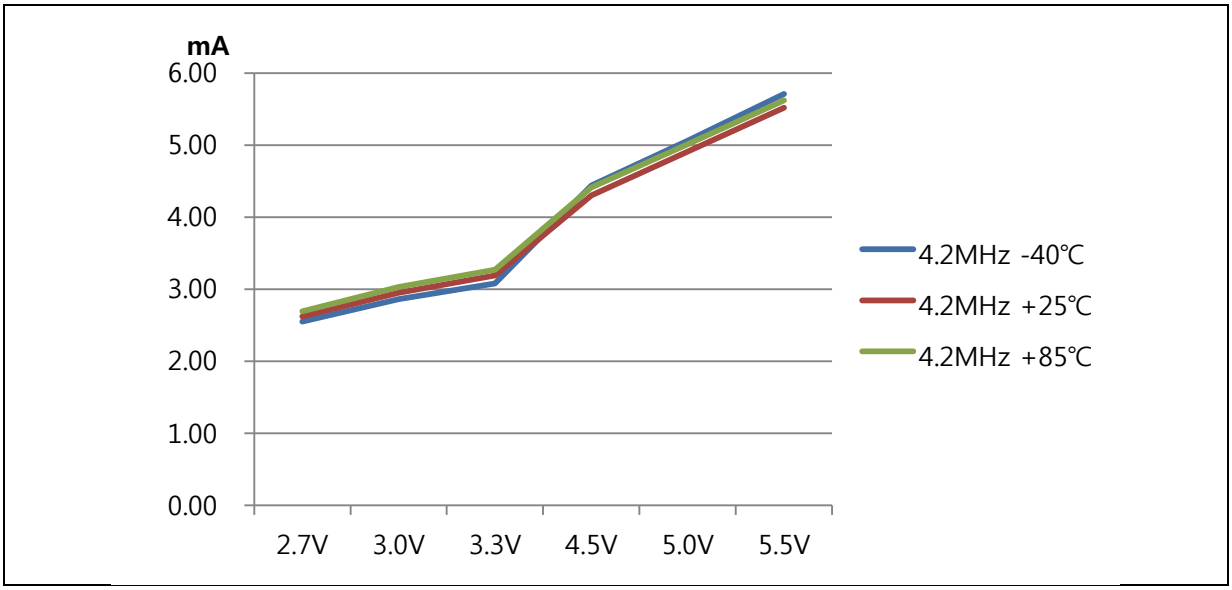


Figure 7.14 RUN (IDD1) Current

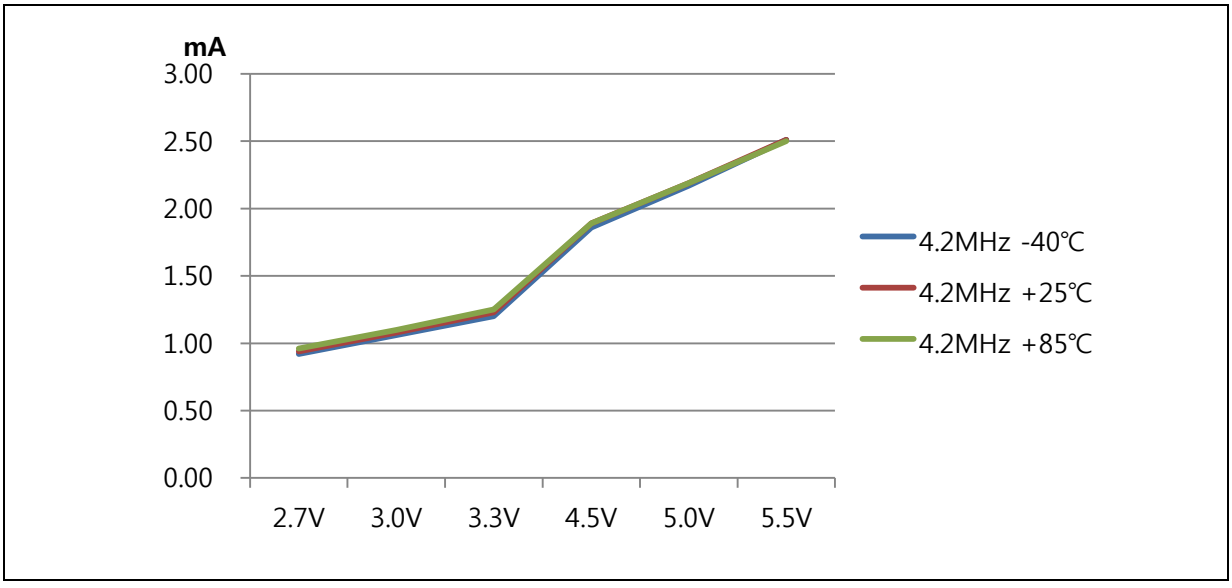


Figure 7.15 IDLE (IDD2) Current

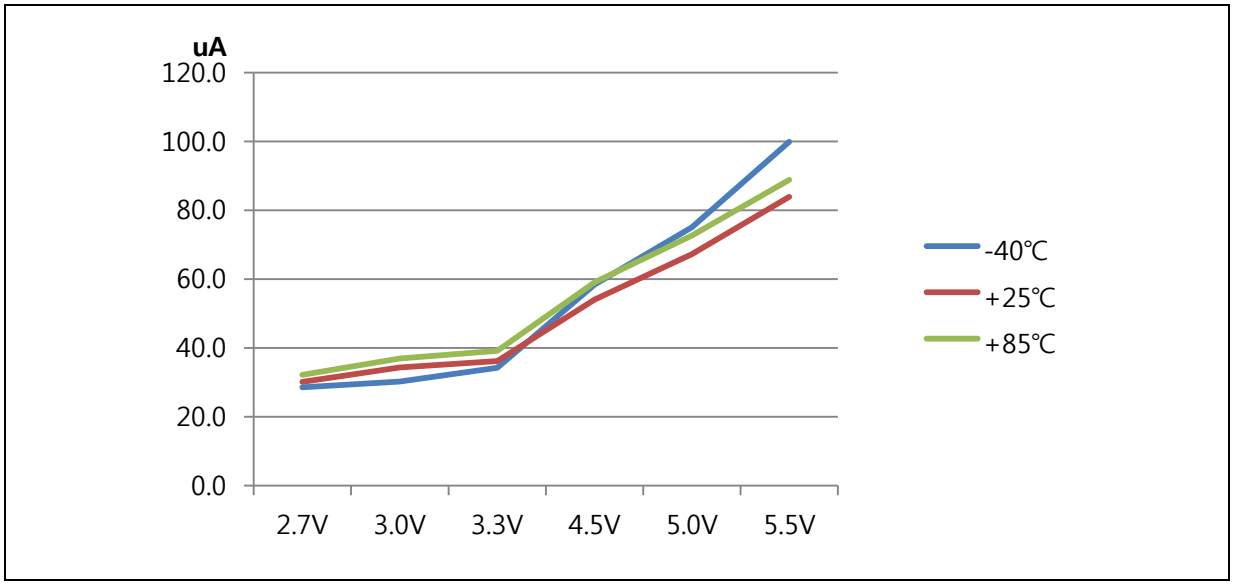


Figure 7.16 SUB RUN (IDD3) Current

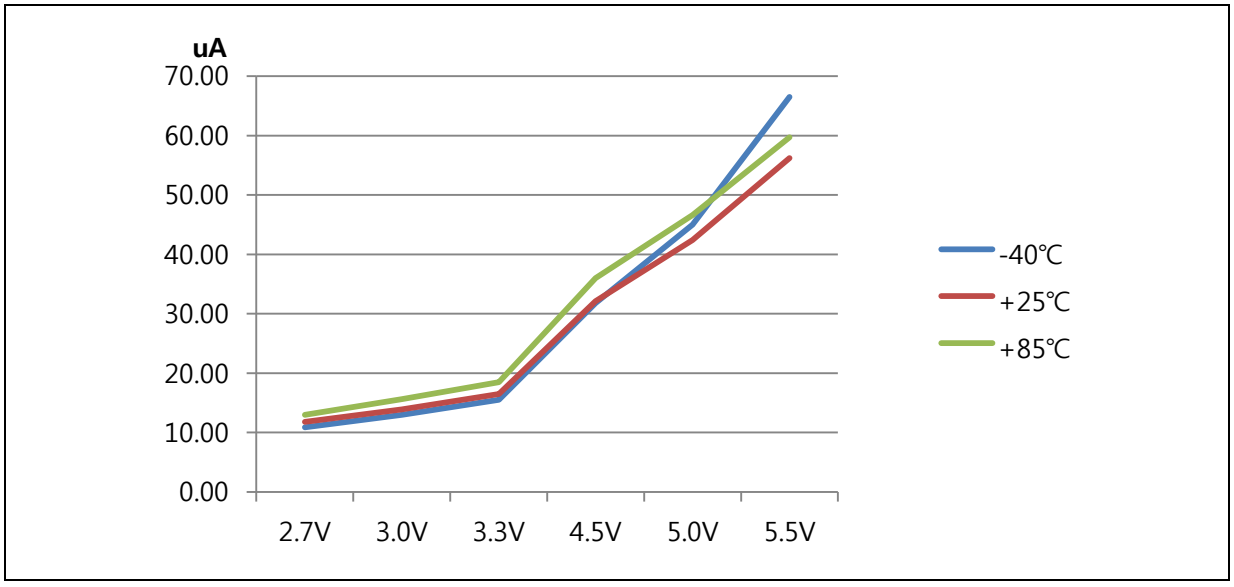


Figure 7.17 SUB IDLE (IDD4) Current

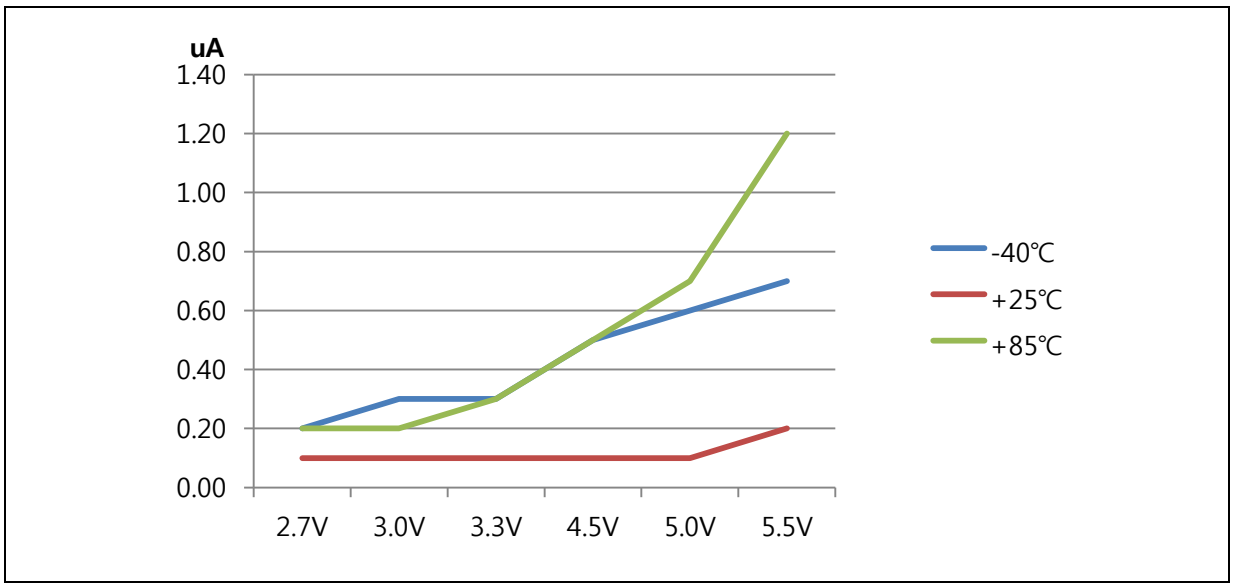


Figure 7.18 STOP (IDD5) Current

8. Memory

The MC96P6608/P6408 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

MC96P6608/P6408 provides on-chip 8k bytes of the OTP type program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes and it includes the stack area and 32 bytes of LCD display RAM.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64k bytes, but this device has just 8k bytes program memory space.

Figure 8-1 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 10, for example, is assigned to location 000BH. If external interrupt 10 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

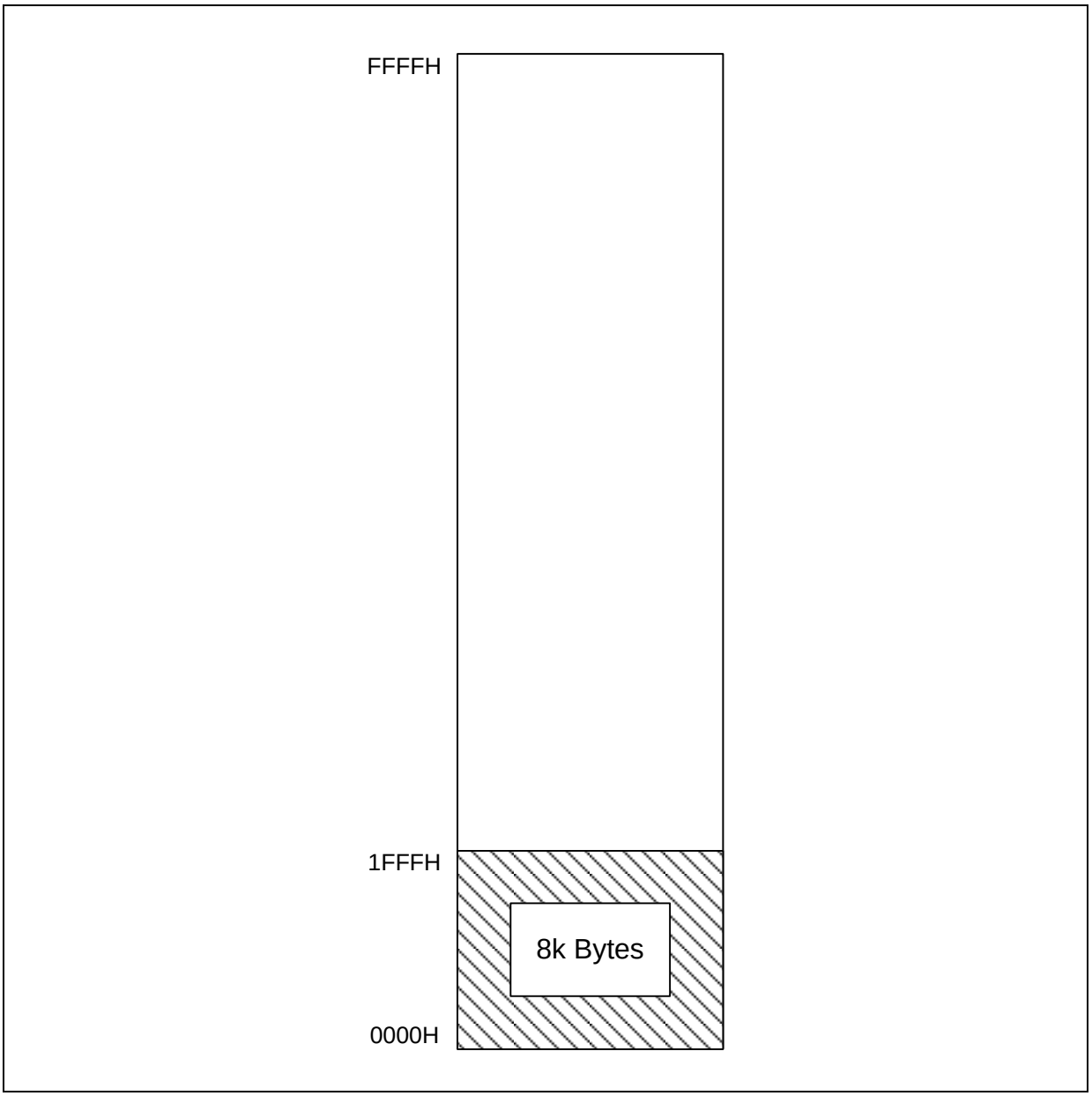


Figure 8.1 Program Memory

- 8k Bytes Including Interrupt Vector Region

8.2 Data Memory

Figure 8-2 shows the internal data memory space available.

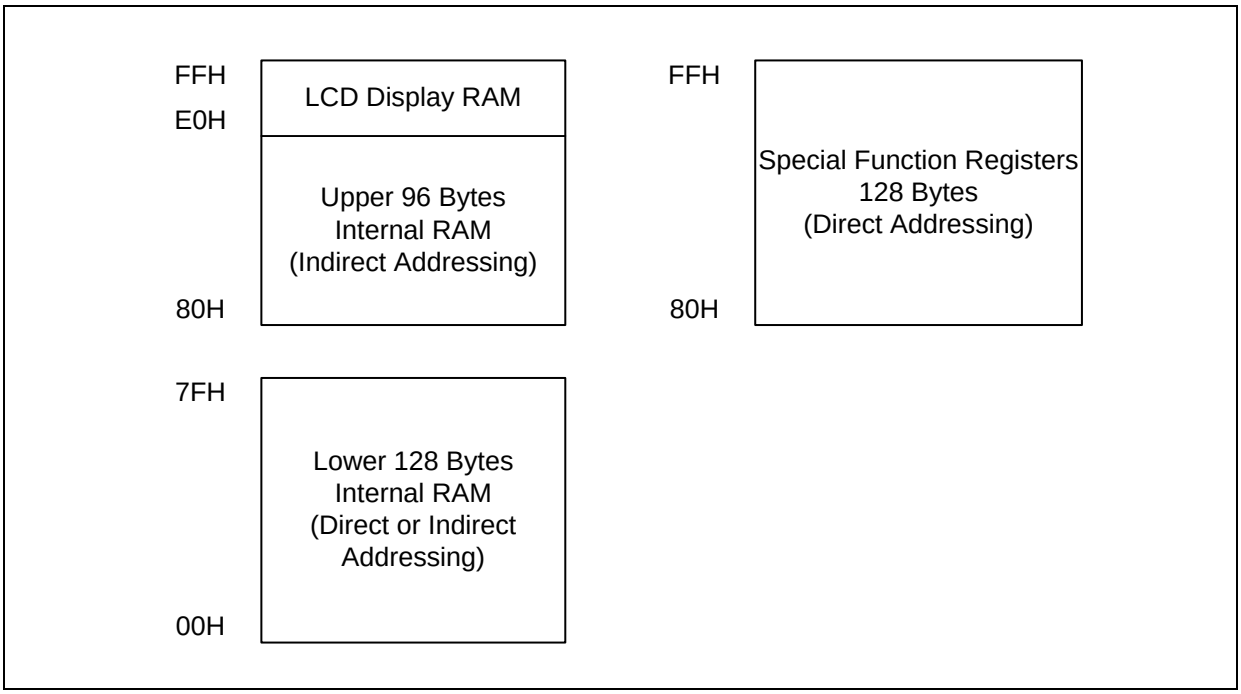


Figure 8.2 Data Memory Map

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, in fact the addressing modes for internal RAM can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 8-2 shows the upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8-3. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack and LCD Display RAM.

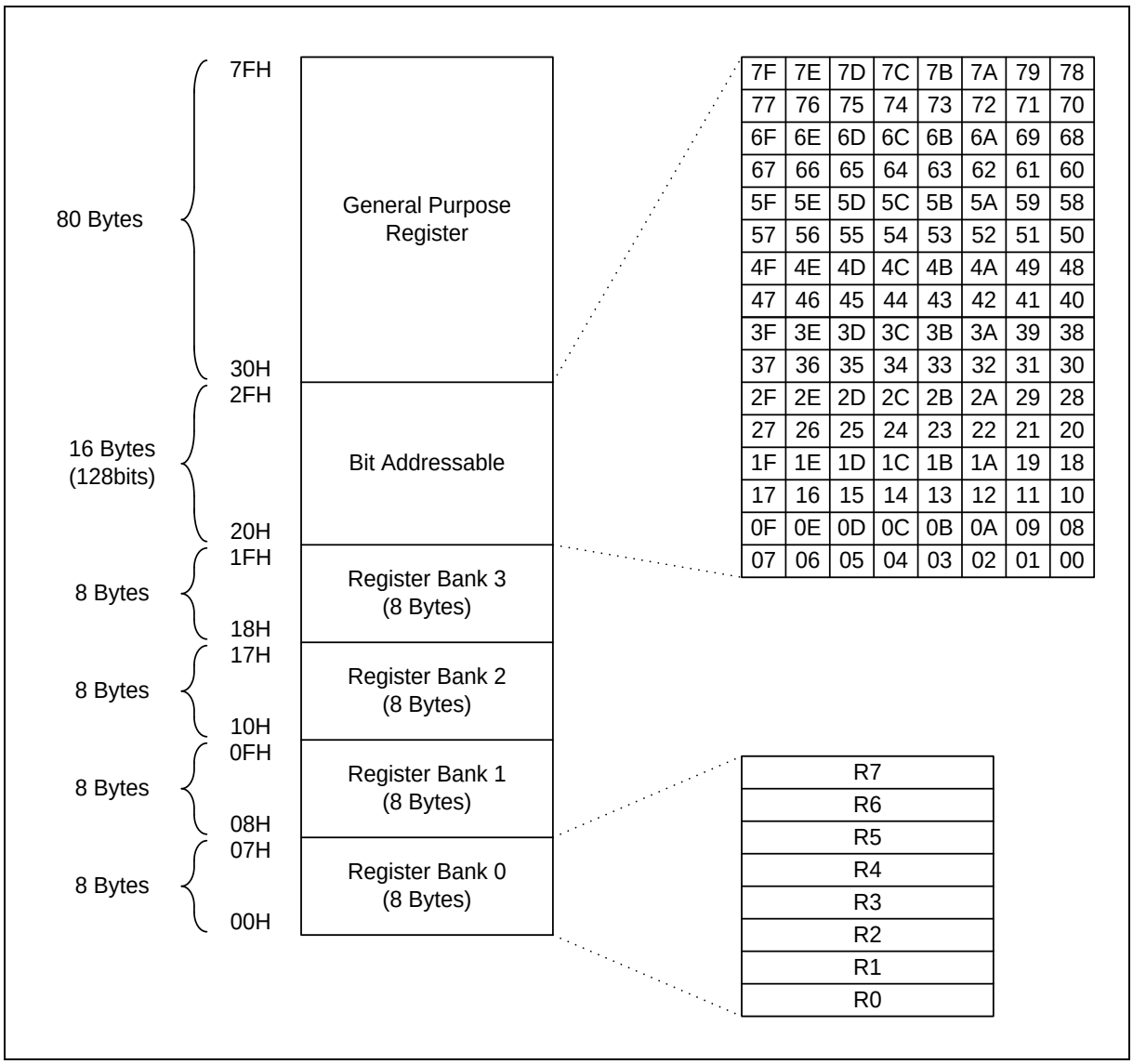


Figure 8.3 Lower 128 Bytes RAM

8.3 SFR Map

8.3.1 SFR Map Summary

Table 8-1 SFR Map Summary

-	Reserved
	M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	–	–	–	–	PORCR	PLLCR
0F0H	B	P4FSR	P5FSR	P6FSR	–	–	–	–
0E8H	KFLAG	P0DB	P1DB	LCDCRL	LCDCRH	P0FSR	P2FSR	P3FSR
0E0H	ACC	LVICR	–	–	–	–	–	–
0D8H	–	OSCCR	P4PU	P5PU	P6PU	P7PU	–	–
0D0H	PSW	–	–	–	P0PU	P1PU	P2PU	P3PU
0C8H	P7	P7IO	T1CR	T1CNT	T1DRL	T1DRH/ T1CDR	CARCR	–
0C0H	P6	P6IO	T3CR	TIFR	T3CNT	–	T3DR/ T3CDR	–
0B8H	IP	P5IO	T2CR	–	T2CNT	–	T2DR/ T2CDR	–
0B0H	P5	P4IO	T0CR	T0CNT	T0DR/ T0CDR	SIOCR	SIODR	SIOPS
0A8H	IE	IE1	IE2	IE3	–	–	KPOL0	KPOL1
0A0H	P4	P3IO	EO	–	EIFLAG	EIPOL	–	–
98H	P3	P2IO	P5OD	P6OD	P7OD	–	WTCR	WTDR/ WTCNT
90H	P2	P1IO	P0OD	P1OD	P2OD	P3OD	P4OD	BUZCR
88H	P1	P0IO	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	RSTFR	PCON

NOTE)

1. 00H/8H(1), These registers are bit-addressable.
2. Do not use the “direct bit test and branch” instruction on P0, P1, P2, P3, P4, P5, P6, P7 and KFLAG registers. More detail information is at Appendix B.
   Example) Avoid direct input port bit test and branch condition as below
   if(P00) → if(P0 & 0x01)

8.3.2 SFR Map

Table 8-2 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reset Flag Register	RSTFR	R/W	1	x	0	0	–	–	–	–
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	–	–	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
92H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
93H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
94H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
95H	P3 Open-drain Selection Register	P3OD	R/W	0	0	0	0	0	0	0	0
96H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
99H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
9AH	P5 Open-drain Selection Register	P5OD	R/W	0	0	0	0	0	0	0	0
9BH	P6 Open-drain Selection Register	P6OD	R/W	–	–	0	0	0	0	0	0
9CH	P7 Open-drain Selection Register	P7OD	R/W	–	–	–	0	0	–	0	0
9DH	Reserved	–	–								
9EH	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
9FH	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0

NOTE) Where x is “don’t care.”

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	0	0	0	0	0	0	0	0
A1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	External Interrupt Flag Register	EIFLAG	R/W	–	–	–	–	–	–	0	0
A5H	External Interrupt Polarity Register	EIPOL	R/W	–	–	–	–	0	0	0	0
A6H	Reserved	–	–	–							
A7H	Reserved	–	–	–							
A8H	Interrupt Enable Register	IE	R/W	0	–	0	–	–	0	0	–
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	–	–	–	–	–
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	–	0	0	0	0	–
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	0	–	–
ACH	Reserved	–	–	–							
ADH	Reserved	–	–	–							
AEH	Key Interrupt Polarity 0 Register	KPOL0	R/W	0	0	0	0	0	0	0	0
AFH	Key Interrupt Polarity 1 Register	KPOL1	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	0	0	0	0	0	0	0	0
B1H	P4 Direction Register	P4IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	SIO Control Register	SIOCR	R/W	0	0	0	0	0	0	0	0
B6H	SIO Data Register	SIODR	R/W	0	0	0	0	0	0	0	0
B7H	SIO Pre-scaler Register	SIOPS	R/W	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P5 Direction Register	P5IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 2 Control Register	T2CR	R/W	0	–	0	0	0	0	0	0
BBH	Reserved	–	–	–							
BCH	Timer 2 Counter Register	T2CNT	R	0	0	0	0	0	0	0	0
BDH	Reserved	–	–	–							
BEH	Timer 2 Data Register	T2DR	R/W	1	1	1	1	1	1	1	1
	Timer 2 Capture Data Register	T2CDR	R	0	0	0	0	0	0	0	0
BFH	Reserved	–	–	–							

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	P6 Data Register	P6	R/W	–	–	0	0	0	0	0	0
C1H	P6 Direction Register	P6IO	R/W	–	–	0	0	0	0	0	0
C2H	Timer 3 Control Register	T3CR	R/W	0	0	–	0	0	0	0	0
C3H	Timer Interrupt Flag Register	TIFR	R/W	0	–	–	–	0	0	0	0
C4H	Timer 3 Counter Register	T3CNT	R	0	0	0	0	0	0	0	0
C5H	Reserved	–	–	–							
C6H	Timer 3 Data Register	T3DR	R/W	1	1	1	1	1	1	1	1
	Timer 3 Capture Data Register	T3CDR	R	0	0	0	0	0	0	0	0
C7H	Reserved	–	–	–							
C8H	P7 Data Register	P7	R/W	–	–	–	0	0	–	0	0
C9H	P7 Direction Register	P7IO	R/W	0	0	–	0	0	0	0	0
CAH	Timer 1 Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
CBH	Timer 1 Counter Register	T1CNT	R	0	0	0	0	0	0	0	0
CCH	Timer 1 Data Low Register	T1DRL	R/W	1	1	1	1	1	1	1	1
CDH	Timer 1 Data High Register	T1DRH	R/W	1	1	1	1	1	1	1	1
	Timer 1 Capture Data Register	T1CDR	R	0	0	0	0	0	0	0	0
CEH	Carrier Mode Control Register	CARCR	R/W	–	–	0	0	–	–	0	0
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
D5H	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
D6H	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
D7H	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
D8H	Reserved	–	–	–							
D9H	Oscillator Control Register	OSCCR	R/W	–	–	–	0	0	0	0	0
DAH	P4 Pull-up Resistor Selection Register	P4PU	R/W	0	0	0	0	0	0	0	0
DBH	P5 Pull-up Resistor Selection Register	P5PU	R/W	0	0	0	0	0	0	0	0
DCH	P6 Pull-up Resistor Selection Register	P6PU	R/W	–	–	0	0	0	0	0	0
DDH	P7 Pull-up Resistor Selection Register	P7PU	R/W	–	–	–	0	0	–	0	0
DEH	Reserved	–	–	–							
DFH	Reserved	–	–	–							

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	–	–	0	0
E2H	Reserved	–	–	–							
E3H	Reserved	–	–	–							
E4H	Reserved	–	–	–							
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Key Interrupt Flag Register	KFLAG	R/W	0	0	0	0	0	0	0	0
E9H	P0 Debounce Enable Register	P0DB	R/W	0	0	–	–	–	–	0	0
EAH	P1 Debounce Enable Register	P1DB	R/W	0	0	0	0	0	0	0	0
EBH	LCD Driver Control Low Register	LCDCRL	R/W	–	–	–	–	–	–	0	0
ECH	LCD Driver Control High Register	LCDCRH	R/W	0	0	0	0	0	0	0	0
EDH	Port 0 Function Selection Register	P0FSR	R/W	–	–	0	0	0	0	0	0
EEH	Port 2 Function Selection Register	P2FSR	R/W	0	0	0	0	0	0	0	0
EFH	Port 3 Function Selection Register	P3FSR	R/W	0	0	0	0	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Port 4 Function Selection Register	P4FSR	R/W	0	0	0	0	0	0	0	0
F2H	Port 5 Function Selection Register	P5FSR	R/W	0	0	0	0	0	0	0	0
F3H	Port 6 Function Selection Register	P6FSR	R/W	–	–	0	0	0	0	0	0
F4H	Reserved	–	–	–							
F5H	Reserved	–	–	–							
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Reserved	–	–	–							
FBH	Reserved	–	–	–							
FCH	Reserved	–	–	–							
FDH	Reserved	–	–	–							
FEH	Power On Reset Control Register	PORCR	R/W	0	0	0	0	0	0	0	0
FFH	Phase Locked Loop Control Register	PLLCR	R/W	0	–	0	0	0	0	0	0

8.3.3 Compiler Compatible SFR

ACC (Accumulator Register) : E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ACC Accumulator

B (B Register) : F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

B B Register

SP (Stack Pointer) : 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 07H

SP Stack Pointer

DPL (Data Pointer Register Low) : 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL Data Pointer Low Byte

DPH (Data Pointer Register High) : 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH Data Pointer High Byte

DPL1 (Data Pointer Register Low 1) : 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL1 Data Pointer Low 1 Byte

DPH1 (Data Pointer Register High 1) : 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH1 Data Pointer High 1 Byte

PSW (Program Status Word Register) : D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

CY Carry Flag

AC Auxiliary Carry Flag

F0 General Purpose User-Definable Flag

RS1 Register Bank Select bit 1

RS0 Register Bank Select bit 0

OV Overflow Flag

F1 User-Definable Flag

P Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator

EO (Extended Operation Register) : A2H

7	6	5	4	3	2	1	0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value : 00H

TRAP_EN Select the Instruction **(Keep always '0')**.

0 Select Software TRAP Instruction

1 Select MOVC @(DPTR++), A

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	SPSEL0	Description
0	0	0	DPTR0
0	0	1	DPTR1

Reserved

9. I/O Ports

9.1 I/O Ports

The MC96P6608/P6408 has eight groups of I/O ports (P0 ~ P7). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. Also P00 and P06 includes function that can generate interrupt according to change of state of the pin.

9.2 Port Register

9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

9.2.2 Direction Register (PxIO)

Each I/O pin can be independently used as an input or an output through the PxIO register. Bits cleared in this register will make the corresponding pin of Px to input mode. Set bits of this register will make the pin to output mode. Almost bits are cleared by a system reset, but some bits are set by a system reset.

9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to I/O ports individually with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset.

9.2.4 Open-drain Selection Register (PxOD)

There are internally open-drain selection registers (PxOD) for P0 ~ P7. The open-drain selection register controls the open-drain enable/disable of each port. Almost ports become push-pull by a system reset, but some ports become open-drain by a system reset.

9.2.5 Debounce Enable Register (PxDB)

P1[0:7], P00, and P05 support debounce function. Debounce clocks of each ports are fx/1, fx/4, and fx/4096.

9.2.6 Port Function Selection Register (PxFSR)

These registers define alternative functions of ports. Please remember that these registers should be set properly for alternative port function. A reset clears the PxFSR register to ‘00H’, which makes all pins to normal I/O ports.

9.2.7 Register Map

Table 9-1 Port Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	89H	R/W	00H	P0 Direction Register
P0PU	D4H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	92H	R/W	00H	P0 Open-drain Selection Register
P0DB	E9H	R/W	00H	P0 Debounce Enable Register
P0FSR	EDH	R/W	00H	Port 0 Function Selection Register
P1	88H	R/W	00H	P1 Data Register
P1IO	91H	R/W	00H	P1 Direction Register
P1PU	D5H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	93H	R/W	00H	P1 Open-drain Selection Register
P1DB	EAH	R/W	00H	P1 Debounce Enable Register
P2	90H	R/W	00H	P2 Data Register
P2IO	99H	R/W	00H	P2 Direction Register
P2PU	D6H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	94H	R/W	00H	P2 Open-drain Selection Register
P2FSR	EEH	R/W	00H	Port 2 Function Selection Register
P3	98H	R/W	00H	P3 Data Register
P3IO	A1H	R/W	00H	P3 Direction Register
P3PU	D7H	R/W	00H	P3 Pull-up Resistor Selection Register
P3OD	95H	R/W	00H	P3 Open-drain Selection Register
P3FSR	EFH	R/W	00H	Port 3 Function Selection Register
P4	A0H	R/W	00H	P4 Data Register
P4IO	B1H	R/W	00H	P4 Direction Register
P4PU	DAH	R/W	00H	P4 Pull-up Resistor Selection Register
P4OD	96H	R/W	00H	P4 Open-drain Selection Register
P4FSR	F1H	R/W	00H	Port 4 Function Selection Register
P5	B0H	R/W	00H	P5 Data Register
P5IO	B9H	R/W	00H	P5 Direction Register
P5PU	DBH	R/W	00H	P5 Pull-up Resistor Selection Register
P5OD	9AH	R/W	00H	P5 Open-drain Selection Register
P5FSR	F2H	R/W	00H	Port 5 Function Selection Register

Table 9-1 Register Map (Continued)

Name	Address	Dir	Default	Description
P6	C0H	R/W	00H	P6 Data Register
P6IO	C1H	R/W	00H	P6 Direction Register
P6PU	DCH	R/W	00H	P6 Pull-up Resistor Selection Register
P6OD	9BH	R/W	00H	P6 Open-drain Selection Register
P6FSR	F3H	R/W	00H	Port 6 Function Selection Register
P7	C8H	R/W	00H	P7 Data Register
P7IO	C9H	R/W	00H	P7 Direction Register
P7PU	DDH	R/W	00H	P7 Pull-up Resistor Selection Register
P7OD	9CH	R/W	00H	P7 Open-drain Selection Register

9.3 P0 Port

9.3.1 P0 Port Description

P0 is 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). The P01 and P03~P07 function can be selected by the P0FSR[5:0] bits of the P0FSR register. Refer to the port function selection registers.

9.3.2 Register description for P0

P0 (P0 Data Register) : 80H

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P00) → if(P0 & 0x01)

P0IO (P0 Direction Register) : 89H

7	6	5	4	3	2	1	0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0IO[7:0] P0 Data I/O Direction.
0 Input
1 Output
NOTE: EINT0/EC0/SI/SCK-in/EC2 function possible when input

P0PU (P0 Pull-up Resistor Selection Register) : D4H

7	6	5	4	3	2	1	0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0PU[7:0] Configure Pull-up Resistor of P0 Port
0 Disable
1 Enable

P0OD (P0 Open-drain Selection Register) : 92H

7	6	5	4	3	2	1	0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0OD[7:0] Configure Open-drain of P0 Port

0 Push-pull output

1 Open-drain output

P0DB (P0 Debounce Enable Register) : E9H

7	6	5	4	3	2	1	0
DBCLK1	DBCLK0	–	–	–	–	P01DB	P00DB
R/W	R/W	–	–	–	–	R/W	R/W

Initial value : 00H

DBCLK[1:0] Configure Debounce Clock of Port

DBCLK1	DBCLK0	Description
0	0	fx/1
0	1	fx/4
1	0	fx/4096
1	1	Reserved

P01DB Configure Debounce of P05 Port

0 Disable

1 Enable

P00DB Configure Debounce of P00 Port

0 Disable

1 Enable

NOTES) 1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.

2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.

3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.

9.4 P1 Port

9.4.1 P1 Port Description

P1 is 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD) .

9.4.2 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P10) → if(P1 & 0x01)

P1IO (P1 Direction Register) : 91H

7	6	5	4	3	2	1	0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1IO[7:0] P1 Data I/O Direction

0 Input

1 Output

Note: KEY0 – KEY7 function possible when input

P1PU (P1 Pull-up Resistor Selection Register) : D5H

7	6	5	4	3	2	1	0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1PU[7:0] Configure Pull-up Resistor of P1 Port

0 Disable

1 Enable

P1OD (P1 Open-drain Selection Register) : 93H

7	6	5	4	3	2	1	0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1OD[7:0] Configure Open-drain of P1 Port

0 Push-pull output

1 Open-drain output

P1DB (P1 Debounce Enable Register): EAH

7	6	5	4	3	2	1	0
P17DB	P16DB	P15DB	P14DB	P13DB	P12DB	P11DB	P10DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1DB[7:0] Configure Debounce of P1 Port

0 Disable

1 Enable

NOTES) 1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.

2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.

3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.

4. Refer to the port 0 debounce enable register (P0DB) for the debounce clock of port 1.

9.5 P2 Port

9.5.1 P2 Port Description

P2 is 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers (P2FSR) for the P2 function selection.

9.5.2 Register description for P2

P2 (P2 Data Register) : 90H

7	6	5	4	3	2	1	0
P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P2[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P20) → if(P2 & 0x01)

P2IO (P2 Direction Register) : 99H

7	6	5	4	3	2	1	0
P27IO	P26IO	P25IO	P24IO	P23IO	P22IO	P21IO	P20IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P2IO[7:0] P2 Data I/O Direction

0 Input

1 Output

P2PU (P2 Pull-up Resistor Selection Register) : D6H

7	6	5	4	3	2	1	0
P27PU	P26PU	P25PU	P24PU	P23PU	P22PU	P21PU	P20PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P2PU[7:0] Configure Pull-up Resistor of P2 Port

0 Disable

1 Enable

P2OD (P2 Open-drain Selection Register) : 94H

7	6	5	4	3	2	1	0
P27OD	P26OD	P25OD	P24OD	P23OD	P22OD	P21OD	P20OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P2OD[7:0] Configure Open-drain of P2 Port

0 Push-pull output

1 Open-drain output

9.6 P3 Port

9.6.1 P3 Port Description

P3 is 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO), P3 pull-up resistor selection register (P3PU) and P3 open-drain selection register (P3OD). Refer to the port function selection registers (P3FSR) for the P3 function selection.

9.6.2 Register description for P3

P3 (P3 Data Register) : 98H

7	6	5	4	3	2	1	0
P37	P36	P35	P34	P33	P32	P31	P30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P3[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P30) → if(P3 & 0x01)

P3IO (P3 Direction Register) : A1H

7	6	5	4	3	2	1	0
P37IO	P36IO	P35IO	P34IO	P33IO	P32IO	P31IO	P30IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P3IO[7:0] P3 Data I/O Direction

0 Input

1 Output

P3PU (P3 Pull-up Resistor Selection Register) : D7H

7	6	5	4	3	2	1	0
P37PU	P36PU	P35PU	P34PU	P33PU	P32PU	P31PU	P30PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P3PU[7:0] Configure Pull-up Resistor of P3 Port

0 Disable

1 Enable

P3OD (P3 Open-drain Selection Register) : 95H

7	6	5	4	3	2	1	0
P37OD	P36OD	P35OD	P34OD	P33OD	P32OD	P31OD	P30OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P3OD[7:0] Configure Open-drain of P3 Port

0 Push-pull output

1 Open-drain output

9.7 P4 Port

9.7.1 P4 Port Description

P4 is 8-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO), P4 pull-up resistor selection register (P4PU) and P4 open-drain selection register (P4OD). Refer to the port function selection registers (P4FSR) for the P4 function selection.

9.7.2 Register description for P4

P4 (P4 Data Register) : A0H

7	6	5	4	3	2	1	0
P47	P46	P45	P44	P43	P42	P41	P40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P4[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P40) → if(P4 & 0x01)

P4IO (P4 Direction Register) : B1H

7	6	5	4	3	2	1	0
P47IO	P46IO	P45IO	P44IO	P43IO	P42IO	P41IO	P40IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P4IO[7:0] P4 Data I/O Direction

0 Input

1 Output

P4PU (P4 Pull-up Resistor Selection Register) : DAH

7	6	5	4	3	2	1	0
P47PU	P46PU	P45PU	P44PU	P43PU	P42PU	P41PU	P40PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P4PU[7:0] Configure Pull-up Resistor of P4 Port

0 Disable

1 Enable

P4OD (P4 Open-drain Selection Register) : 96H

7	6	5	4	3	2	1	0
P47OD	P46OD	P45OD	P44OD	P43OD	P42OD	P41OD	P40OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P4OD[7:0] Configure Open-drain of P4 Port

0 Push-pull output

1 Open-drain output

9.8 P5 Port

9.8.1 P5 Port Description

P5 is 8-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO), P5 pull-up resistor selection register (P5PU) and P5 open-drain selection register (P5OD). Refer to the port function selection registers (P5FSR) for the P5 function selection.

9.8.2 Register description for P5

P5 (P5 Data Register) : B0H

7	6	5	4	3	2	1	0
P57	P56	P55	P54	P53	P52	P51	P50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P5[7:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P50) → if(P5 & 0x01)

P5IO (P5 Direction Register) : B9H

7	6	5	4	3	2	1	0
P57IO	P56IO	P55IO	P54IO	P53IO	P52IO	P51IO	P50IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P5IO[7:0] P5 Data I/O Direction

0 Input

1 Output

P5PU (P5 Pull-up Resistor Selection Register) : DBH

7	6	5	4	3	2	1	0
P57PU	P56PU	P55PU	P54PU	P53PU	P52PU	P51PU	P50PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P5PU[7:0] Configure Pull-up Resistor of P5 Port

0 Disable

1 Enable

P5OD (P5 Open-drain Selection Register) : 9AH

7	6	5	4	3	2	1	0
P57OD	P56OD	P55OD	P54OD	P53OD	P52OD	P51OD	P50OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P5OD[7:0] Configure Open-drain of P5 Port

0 Push-pull output

1 Open-drain output

9.9 P6 Port

9.9.1 P6 Port Description

P6 is 6-bit I/O port. P6 control registers consist of P6 data register (P6), P6 direction register (P6IO), P6 pull-up resistor selection register (P6PU) and P6 open-drain selection register (P6OD). Refer to the port function selection registers for the P6 function selection.

9.9.2 Register description for P6

P6 (P6 Data Register) : C0H

7	6	5	4	3	2	1	0
–	–	P65	P64	P63	P62	P61	P60
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6[5:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P60) → if(P6 & 0x01)

P6IO (P6 Direction Register) : C1H

7	6	5	4	3	2	1	0
–	–	P65IO	P64IO	P63IO	P62IO	P61IO	P60IO
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6IO[5:0] P6 Data I/O Direction

0 Input

1 Output

P6PU (P6 Pull-up Resistor Selection Register) : DCH

7	6	5	4	3	2	1	0
–	–	P65PU	P64PU	P63PU	P62PU	P61PU	P60PU
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6PU[5:0] Configure Pull-up Resistor of P6 Port

0 Disable

1 Enable

P6OD (P6 Open-drain Selection Register) : 9BH

7	6	5	4	3	2	1	0
–	–	P65OD	P64OD	P63OD	P62OD	P61OD	P60OD
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P6OD[5:0] Configure Open-drain of P6 Port

0 Push-pull output

1 Open-drain output

9.10 P7 Port

9.10.1 P7 Port Description

P7 is 4-bit I/O port. P7 control registers consist of P7 data register (P7), P7 direction register (P7IO), P7 pull-up resistor selection register (P7PU) and P7 open-drain selection register (P7OD).

9.10.2 Register description for P7

P7 (P7 Data Register) : C8H

7	6	5	4	3	2	1	0
–	–	–	P74	P73	–	P71	P70
–	–	–	R/W	R/W	–	R/W	R/W

Initial value : 00H

P7[4:0] I/O Data

Note) Do not use the “direct bit test and branch” instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(P70) → if(P7 & 0x01)

P7IO (P7 Direction Register) : C9H

7	6	5	4	3	2	1	0
–	–	–	P74IO	P73IO	–	P71IO	P70IO
–	–	–	R/W	R/W	–	R/W	R/W

Initial value : 00H

P7IO[4:0] P7 Data I/O Direction
0 Input
1 Output

P7PU (P7 Pull-up Resistor Selection Register) : DDH

7	6	5	4	3	2	1	0
–	–	–	P74PU	P73PU	–	P71PU	P70PU
–	–	–	R/W	R/W	–	R/W	R/W

Initial value : 00H

P7PU[4:0] Configure Pull-up Resistor of P7 Port
0 Disable
1 Enable

P7OD (P7 Open-drain Selection Register) : 9CH

7	6	5	4	3	2	1	0
–	–	–	P74OD	P73OD	–	P71OD	P70OD
–	–	–	R/W	R/W	–	R/W	R/W

Initial value : 00H

P7OD[4:0] Configure Open-drain of P7 Port
0 Push-pull output
1 Open-drain output

9.11 Port Function

9.11.1 Port Function Description

Port function control registers consist of Port 0~6 function selection register. (P0FSR and P2FSR ~ P6FSR).

9.11.2 Register description for P0FSR ~ P6FSR

P0FSR (Port 0 Function Selection Register) : EDH

7	6	5	4	3	2	1	0
–	–	PFSR05	PFSR04	PFSR03	PFSR02	PFSR01	PFSR00
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR05 P07 Function Select
- 0 Port
- 1 REM Function

PFSR04 P06 Function Select
- 0 Port
- 1 BUZO Function

PFSR03 P05 Function Select
- 0 Port
- 1 T2O Function

PFSR02 P04 Function Select
- 0 Port
- 1 SO Function

PFSR01 P03 Function Select
- 0 Port
- 1 SCK-out Function

PFSR00 P01 Function Select
- 0 Port
- 1 T0O Function

P2FSR (Port 2 Function Selection Register 1) : EEH

7	6	5	4	3	2	1	0
PFSR27	PFSR26	PFSR25	PFSR24	PFSR23	PFSR22	PFSR21	PFSR20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR27 P27 Function select
- 0 Port
- 1 COM3/SEG1 Function

PFSR26 P26 Function select
- 0 Port
- 1 COM2/SEG0 Function

PFSR25 P25 Function select
- 0 Port
- 1 COM1 Function

PFSR24 P24 Function select
- 0 Port
- 1 COM0 Function

PFSR23 P23 Function select
- 0 Port
- 1 VLC3 Function

PFSR22 P22 Function select
- 0 Port
- 1 VLC2 Function

PFSR21 P21 Function select
- 0 Port
- 1 VLC1 Function

PFSR20 P20 Function select
- 0 Port
- 1 VLC0 Function

P3FSR (Port 3 Function Selection Register) : EFH

7	6	5	4	3	2	1	0
PFSR37	PFSR36	PFSR35	PFSR34	PFSR33	PFSR32	PFSR31	PFSR30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR37 P37 Function select
- 0 Port
- 1 SEG9 Function

PFSR36 P36 Function select
- 0 Port
- 1 SEG8 Function

PFSR35 P35 Function select
- 0 Port
- 1 SEG7 Function

PFSR34 P34 Function select
- 0 Port
- 1 SEG6 Function

PFSR33 P33 Function select
- 0 Port
- 1 COM7/SEG5 Function

PFSR32 P32 Function select
- 0 Port
- 1 COM6/SEG4 Function

PFSR31 P31 Function select
- 0 Port
- 1 COM5/SEG3 Function

PFSR30 P30 Function select
- 0 Port
- 1 COM4/SEG2 Function

P4FSR (Port 4 Function Selection Register) : F1H

7	6	5	4	3	2	1	0
PFSR47	PFSR46	PFSR45	PFSR44	PFSR43	PFSR42	PFSR41	PFSR40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR47 P47 Function select
- 0 Port
- 1 SEG17 Function

PFSR46 P46 Function select
- 0 Port
- 1 SEG16 Function

PFSR45 P45 Function select
- 0 Port
- 1 SEG15 Function

PFSR44 P44 Function select
- 0 Port
- 1 SEG14 Function

PFSR43 P43 Function select
- 0 Port
- 1 SEG13 Function

PFSR42 P42 Function select
- 0 Port
- 1 SEG12 Function

PFSR41 P41 Function select
- 0 Port
- 1 SEG11 Function

PFSR40 P40 Function select
- 0 Port
- 1 SEG10 Function

P5FSR (Port 5 Function Selection Register) : F2H

7	6	5	4	3	2	1	0
PFSR57	PFSR56	PFSR55	PFSR54	PFSR53	PFSR52	PFSR51	PFSR50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR57 P57 Function Select
- 0 Port
- 1 SEG25 Function

PFSR56 P56 Function Select
- 0 Port
- 1 SEG24 Function

PFSR55 P55 Function select
- 0 Port
- 1 SEG23 Function

PFSR54 P54 Function select
- 0 Port
- 1 SEG22 Function

PFSR53 P53 Function select
- 0 Port
- 1 SEG21 Function

PFSR52 P52 Function select
- 0 Port
- 1 SEG20 Function

PFSR51 P51 Function select
- 0 Port
- 1 SEG19 Function

PFSR50 P50 Function select
- 0 Port
- 1 SEG18 Function

P6FSR (Port 6 Function Selection Register) : F3H

7	6	5	4	3	2	1	0
–	–	PFSR65	PFSR64	PFSR63	PFSR62	PFSR61	PFSR60
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR65 P65 Function Select
- 0 Port
- 1 SEG31 Function

PFSR64 P64 Function Select
- 0 Port
- 1 SEG30 Function

PFSR63 P63 Function Select
- 0 Port
- 1 SEG29 Function

PFSR62 P62 Function Select
- 0 Port
- 1 SEG28 Function

PFSR61 P61 Function Select
- 0 Port
- 1 SEG27 Function

PFSR60 P60 Function Select
- 0 Port
- 1 SEG26 Function

10. Interrupt Controller

10.1 Overview

The MC96P6608/P6408 supports up to 18 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

- Receive the request from 18 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency: 3~9 machine cycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The MC96P6608/P6408 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Table 10-1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Table 10-1 Interrupt Group Priority Level

Interrupt Group	Highest → Lowest				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	Lowest

10.2 External Interrupt

The external interrupt on INT1, INT2 and INT5 pins receive various interrupt request depending on the external interrupt polarity register (EIPOL), key interrupt polarity 0 register (KPOL0) and key interrupt polarity 1 register (KPOL1) as shown in Figure 10.1. The external interrupt flag register (EIFLAG) and key interrupt Flag register (KFLAG) provides the status of external interrupts.

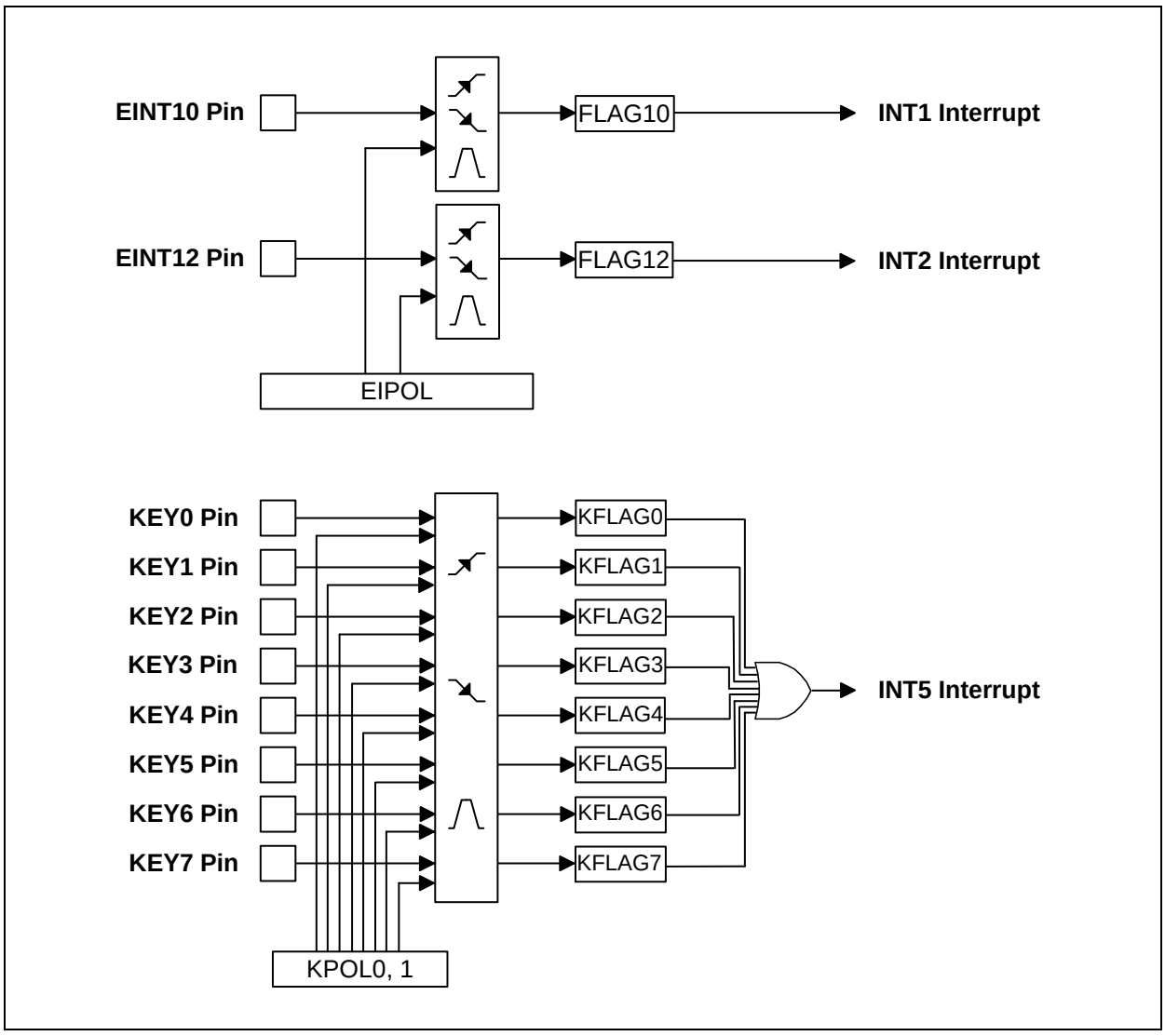


Figure 10.1 External Interrupt Description

10.3 Block Diagram

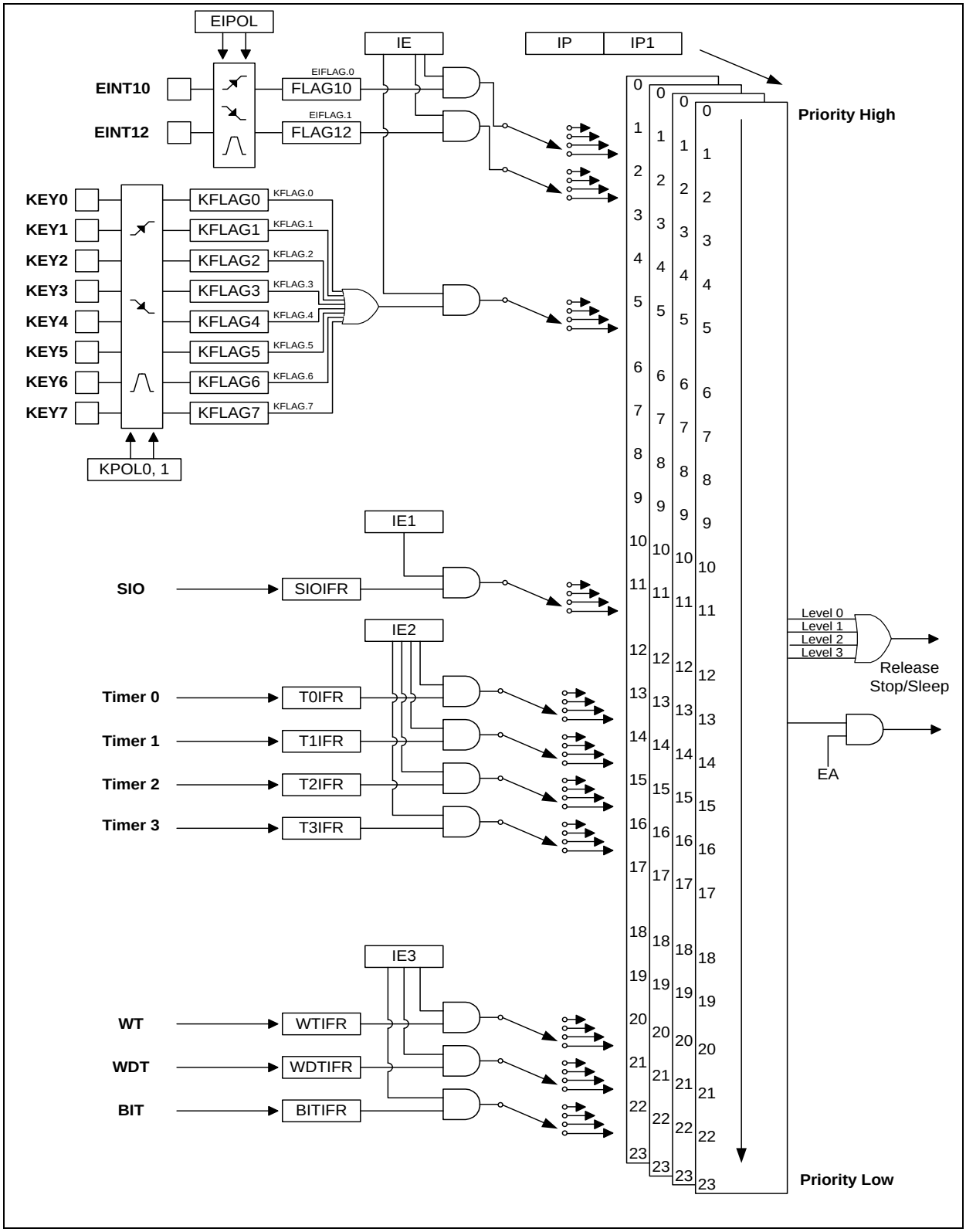


Figure 10.2 Block Diagram of Interrupt

NOTES) 1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.

2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

10.4 Interrupt Vector Table

The interrupt controller supports 24 interrupt sources as shown in the Table 10-2. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 10-2 Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Polarity	Mask	Vector Address
Hardware Reset	RESETB	0 0	0	Non-Maskable	0000H
-	INT0	IE.0	1	Maskable	0003H
External Interrupt 10	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
-	INT3	IE.3	4	Maskable	001BH
-	INT4	IE.4	5	Maskable	0023H
KEY Interrupt	INT5	IE.5	6	Maskable	002BH
-	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
-	INT8	IE1.2	9	Maskable	0043H
-	INT9	IE1.3	10	Maskable	004BH
-	INT10	IE1.4	11	Maskable	0053H
SIO Interrupt	INT11	IE1.5	12	Maskable	005BH
-	INT12	IE2.0	13	Maskable	0063H
T0 Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Interrupt	INT16	IE2.4	17	Maskable	0083H
-	INT17	IE2.5	18	Maskable	008BH
-	INT18	IE3.0	19	Maskable	0093H
-	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
-	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to ‘0’ by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC at stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. Since the end of the execution of current instruction, it needs 3~9 machine cycles to go to the interrupt service routine. The interrupt service task is terminated by the interrupt return instruction [RETI]. Once an interrupt request is generated, the following process is performed.

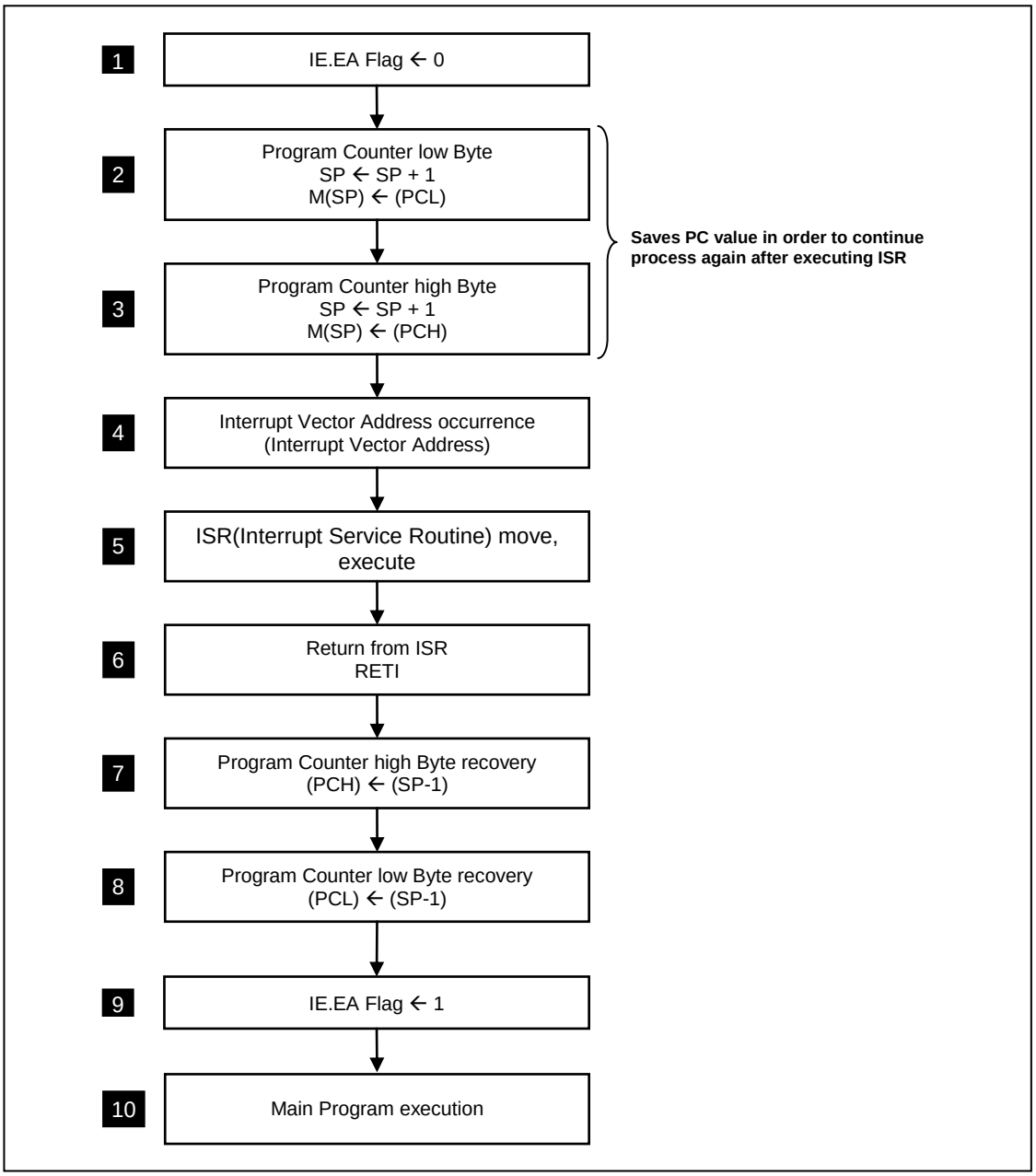


Figure 10.3 Interrupt Vector Address Table

10.6 Effective Timing after Controlling Interrupt Bit

Case a) Control Interrupt Enable Register (IE, IE1, IE2, IE3)

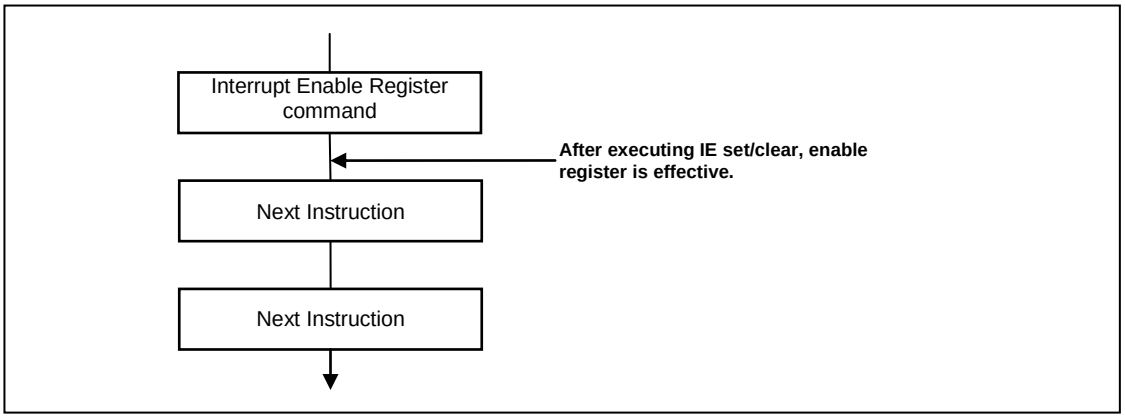


Figure 10.4 Effective Timing of Interrupt Enable Register

Case b) Interrupt flag Register

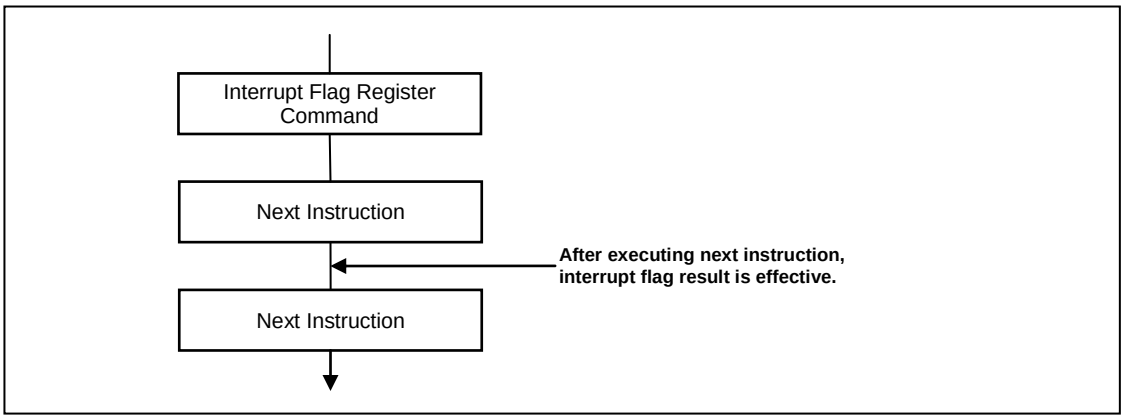


Figure 10.5 Effective Timing of Interrupt Flag Register

10.7 Multi Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is served first. If more than one interrupt request are received, the interrupt polling sequence determines which request is served first by hardware. However, for special features, multi-interrupt processing can be executed by software.

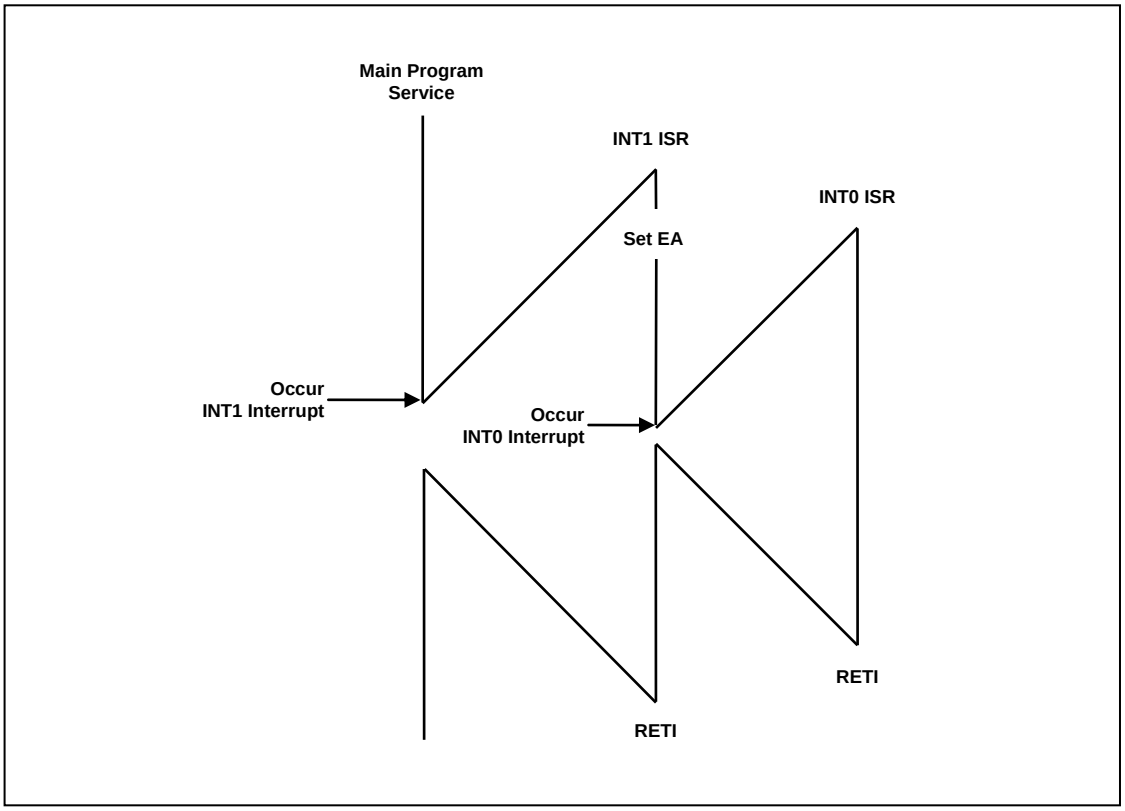


Figure 10.6 Effective Timing of Interrupt

Figure 10.6 shows an example of multi-interrupt processing. While INT1 is served, INT0 which has higher priority than INT1 is occurred. Then INT0 is served immediately and then the remain part of INT1 service routine is executed. If the priority level of INT0 is same or lower than INT1, INT0 will be served after the INT1 service has completed.

An interrupt service routine may be only interrupted by an interrupt of higher priority and, if two interrupts of different priority occur at the same time, the higher level interrupt will be served first. An interrupt cannot be interrupted by another interrupt of the same or a lower priority level. If two interrupts of the same priority level occur simultaneously, the service order for those interrupts is determined by the scan order.

10.8 Interrupt Enable Accept Timing

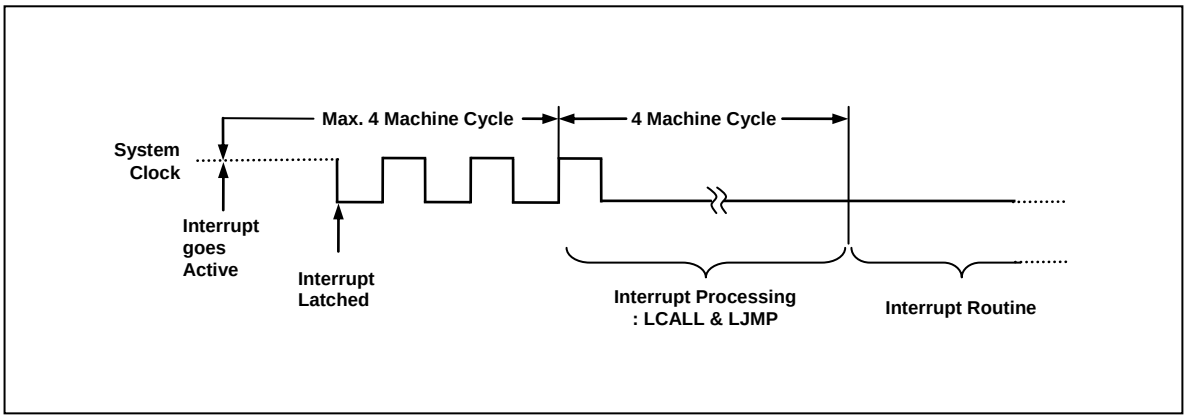


Figure 10.7 Interrupt Response Timing Diagram

10.9 Interrupt Service Routine Address

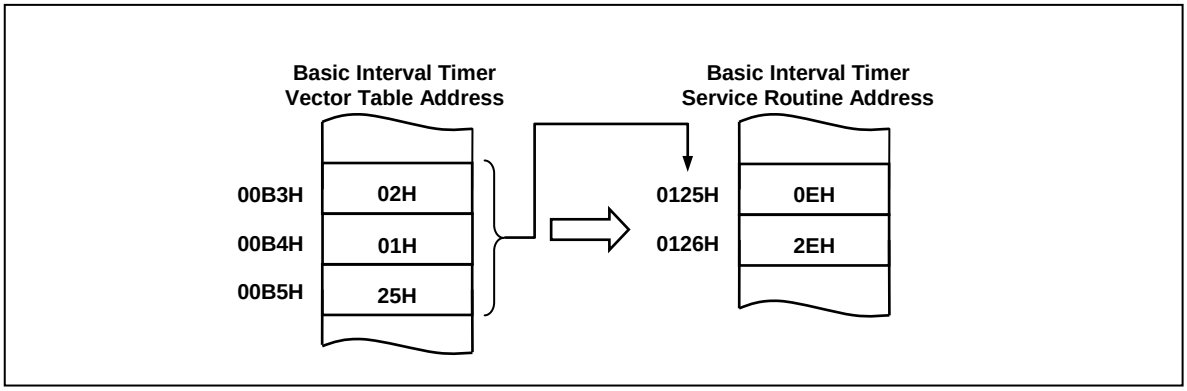


Figure 10.8 Correspondence between Vector Table Address and the Entry Address of ISP

10.10 Saving/Restore General-Purpose Registers

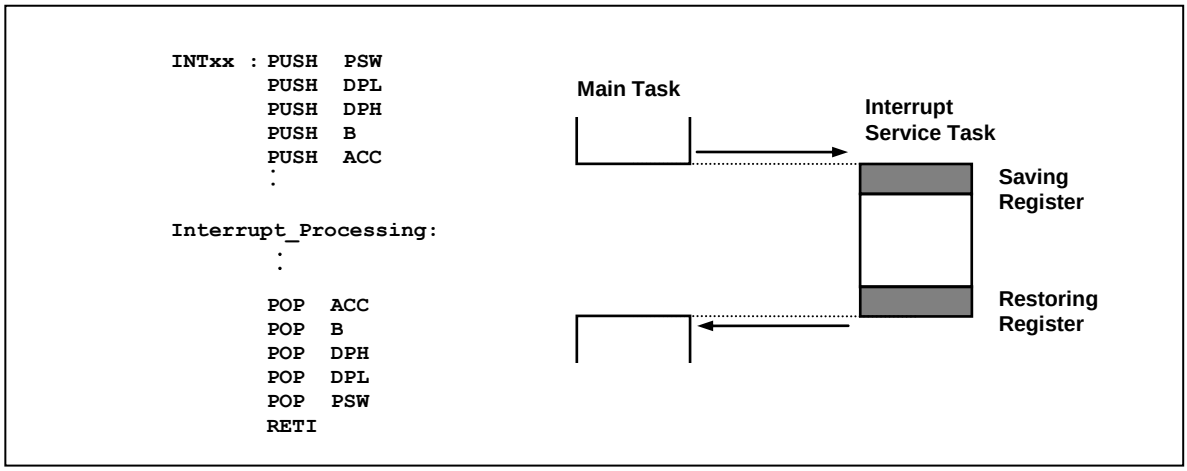


Figure 10.9 Saving/Restore Process Diagram and Sample Source

10.11 Interrupt Timing

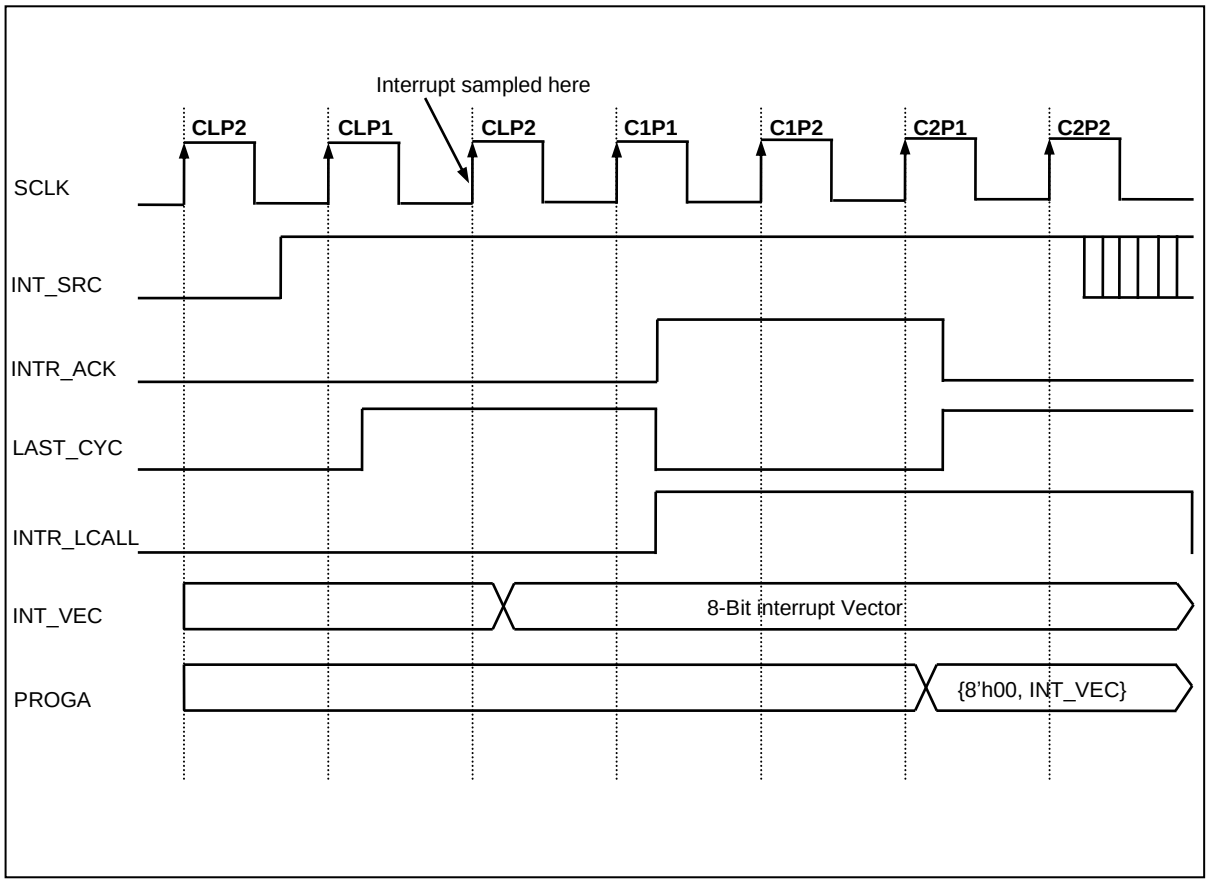


Figure 10.10 Timing Chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt sources are sampled at the last cycle of a command. If an interrupt source is detected the lower 8-bit of interrupt vector (INT_VEC) is decided. M8051W core makes interrupt acknowledge at the first cycle of a command, and executes long call to jump to interrupt service routine.

Note) command cycle CLPx: L=Last cycle, 1=1st cycle or 1st phase, 2=2nd cycle or 2nd phase

10.12 Interrupt Register Overview

10.12.1 Interrupt Enable Register (IE, IE1, IE2, IE3)

Interrupt enable register consists of global interrupt control bit (EA) and peripheral interrupt control bits. Total 24 peripherals are able to control interrupt.

10.12.2 Interrupt Priority Register (IP, IP1)

The 24 interrupts are divided into 6 groups which have each 4 interrupt sources. A group can be assigned 4 levels interrupt priority using interrupt priority register. Level 3 is the highest priority, while level 0 is the lowest priority. After a reset IP and IP1 are cleared to '00H'. If interrupts have the same priority level, lower number interrupt is served first.

10.12.3 External/Key Interrupt Flag Register (EIFLAG, KFLAG)

The external interrupt flag register (EIFLAG) and key interrupt flag register (KFLAG) are set to '1' when the external interrupt generating condition is satisfied. The flag is cleared when the interrupt service routine is executed. Alternatively, the flag can be cleared by writing '0' to it.

10.12.4 External/Key Interrupt Polarity Register (EIPOL, KPOL0, KPOL1)

The external interrupt polarity register (EIPOL) and key interrupt polarity 0/1 register (KPOL0, KPOL1) determine the edge of interrupt (rising, falling and both edge).

10.12.5 Register Map

Table 10-3 Interrupt Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Polarity Register
IP1	F8H	R/W	00H	Interrupt Polarity Register 1
EIFLAG	A4H	R/W	00H	External Interrupt Flag Register
EIPOL	A5H	R/W	00H	External Interrupt Polarity Register
KFLAG	E8H	R/W	00H	Key Interrupt Flag Register
KPOL1	AFH	R/W	00H	Key Interrupt Polarity 0 Register
KPOL0	AEH	R/W	00H	Key Interrupt Polarity 1 Register

10.13 Interrupt Register Description

The interrupt register is used for controlling interrupt functions. Also it has external interrupt control registers. The interrupt register consists of interrupt enable register (IE), interrupt enable register 1 (IE1), interrupt enable register 2 (IE2) and interrupt enable register 3 (IE3). For external interrupt, it consists of external interrupt flag register (EIFLAG), external interrupt polarity register (EIPOL), Key interrupt flag register (KFLAG), key interrupt polarity 0 register (KPOL0) and key interrupt polarity 1 register (KPOL1).

10.13.1 Register Description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	–	INT5E	–	–	INT2E	INT1E	–
R/W	–	R/W	–	–	R/W	R/W	–

Initial value : 00H

EA Enable or Disable All Interrupt bits
- 0 All Interrupt disable
- 1 All Interrupt enable

INT5E Enable or Disable Key Interrupt 0 ~ 7 (KEY0 ~ KEY7)
- 0 Disable
- 1 Enable

INT2E Enable or Disable External Interrupt 12 (EINT12)
- 0 Disable
- 1 Enable

INT1E Enable or Disable External Interrupt 10 (EINT10)
- 0 Disable
- 1 Enable

IE1 (Interrupt Enable Register 1): A9H

7	6	5	4	3	2	1	0
–	–	INT11E	–	–	–	–	–
–	–	R/W	–	–	–	–	–

Initial value: 00H

INT11E Enable or Disable SIO Interrupt
- 0 Disable
- 1 Enable

IE2 (Interrupt Enable Register 2) : AAH

7	6	5	4	3	2	1	0
–	–	–	INT16E	INT15E	INT14E	INT13E	–
–	–	–	R/W	R/W	R/W	R/W	–

Initial value : 00H

INT16E Enable or Disable Timer 3 Interrupt
0 Disable
1 Enable

INT15E Enable or Disable Timer 2 Interrupt
0 Disable
1 Enable

INT14E Enable or Disable Timer 1 Interrupt
0 Disable
1 Enable

INT13E Enable or Disable Timer 0 Interrupt
0 Disable
1 Enable

IE3 (Interrupt Enable Register 3) : ABH

7	6	5	4	3	2	1	0
–	–	–	INT22E	INT21E	INT20E	–	–
–	–	–	R/W	R/W	R/W	–	–

Initial value : 00H

INT22E Enable or Disable BIT Interrupt
0 Disable
1 Enable

INT21E Enable or Disable WDT Interrupt
0 Disable
1 Enable

INT20E Enable or Disable WT Interrupt
0 Disable
1 Enable

IP (Interrupt Priority Register) : B8H

7	6	5	4	3	2	1	0
–	–	IP5	IP4	IP3	IP2	IP1	IP0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP1 (Interrupt Priority Register 1) : F8H

7	6	5	4	3	2	1	0
–	–	IP15	IP14	IP13	IP12	IP11	IP10
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG (External Interrupt Flag Register) : A4H

7	6	5	4	3	2	1	0
–	–	–	–	–	–	FLAG12	FLAG10
–	–	–	–	–	–	R/W	R/W

Initial value : 00H

FLAG[1:0] When an external interrupt is occurred, the flag becomes ‘1’. The flag is cleared only by writing ‘0’ to the bit or automatically cleared by INT_ACK signal.

0 External Interrupt not occurred

1 External Interrupt occurred

EIPOL (External Interrupt Polarity Register): A5H

7	6	5	4	3	2	1	0
–	–	–	–	POL12		POL10	
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

POL[3:0] External Interrupt (EINT10/EINT12) Polarity Selection

POLn[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 10, 12

KFLAG (Key Interrupt Flag Register) : E8H

7	6	5	4	3	2	1	0
KFLAG7	KFLAG6	KFLAG5	KFLAG4	KFLAG3	KFLAG2	KFLAG1	KFLAG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

KFLAG[7:0] When key interrupt is occurred, the flag becomes '1'. The flag is cleared only by writing '0' to the bit. So, the flag should be cleared by software.

0 Key Interrupt 0~7 not occurred

1 Key Interrupt 0~7 occurred

Note) Do not use the "direct bit test and branch" instruction for input port, more detail information is at Appendix B.
Example) Avoid direct input port bit test and branch condition as below
If(KFLAG0) → if(KFLAG & 0x01)

KPOL1 (Key Interrupt Polarity 1 Register) : AFH

7	6	5	4	3	2	1	0
KPOL7		KPOL6		KPOL5		KPOL4	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

KPOL1[7:0] Key Interrupt (KEY4/KEY5/KEY6/KEY7) Polarity Selection

KPOL1n[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 4, 5, 6, and 7

KPOL0 (Key Interrupt Polarity 0 Register) : AEH

7	6	5	4	3	2	1	0
KPOL3		KPOL2		KPOL1		KPOL0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

KPOL0[7:0] Key Interrupt (KEY0/KEY1/KEY2/KEY3) Polarity Selection

KPOL0n[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 0, 1, 2, and 3

11. Peripheral Hardware

11.1 Clock Generator

11.1.1 Overview

As shown in Figure 11.1, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains main/sub-frequency clock oscillator. The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin. The default system clock is 1MHz INT-RC Oscillator and the default division rate is eight. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

- Calibrated Internal RC Oscillator (8 MHz)
  . INT-RC OSC/1 (8 MHz)
  . INT-RC OSC/2 (4 MHz)
  . INT-RC OSC/4 (2 MHz)
  . INT-RC OSC/8 (1 MHz, Default system clock)
- Main Crystal Oscillator (1~12 MHz)
- Sub Crystal Oscillator (32.768 kHz)
- Internal WDTRC Oscillator (60 kHz)

11.1.2 Block Diagram

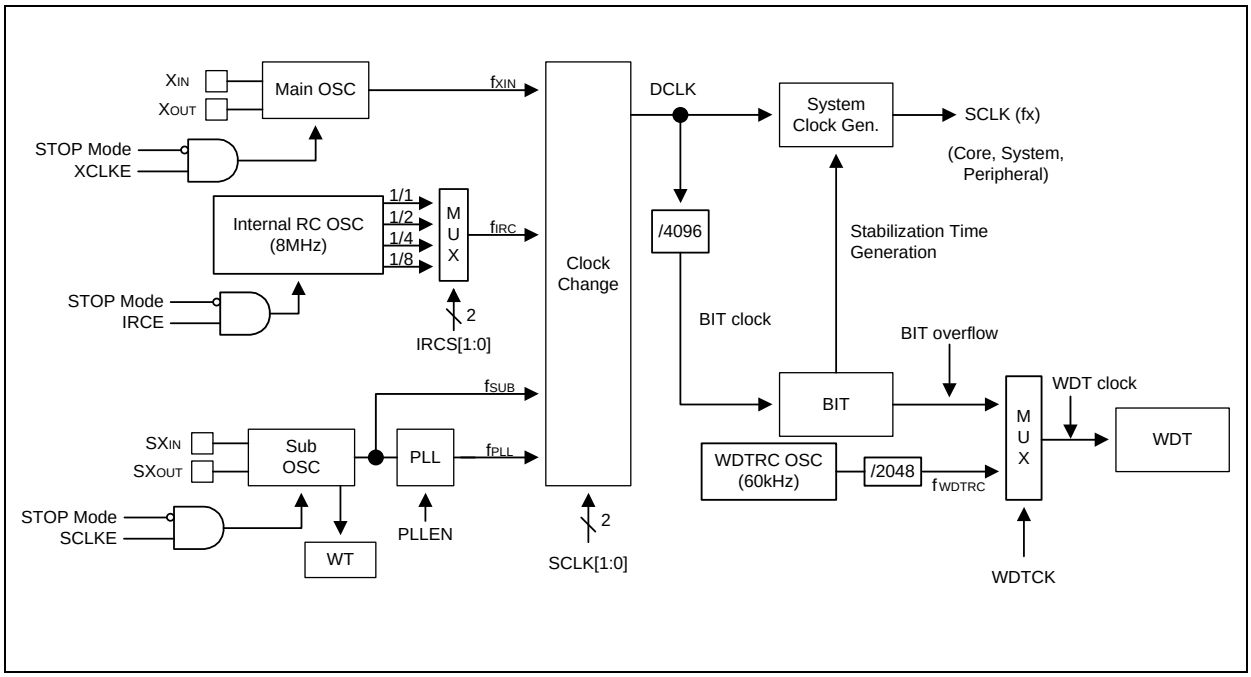


Figure 11.1 Clock Generator Block Diagram

11.1.3 PLL Circuit Diagram

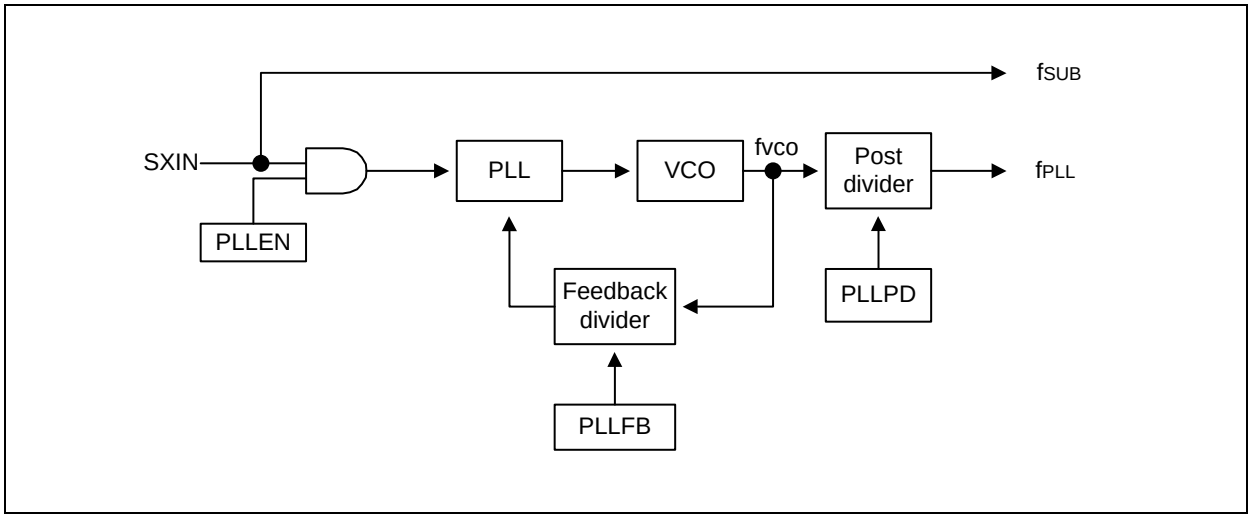


Figure 11.2 PLL Circuit Diagram

11.1.4 Register Map

Table 11-1 Clock Generator Register Map

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register
OSCCR	D9H	R/W	00H	Oscillator Control Register
PLLCR	FFH	R/W	00H	Phase Locked Loop Control Register

11.1.5 Clock Generator Register Description

The clock generator register uses clock control for system operation. The clock generation consists of system and clock control register (SCCR), oscillator control register (OSCCR) and phase locked loop control register (PLLCR).

11.1.6 Register Description for Clock Generator

SCCR (System and Clock Control Register) : 8AH

7	6	5	4	3	2	1	0
–	–	–	–	–	–	SCLK1	SCLK0
–	–	–	–	–	–	R/W	R/W

Initial value : 00H

SCLK [1:0] System Clock Selection Bit

SCLK1	SCLK0	Description
0	0	INT RC OSC for system clock
0	1	External Main OSC (f_{XIN}) for system clock
1	x	External Sub OSC (f_{SUB}) for system clock

Where x is “don’t care.”

OSCCR (Oscillator Control Register) : D9H

7	6	5	4	3	2	1	0
–	–	–	IRCS1	IRCS0	IRCE	XCLKE	SCLKE
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IRCS[1:0] Internal RC Oscillator Post-divider Selection

IRCS1	IRCS0	Description
0	0	INT-RC/8 (1MHz)
0	1	INT-RC/4 (2MHz)
1	0	INT-RC/2 (4MHz)
1	1	INT-RC/1 (8MHz)

IRCE Control the Operation of the Internal RC Oscillator

0	Enable operation of INT-RC OSC
1	Disable operation of INT-RC OSC

XCLKE Control the Operation of the External Main Oscillator

0	Disable operation of X-TAL
1	Enable operation of X-TAL

SCLKE Control the Operation of the External Sub Oscillator

0	Disable operation of SX-TAL
1	Enable operation of SX-TAL

PLLCR (Phase Locked Loop Control Register) : FFH

7	6	5	4	3	2	1	0
FPLL	–	PLLSTA	PLLFB1	PLLFB0	PLLPD1	PLLPD0	PLLEN
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

FPLL PLL Clock (f_{PLL}) Selection Bit

0 External Sub OSC (f_{SUB}) for system clock

1 PLL clock (f_{PLL}) for system clock

NOTE) When the sub oscillator is selected as system clock. (SCLK = 1xb)

PLLSTA PLL Locked/Unlocked Status Bits

0 PLL currently in unlocked state

1 PLL currently in locked state

PLLFB[1:0] PLL Feedback Divider Control Bit

PLLFB1	PLLFB0	Description
0	0	FBdiv = 610
0	1	FBdiv = 550
1	0	FBdiv = 428
1	1	FBdiv = 366

PLLPD[1:0] PLL Post Divider Control Bits

PLLPD1	PLLPD0	Description
0	0	M = 1
0	1	M = 2
1	0	M = 4
1	1	M = 8

PLLEN PLL Enable/Disable Control Bit

0 PLL Disable

1 PLL Enable

NOTES) 1. $f_{SUB} = f_{VCOIN}$ = 32.768 kHz, $f_{VCO} = (f_{VCOIN}$ x FB-divider), f_{OUT} / post divider

f_{VCO} = (32.768 kHz) x 610 = 19.98848 MHz

f_{VCO} = (32.768 kHz) x 550 = 18.0224 MHz

f_{VCO} = (32.768 kHz) x 428 = 14.024704 MHz

f_{VCO} = (32.768 kHz) x 366 = 11.993088 MHz

2. When system clock is f_{PLL}, should not be entered the STOP mode.

11.2 Basic Interval Timer

11.2.1 Overview

The MC96P6608/P6408 has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 11.3. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

The MC96P6608/6408 has these basic interval timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As timer function, timer interrupt occurrence

11.2.2 Block Diagram

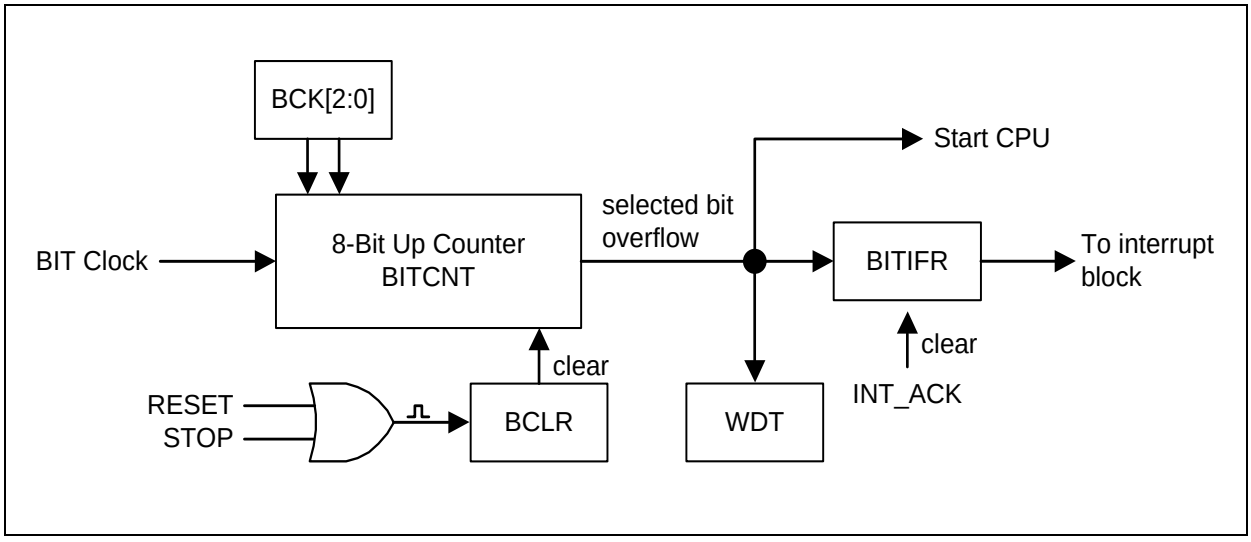


Figure 11.3 Basic Interval Timer Block Diagram

11.2.3 Register Map

Table 11-2 Basic Interval Timer Register Map

Name	Address	Dir	Default	Description
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register
BITCR	8BH	R/W	01H	Basic Interval Timer Control Register

11.2.4 Basic Interval Timer Register Description

The basic interval timer register consists of basic interval timer counter register (BITCNT) and basic interval timer control register (BITCR). If BCLR bit is set to '1', BITCNT becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared to '0' automatically.

11.2.5 Register Description for Basic Interval Timer

BITCNT (Basic Interval Timer Counter Register) : 8CH

7	6	5	4	3	2	1	0
BITCNT7	BITCNT6	BITCNT5	BITCNT4	BITCNT3	BITCNT2	BITCNT1	BITCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

BITCNT[7:0] BIT Counter

BITCR (Basic Interval Timer Control Register) : 8BH

7	6	5	4	3	2	1	0
BITIFR	–	–	–	BCLR	BCK2	BCK1	BCK0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value : 01H

BITIFR When BIT interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 BIT interrupt no generation

1 BIT interrupt generation

BCLR If this bit is written to '1', BIT Counter is cleared to '0'

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	Description
0	0	0	Bit 0 overflow (BIT Clock * 2)
0	0	1	Bit 1 overflow (BIT Clock * 4) (default)
0	1	0	Bit 2 overflow (BIT Clock * 8)
0	1	1	Bit 3 overflow (BIT Clock * 16)
1	0	0	Bit 4 overflow (BIT Clock * 32)
1	0	1	Bit 5 overflow (BIT Clock * 64)
1	1	0	Bit 6 overflow (BIT Clock * 128)
1	1	1	Bit 7 overflow (BIT Clock * 256)

11.3 Watch Dog Timer

11.3.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTCNT, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

11.3.2 WDT Interrupt Timing Waveform

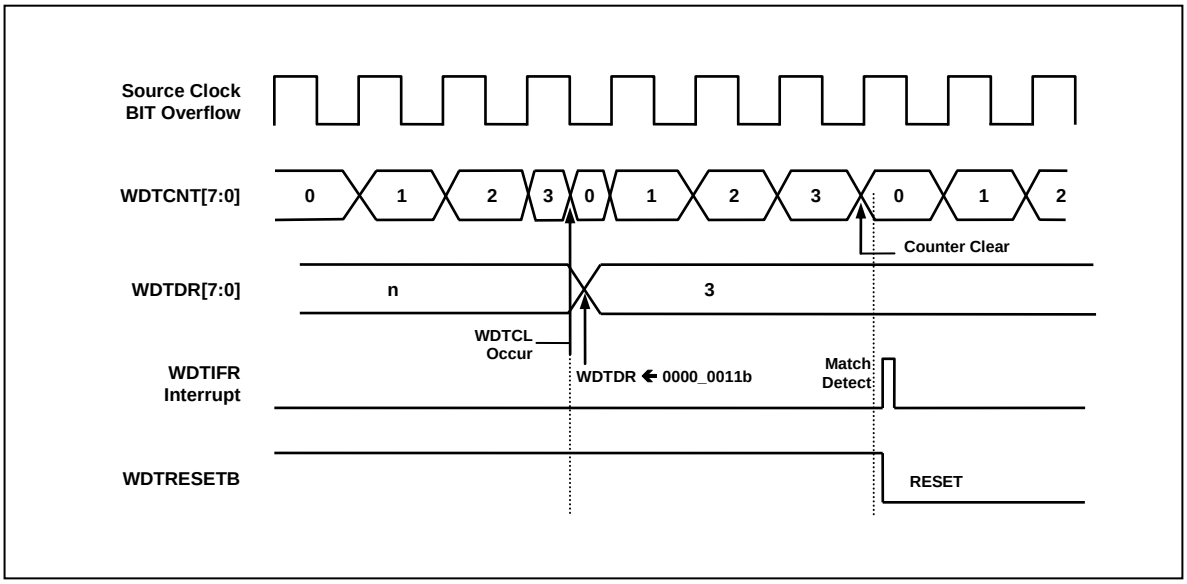


Figure 11.4 Watch Dog Timer Interrupt Timing Waveform

11.3.3 Block Diagram

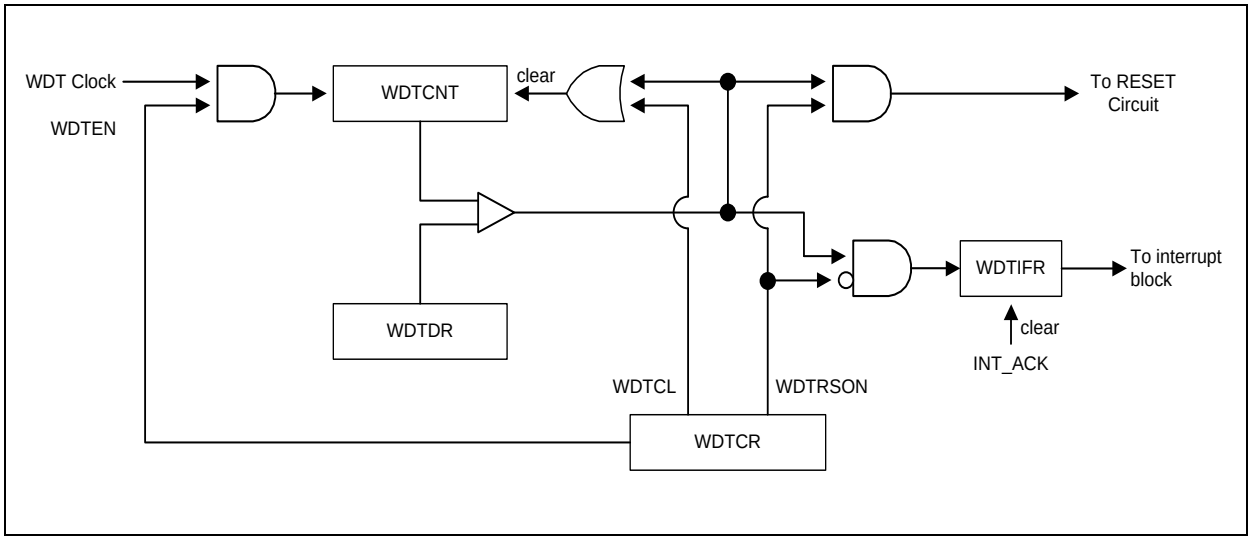


Figure 11.5 Watch Dog Timer Block Diagram

11.3.4 Register Map

Table 11-3 Watch Dog Timer Register Map

Name	Address	Dir	Default	Description
WDTCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTDR	8EH	W	FFH	Watch Dog Timer Data Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

11.3.5 Watch Dog Timer Register Description

The watch dog timer register consists of watch dog timer counter register (WDTCNT), watch dog timer data register (WDTDR) and watch dog timer control register (WDTCR).

11.3.6 Register Description for Watch Dog Timer

WDTCNT (Watch Dog Timer Counter Register: Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register: Write Case) : 8EH

7	6	5	4	3	2	1	0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value : FFH

WDTDR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTDR Value+1)
Note) Do not write “0” in the WDTDR register.

WDTCR (Watch Dog Timer Control Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	–	–	–	WDTCK	WDTIFR
R/W	R/W	R/W	–	–	–	R/W	R/W

Initial value : 00H

WDTEN Control WDT Operation
0 Disable
1 Enable

WDTRSON Control WDT RESET Operation
0 Free Running 8-bit timer
1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WDTCK Control WDT Clock Selection Bit
0 BIT overflow for WDT clock (WDTRC disable)
1 WDTRC for WDT clock (WDTRC enable)

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.
0 WDT Interrupt no generation
1 WDT Interrupt generation

11.4 Watch Timer

11.4.1 Overview

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit, and watch timer control register. To operate the watch timer, determine the input clock source, output interval, and set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock is able to be so alive that WT can continue the operation. The watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to raise resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

The watch timer supplies the clock frequency for the LCD driver (f_{LCD}). Therefore, if the watch timer is disabled, the LCD driver controller does not operate.

11.4.2 Block Diagram

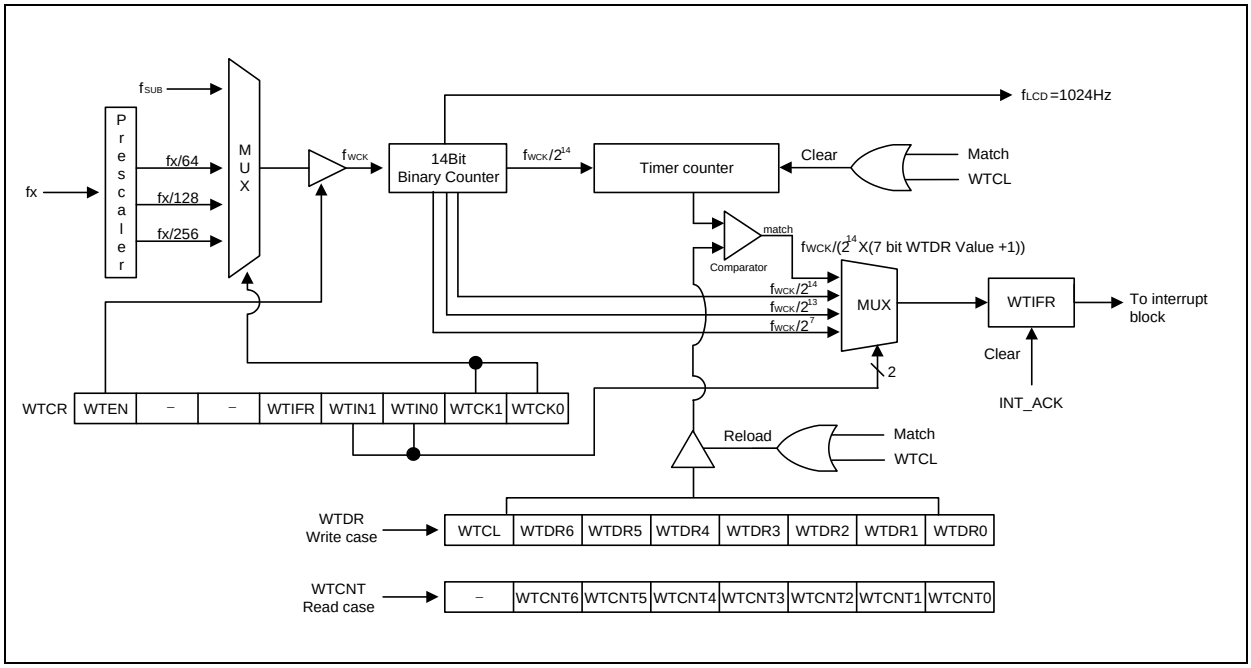


Figure 11.6 Watch Timer Block Diagram

11.4.3 Register Map

Table 11-4 Watch Timer Register Map

Name	Address	Dir	Default	Description
WTCNT	9FH	R	00H	Watch Timer Counter Register
WTDR	9FH	W	7FH	Watch Timer Data Register
WTCR	9EH	R/W	00H	Watch Timer Control Register

11.4.4 Watch Timer Register Description

The watch timer register consists of watch timer counter register (WTCNT), watch timer data register (WTDR), and watch timer control register (WTCR). As WTCR is 6-bit writable/ readable register, WTCR can control the clock source (WTCK[1:0]), interrupt interval (WTIN[1:0]), and function enable/disable (WTEN). Also there is WT interrupt flag bit (WTIFR).

11.4.5 Register Description for Watch Timer

WTCNT (Watch Timer Counter Register: Read Case) : 9FH

7	6	5	4	3	2	1	0
–	WTCNT6	WTCNT5	WTCNT4	WTCNT3	WTCNT2	WTCNT1	WTCNT0
–	R	R	R	R	R	R	R

Initial value : 00H

WTCNT[6:0] WT Counter

WTDR (Watch Timer Data Register: Write Case) : 9FH

7	6	5	4	3	2	1	0
WTCL	WTDR6	WTDR5	WTDR4	WTDR3	WTDR2	WTDR1	WTDR0
R/W	W	W	W	W	W	W	W

Initial value : 7FH

WTCL Clear WT Counter

0 Free Run

1 Clear WT Counter (auto clear after 1 Cycle)

WTDR[6:0] Set WT Period

WT Interrupt Interval=fwck/(2^14 x(7bit WTDR Value+1))

NOTE) Do not write “0” in the WTDR register.

WTCR (Watch Timer Control Register) : 9EH

7	6	5	4	3	2	1	0
WTEN	–	–	WTIFR	WTIN1	WTIN0	WTCK1	WTCK0
R/W	–	–	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

WTEN Control Watch Timer

0 Disable

1 Enable

WTIFR When WT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 WT Interrupt no generation

1 WT Interrupt generation

WTIN[1:0] Determine Interrupt Interval

WTIN1	WTIN0	Description
0	0	f_{WCK}/2^7
0	1	f_{WCK}/2^13
1	0	f_{WCK}/2^14
1	1	f_{WCK}/(2^14 x (7bit WTDR Value+1))

WTCK[1:0] Determine Source Clock

WTCK1	WTCK0	Description
0	0	f_{SUB}
0	1	f_X/256
1	0	f_X/128
1	1	f_X/64

NOTE) f_X – System clock frequency (Where fx= 4.19MHz)

f_{SUB} – Sub clock oscillator frequency (32.768kHz)

f_{WCK} – Selected Watch timer clock

f_{LCD} – LCD frequency (Where f_X= 4.19MHz, WTCK[1:0]='10'; f_{LCD}= 1024Hz)

11.5 Timer 0, 1

11.5.1 Overview

Timer 0 and timer 1 can be used either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register, capture data register, carrier mode control register and timer interrupt flag register. (T0CNT, T0DR, T0CDR, T0CR, T1CNT, T1DRH, T1DRL, T1CDR, T1CR, CARCR, TIFR).

It has five operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 16-bit timer/counter mode
- 16-bit capture mode
- Carrier mode

The timer/counter 0 and 1 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T0CK[2:0], T1CK[2:0]).

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048, EC0

- TIMER1 clock source: f_X/1, 2, 4, 8, 64, 256, 512, 1024

In the capture mode, by EINT10, the data is captured into input capture data register (T0CDR, T1CDR).
In 8-bit timer/counter 0/1 mode, whenever counter value is equal to T0DR/T1DRH, T0O/REM port toggles. Also In 16-bit timer/counter 0 mode, Timer 0 outputs the comparison result between counter and data register through T0O port.
In the carrier mode, Timer 1 can be used to generate the carrier frequency or a remote controller signal. Timer 1 can output the comparison result between T1CNT & T1DRH/L and carrier frequency through REM port. T1CNT value is cleared by hardware.

Table 11-5 Timer 0/1 Operating Modes

16BIT0	T0MS	T1MS	T0CK[2:0]	T1CK[2:0]	Timer 0	Timer 1
0	0	0	XXX	XXX	8 Bit Timer/Counter Mode	8 Bit Timer/Counter Mode
0	1	0	XXX	XXX	8 Bit Capture Mode	-
0	0	1	XXX	XXX	-	Carrier Mode
1	0	0	XXX	XXX	16 Bit Tamer/Counter Mode	
1	1	0	XXX	XXX	16 Bit Capture Mode	

11.5.2 8-Bit Timer/Counter 0, 1 Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 11.7.

The two 8-bit timers have each counter and data register. The counter register is increased by internal or external clock input. Timer 0 can use the input clock with one of 2, 4, 8, 32, 128, 512 , 2048 and EC0 prescaler division rates (T0CK[2:0]). Timer 1 can use the input clock with one of 1, 2, 4, 8, 64, 256, 512, and 1024 prescaler division rates (T1CK[2:0]). When the value of T0CNT, T1CNT and T0DR, T1DRH are respectively identical in Timer 0, 1, the interrupt of Timer 0, 1 occurs.

The external clock (EC0) counts up the timer at the rising edge. If the EC0 is selected as a clock source by T0CK[2:0], EC0 port should be set to the input port by P01IO bit

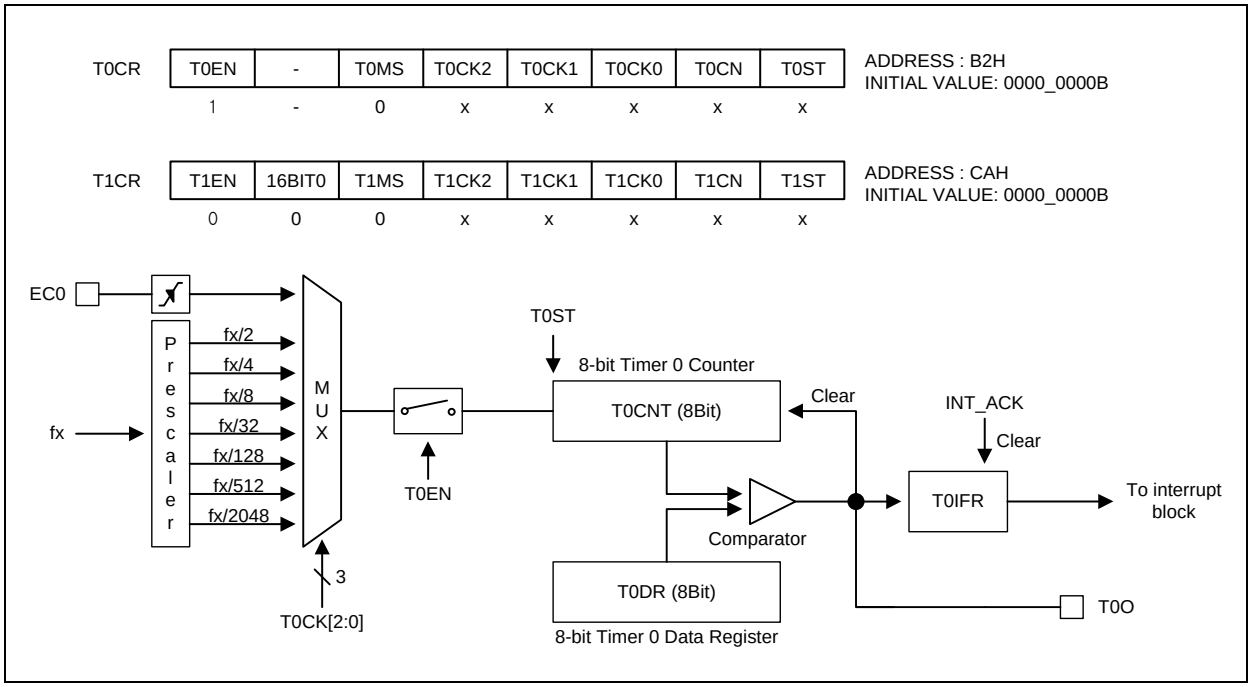


Figure 11.7 8-Bit Timer/Event Counter Mode for Timer 0

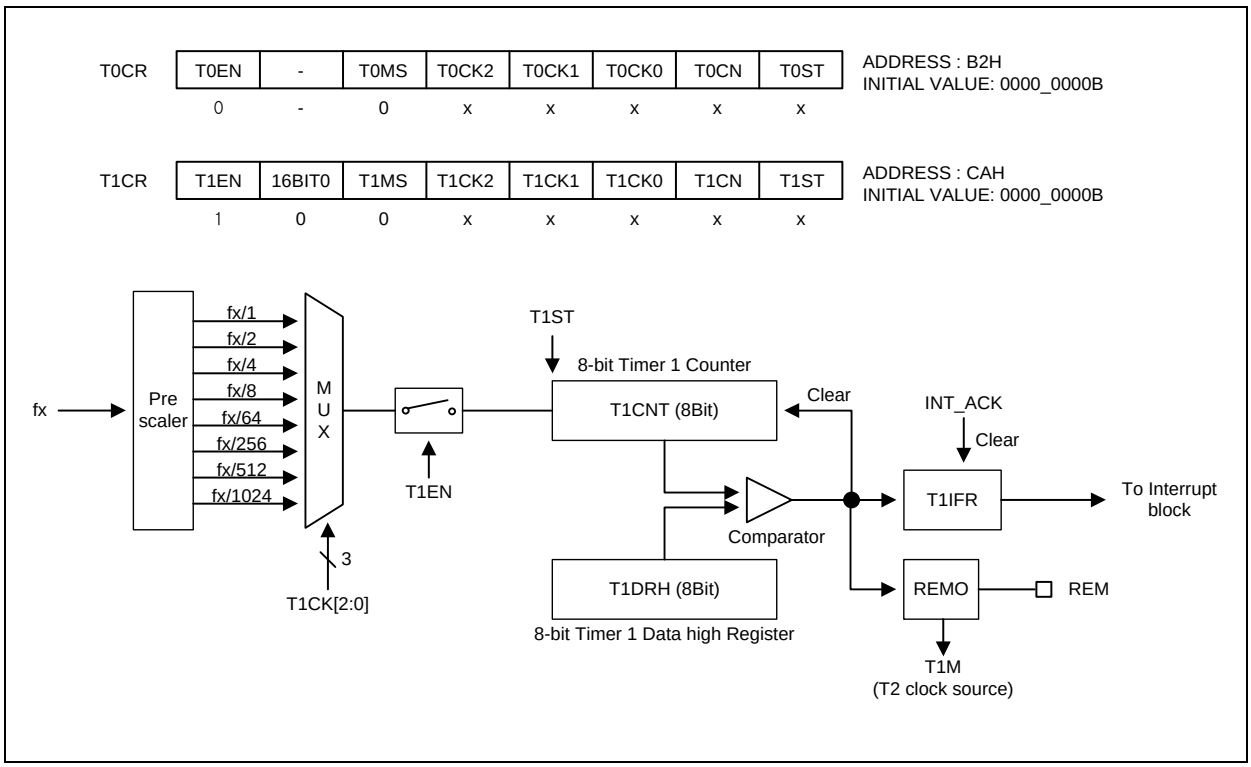


Figure 11.8 8-Bit Timer Counter Mode for Timer 1

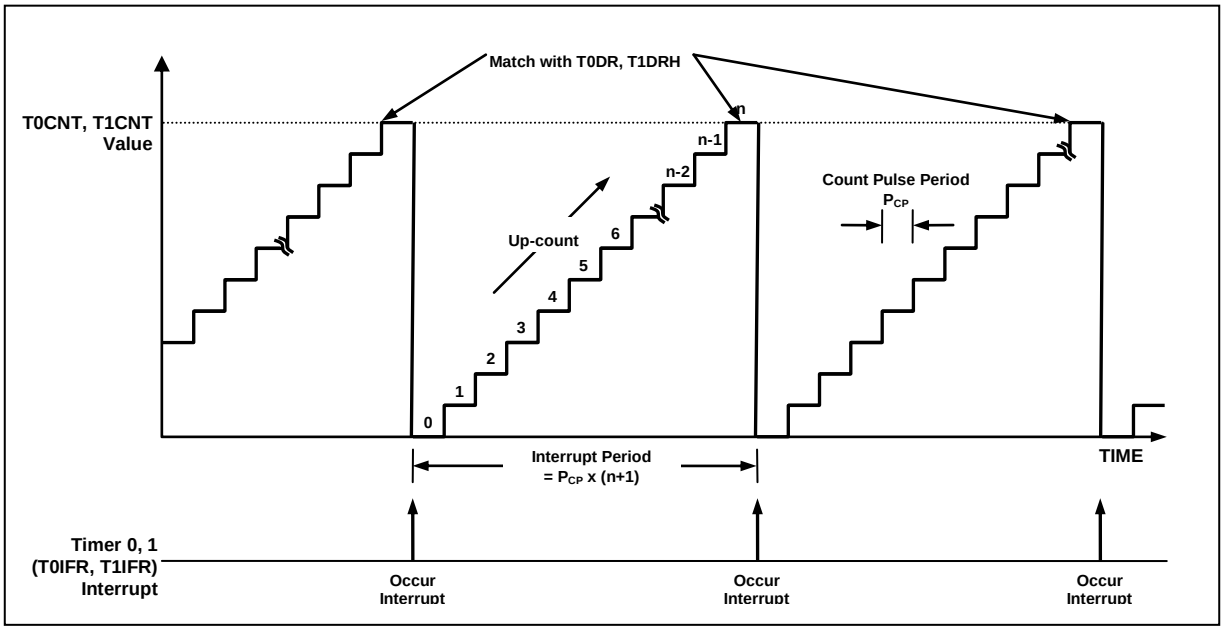


Figure 11.9 8-Bit Timer/Counter 0, 1 Example

11.5.3 16-Bit Timer/Counter 0 Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 11.10.

The timer register is being run with all 16 bits. A 16-bit timer/counter register T0CNT, T1CNT are incremented 0000H to FFFFFH until it matches T0DR, T1DRH and then resets to 0000H. The match output generates the Timer 0 interrupt (No Timer 1 interrupt). The clock source is selected from T0CK[2:0] and 16BIT0 bit must be set to '1'. Timer 0 is LSB 8-bit, the timer 1 is MSB 8-bit.

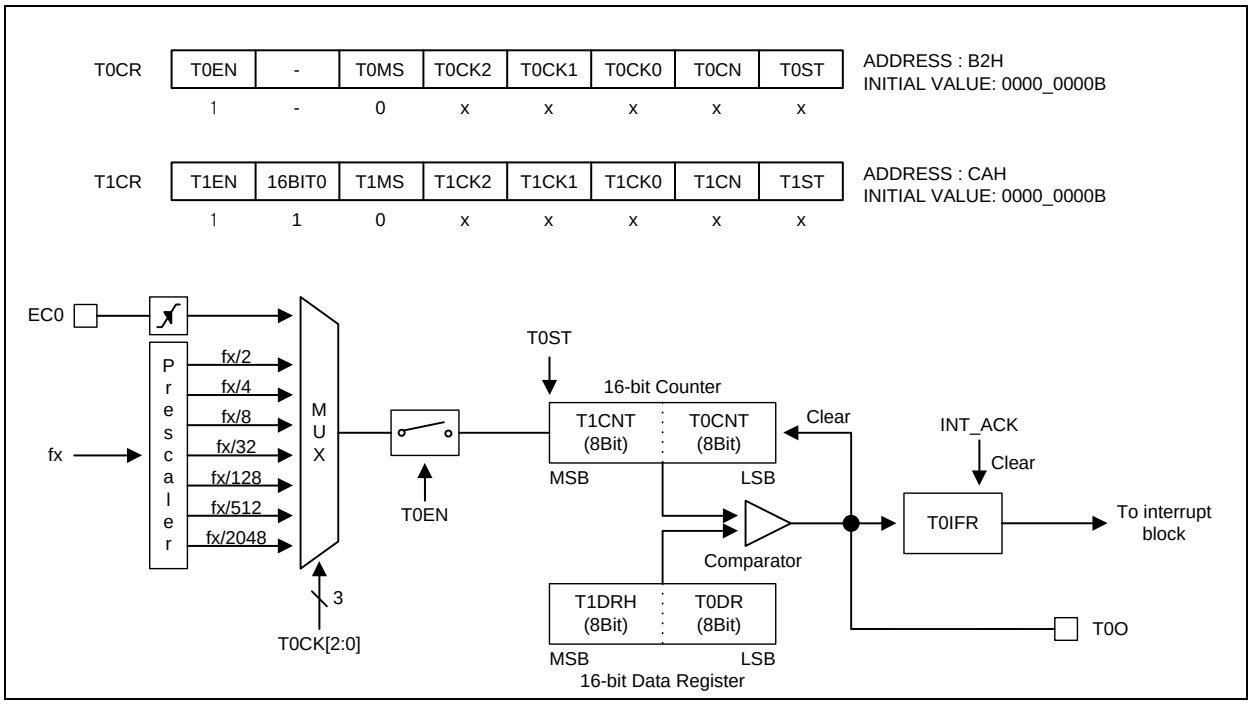


Figure 11.10 16-Bit Timer/Event Counter Mode for Timer 0

11.5.4 8-Bit Timer 0 Capture Mode

The 8-bit Capture mode is selected by control register as shown in Figure 11.11.

The timer 0 capture mode is set by T0MS as '1'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode and the interrupt occurs when T0CNT is equal to T0DR. T0CNT value is automatically cleared by hardware and it can be also cleared by software (T0ST).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0CDR. In the timer 0 capture mode, timer 0 output (T0O) waveform is not available.

According to the EIPOL register setting, the external interrupt EINT10 function is chose. Of course, the EINT10 pin must be set to an input port.

T0CDR and T0DR are in the same address. In the capture mode, reading operation reads T0CDR, not T0DR and writing operation will update T0DR.

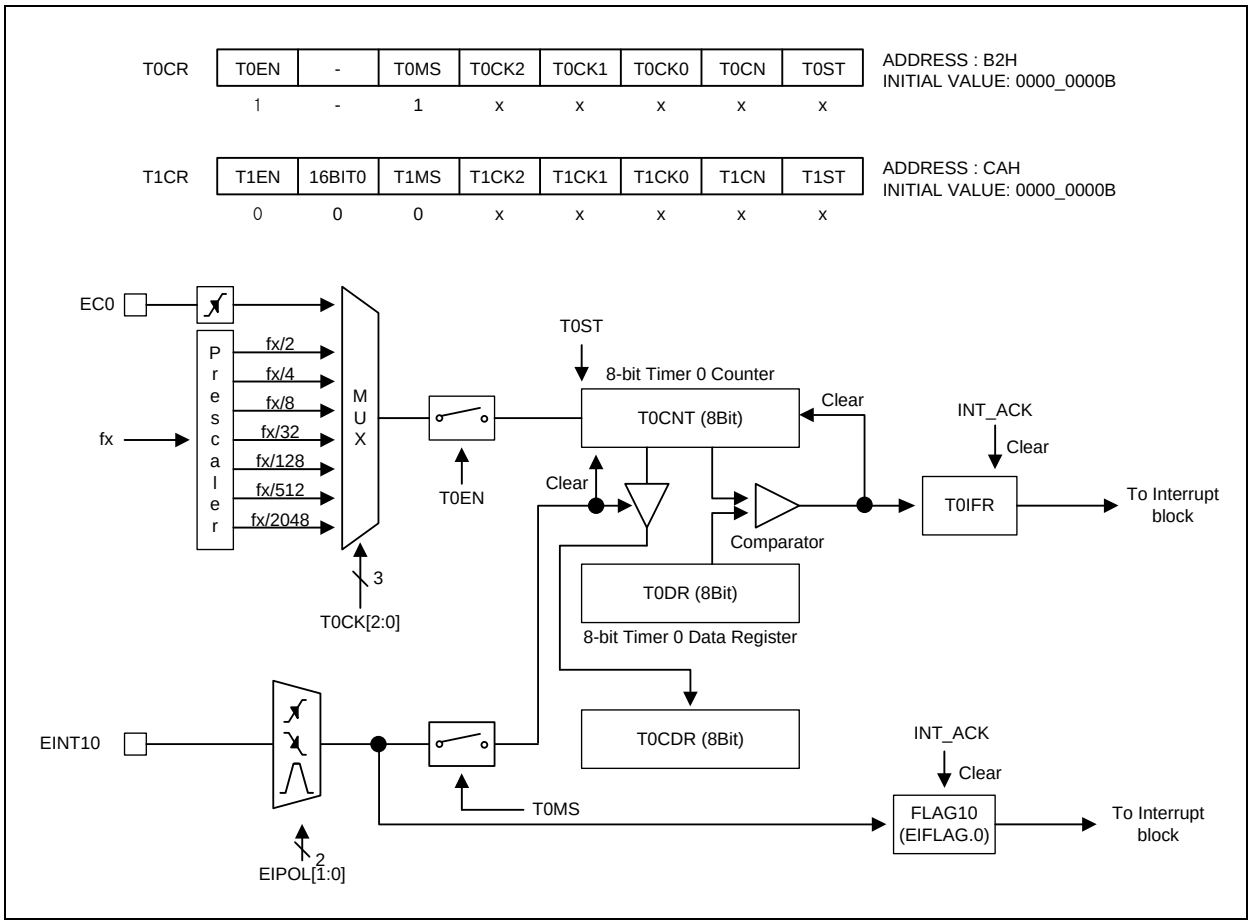


Figure 11.11 8-Bit Capture Mode for Timer 0

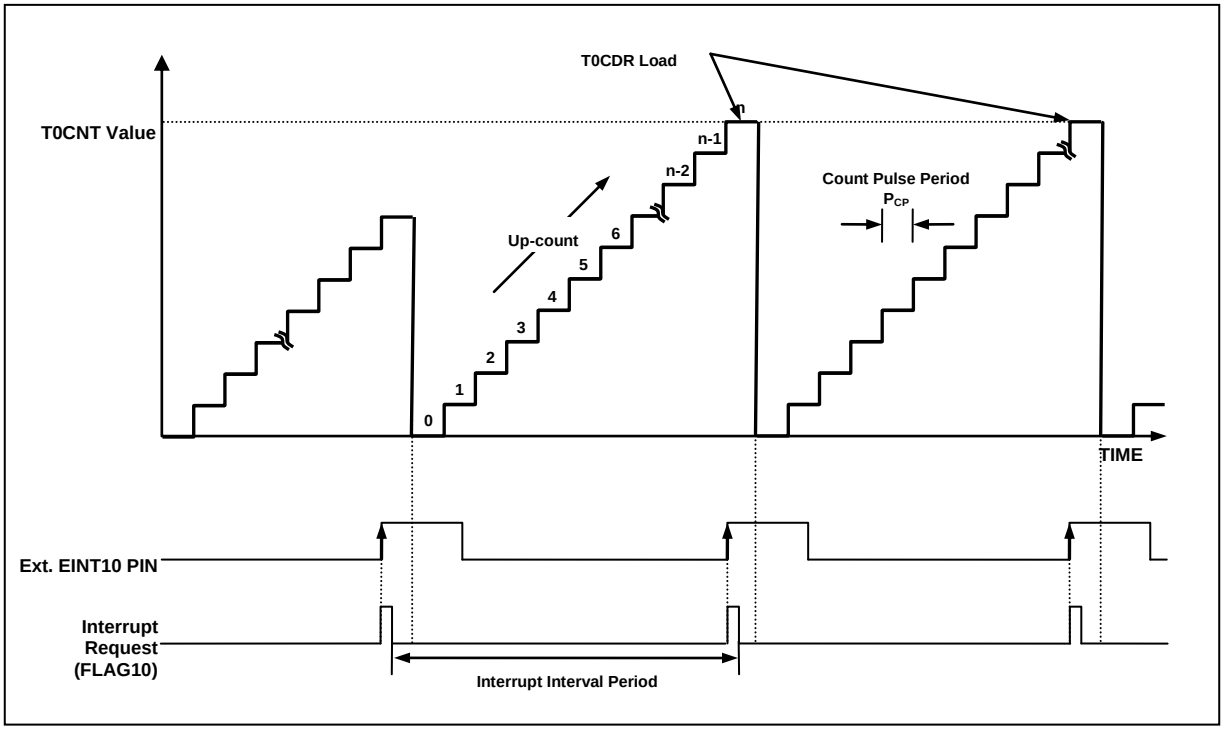


Figure 11.12 Input Capture Mode Operation for Timer 0

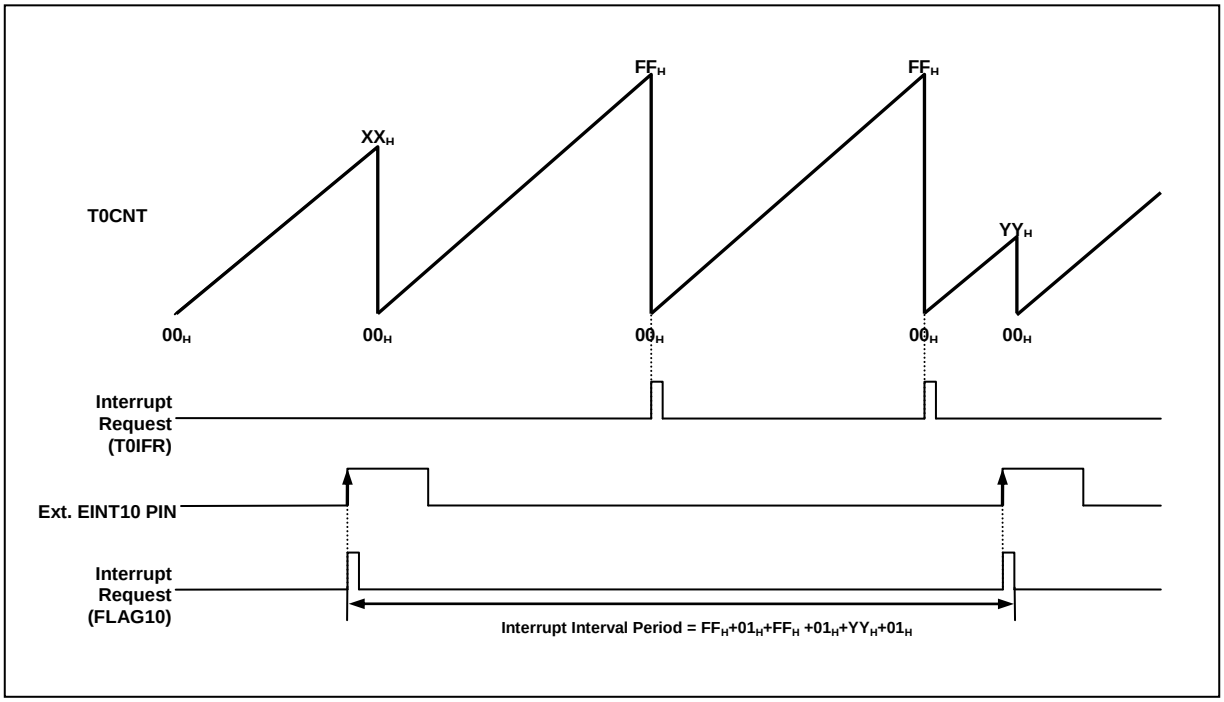


Figure 11.13 Express Timer Overflow in Capture Mode

11.5.5 16-Bit Timer 0 Capture Mode

The 16-bit capture mode is selected by control register as shown in Figure 11.14.

The 16-bit capture mode is the same operation as 8-bit capture mode, except that the timer register uses 16 bits. The clock source is selected from T0CK[2:0] and 16BIT0 bit must be set to '1'.

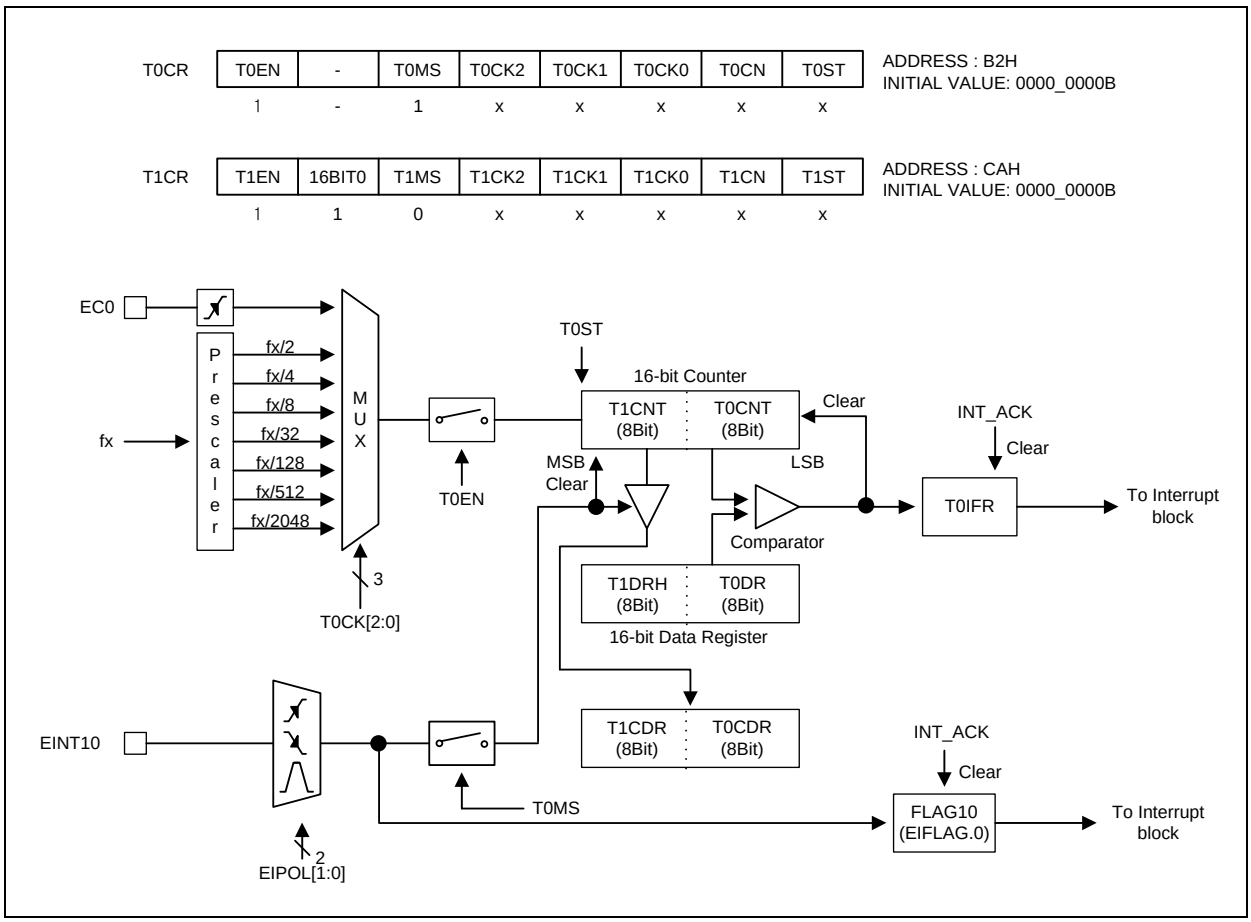


Figure 11.14 16-Bit Capture Mode for Timer 0

11.5.6 8-Bit Timer 1 Carrier Frequency Mode.

The carrier frequency and the pulse of data are calculated by the formula in the following sheet .The Figure 11.15 shows the block diagram of Timer 1 for carrier frequency mode.

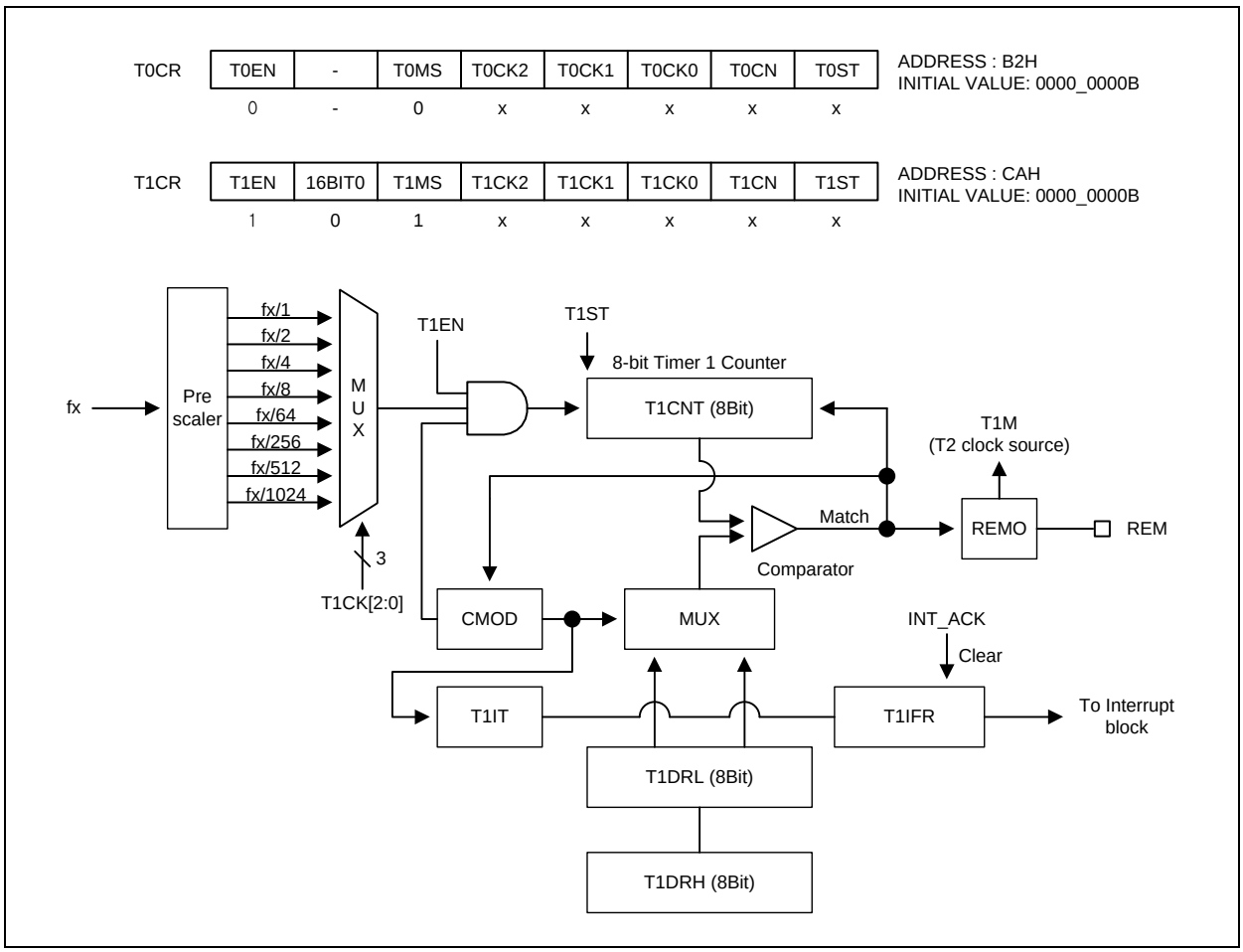
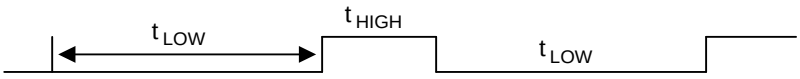


Figure 11.15 Carrier Mode for Timer 1

NOTE) When one of T1DRH and T1DRL values is “00H”, the carrier frequency generator (REM) output always becomes a “High” or “Low”. At that time, Timer 1 Interrupt Flag Bit (T1IFR) is not set.

11.5.7 Carrier Output Pulse Width Calculations



To generate the above repeated waveform consisted of low period time (t_{LOW}), and high period time (t_{HIGH}).

When REMO = 0,

t_{LOW} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH < 100H, where f_{T1} = The selected clock.

When REMO = 1,

t_{LOW} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH < 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

To make t_{LOW} = 24 us and t_{HIGH} = 15 us. f_X = 4 MHz, f_{T1} = 4 MHz/4 = 1 MHz

When REMO = 0,

t_{LOW} = 24 us = (T1DRL + 1) /f_{T1} = (T1DRL + 1) x 1us, T1DRL = 22.

t_{HIGH} = 15 us = (T1DRH + 1) /f_{T1} = (T1DRH + 1) x 1us, T1DRH = 13.

When REMO = 1,

t_{LOW} = 24 us = (T1DRH + 1) / f_{T1} = (T1DRH + 1) x 1us, T1DRH = 22.

t_{HIGH} = 15 us = (T1DRL + 1) / f_{T1} = (T1DRL + 1) x 1us, T1DRL = 13.

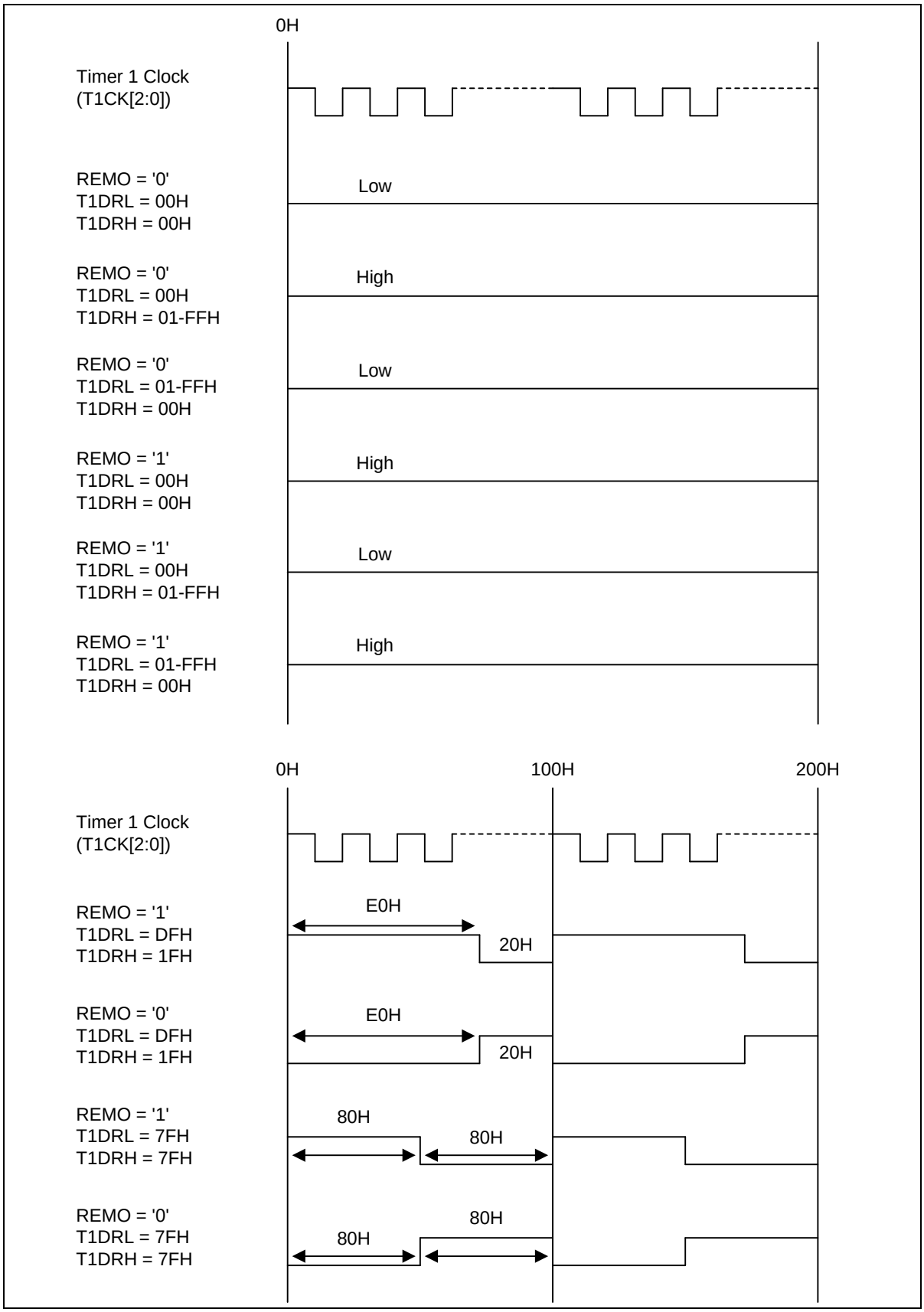


Figure 11.16 Carrier Output Waveforms in Repeat Mode for Timer 1

11.5.8 Block Diagram

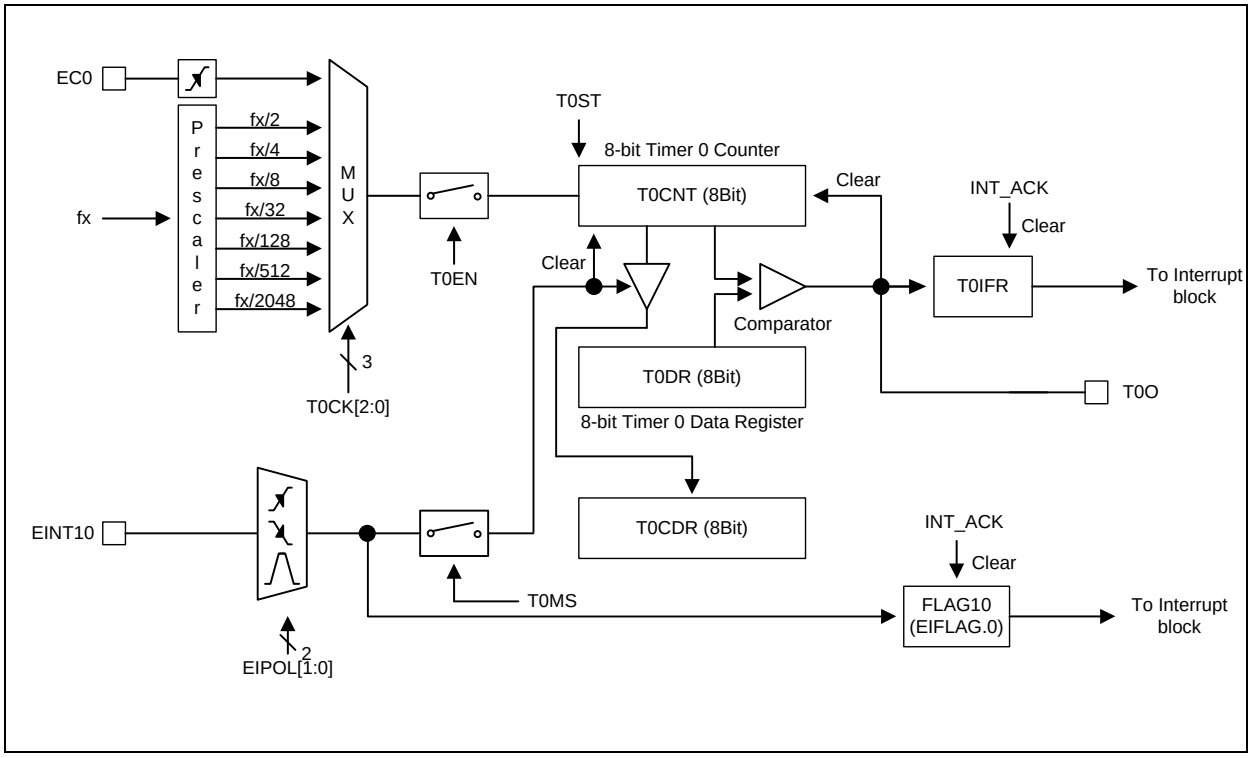


Figure 11.17 8-Bit Timer 0 Block Diagram

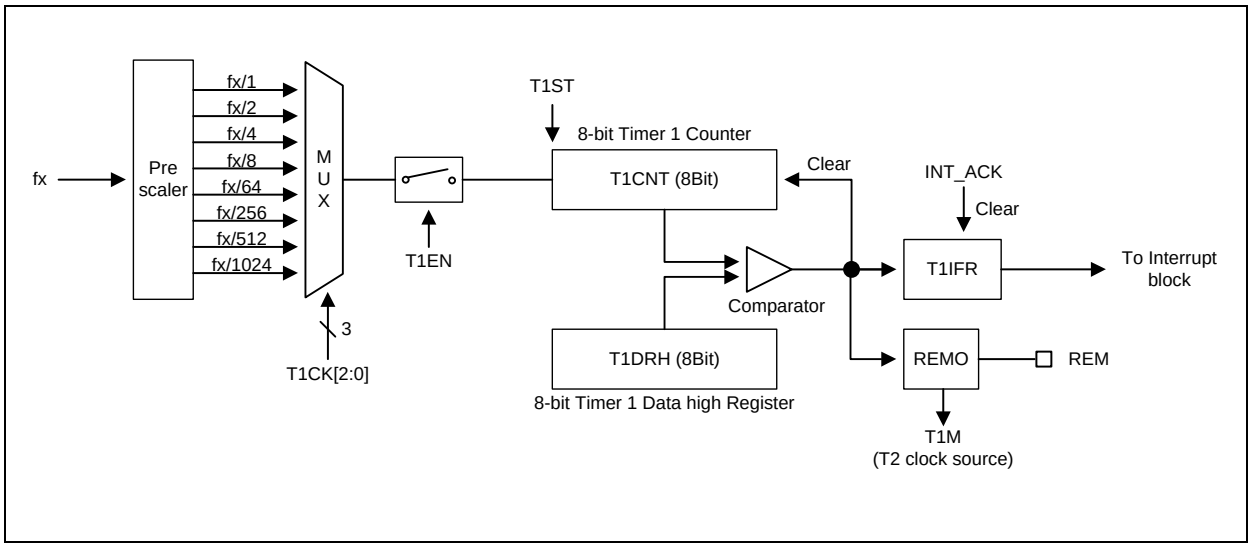


Figure 11.18 8-Bit Timer Counter 1 Block Diagram

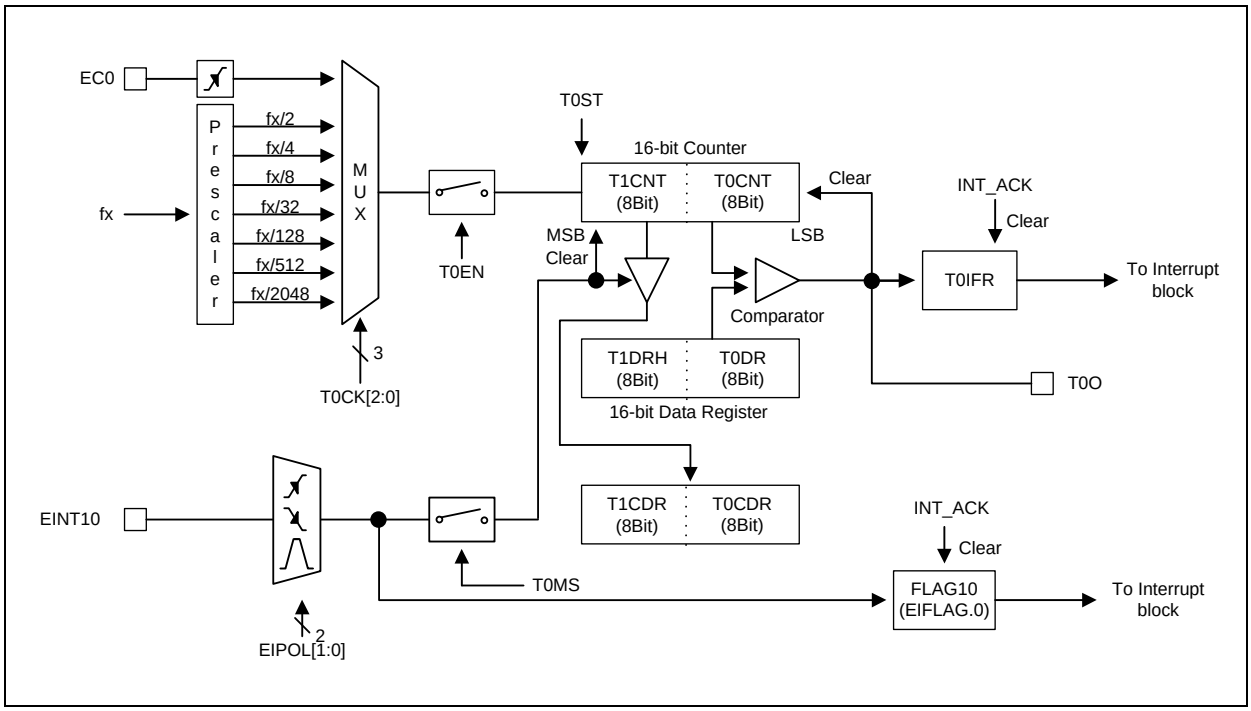


Figure 11.19 16-Bit Timer/Event Counter 0 Block Diagram

11.5.9 Register Map

Table 11-6 Timer 0, 1 Register Map

Name	Address	Dir	Default	Description
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register
T0CDR	B4H	R	00H	Timer 0 Capture Data Register
T0CR	B2H	R/W	00H	Timer 0 Control Register
T1CNT	CBH	R	00H	Timer 1 Counter Register
T1DRH	CDH	R/W	FFH	Timer 1 Data High Register
T1DRL	CCH	R/W	FFH	Timer 1 Data Low Register
T1CDR	CDH	R	00H	Timer 1 Capture Data Register
T1CR	CAH	R/W	00H	Timer 1 Control Register
CARCR	CEH	R/W	00H	Carrier Mode Control Register
TIFR	C3H	R/W	00H	Timer Interrupt Flag Register

11.5.9.1 Timer/Counter 0, 1 Register Description

The timer/counter 0, 1 register consists of timer 0 counter register (T0CNT), timer 0 data register (T0DR), timer 0 capture data register (T0CDR), timer 0 control register (T0CR), timer 1 counter register (T1CNT), timer 1 data high/low register (T1DRH/L), timer 1 capture data register (T1CDR), timer 1 control register (T1CR) and carrier mode control register(CARCR). T0IFR and T1IFR bits are in the timer interrupt flag register (TIFR).

11.5.9.2 Register Description for Timer/Counter 0, 1

T0CNT (Timer 0 Counter Register) : B3H

7	6	5	4	3	2	1	0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T0CNT[7:0] T0 Counter

T0DR (Timer 0 Data Register) : B4H

7	6	5	4	3	2	1	0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T0DR[7:0] T0 Data

T0CDR (Timer 0 Capture Data Register: Read Case, Capture mode only) : B4H

7	6	5	4	3	2	1	0
T0CDR7	T0CDR6	T0CDR5	T0CDR4	T0CDR3	T0CDR2	T0CDR1	T0CDR0
R	R	R	R	R	R	R	R

Initial value : 00H

T0CDR[7:0] T0 Capture

T0CR (Timer 0 Control Register) : B2H

7	6	5	4	3	2	1	0
T0EN	–	T0MS	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T0EN Control Timer 0

0 Timer 0 disable

1 Timer 0 enable

T0MS Control Timer 0 Operation Mode

0 Timer/Counter mode

1 Capture mode

T0CK[2:0] Select Timer 0 clock source. fx is a system clock frequency

T0CK2	T0CK1	T0CK0	Description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/32
1	0	0	fx/128
1	0	1	fx/512
1	1	0	fx/2048
1	1	1	External Clock (EC0)

T0CN Clear Timer 0 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T0ST Control Timer 0 Start/Stop

0 Counter stop

1 Clear counter and start

NOTE) Match Interrupt is generated in Capture mode.

T1CNT (Timer 1 Counter Register) : CBH

7	6	5	4	3	2	1	0
T1CNT7	T1CNT6	T1CNT5	T1CNT4	T1CNT3	T1CNT2	T1CNT1	T1CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T1CNT[7:0] T1 Counter

T1DRH (Timer 1 Data High Register) : CDH

7	6	5	4	3	2	1	0
T1DRH7	T1DRH6	T1DRH5	T1DRH4	T1DRH3	T1DRH2	T1DRH1	T1DRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T1DRH[7:0] T1 Data High

T1DRL (Timer 1 Data Low Register: Carrier mode only) : CCH

7	6	5	4	3	2	1	0
T1DRL7	T1DRL6	T1DRL5	T1DRL4	T1DRL3	T1DRL2	T1DRL1	T1DRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T1DRL[7:0] T1 Data Low

T1CDR (Timer 1 Capture Data Register: Read Case, 16bit Capture mode only) : CDH

7	6	5	4	3	2	1	0
T1CDR7	T1CDR6	T1CDR5	T1CDR4	T1CDR3	T1CDR2	T1CDR1	T1CDR0
R	R	R	R	R	R/	R	R

Initial value : 00H

T1CDR[7:0] 16bit T0 Capture

T1CR (Timer 1 Control Register) : CAH

7	6	5	4	3	2	1	0
T1EN	16BIT0	T1MS	T1CK2	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T1EN Control Timer 1

0 Timer 1 disable

1 Timer 1 enable

16BIT0 Select Timer 1 8/16Bit

0 8 Bit

1 16 Bit

T1MS Control Timer 1 Operation Mode

0 Timer/counter mode

1 Carrier mode

T1CK[2:0] Select Timer 1 clock source. fx is main system clock frequency

T1CK2	T1CK1	T1CK0	Description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/4
0	1	1	fx/8
1	0	0	fx/64
1	0	1	fx/256
1	1	0	fx/512
1	1	1	fx/1024

T1CN Control Timer 1 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T1ST Control Timer 1 Start/Stop

0 Counter stop

1 Clear counter and start

CARCR (Carrier Control Register: Carrier mode only) : CEH

7	6	5	4	3	2	1	0
–	–	T1IT1	T1IT0	–	–	CMOD	REMO
–	–	R/W	R/W	–	–	R/W	R/W

Initial value : 00H

T1IT[1:0] T1 Interrupt Time Select

T1IT1	T1IT0	Description
0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data value
1	1	Not available

CMOD Carrier Frequency Mode Select

0 One-shot mode

1 Repeating mode

REMO REM Output Control

0 T1DRL→ Low width, T1DRH→ High width

1 T1DRL→ High width, T1DRH→ Low width

TIFR (Timer Interrupt Flag Register) : C3H

7	6	5	4	3	2	1	0
SIOIFR	–	–	–	T3IFR	T2IFR	T1IFR	T0IFR
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value : 00H

SIOIFR When SIO interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 SIO Interrupt no generation

1 SIO Interrupt generation

NOTE) For clearing this bit, use “ANL” instruction.

T3IFR When T3 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T3 Interrupt no generation

1 T3 Interrupt generation

T2IFR When T2 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T2 Interrupt no generation

1 T2 Interrupt generation

T1IFR When T1 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T1 Interrupt no generation

1 T1 Interrupt generation

T0IFR When T0 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T0 Interrupt no generation

1 T0 Interrupt generation

11.6 Timer 2, 3

11.6.1 Overview

Timer 2 and timer 3 can be used either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register, capture data register and timer interrupt flag register. (T2CNT, T2DR, T2CDR, T2CR, T3CNT, T3DR, T3CDR, T3CR, TIFR).

It has five operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 16-bit timer/counter mode
- 16-bit capture mode

The timer/counter 2 and 3 can be clocked by an internal or an external clock source (EC2). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T2CK[2:0], T3CK[2:0]).

- TIMER2 clock source: f_X/4, 16, 64, 256, 1024, 4096, T1M, EC2

- TIMER3 clock source: f_X/1, 2, 32, 128, 256, 512, 1024, 2048

In the capture mode, by EINT12, the data is captured into input capture data register (T2CDR, T3CDR).
In 8-bit timer/counter 2/3 mode, whenever counter value is equal to T2DR/T2CDR, T2O port toggles. Also In 16-bit timer/counter 2 mode, Timer 2 outputs the comparison result between counter and data register through T2O port.

Table 11-7 Timer 2/3 Operating Modes

16BIT2	T2MS	T2CK[2:0]	T3CK[2:0]	Timer 2	Timer 3
0	0	XXX	XXX	8 Bit Timer/Counter Mode	8 Bit Timer/Counter Mode
0	1	XXX	XXX	8 Bit Capture Mode	-
1	0	XXX	XXX	16 Bit Timer/Counter Mode	
1	1	XXX	XXX	16 Bit Capture Mode	

11.6.2 8-Bit Timer/Counter 2, 3 Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 11.20.

The two 8-bit timers have each counter and data register. The counter register is increased by internal or external clock input. Timer 2 can use the input clock with one of 4, 16, 64, 256, 1024, 4096, T1M and EC2 prescaler division rates (T2CK[2:0]). Timer 3 can use the input clock with one of 1, 2, 32, 128, 256, 512, 1024, and 2048. When the value of T2CNT, T3CNT and T2DR, T3DR are respectively identical in Timer 2, 3, the interrupt of Timer 2, 3 occurs.

The external clock (EC2) counts up the timer at the rising edge. If the EC2 is selected as a clock source by T2CK[2:0], EC2 port becomes input port.

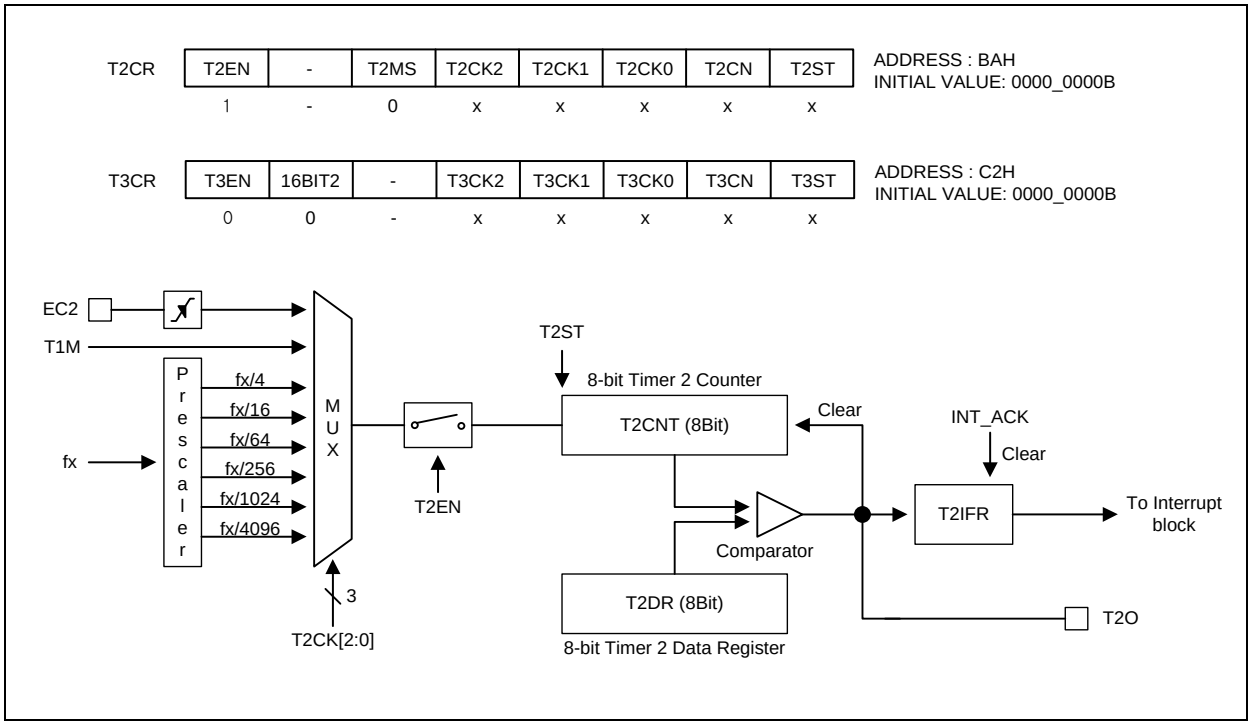


Figure 11.20 8-Bit Timer/Event Counter Mode for Timer 2

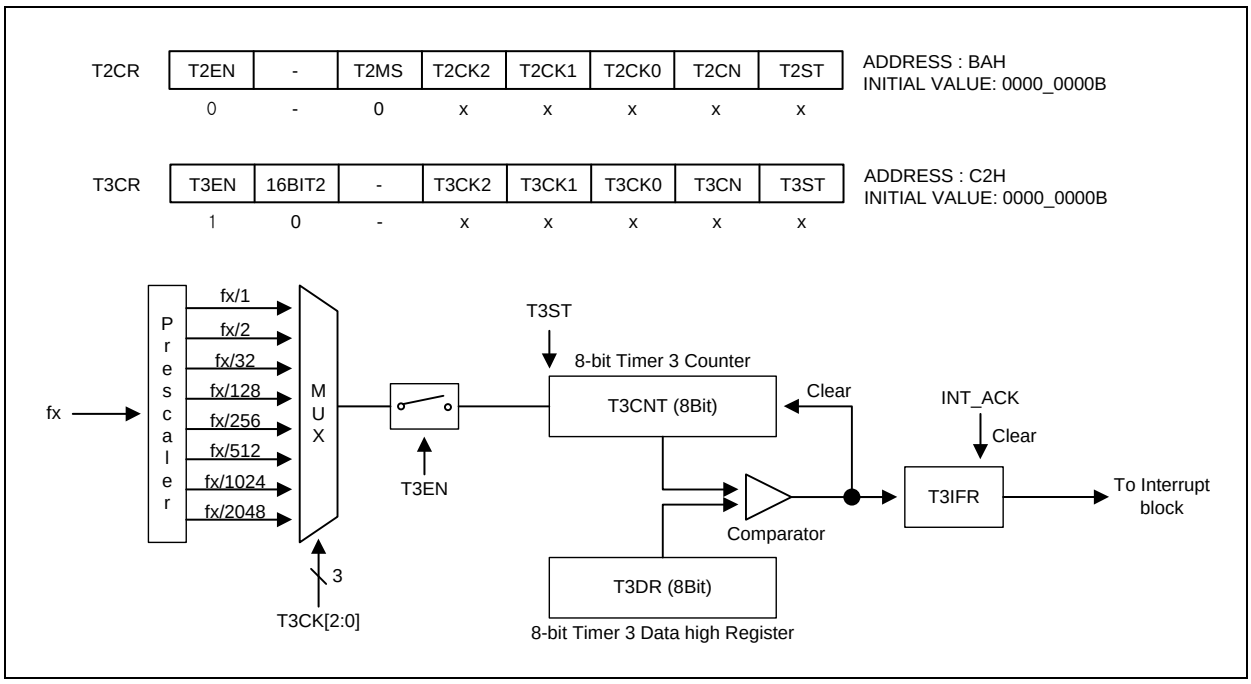


Figure 11.21 8-Bit Timer Counter Mode for Timer 3

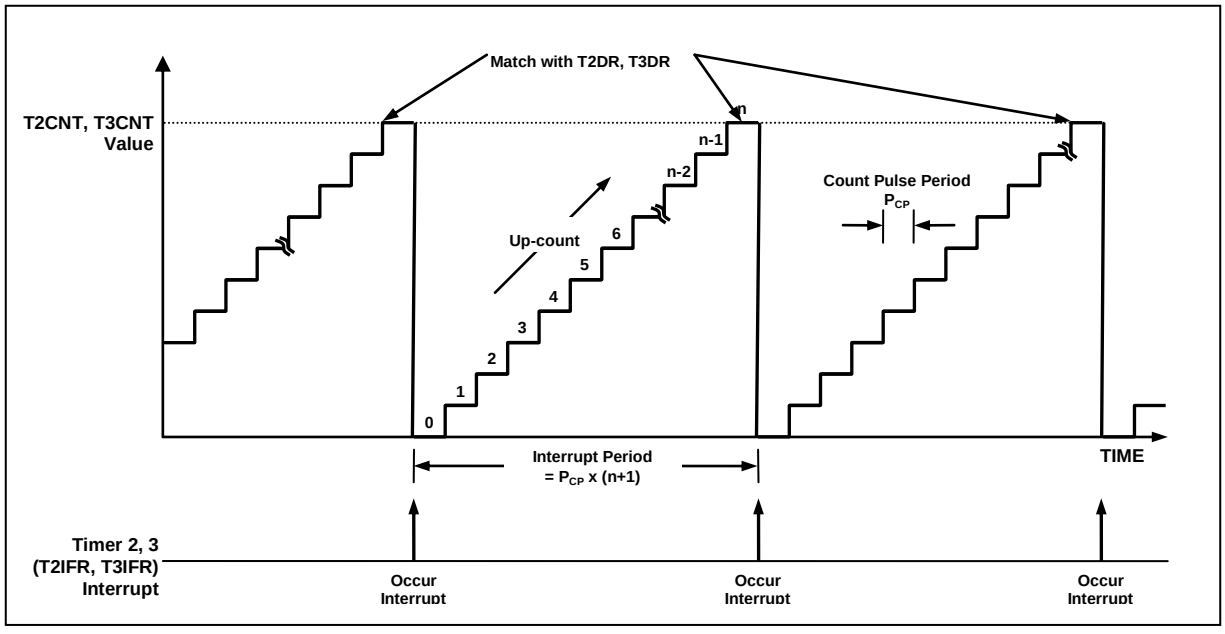


Figure 11.22 8-Bit Timer/Counter 2, 3 Example

11.6.3 16-Bit Timer/Counter 2 Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 11.23.

The timer register is being run with all 16 bits. A 16-bit timer/counter register T2CNT, T3CNT are incremented 0000H to FFFFFH until it matches T2DR, T3DR and then resets to 0000H. The match output generates the Timer 2 interrupt (No Timer 3 interrupt). The clock source is selected from T2CK[2:0] and 16BIT2 bit must be set to '1'. Timer 2 is LSB 8-bit, the timer 3 is MSB 8-bit.

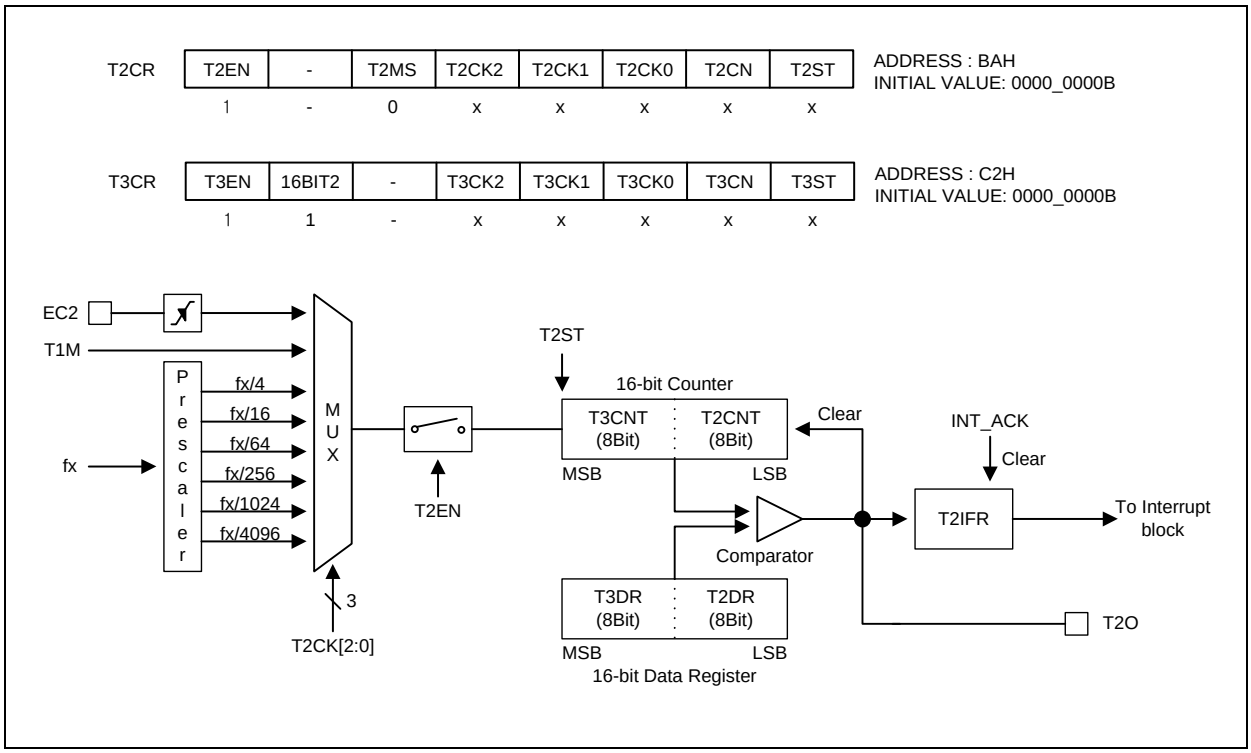


Figure 11.23 16-Bit Timer/Event Counter Mode for Timer 2

11.6.4 8-Bit Timer 2 Capture Mode

The 8-bit Capture mode is selected by control register as shown in Figure 11.24.

The timer 2 capture mode is set by T2MS as '1'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode and the interrupt occurs when T2CNT is equal to T2DR. T2CNT value is automatically cleared by hardware and it can be also cleared by software (T2ST).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T2CDR. In the timer 2 capture mode, timer 2 output (T2O) waveform is not available.

According to the EIPOL register setting, the external interrupt EINT12 function is chose. Of course, the EINT12 pin must be set to an input port.

T2CDR and T2DR are in the same address. In the capture mode, reading operation reads T2CDR, not T2DR and writing operation will update T2DR.

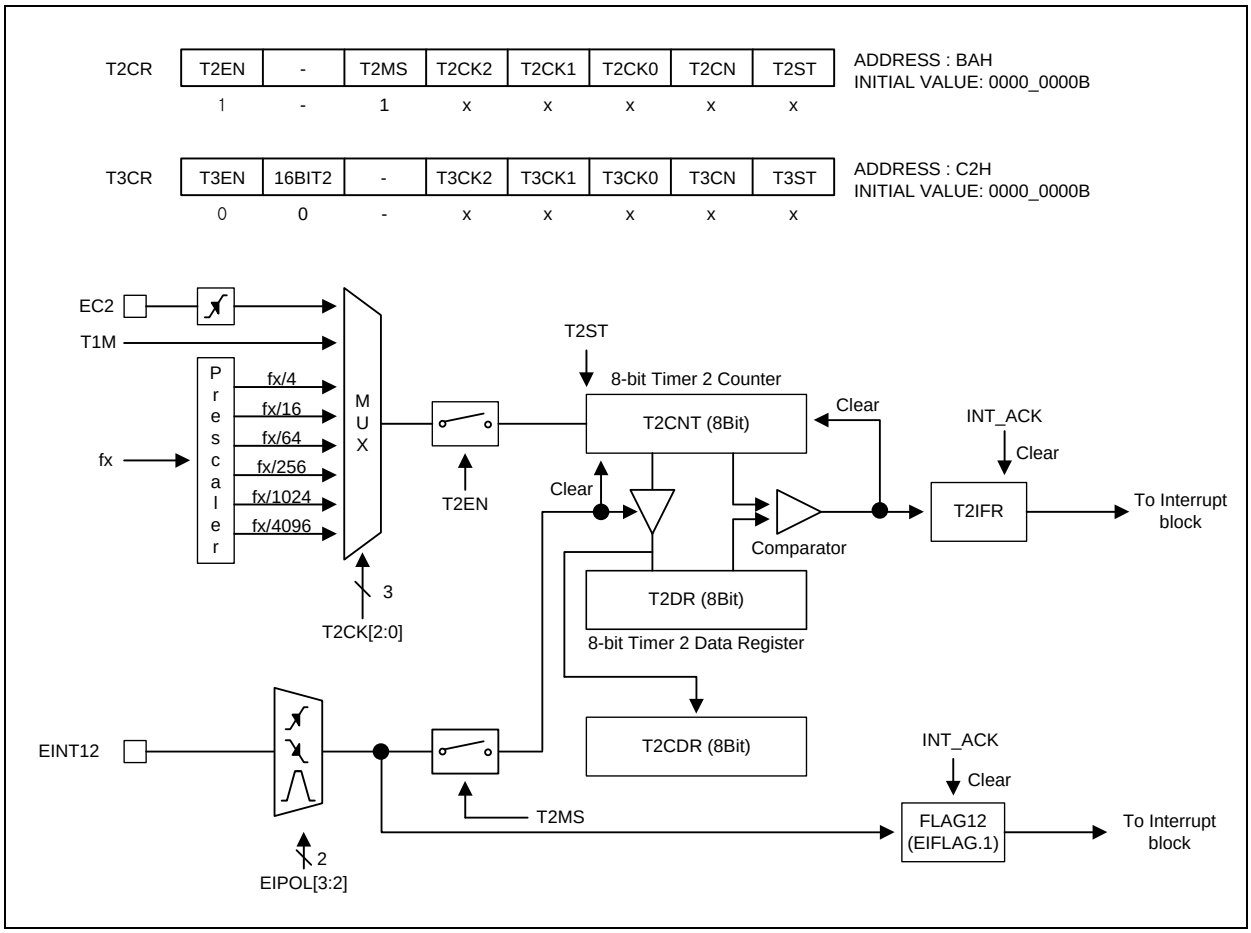


Figure 11.24 8-Bit Capture Mode for Timer 2

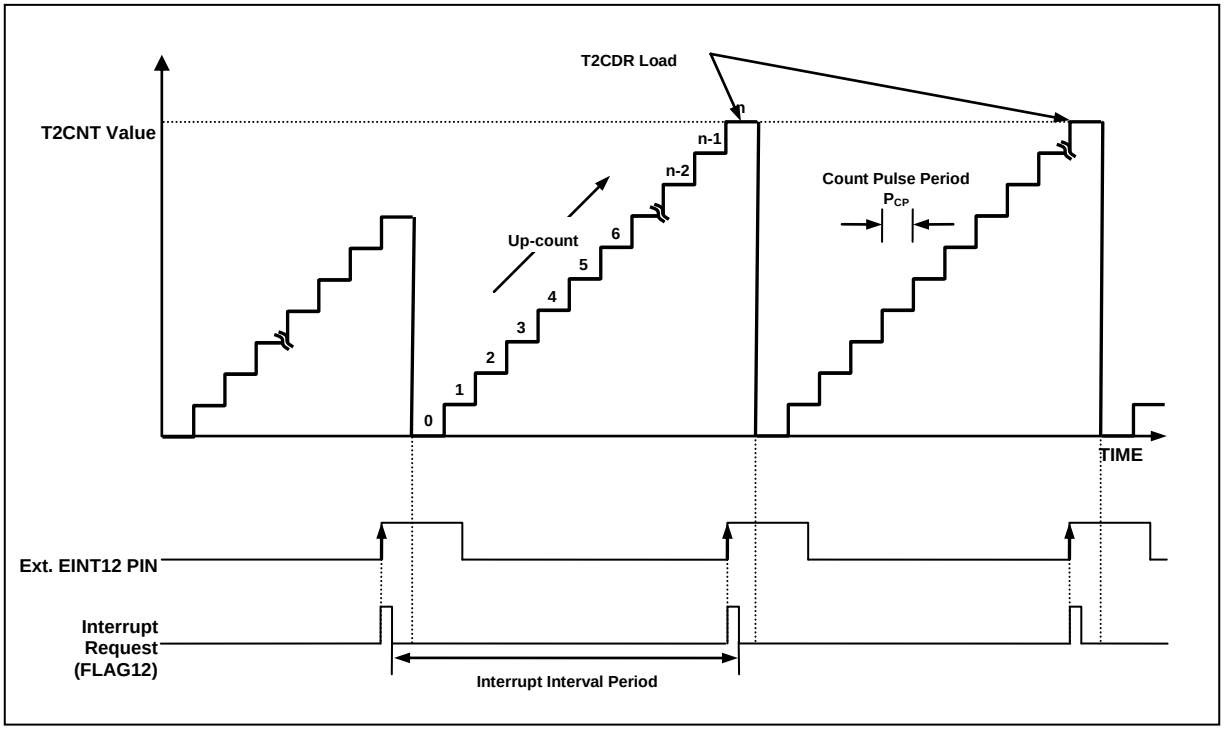


Figure 11.25 Input Capture Mode Operation for Timer 2

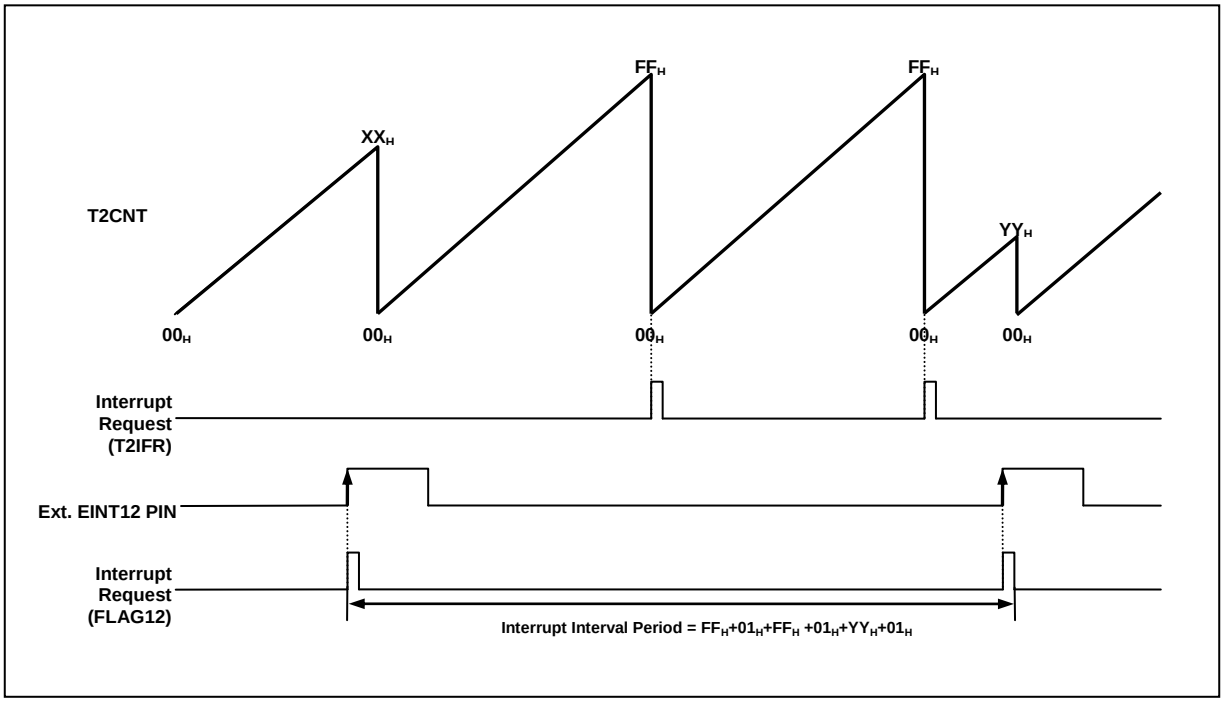


Figure 11.26 Express Timer Overflow in Capture Mode

11.6.5 16-Bit Timer 2 Capture Mode

The 16-bit capture mode is selected by control register as shown in Figure 11.27.

The 16-bit capture mode is the same operation as 8-bit capture mode, except that the timer register uses 16 bits. The clock source is selected from T2CK[2:0] and 16BIT2 bit must be set to '1'.

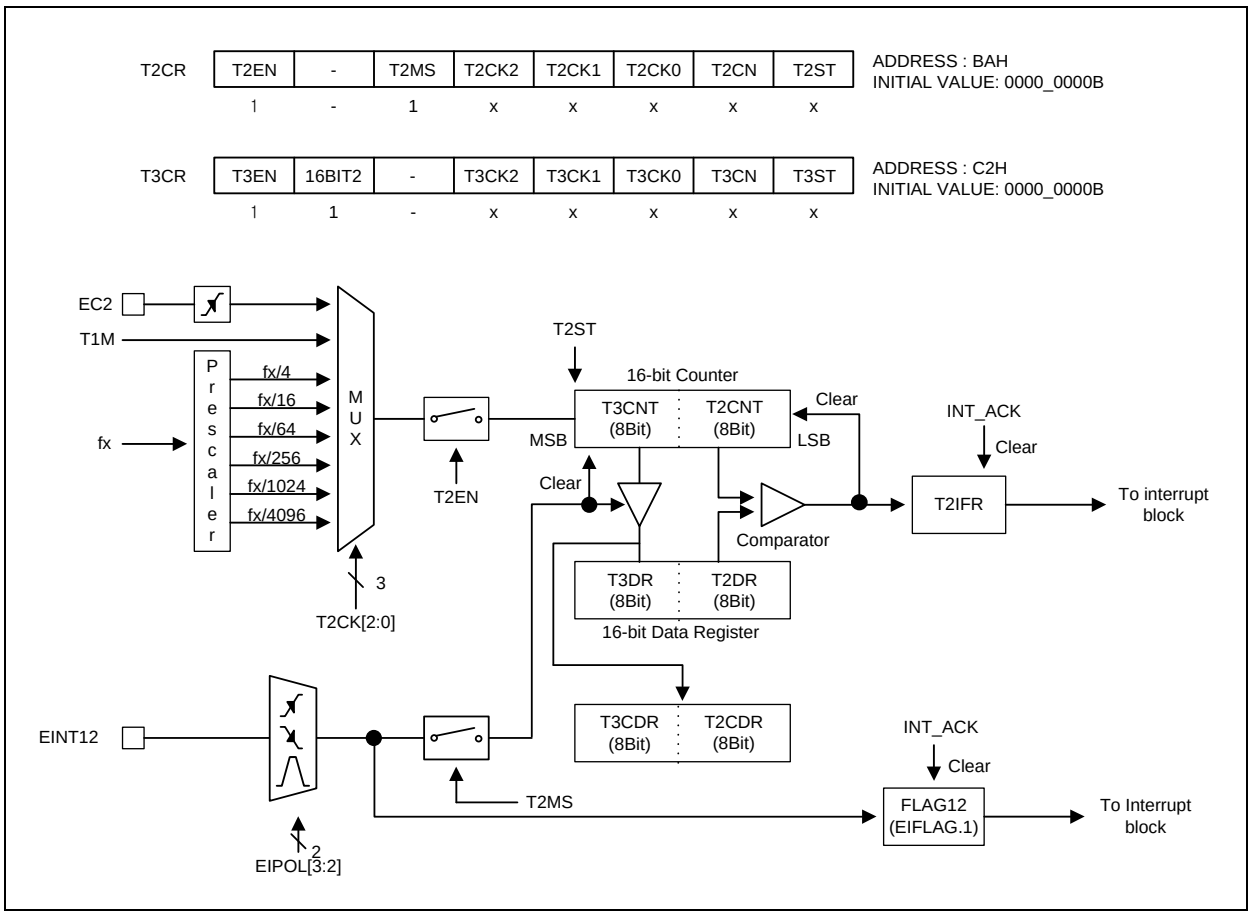


Figure 11.27 16-Bit Capture Mode for Timer 2

11.6.6 Block Diagram

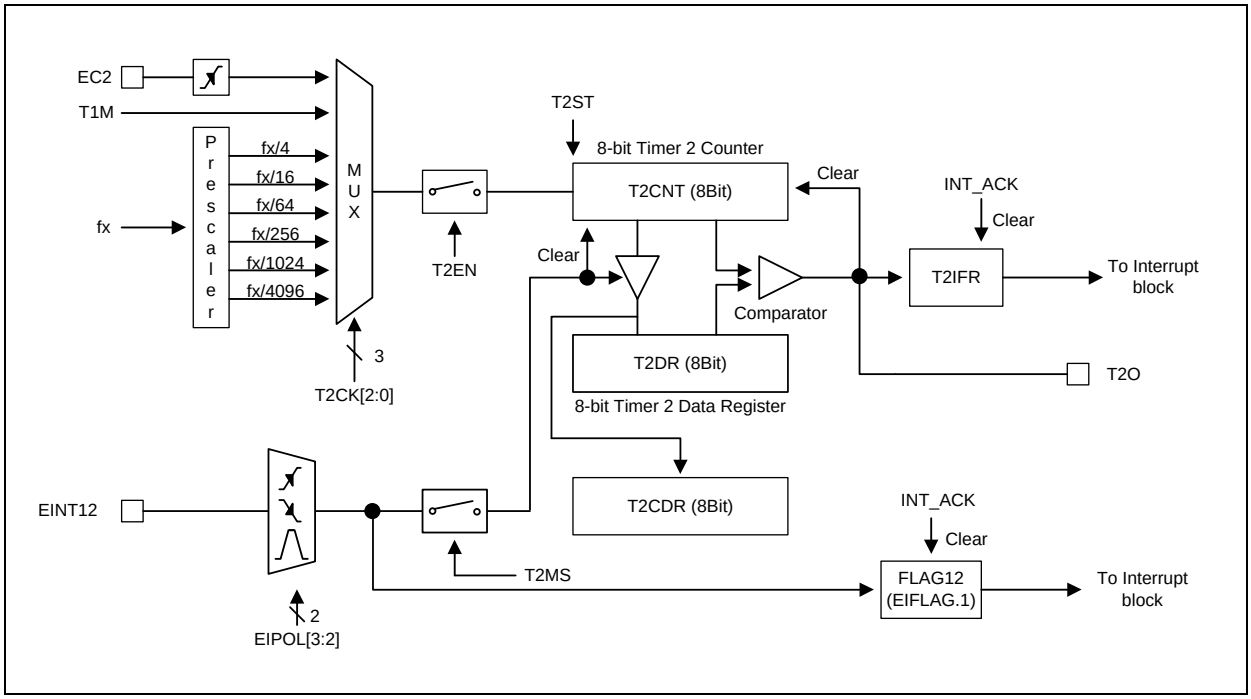


Figure 11.28 8-Bit Timer 2 Block Diagram

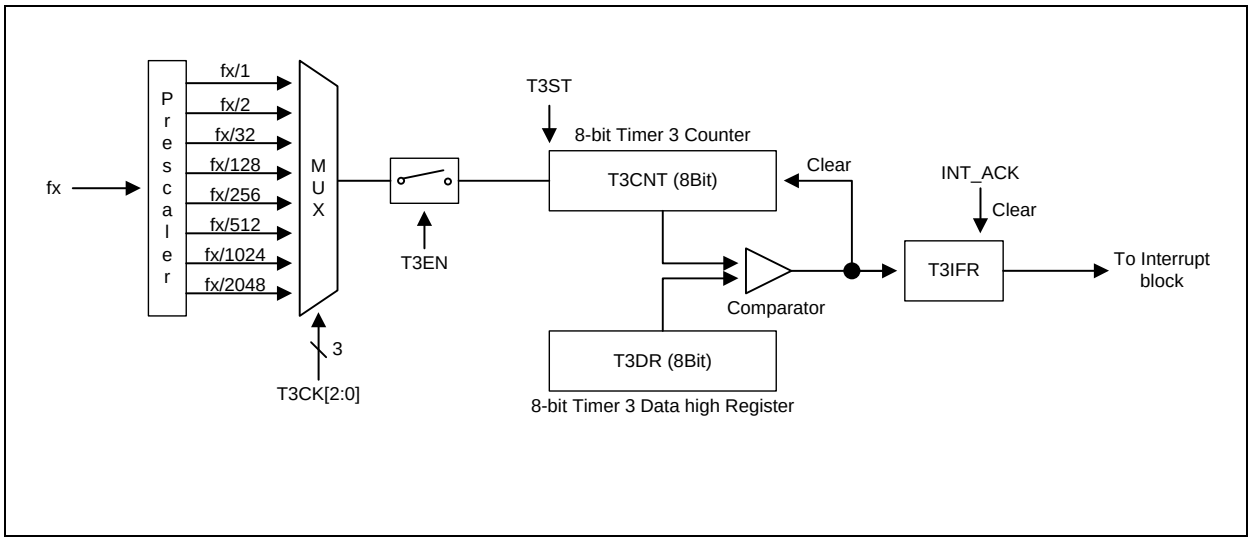


Figure 11.29 8-Bit Timer Counter 3 Block Diagram

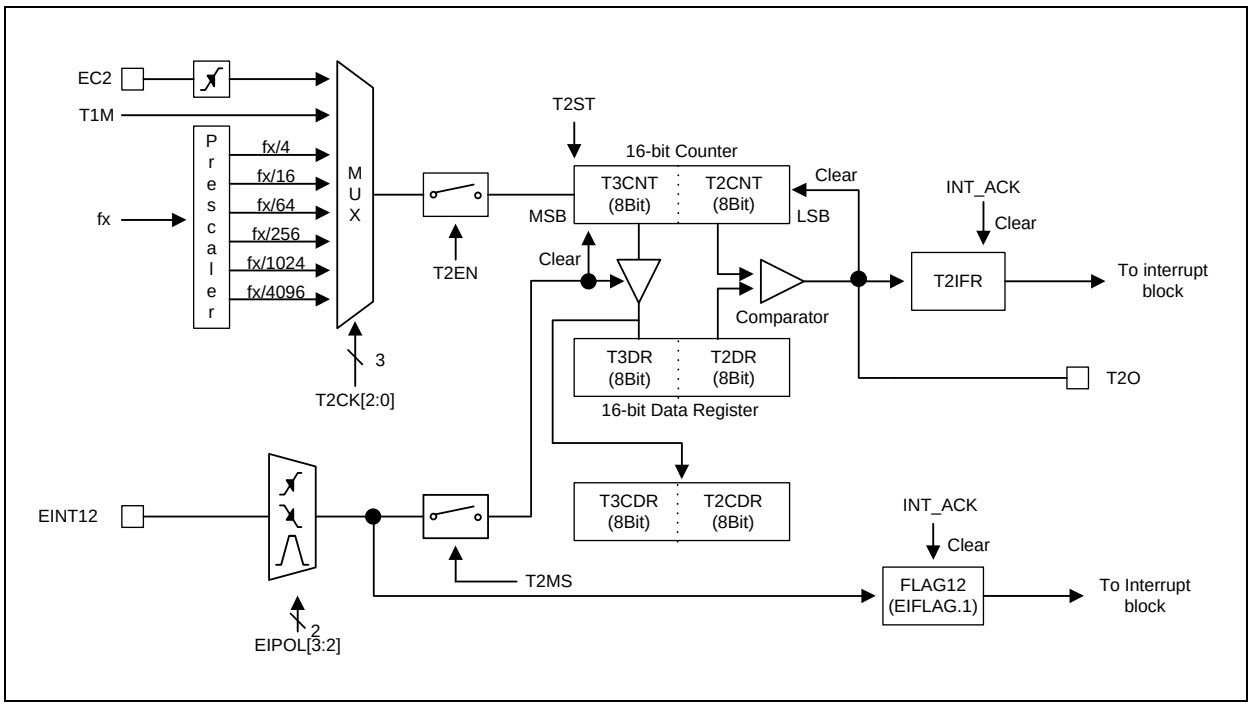


Figure 11.30 16-Bit Timer/Event Counter 2 Block Diagram

11.6.7 Register Map

Table 11-8 Timer 2, 3 Register Map

Name	Address	Dir	Default	Description
T2CNT	BCH	R	00H	Timer 2 Counter Register
T2DR	BEH	R/W	FFH	Timer 2 Data Register
T2CDR	BEH	R	00H	Timer 2 Capture Data Register
T2CR	BAH	R/W	00H	Timer 2 Control Register
T3CNT	C4H	R	00H	Timer 3 Counter Register
T3DR	C6H	R/W	FFH	Timer 3 Data Register
T3CDR	C6H	R	00H	Timer 3 Capture Data Register
T3CR	C2H	R/W	00H	Timer 3 Control Register
T1FR	C3H	R/W	00H	Timer Interrupt Flag Register

11.6.7.1 Timer/Counter 2, 3 Register Description

The timer/counter 2, 3 register consists of timer 2 counter register (T2CNT), timer 2 data register (T2DR), timer 2 capture data register (T2CDR), timer 2 control register (T2CR), timer 3 counter register (T3CNT), timer 3 data register (T3DR), timer 3 capture data register (T3CDR), timer 3 control register (T3CR). T2IFR and T3IFR bits are in the timer interrupt flag register (TIFR).

11.6.7.2 Register Description for Timer/Counter 2, 3

T2CNT (Timer 2 Counter Register) : BCH

7	6	5	4	3	2	1	0
T2CNT7	T2CNT6	T2CNT5	T2CNT4	T2CNT3	T2CNT2	T2CNT1	T2CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T2CNT[7:0] T2 Counter

T2DR (Timer 2 Data Register) : BEH

7	6	5	4	3	2	1	0
T2DR7	T2DR6	T2DR5	T2DR4	T2DR3	T2DR2	T2DR1	T2DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T2DR[7:0] T2 Data

T2CDR (Timer 2 Capture Data Register: Read Case, Capture mode only) : BEH

7	6	5	4	3	2	1	0
T2CDR7	T2CDR6	T2CDR5	T2CDR4	T2CDR3	T2CDR2	T2CDR1	T2CDR0
R	R	R	R	R	R	R	R

Initial value : 00H

T2CDR[7:0] T2 Capture

T2CR (Timer 2 Control Register) : BAH

7	6	5	4	3	2	1	0
T2EN	–	T2MS	T2CK2	T2CK1	T2CK0	T2CN	T2ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T2EN Control Timer 2

0 Timer 2 disable

1 Timer 2 enable

T2MS Control Timer 2 Operation Mode

0 Timer/Counter mode

1 Capture mode

T2CK[2:0] Select Timer 2 clock source. fx is main system clock frequency

T2CK2	T2CK1	T2CK0	Description
0	0	0	T1M
0	0	1	fx/4
0	1	0	fx/16
0	1	1	fx/64
1	0	0	fx/256
1	0	1	fx/1024
1	1	0	fx/4096
1	1	1	External Clock (EC2)

T2CN Clear Timer 2 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T2ST Control Timer 2 Start/Stop

0 Counter stop

1 Clear counter and start

NOTE) Match Interrupt is generated in Capture mode.

T3CNT (Timer 3 Counter Register) : C4H

7	6	5	4	3	2	1	0
T3CNT7	T3CNT6	T3CNT5	T3CNT4	T3CNT3	T3CNT2	T3CNT1	T3CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T3CNT[7:0] T3 Counter

T3DR (Timer 3 Data Register) : C6H

7	6	5	4	3	2	1	0
T3DR7	T3DR6	T3DR5	T3DR4	T3DR3	T3DR2	T3DR1	T3DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T3DR[7:0] T3 Data

T3CDR (Timer 3 Capture Data Register: Read Case, 16bit Capture mode only) : C6H

7	6	5	4	3	2	1	0
T3CDR7	T3CDR6	T3CDR5	T3CDR4	T3CDR3	T3CDR2	T3CDR1	T3CDR0
R	R	R	R	R	R/	R	R

Initial value : 00H

T3CDR[7:0] 16bit T2 Capture

T3CR (Timer 3 Control Register) : C2H

7	6	5	4	3	2	1	0
T3EN	16BIT2	–	T3CK2	T3CK1	T3CK0	T3CN	T3ST
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T3EN Control Timer 3

0 Timer 3 disable

1 Timer 3 enable

16BIT2 Select Timer 2 8/16Bit

0 8 Bit

1 16 Bit

T3CK[2:0] Select Timer 3 clock source. fx is main system clock frequency

T3CK1	T3CK0	T3CK2	Description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/32
0	1	1	fx/128
1	0	0	fx/256
1	0	1	fx/512
1	1	0	fx/1024
1	1	1	fx/2048

T3CN Control Timer 3 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T3ST Control Timer 3 Start/Stop

0 Counter stop

1 Clear counter and start

TIFR (Timer Interrupt Flag Register) : C3H

7	6	5	4	3	2	1	0
SIOIFR	–	–	–	T3IFR	T2IFR	T1IFR	T0IFR
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value : 00H

SIOIFR When SIO interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 SIO Interrupt no generation

1 SIO Interrupt generation

NOTE) For clearing this bit, use “ANL” instruction.

T3IFR When T3 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T3 Interrupt no generation

1 T3 Interrupt generation

T2IFR When T2 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T2 Interrupt no generation

1 T2 Interrupt generation

T1IFR When T1 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T1 Interrupt no generation

1 T1 Interrupt generation

T0IFR When T0 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T0 Interrupt no generation

1 T0 Interrupt generation

11.7 Buzzer Driver

11.7.1 Overview

The Buzzer consists of 8 bit counter, buzzer data register (BUZDR), and buzzer control register (BUZCR). The Square Wave (61.035Hz~125.0 kHz @8MHz) is outputted through P06/BUZO pin. The buzzer data register (BUZDR) controls the buzzer frequency (look at the following expression). In buzzer control register (BUZCR), BUCK[1:0] selects source clock divided by prescaler.

$$f_{BUZ}(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR}+1)}$$

Table 11-9 Buzzer Frequency at 8 MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125kHz	62.5kHz	31.25kHz	15.625kHz
0000_0001	62.5kHz	31.25kHz	15.625kHz	7.812kHz
…	…	…	…	…
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

11.7.2 Block Diagram

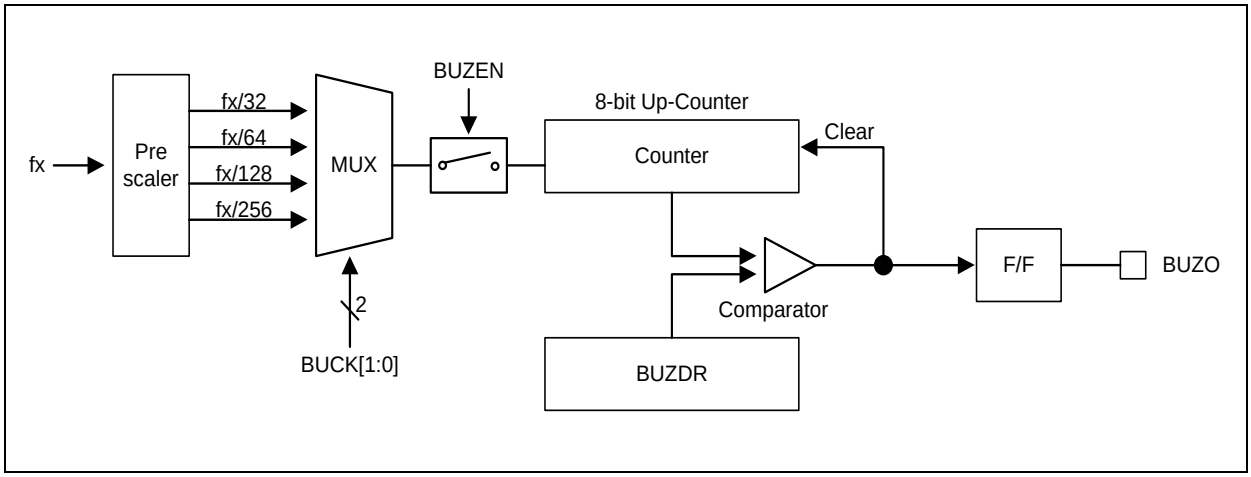


Figure 11.31 Buzzer Driver Block Diagram

11.7.3 Register Map

Table 11-10 Buzzer Driver Register Map

Name	Address	Dir	Default	Description
BUZDR	8FH	R/W	FFH	Buzzer Data Register
BUZCR	97H	R/W	00H	Buzzer Control Register

11.7.4 Buzzer Driver Register Description

Buzzer driver consists of buzzer data register (BUZDR) and buzzer control register (BUZCR).

11.7.5 Register Description for Buzzer Driver

BUZDR (Buzzer Data Register) : 8FH

7	6	5	4	3	2	1	0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

BUZDR[7:0] This bits control the Buzzer frequency
Its resolution is 00H ~ FFH

BUZCR (Buzzer Control Register) : 97H

7	6	5	4	3	2	1	0
–	–	–	–	–	BUCK1	BUCK0	BUZEN
–	–	–	–	–	R/W	R/W	R/W

Initial value : 00H

BUCK[1:0] Buzzer Driver Source Clock Selection

BUCK1	BUCK0	Description
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

BUZEN Buzzer Driver Operation Control

0	Buzzer Driver disable
1	Buzzer Driver enable

NOTE) fx: System clock oscillation frequency.

11.8 SIO

11.8.1 Overview

The serial input/output is used to transmit/receive 8-bit data serially. The serial input/output(SIO) module is a useful serial interface to communicate with other peripheral of microcontroller devices. This SIO is 8-bit clock synchronous type and consists of SIO pre-scaler register, SIO data register, SIO control register, and control circuit as illustrated in Figure 11.32. The SO pin is designed to input and output. So SIO can operate with two pins minimally. Pin P04/SO, P03/SCK and P02/SI pins are controlled by the SIO control register (SIOCR) and port function selection control registers (PFSR02, PFSR01, and P02IO).

The contents of the SIO data register can be written into or read out by software. The data in the SIO data register can be shifted synchronously with the transfer clock signal. SIO data register (SIODR) is an 8 bit shift register. MSB-first and LSB-first transfers are possible.

11.8.2 Block Diagram

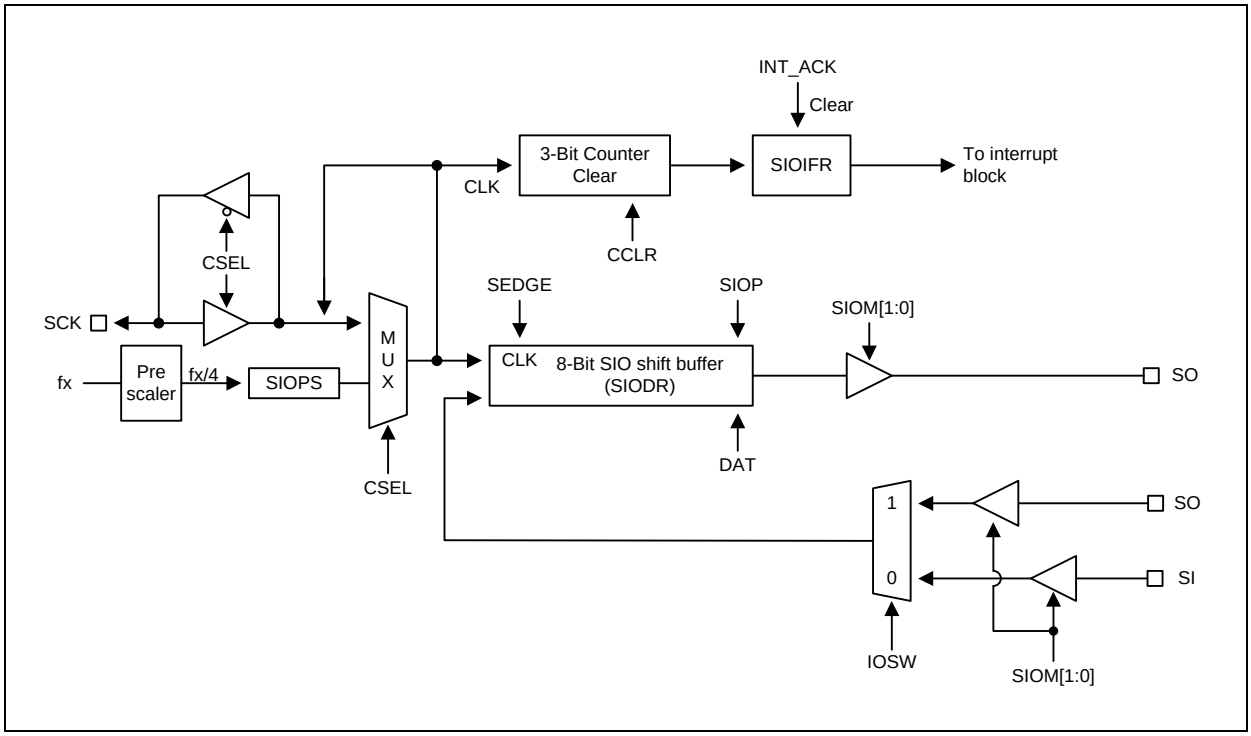


Figure 11.32 SIO Block Diagram

11.8.3 SIO Pre-Scaler Register (SIOPS)

SIOPS contains the SIO pre-scaler value. The SIO clock rate (baud rate) is calculated by the following formula.

Baud rate = Input clock (fx/4)/(Pre-scaler value + 1)

or SCK input clock, where the input clock is fx/4

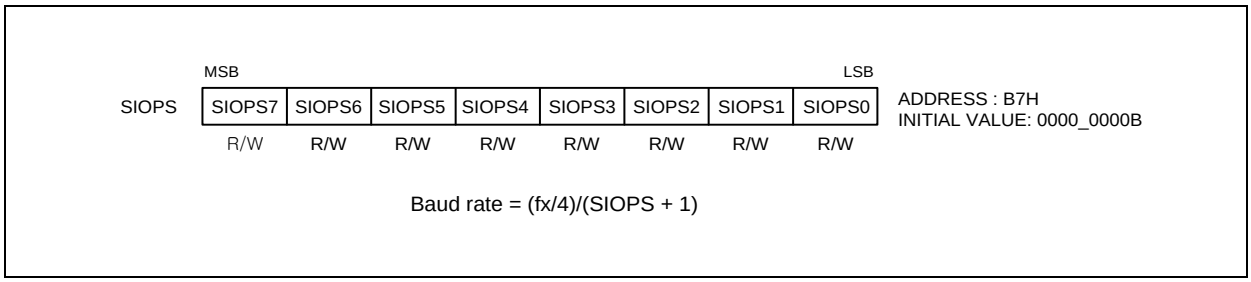


Figure 11.33 SIO Pre-Scaler Register (SIOPS)

11.8.4 The usage of SIO

1. Select transmitter/receiver mode.
2. In transmitter mode, write data to be sent to SIODR.
3. Set CCLR to “1” to clear SIO counter and start shifting.
4. If Tx or Rx is completed, the SIO interrupt is generated and SIOIFR is set to “1”.
5. In receiver mode, the received data can be acquired by reading SIODR.

11.8.5 SIO Timing Diagram

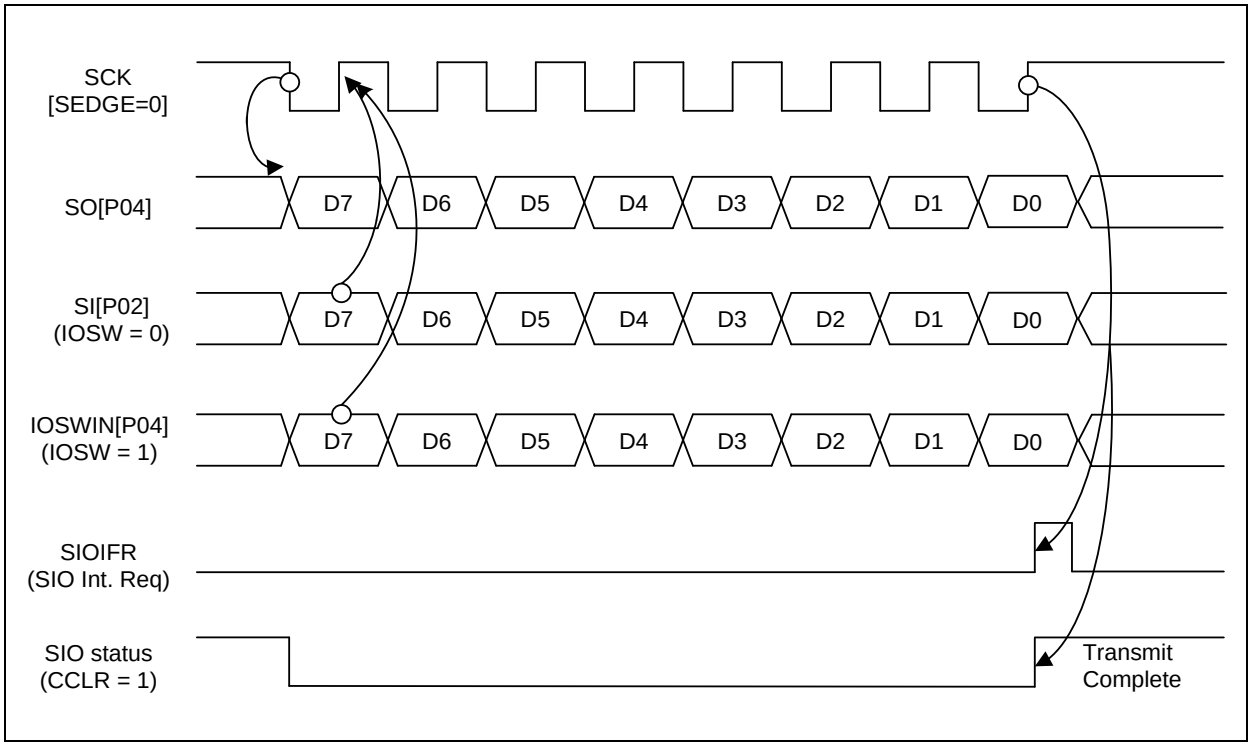


Figure 11.34 SIO Timing Diagram at SEDGE=0

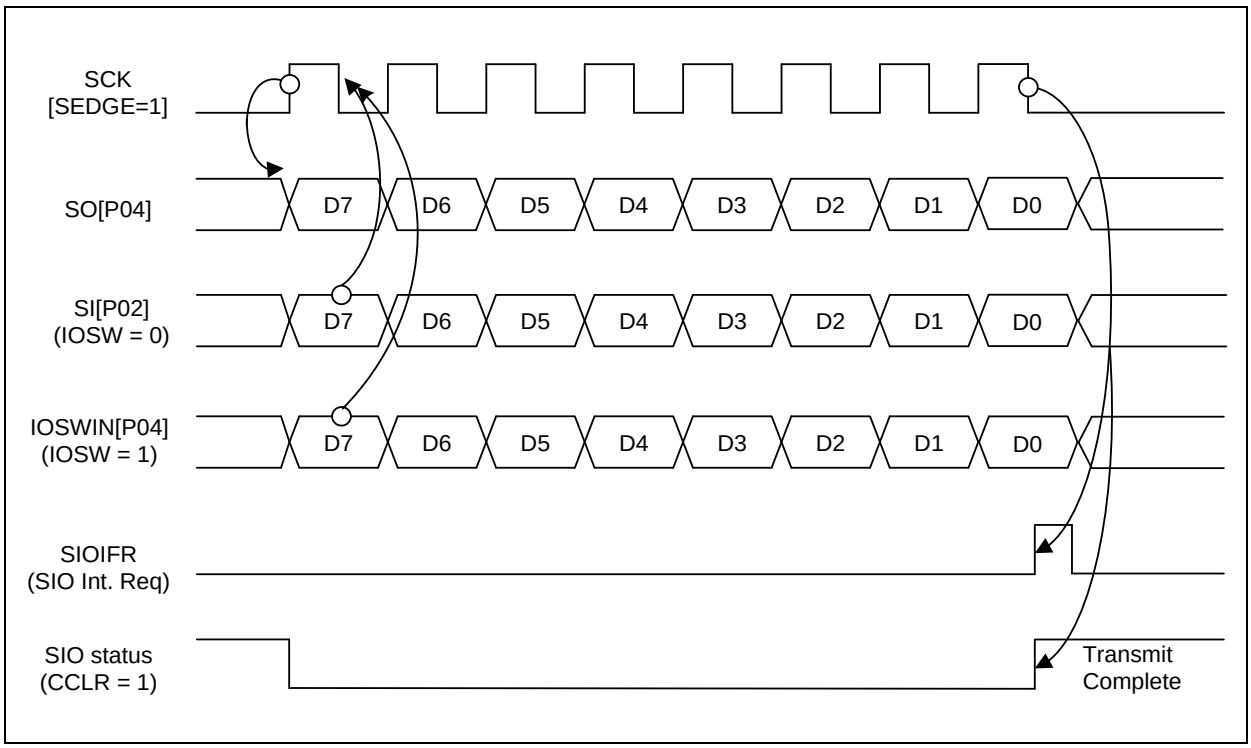


Figure 11.35 SIO Timing Diagram at SEDGE=1

11.8.6 Register Map

Table 11-11 SIO Register Map

Name	Address	Dir	Default	Description
SIOPS	B7H	R/W	00H	SIO Pre-scaler Register
SIODR	B6H	R/W	00H	SPI Data Register
SIOCR	B5H	R/W	00H	SIO Control Register

11.8.7 SIO Register Description

The SIO register consists of SIO pre-scaler register (SIOPS), SIO data Register (SIODR), and SIO control register (SIOCR). The SIOIFR bit is in the timer interrupt flag register (TIFR).

11.8.8 Register Description for SIO

SIOPS (SIO Pre-scaler Register) : B7H

7	6	5	4	3	2	1	0
SIOPS7	SIOPS6	SIOPS5	SIOPS4	SIOPS3	SIOPS2	SIOPS1	SIOPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

SIOPS [7:0] SIO Pre-scaler
Baud Rate = (fx/4)/(SIOPS+1)

SIODR (SIO Data Register) : B6H

7	6	5	4	3	2	1	0
SIODR7	SIODR6	SIODR5	SIODR4	SIODR3	SIODR2	SIODR1	SIODR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

SIODR [7:0] SIO Data

SIOCR (SIO Control Register) : B5H

7	6	5	4	3	2	1	0
CSEL	DAT	SIOP	IOSW	SIOM1	SIOM0	CCLR	SEDGE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

CSEL SIO Shift Clock Selection

0 Internal clock (P.S clock)

1 External clock (SCK)

DAT Data Direction Control

0 MSB first mode

1 LSB first mode

SIOP SIO Shift Operation Enable

0 Disable shifter and clock counter

1 Enable shifter and clock counter

IOSW Serial Input Pin Selection Bit

0 SI pin selection

1 SO pin selection

NOTE) If SO pin is selected for a serial data input, SO pin should be set to an input and port. So, the SIOM, PFSR02, and P04IO bits should be set to '01b', '0b' and '0b' respectively. Refer to the P0IO and P0FSR register for setting

SIOM[1:0] SIO Mode Selection

SIOM1	SIOM0	Description
0	0	Transmit mode
0	1	Receive mode
1	x	Transmit/Receive mode

CCLR SIO Counter Clear and Shift Start

0 No action

1 Clear 3-bit counter and start shifting

SEDGE SIO Clock Edge Selection

0 Tx at falling edges, Rx at rising edges

1 Tx at rising edge, Rx at falling edges

NOTE) The serial I/O interrupt flag (SIOIFR bit) is in the timer interrupt flag register (TIFR register).

11.9 LCD Driver

11.9.1 Overview

The LCD driver is controlled by the LCD Control Register (LCDCRH/L). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCDCRH and LCDCRL values to logic ‘0’.

The LCD display can continue operating during IDLE and STOP modes if a sub-frequency clock is used as system clock source.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don’t rewrite LCDCRH frequently.

11.9.2 LCD Display RAM Organization

Display data are stored to the display data area in the internal data memory.

The display data which stored to the display internal data area (address E0H-FFH) are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with a program.

Figure 11-36 shows the correspondence between the display external data area and the COM/SEG pins. The LCD is turned on when the display data is “1” and turned off when “0”.

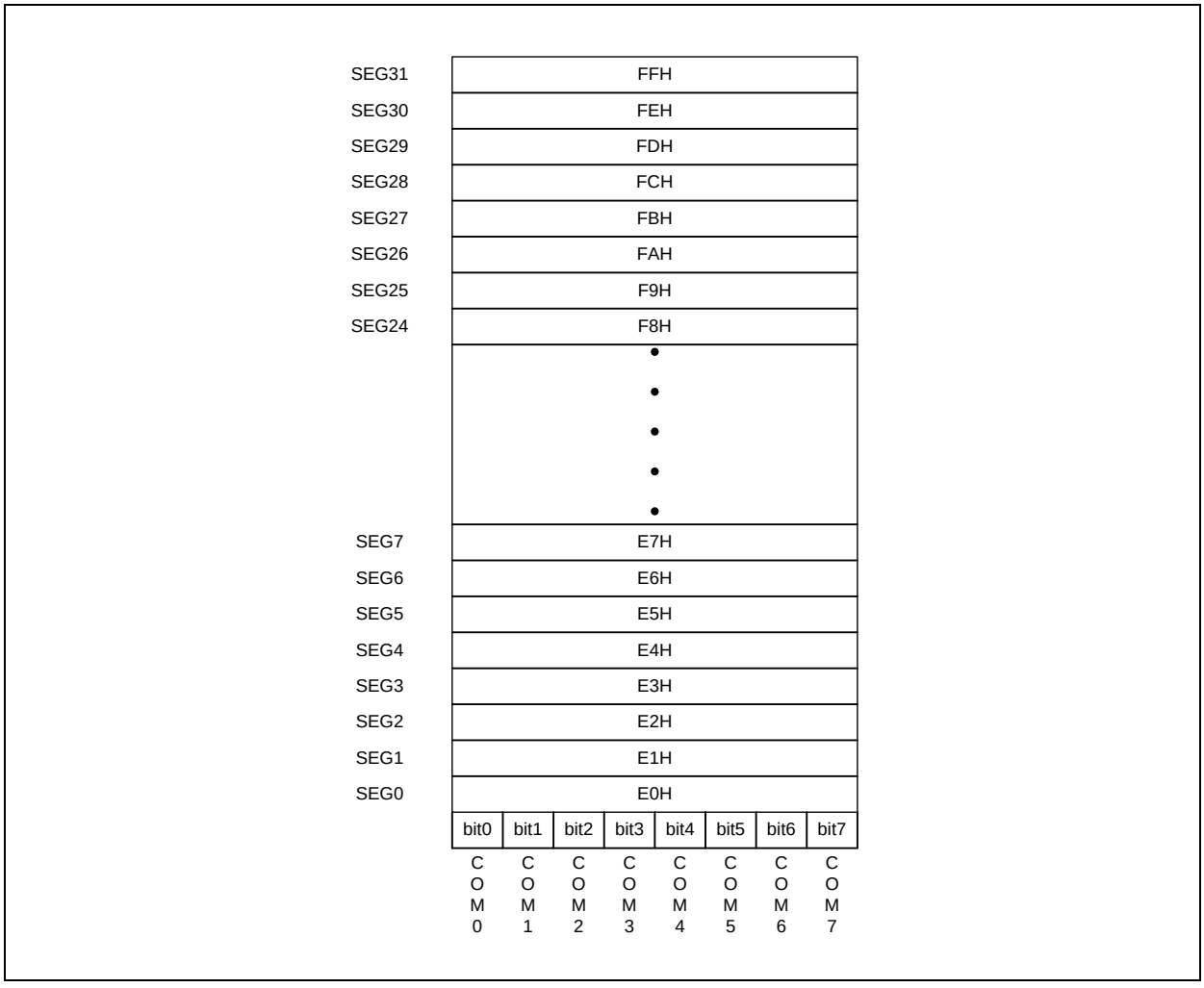


Figure 11.36 LCD Circuit Block Diagram

11.9.3 LCD Signal Waveform

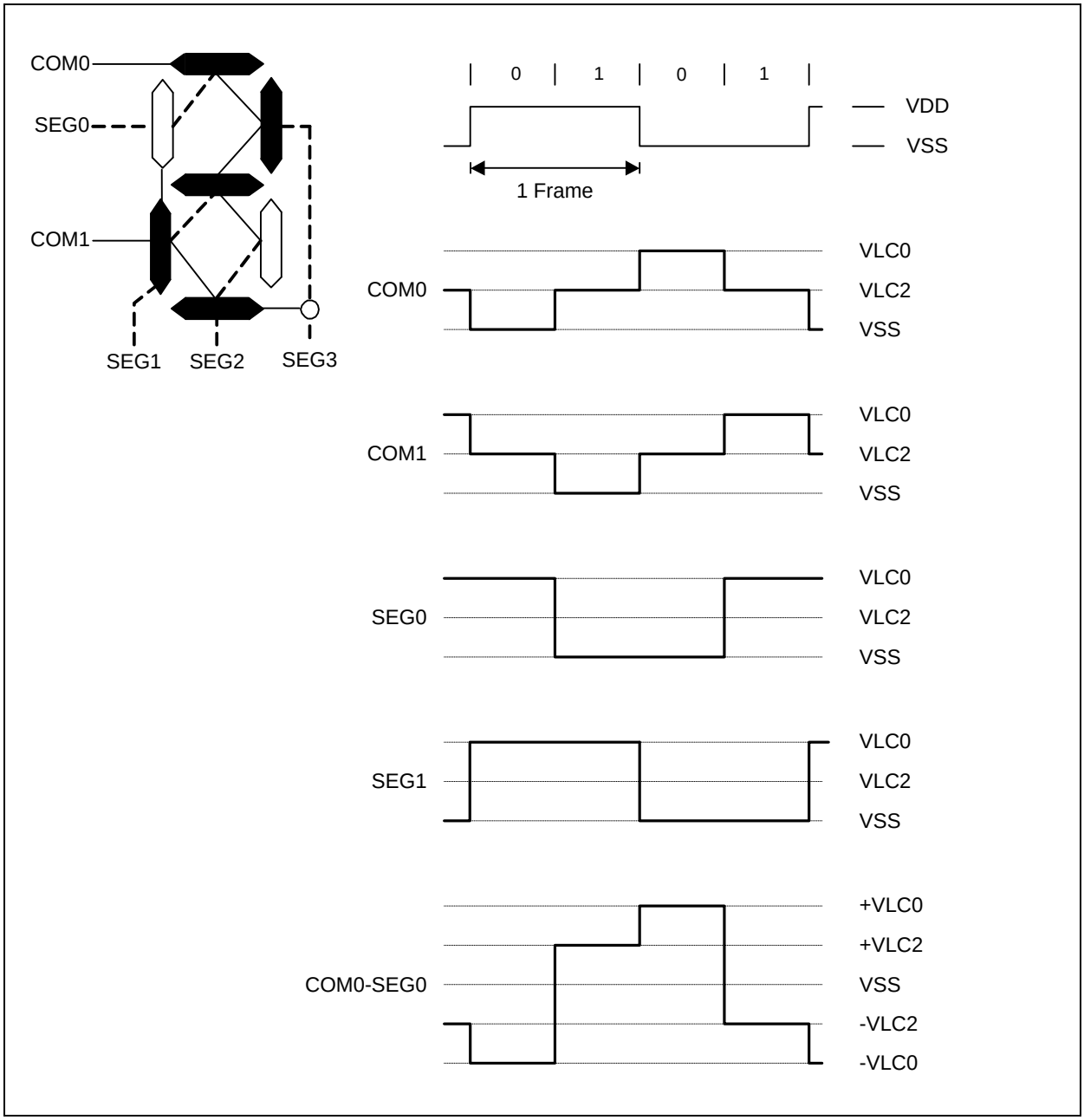


Figure 11.37 LCD Signal Waveforms (1/2Duty, 1/2Bias)

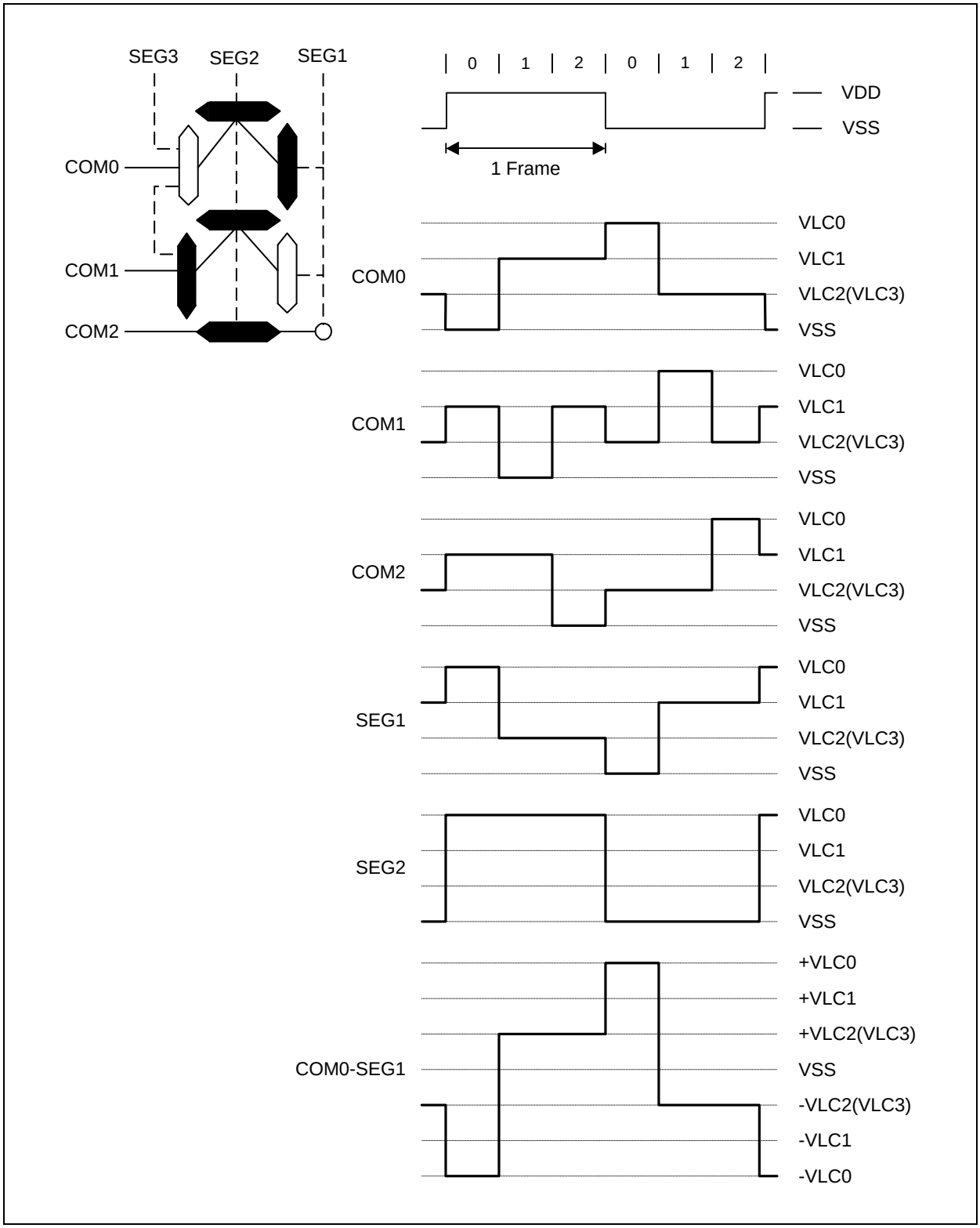


Figure 11.38 LCD Signal Waveforms (1/3Duty, 1/3Bias)

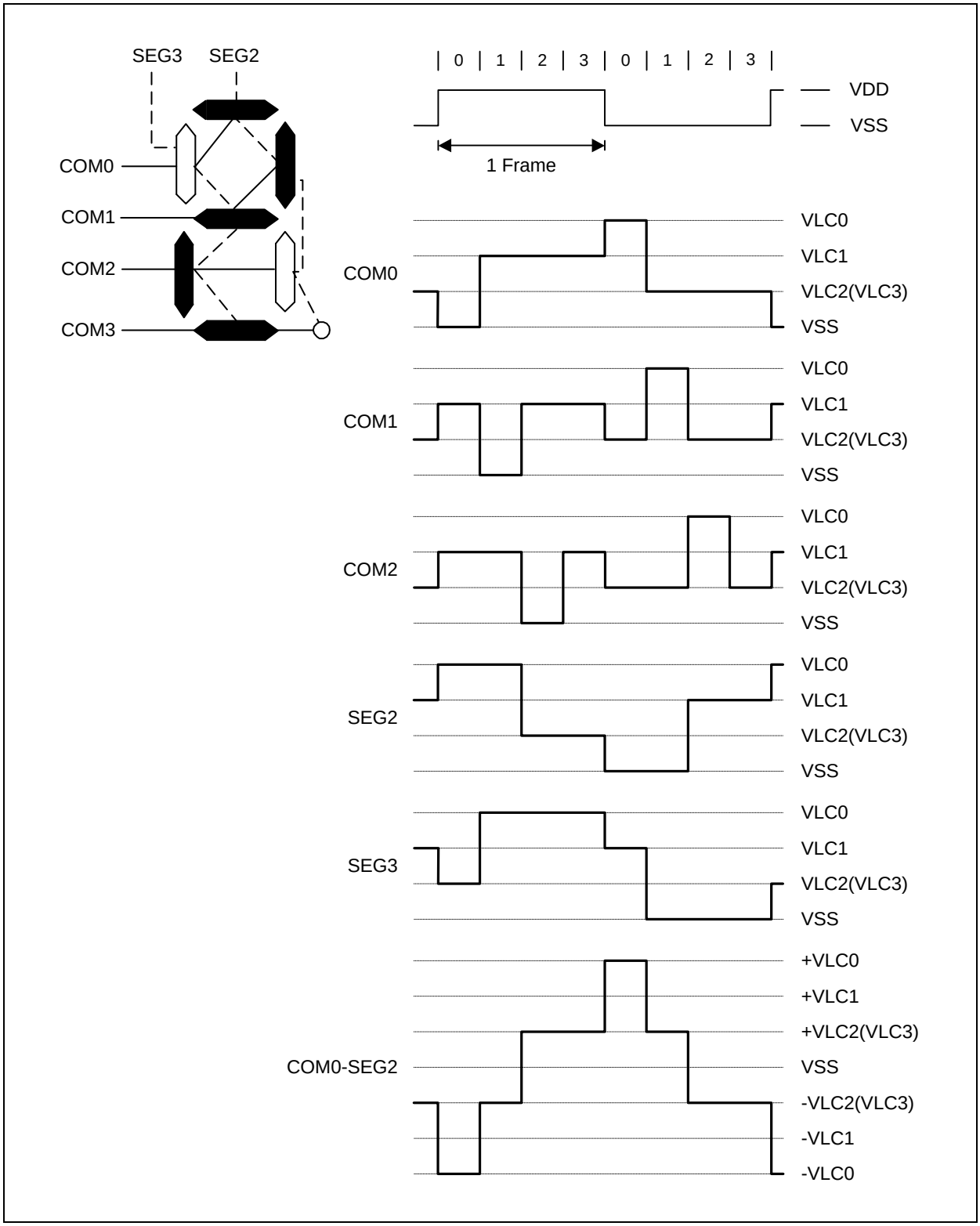


Figure 11.39 LCD Signal Waveforms (1/4Duty, 1/3Bias)

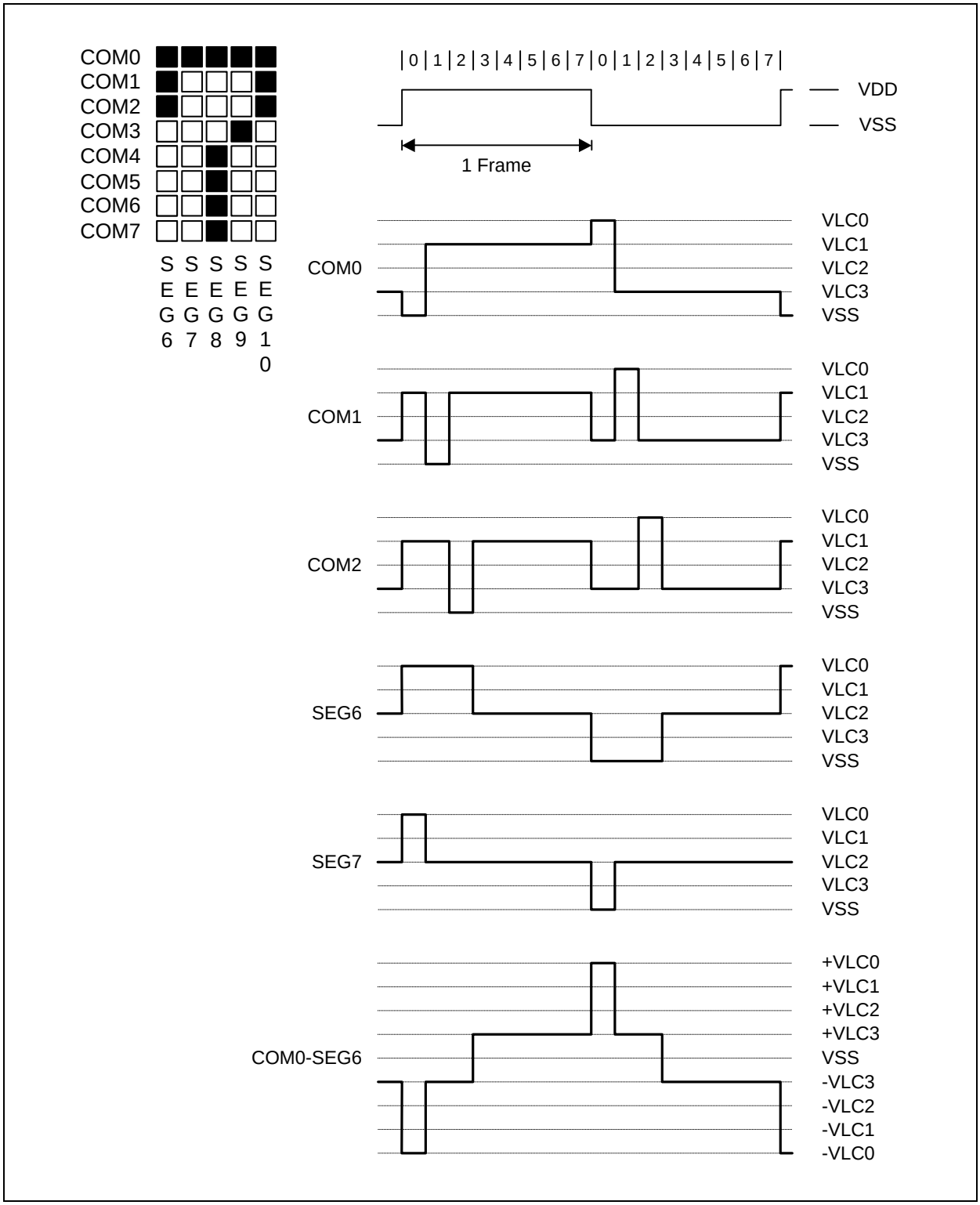
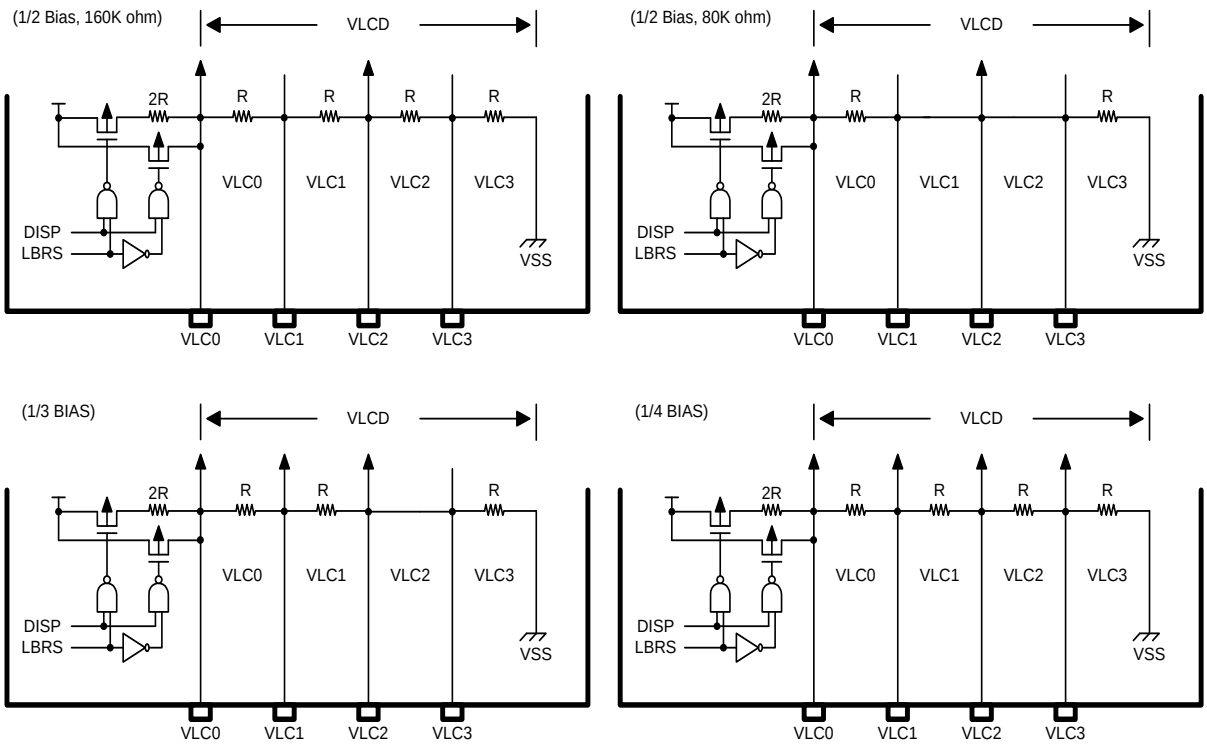


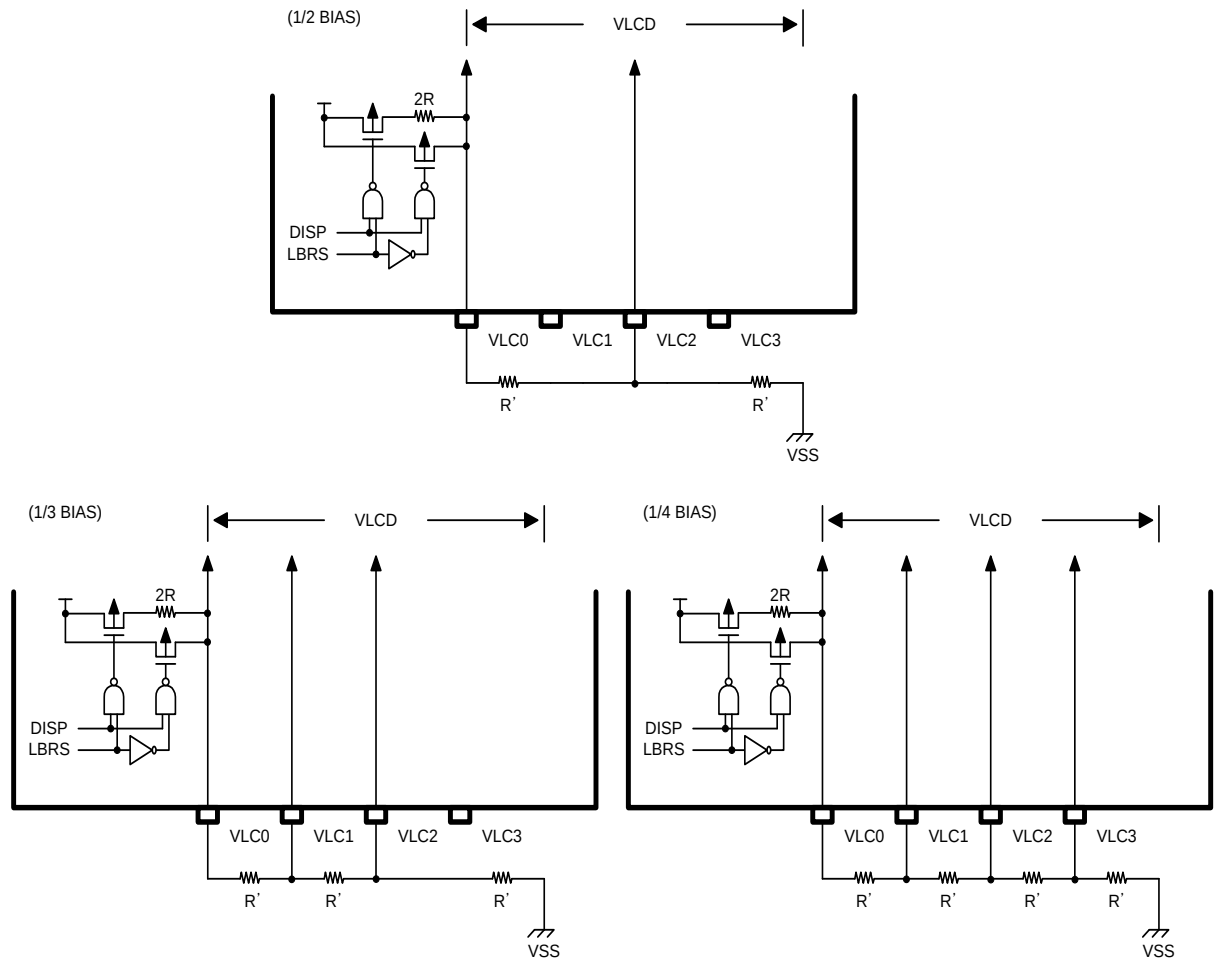
Figure 11.40 LCD Signal Waveforms (1/8Duty, 1/4Bias)

11.9.4 LCD Voltage Dividing Resistor Connection



NOTES) 1. When 1/2 bias are selected, the VLC0, VLC1 and VLC2, VLC3 are internally connected.
2. When 1/3 bias are selected, the VLC2 and VLC3 are internally connected.
3. When the internal resistors are selected, all the P20/VLC0, P21/VLC1, P22/VLC2, and P23/VLC3 pins can be used for normal I/O

Figure 11.41 Internal Resistor Bias Connection



NOTES) 1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC1, VLC2, and VLC3) by P2FSR register.
- When it is 1/2 bias, the P20/VLC0 and P22/VLC2 pins should be selected as VLC0 and VLC2 functions. The other pins can be used for normal I/O.
- When it is 1/3 bias, the P20/VLC0, P21/VLC1, and P22/VLC2 pins should be selected as VLC0, VLC1, and VLC2 functions. The other pins can be used for normal I/O.
- When it is 1/4 bias, the P20/VLC0, P21/VLC1, P22/VLC2, and P23/VLC3 pins should be selected as VLC0, VLC1, VLC2, and VLC3 functions

Figure 11.42 External Resistor Bias Connection

11.9.5 Block Diagram

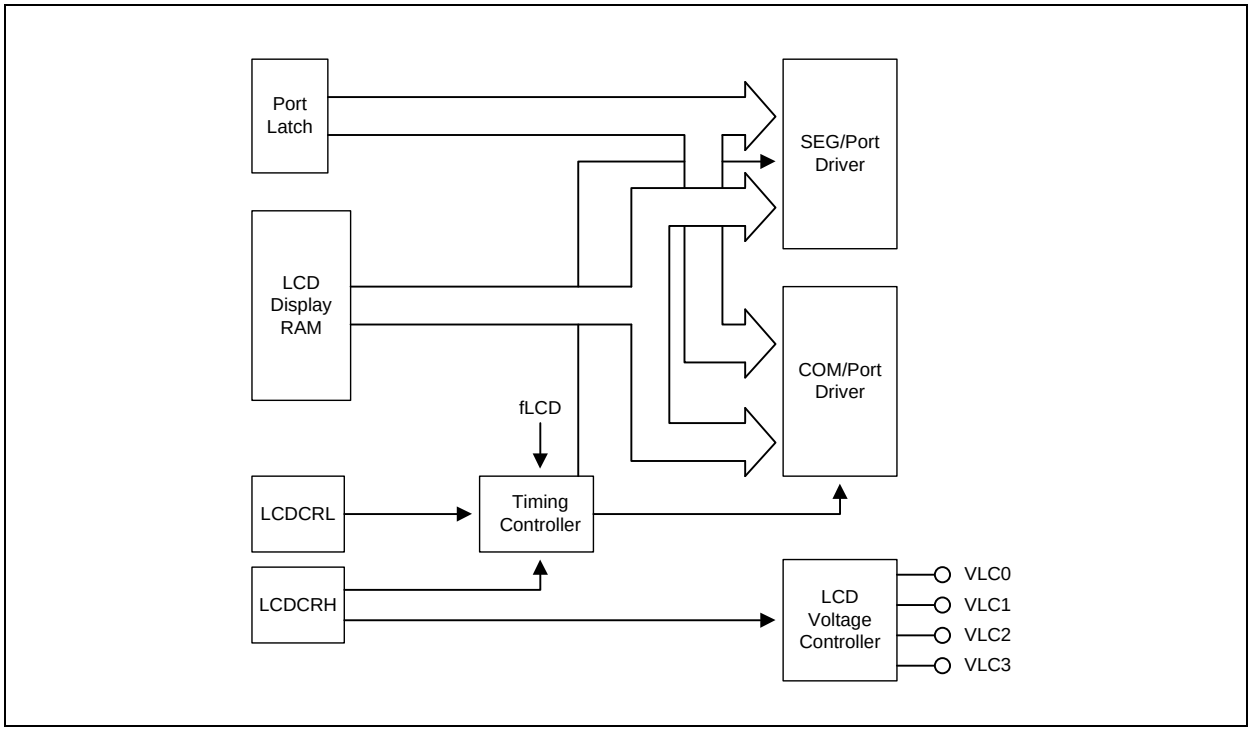


Figure 11.43 LCD Circuit Block Diagram

NOTE) The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don't rewrite LCDCRH frequently.

11.9.6 Register Map

Table 11-12 LCD Register Map

Name	Address	Dir	Default	Description
LCDCRH	ECH	R/W	00H	LCD Driver Control High Register
LCDCRL	EBH	R/W	00H	LCD Driver Control Low Register

11.9.7 LCD Driver Register Description

LCD driver register has two control registers, LCD driver control high register (LCDCRH) and LCD driver control low register (LCDCRL).

11.9.8 Register Description for LCD Driver

LCDCRH (LCD Driver Control High Register) : ECH

7	6	5	4	3	2	1	0
–	–	–	–	LBRS	–	BTYPE	DISP
–	–	–	–	R/W	–	R/W	R/W

Initial value : 00H

LBRS LCD Bias Resistor Select
- 0 Not select P-Tr resistor
- 1 Select P-Tr resistor 2R

BTYPE LCD Bias Type Select
- 0 Internal resistor bias
- 1 External resistor bias

DISP LCD Display Control
- 0 Display off
- 1 Normal Display on

LCDCRL (LCD Driver Control Low Register) : EBH

7	6	5	4	3	2	1	0
–	–	DBS3	DBS2	DBS1	DBS0	LCLK1	LCLK0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DBS[3:0] LCD Duty and Bias Select (note)

DBS3	DBS2	DBS1	DBS0	Description
0	0	0	0	1/8Duty, 1/4Bias (80k ohm)
0	0	0	1	1/6Duty, 1/4Bias (80k ohm)
0	0	1	0	1/5Duty, 1/3Bias (80k ohm)
0	0	1	1	1/4Duty, 1/3Bias (80k ohm)
0	1	0	0	1/3Duty, 1/3Bias (80k ohm)
0	1	0	1	1/3Duty, 1/2Bias (80k ohm)
0	1	1	0	1/3Duty, 1/2Bias (160k ohm)
0	1	1	1	1/2Duty, 1/2Bias (80k ohm)
1	0	0	0	1/2Duty, 12Bias (160k ohm)
Other value				Not available

LCLK[1:0] LCD Clock Select (When f_{WCK}(Watch timer clock)= 32.768 kHz)

LCLK1	LCLK0	Description
0	0	f_{LCD} = 128Hz
0	1	f_{LCD} = 256Hz
1	0	f_{LCD} = 512Hz
1	1	f_{LCD} = 1024Hz

NOTE) The LCD clock is generated by watch timer clock (f_{WCK}). So the watch timer should be enabled when the LCD display is turned on.

12. Power Down Operation

12.1 Overview

The MC96P6608/P6408 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, Sub-IDLE and STOP mode. In three modes, program is stopped.

12.2 Peripheral Operation in IDLE/STOP Mode

Table 12-1 Peripheral Operation during Power Down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~3	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
BUZ	Operates Continuously	Stop
SIO	Operates Continuously	Only operate with external clock
LCD Controller	Operates Continuously	Stop (Can be operated with sub clock)
Internal OSC (8MHz)	Oscillation	Stop when the system clock (fx) is f_{IRC}
WDTRC OSC (60kHz)	Stop	Can be operated with setting value
Main OSC (1~12MHz)	Oscillation	Stop when fx = f_{XIN}
Sub OSC (32.768kHz)	Oscillation	Stop when fx = f_{SUB}
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0,EC2), SIO (External clock), External Interrupt, WT (sub clock), WDT

12.3 IDLE Mode

The power control register is set to '01h' to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

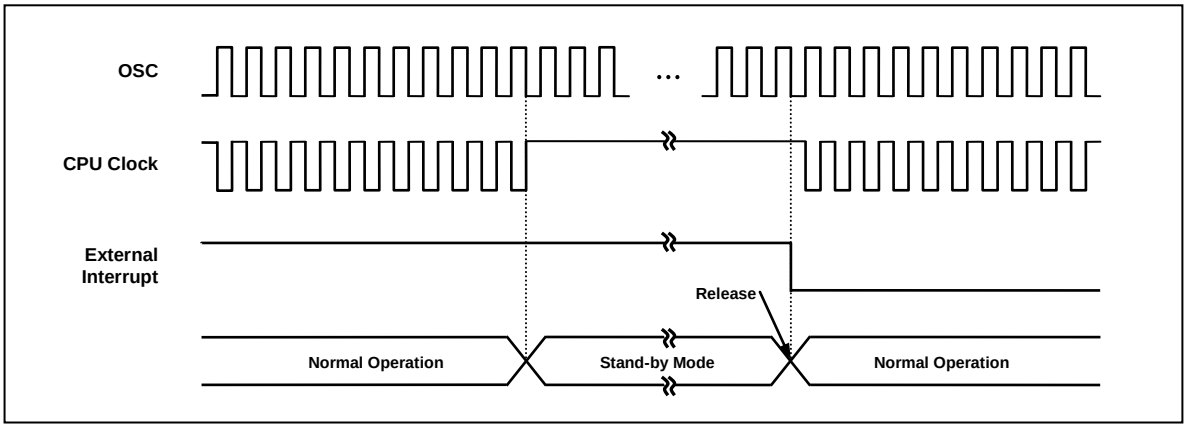


Figure 12.1 IDLE Mode Release Timing by External Interrupt

12.4 STOP Mode

The power control register is set to '03H' to enter the STOP Mode. In the stop mode, the selected oscillator, system clock and peripheral clock is stopped, but watch timer can be continued to operate with sub clock. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held. For example, If the internal RC oscillator (f_{IRC}) is selected for the system clock and the sub clock (f_{SUB}) is oscillated, the internal RC oscillator stops oscillation and the sub clock is continuously oscillated in stop mode. At that time, the watch timer and LCD controller can be operated with the sub clock.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers.

When exit from STOP mode, enough oscillation stabilization time is required to normal operation. Figure 12.2 shows the timing diagram. When released from STOP mode, the Basic interval timer is activated on wake-up. Therefore, before STOP instruction, user must be set its relevant prescale divide ratio to have long enough time. This guarantees that oscillator has started and stabilized.

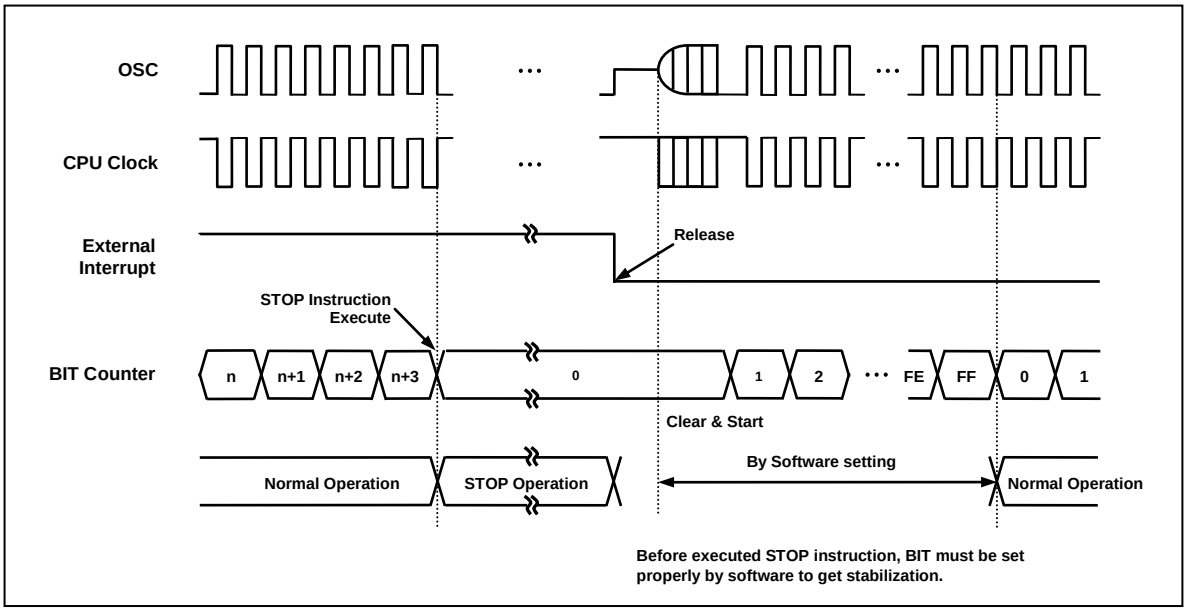


Figure 12.2 STOP Mode Release Timing by External Interrupt

12.5 Release Operation of STOP Mode

After STOP mode is released, the operation begins according to content of related interrupt register just before STOP mode start (Figure 12.3). If the global interrupt Enable Flag (IE.EA) is set to `1`, the STOP mode is released by the interrupt which each interrupt enable flag = `1` and the CPU jumps to the relevant interrupt service routine. Even if the IE.EA bit is cleared to '0', the STOP mode is released by the interrupt of which the interrupt enable flag is set to '1'.

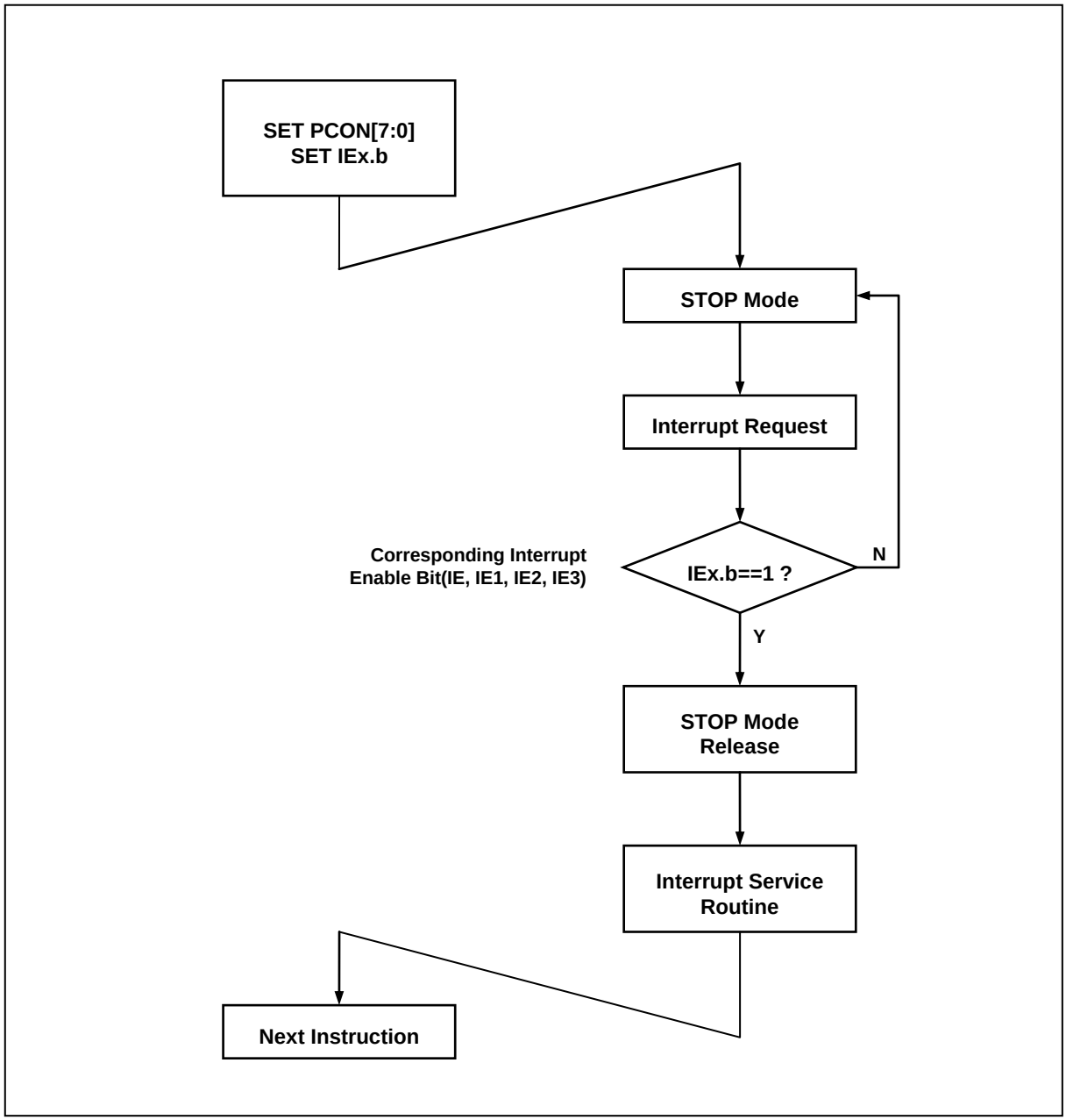


Figure 12.3 STOP Mode Release Flow

12.5.1 Register Map

Table 12-2 Power Down Operation Register Map

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register

12.5.2 Power Down Operation Register Description

The power down operation register consists of the power control register (PCON).

12.5.3 Register Description for Power Down Operation

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value : 00H

PCON[7:0] Power Control

01H IDLE mode enable

03H STOP mode enable

NOTES) 1. To enter IDLE mode, PCON must be set to ‘01H’.

2. To enter STOP mode, PCON must be set to ‘03H’.

3. The PCON register is automatically cleared by a release signal in STOP/IDLE mode.

4. Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples.

```
Ex1)  MOV   PCON, #01H   ; IDLE mode
      NOP
      NOP
      NOP
       •
       •
       •

Ex2)  MOV   PCON, #03H   ; STOP mode
      NOP
      NOP
      NOP
       •
       •
       •
```

13. RESET

13.1 Overview

The following is the hardware setting value.

Table 13-1 Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

13.2 Reset Source

The MC96P6608/P6408 has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset (EVA chip only)

13.3 RESET Block Diagram

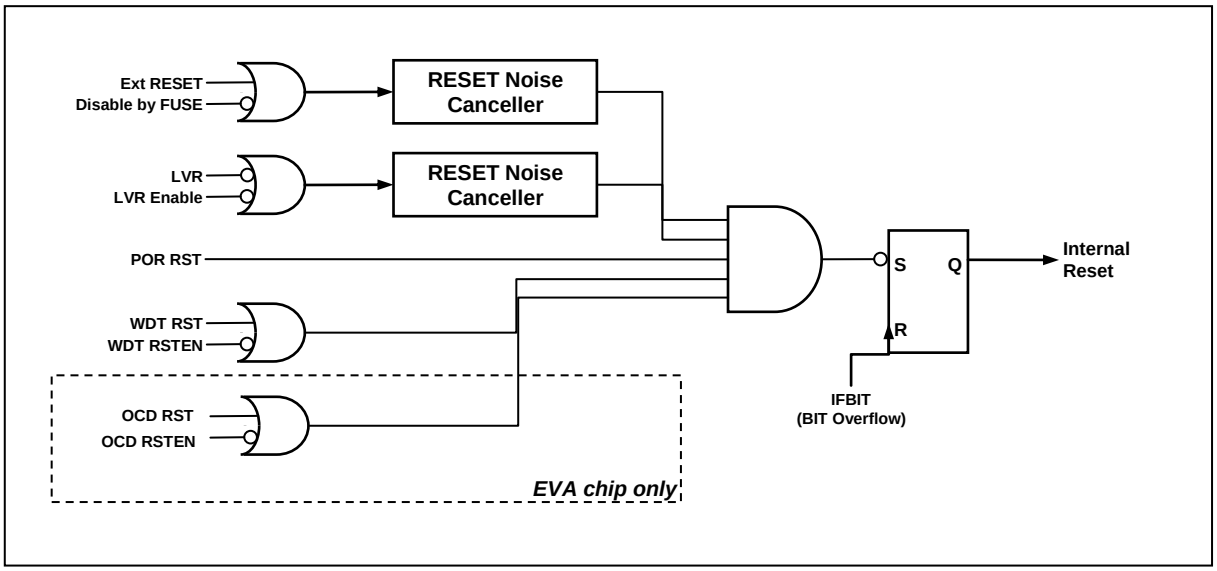


Figure 13.1 RESET Block Diagram

13.4 RESET Noise Canceller

The Figure 13.2 is the noise canceller diagram for noise cancellation of RESET. It has the noise cancellation value of about 2us (@V_{DD}=5V) to the low input of system reset.

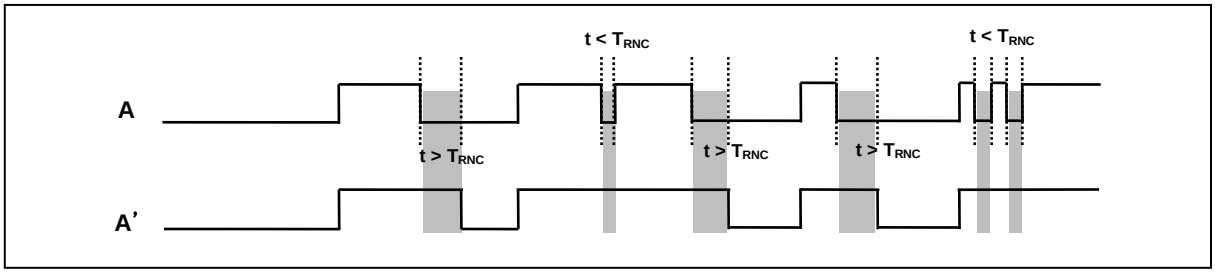


Figure 13.2 Reset Noise Canceller Timer Diagram

13.5 Power On RESET

When rising device power, the POR (Power On Reset) has a function to reset the device. If POR is used, it executes the device RESET function instead of the RESET IC or the RESET circuits.

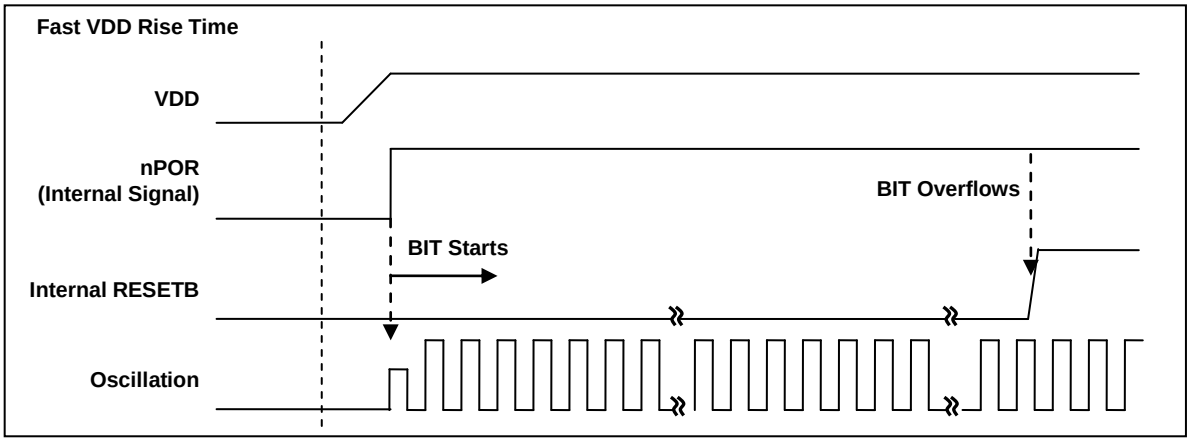


Figure 13.3 Fast VDD Rising Time

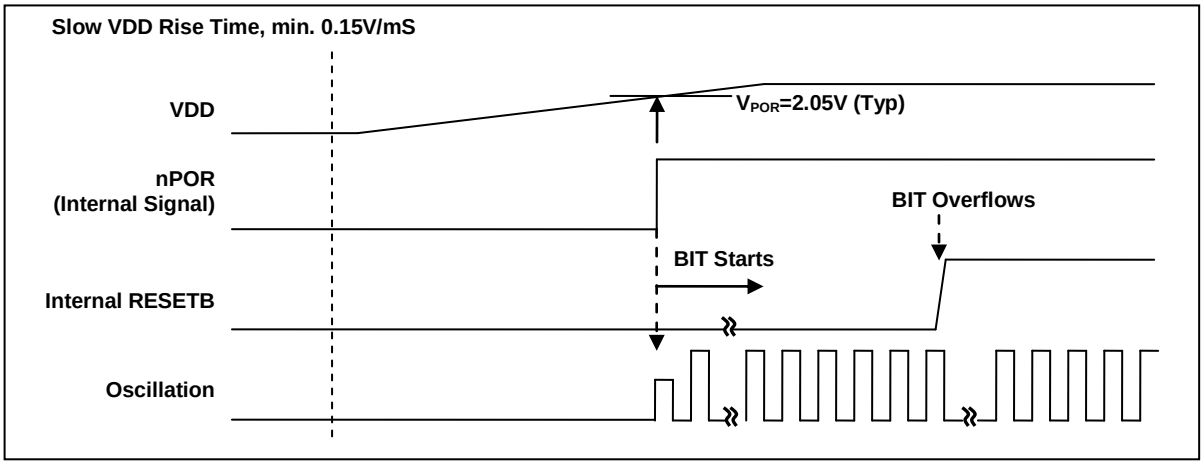


Figure 13.4 Internal RESET Release Timing On Power-Up

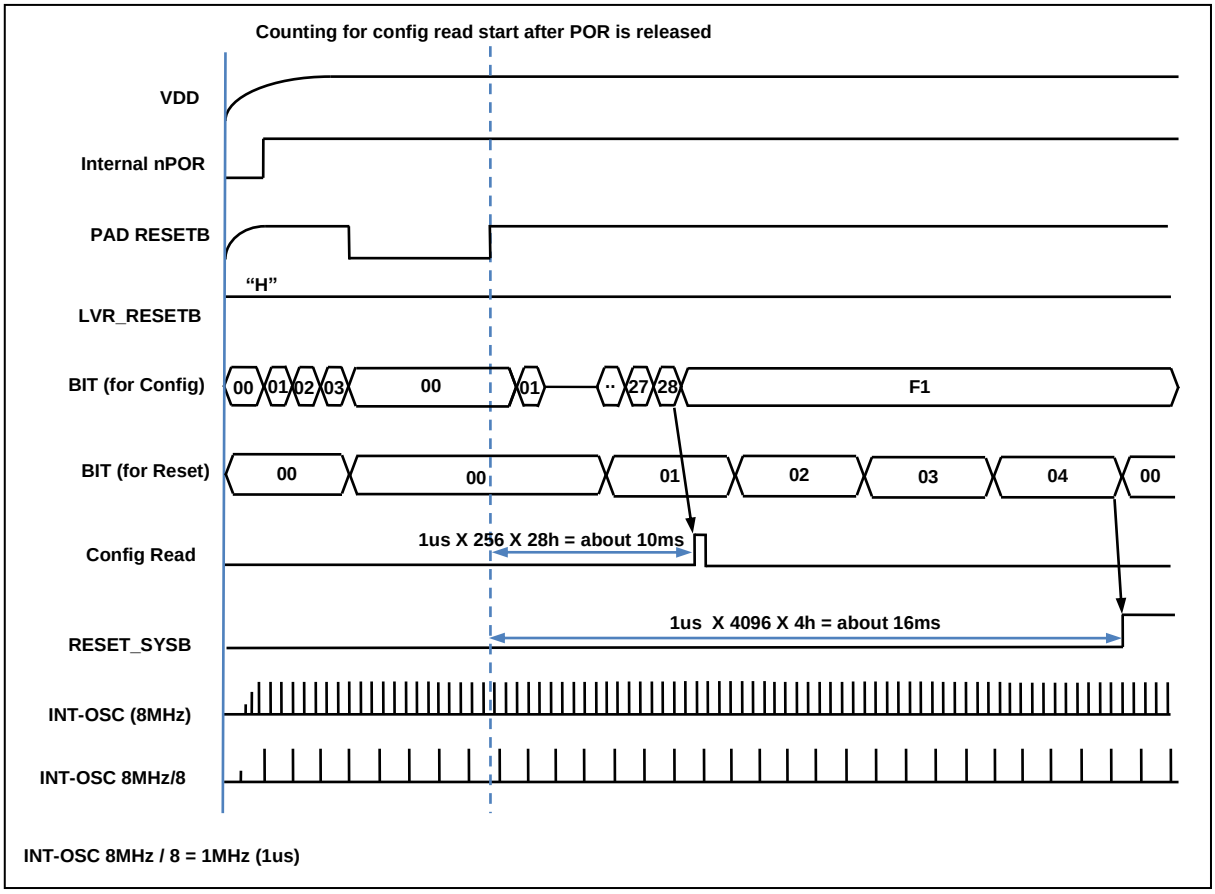


Figure 13.5 Configuration Timing when Power-on

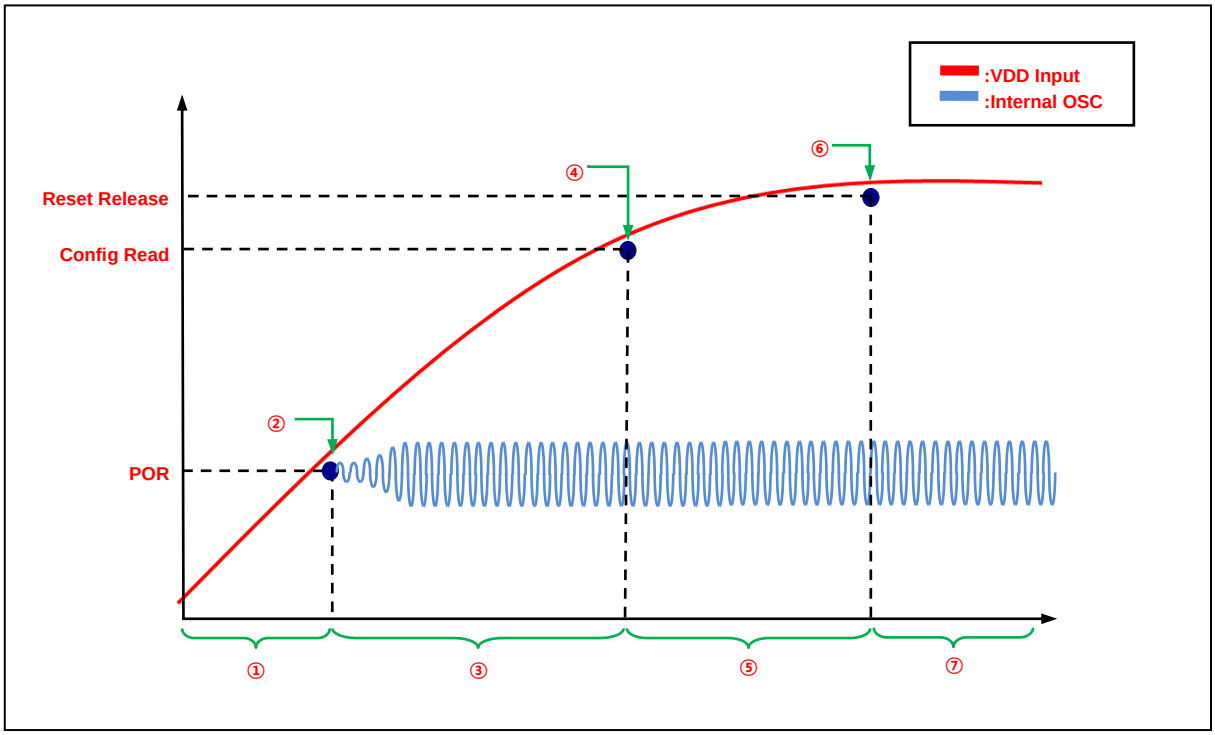


Figure 13.6 Boot Process Wave Form

Table 13-2 Boot Process Description

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection	-about 2.05V
③	- (INT-OSC 8MHz/8)x256x28h Delay section (=10ms) -VDD input voltage must rise over than OTP operating voltage for Config read	-Slew Rate >= 0.15V/ms
④	- Config read point	-over 1.7V -Config Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-18.6ms point after POR or Ext_reset release
⑥	- Reset Release section (BIT overflow) i) after18.6ms, after External Reset Release (External reset) ii) 18.6ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

13.6 External RESETB Input

The External RESETB is the input to a Schmitt trigger. If RESETB pin is held with low for at least 10us over within the operating voltage range and stable oscillation, it is applied and the internal state is initialized. After reset state becomes '1', it needs the stabilization time with 16ms and after the stable state, the internal RESET becomes '1'. The Reset process step needs 5 oscillator clocks. And the program execution starts at the vector address stored at address 0000H.

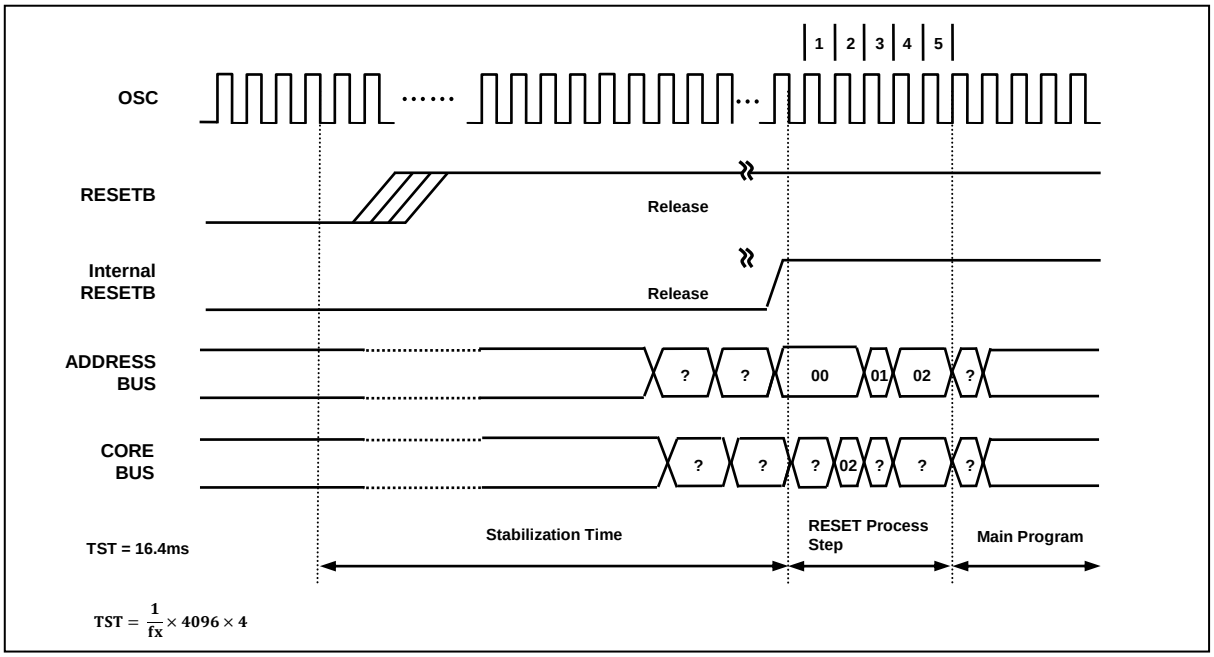


Figure 13.7 Timing Diagram after RESET

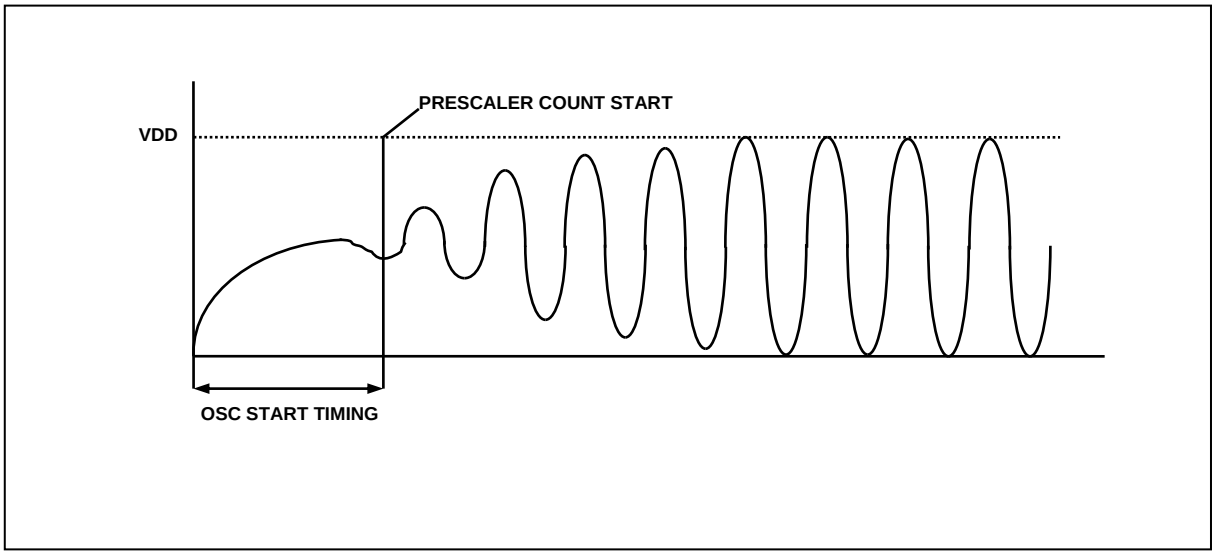


Figure 13.8 Oscillator Generating Waveform Example

Note) As shown Figure 13.8, the stable generating time is not included in the start-up time.
The RESETB pin has not an internal Pull-up register by H/W.

13.7 Brown Out Detector Processor

The MC96P6608/P6408 has an On-chip brown-out detection circuit (BOD) for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by LVRVS[1:0] bit to be 2.4V, 2.7V, 3.0V, 3.9V. In the STOP mode, this will contribute significantly to the total current consumption. So to minimize the current consumption, the LVREN bit is set to off by CONFIGURE OPTION 2.

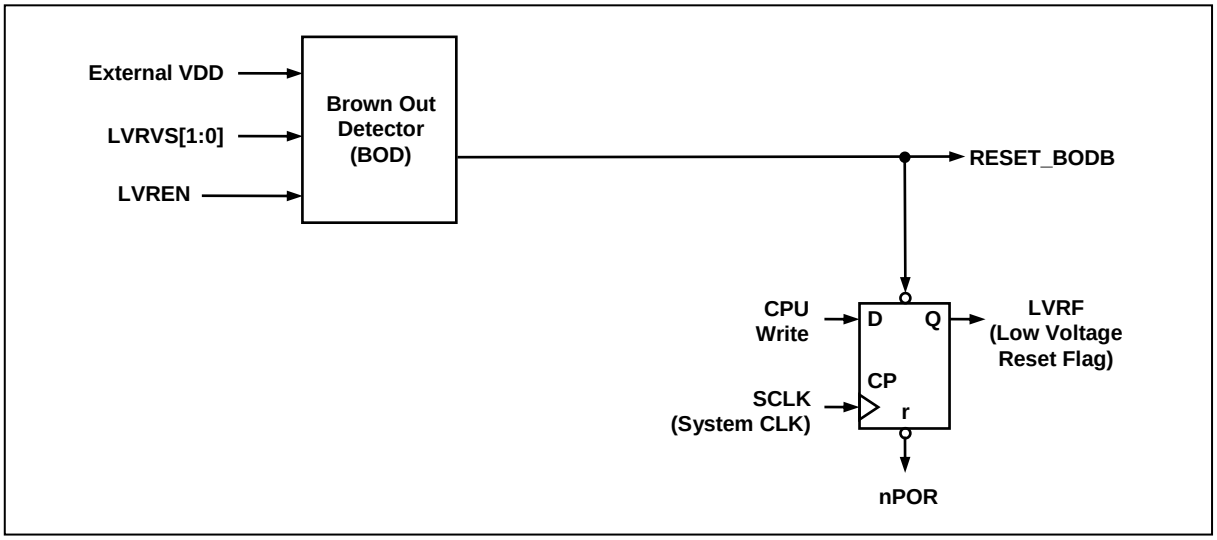


Figure 13.9 Block Diagram of BOD

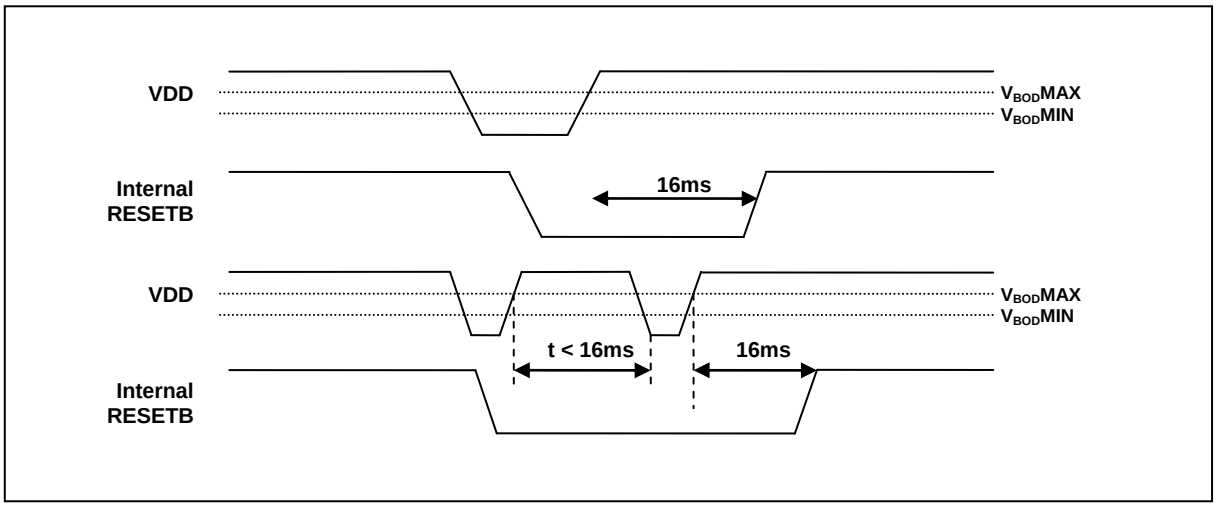


Figure 13.10 Internal Reset at the Power Fail Situation

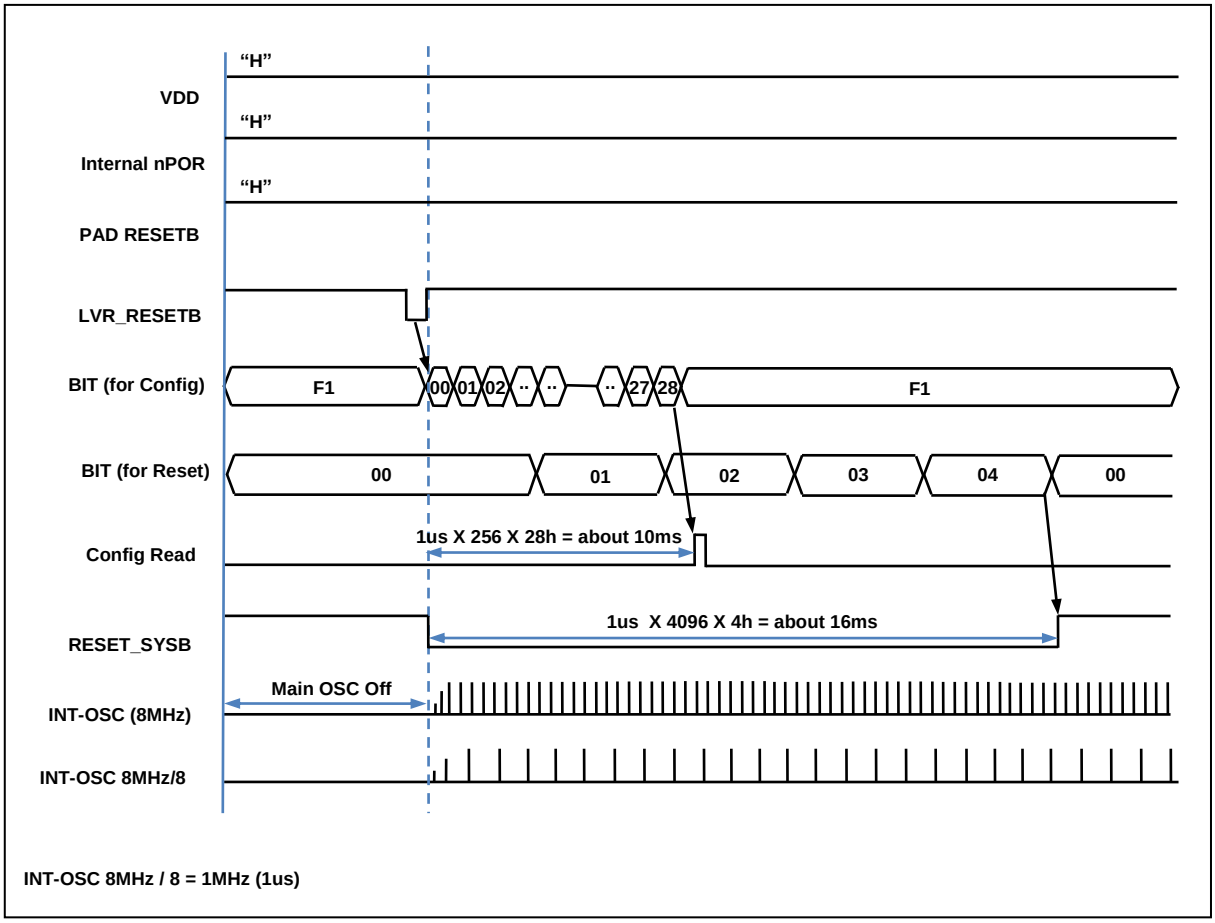


Figure 13.11 Configuration Timing when BOD RESET

13.8 LVI Block Diagram

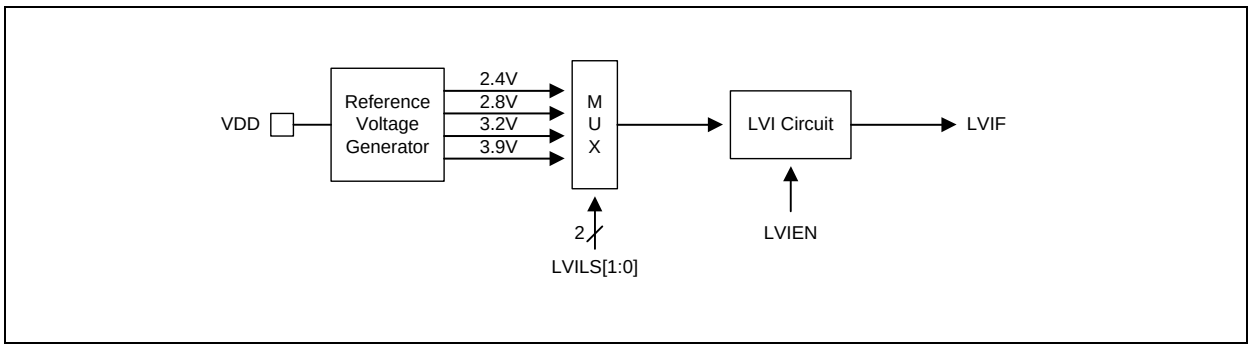


Figure 13.12 LVI Diagram

13.8.1 Register Map

Table 13-3 Reset Operation Register Map

Name	Address	Dir	Default	Description
RSTFR	86H	R/W	80H	Reset Flag Register
PORCR	FEH	R/W	00H	Power On Reset Control Register
LVICR	E1H	R/W	00H	Low Voltage Indicator Control Register

13.8.2 Reset Operation Register Description

The reset control register consists of the reset flag register (RSTFR), power on reset control register (PORCR), and low voltage indicator control register (LVICR).

13.8.3 Register Description for Reset Operation

RSTFR (Reset Flag Register) : 86H

7	6	5	4	3	2	1	0
PORF/LVRF	EXTRF	WDTRF	OCDRF	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–

Initial value : 80H

PORF/LVRF Power-On Reset or Low Voltage Reset flag bit. The bit is reset by writing '0' to this bit.

0 No detection

1 Detection

EXTRF External Reset (RESETB) flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

WDTRF Watch-Dog Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

NOTES) 1. When the Power-On Reset occurs, the PORF/LVRF bit is only set to "1", the other flag (WDTRF and OCDRF) bits are all cleared to "0".

2. When the Power-On Reset occurs, the EXTRF bit is unknown, At that time, the EXTRF bit can be set to "1" when External Reset (RESETB) occurs.

3. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous values.

4. The WDTRF and EXTRF flags are not set to "1", even if a reset occurs by watch-dog and external pin when LVR and POR are disable.

PORCR (Power On Reset Control Register) : FEH

7	6	5	4	3	2	1	0
PORCR7	PORCR6	PORCR5	PORCR4	PORCR3	PORCR2	PORCR1	PORCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PORCR[7:0] POR Enable/Disable

5AH POR disable

Others POR enable (2.05V)

NOTE) If the POR is changed disable to enable during the LVR is selected as disable by configure option, A Reset occurs.

LVICR (Low Voltage Indicator Control Register) : E1H

7	6	5	4	3	2	1	0
–	–	LVIF	LVIEN	–	–	LVILS1	LVILS0
–	–	R/W	R/W	–	–	R/W	R/W

Initial value : 00H

LVIF Low Voltage Indicator Flag Bit

0 No detection

1 Detection

LVIEN LVI Enable/Disable

0 Disable

1 Enable

LVILS[1:0] LVI Level Select

LVILS1	LVILS0	Description
0	0	2.4V
0	1	2.8V
1	0	3.2V
1	1	3.9V

14. On-chip Debug System (EVA Chip Only)

14.1 Overview

14.1.1 Description

The program memory of MC96P6608/P6408 are OTP type, and MC96P6608/P6408 aren't equipped with on-chip debugger (OCD). It is not recommended to develop and debug program with MC96P6608/P6408.

MC96P6608L-EVA/P6408L-EVA are the evaluation chip(EVA chip) for MC96P6608/P6408. OCD is embedded in MC96P6608L-EVA/P6408L-EVA and the program memory of MC96P6608L-EVA/ P6408L-EVA are designed with SRAM. So, it is possible to develop and debug program for MC96P6608/P6408 with MC96P6608L-EVA/ P6408L-EVA. Because SRAM is the program memory of MC96P6608L-EVA/P6408L-EVA, it is required to control power carefully. If the power is off, the contents of the program memory are vanished.

The on-chip debugger system of MC96P6608/P6408 doesn't support ROM writing function. So, it is necessary to equip additional ROM writer("PGM Plus") to write program to MC96P6608/P6408. It is possible to get "PGM Plus" through our web-site(www.abov.co.kr).

Detail descriptions for programming via the OCD interface can be found in the following chapter. Figure 14.5 shows a block diagram of the OCD interface and the On-chip Debug system.

14.1.2 EVA Chip Pin Assignment

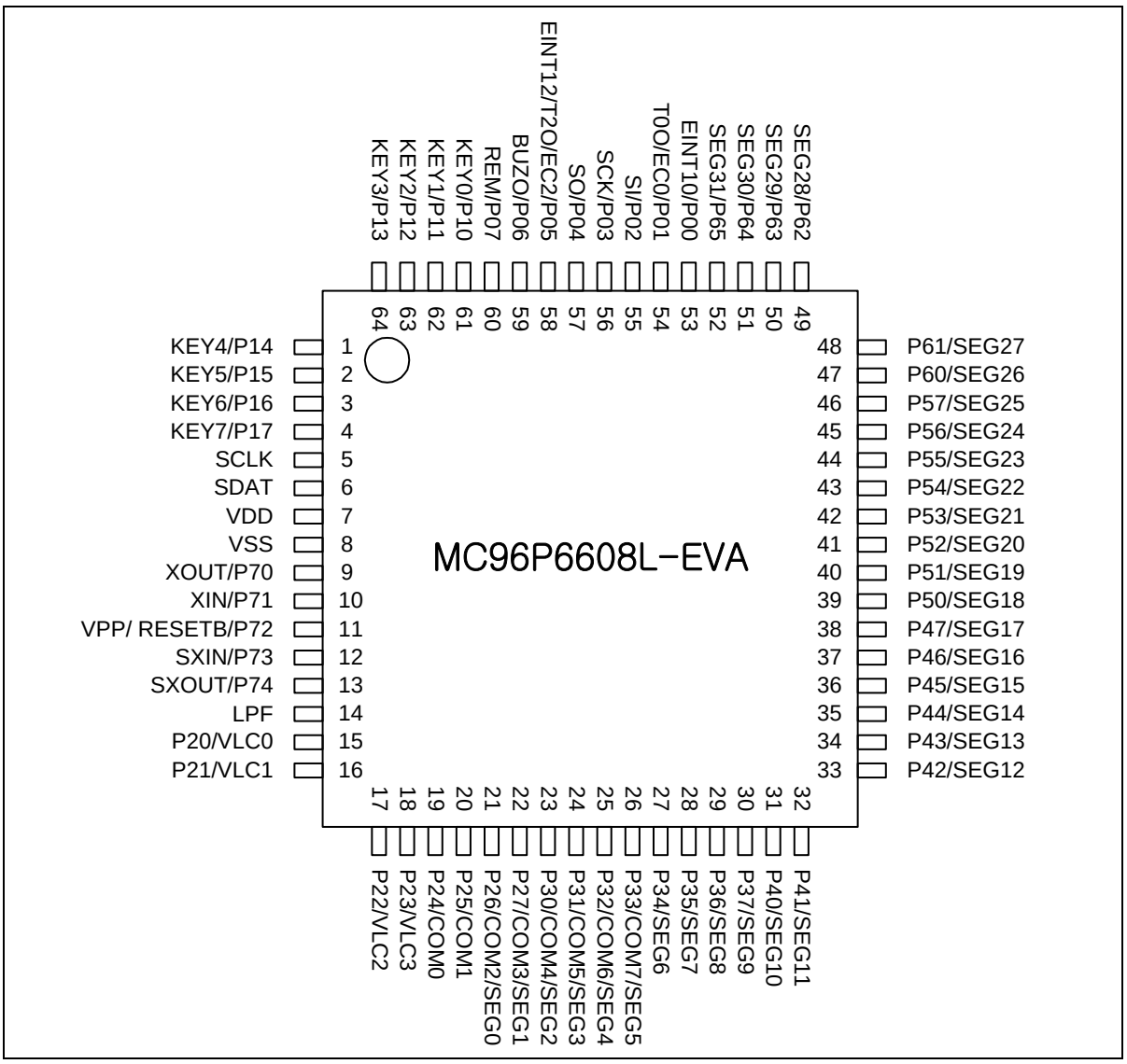


Figure 14.1 MC96P6608L-EVA Pin Assignment

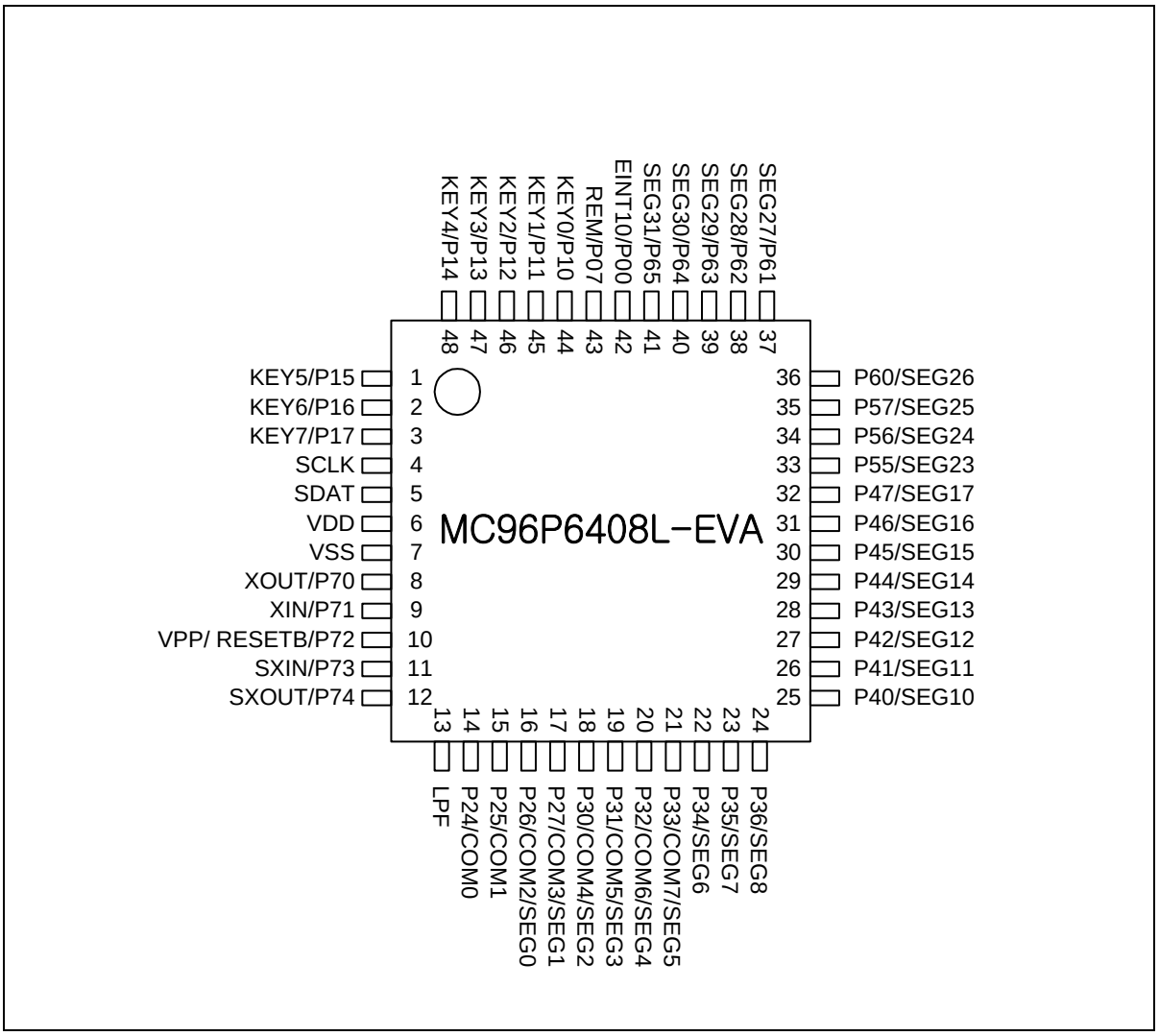


Figure 14.2 MC96P6408L-EVA Pin Assignment

14.1.3 EVA Chip Package Diagram

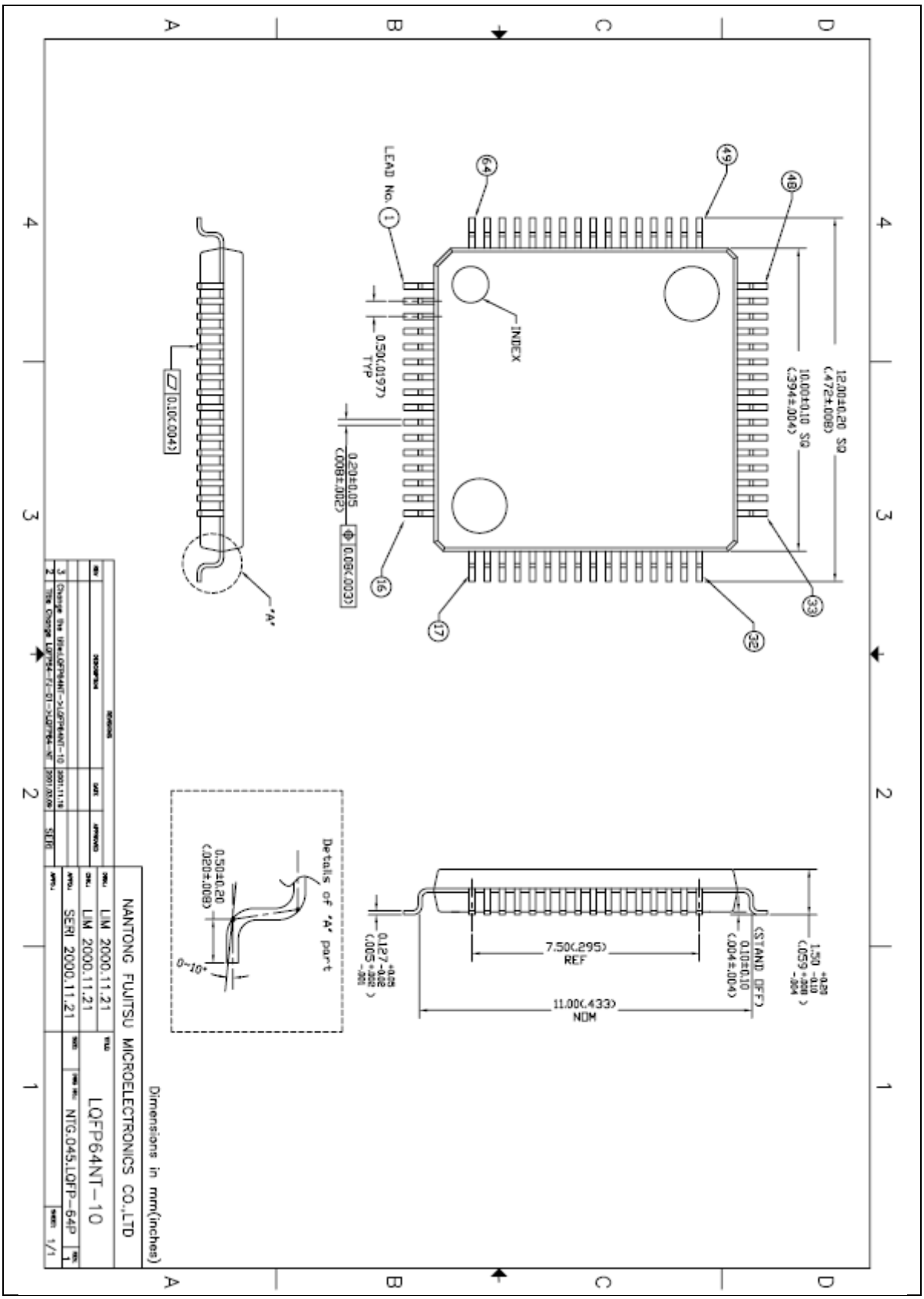
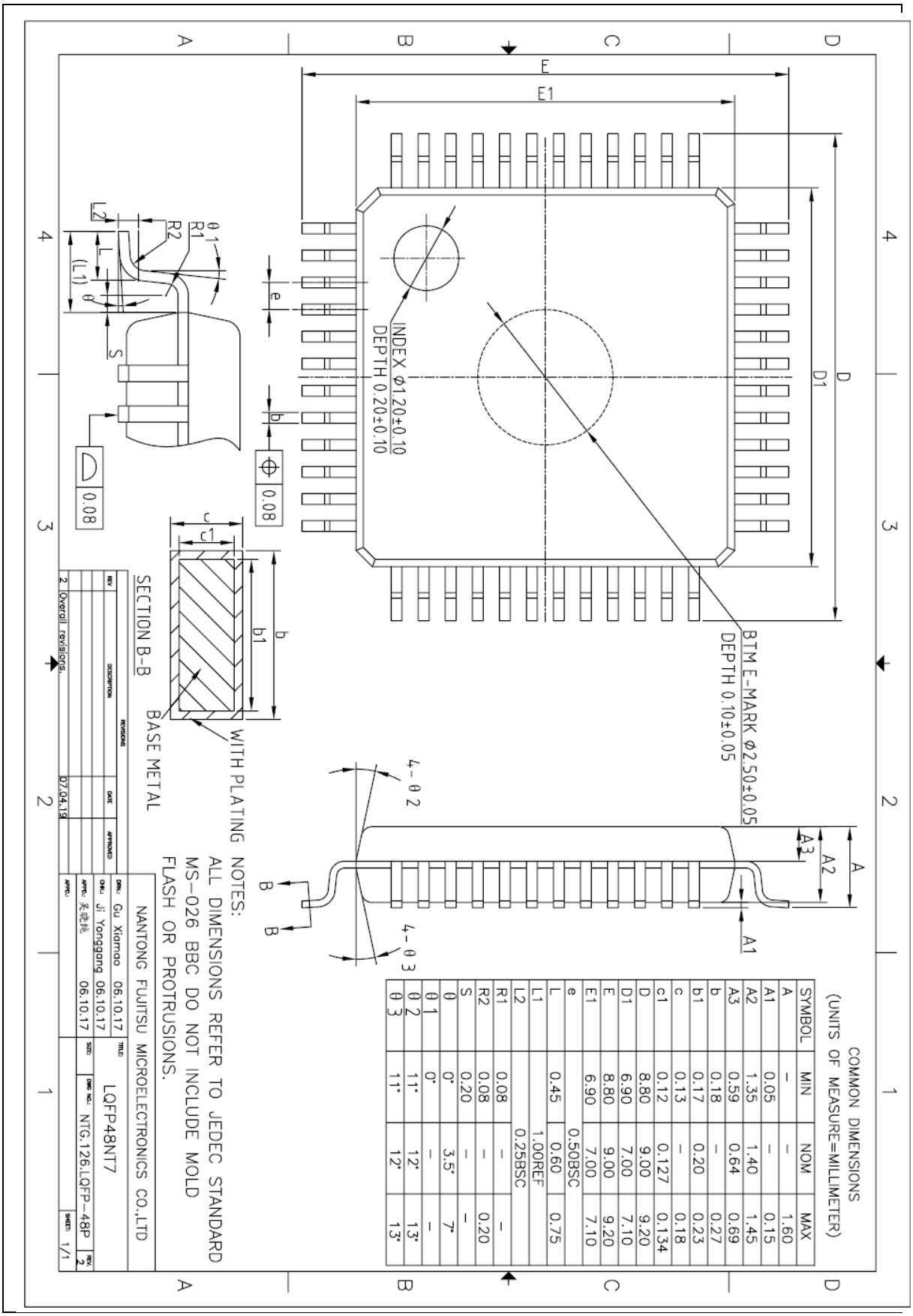


Figure 14.3 MC96P6608L-EVA 64 LQFP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 14.4 MC96P6408L-EVA 48 LQFP Package

14.1.4 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Program Memory (SRAM in cace of EVA chip)
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the two-wire Interface (not support for OTP chip)
  - On-chip Debugging Supported by Dr.Choice®
- Operating frequency

  Supports the maximum frequency of the target MCU

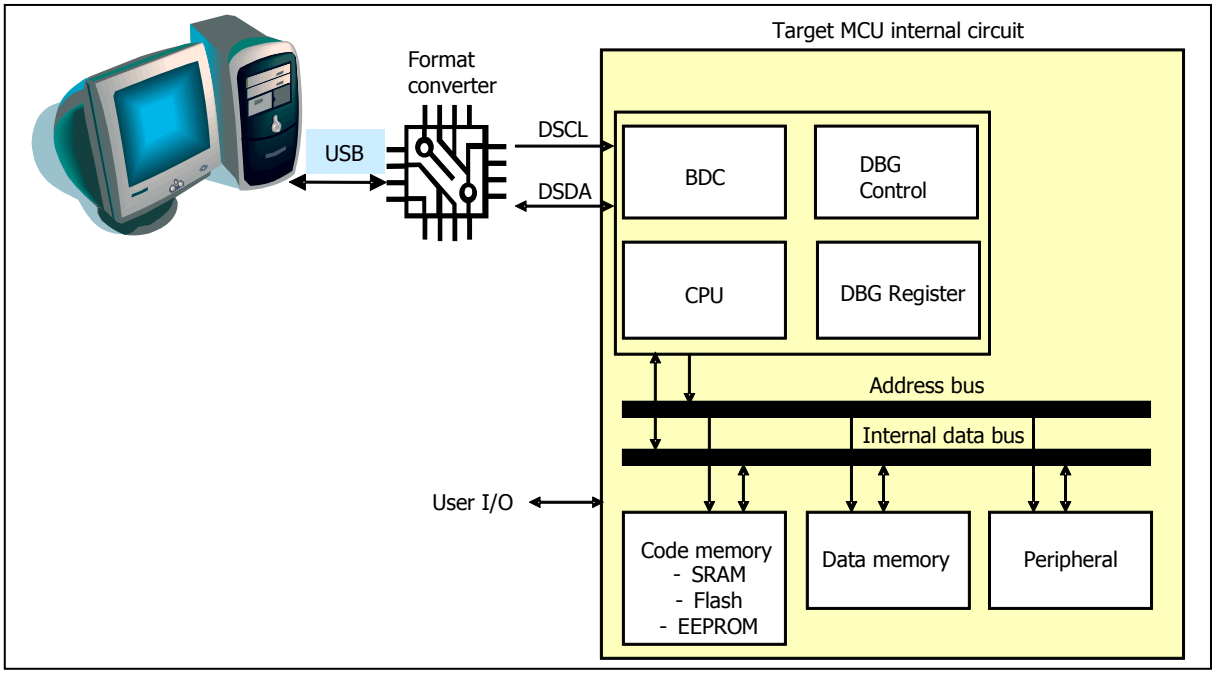


Figure 14.5 Block Diagram of On-Chip Debug System

14.2 EVA Chip OCD Interface

14.2.1 EVA Chip OCD Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

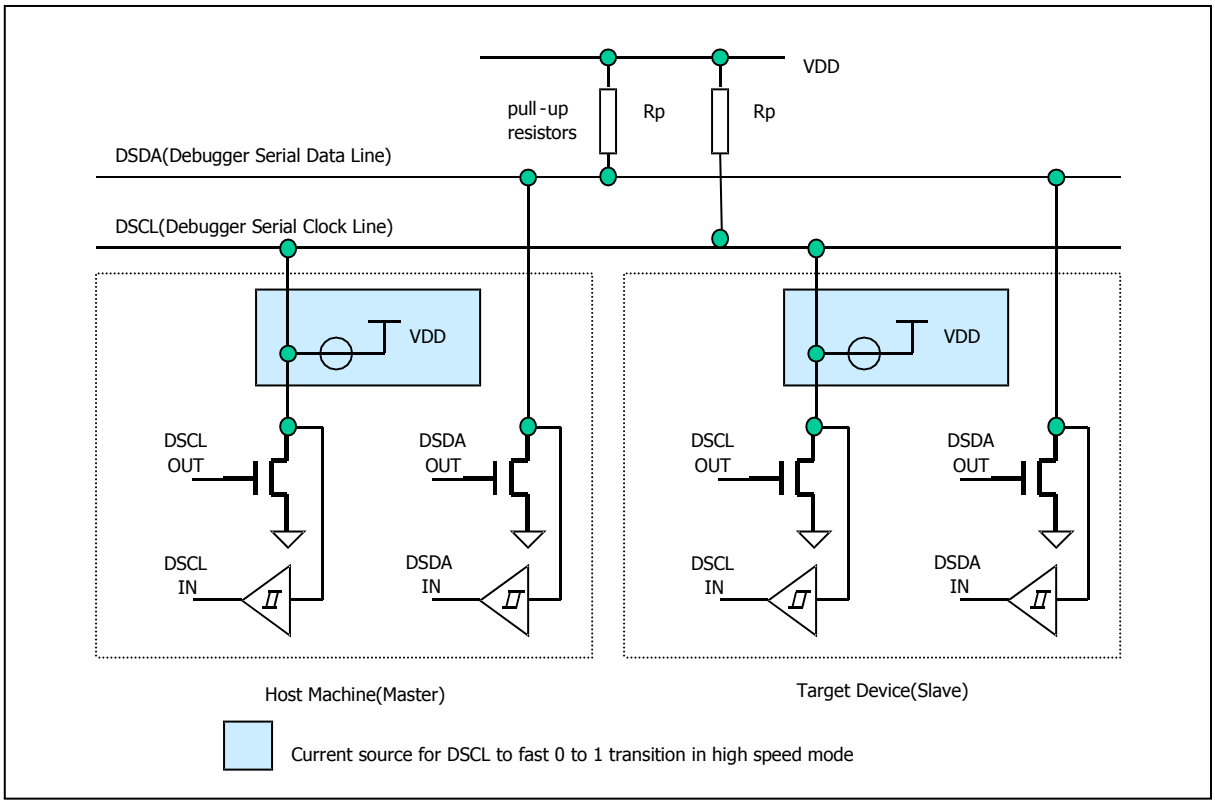


Figure 14.6 Connection of Transmission

15. Configure Option

15.1 Configure Option

The data for configure option should be written in the configure option area (001EH – 001FH) by programmer (Writer tools).

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	–	–	–	–	–	–	–

Initial value : 00H

R_P Read Protection

0 Disable “Read protection”

1 Enable “Read protection”

CONFIGURE OPTION 2 : ROM Address 001EH

7	6	5	4	3	2	1	0
LVREN	LVRVS1	LVRVS0	–	–	–	SOSC	MOSC

Initial value : 00H

LVREN LVR Operation

0 LVR enable (P72 port)

1 LVR disable (RESETB port)

LVRVS [1:0] LVR Voltage Select

LVRVS1	LVRVS0	Description
0	0	2.4V
0	1	2.7V
1	0	3.0V
1	1	3.9V

SOSC Sub Oscillator Select

0 P73/P74 normal ports

1 SXIN/SXOUT sub oscillator

MOSC Main Oscillator Select

0 P71/P70 normal ports

1 XIN/XOUT main oscillator

NOTE) To use LVR function, PORCR must be set to ‘5AH’.

16. APPENDIX

A. Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.
Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65

XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2

ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	3	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

B. Instructions on how to use the input port.

- Error occur status
  - Using compare jump instructions with input port, it could cause error due to the timing conflict inside the MCU.
  - Compare jump Instructions which cause potential error used with input port condition:

```
JB      bit, rel      ; jump on direct bit=1
JNB     bit, rel      ; jump on direct bit=0
JBC     bit, rel      ; jump on direct bit=1 and clear
CJNE    A, dir, rel ; compare A, direct jne relative
DJNZ    dir, rel      ; decrement direct byte, jnz relative
```

  - It is only related with Input port. Internal parameters, SFRs and output bit ports don't cause any error by using compare jump instructions.
  - If input signal is fixed, there is no error in using compare jump instructions.

- Error status example

```
while(1){
  if (P00==1){ P10=1; }
  else { P10=0; }
  P11^=1;
}
```

```
zzz:  JNB    080.0, xxx  ; it possible to be error
      SETB   088.0
      SJMP   yyy
xxx:  CLR    088.0
yyy:  MOV    C,088.1
      CPL    C
      MOV    088.1,C
      SJMP   zzz
```

```
unsigned char ret_bit_err(void)
{
  return !P00;
}
```

```
      MOV    R7, #000
      JB     080.0, xxx  ; it possible to be error
      MOV    R7, #001
xxx:  RET
```

- Preventative measures (2 cases)
  - Do not use input bit port for bit operation but for byte operation. Using byte operation instead of bit oper ation will not cause any error in using compare jump instructions for input port.

```
while(1){
 if ((P0&0x01)==0x01){ P10=1; }
  else { P10=0; }
   P11^=1;
}
```

```
zzz:  MOV    A, 080        ; read as byte
      JNB    0E0.0, xxx    ; compare
      SETB   088.0
      SJMP   yyy
xxx:  CLR    088.0
yyy:  MOV    C,088.1
      CPL    C
      MOV    088.1,C
      SJMP   zzz
```

- If you use input bit port for compare jump instruction, you have to copy the input port as internal paramet er or carry bit and then use compare jump instruction.

```
bit tt;
while(1){
  tt=P00;
  if (tt==0){ P10=1;}
  else {P10=0;}
  P11^=1;
}
```

```
zzz:  MOV   C,080.0     ; input port use internal parameter
      MOV   020.0, C    ; move
      JB    020.0, xxx  ; compare
      SETB  088.0
      SJMP  yyy
xxx:  CLR   088.0
yyy:  MOV   C,088.1
      CPL   C
      MOV   088.1,C
      SJMP  zzz
```