MRTL

INTEGRATED CIRCUITS

mW MRTL

MC800 Series (0 to +75°C)
MC900 Series (−55 to +125°C)

NEW MRTL AND mW MRTL

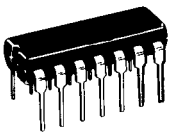
The new MRTL and mW MRTL 800 Series described in this selector quide are now designed to exceed both the old MC700 and the old MC800 Series electrical characteristics. This has been accomplished by combining the critical electrical parameters of both the MC700 and MC800 Series into one standard series, the new MC800 Series.

Medium-power MRTL integrated circuits provide a broad line of low-cost, multi-function, digital circuits. Typical gate speed is 12 ns, with power dissipation averages of 19 mW (input high) and 5.0 mW (inputs low) per logic node. Devices from the MC800 Series have loading factors normalized for compatibility with the low-power mW MRTL devices for ease in mixing the two power levels in a system.

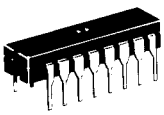
Low-power mW MRTL integrated circuits are designed for use where minimal system power consumption is desired. Typical gate speed is 27 ns, with typical power dissipation of 6.5 mW (input high) and 0.5 mW (inputs low) per logic node. Devices from the mW MRTL Series can be mixed with devices from the medium-power MRTL Series which has loading factors normalized for compatibility.

G SUFFIX
METAL PACKAGE
CASE 601

G SUFFIX
METAL PACKAGE
CASE 603
TO-100

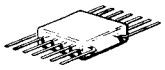


P SUFFIX
PLASTIC PACKAGE
CASE 646

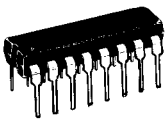


L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

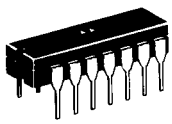


F SUFFIX
CERAMIC PACKAGE
CASE 607



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 632
14 LEAD



Functions	MRTL	mW MRTL	Type 1 MC800 Series 0 to +75°C	MC800 Series Case	Type 1 MC900 Series −55 to +125°C	MC900 Series Case	Loading Factors Each Output: MRTL With mW MRTL	Loading Factors Each Output: MRTL With MRTL	Loading Factors Each Output: mW MRTL With mW MRTL	tp ns typ	Power: MC800 P&L Series	Dissipation: MC900 F&G Series
Buffer	•				MC900	601,606	80	25	–	20		16/45 2
Counter Adapter	•				MC901	601,606	16	5	–	22		55
R.S. Flip-Flop	•				MC902	601,606	13	4	–	14		22
3-Input NOR Gate	•				MC903	601,606	16	5	–	12		19/5 2
Half Adder	•				MC904	601,606	16	5	–	14		45
Half-Shift Register	•				MC905	601,606	13	4	–	22		53
Half-Shift Register (w/o Inverter)	•				MC906	601,606	13	4	–	22		36
4-Input NOR Gate	•				MC907	601,606	16	5	–	12		19/5 2
Half-Adder		•			MC908	601,606	–	–	4	60		14/8.5 2
2-Input Buffer		•			MC909	601,606	–	–	30	57		5.5/16 2
Dual 3-Input (NOR Gate)		•			MC910	601,606	–	–	4	27		8.0/1.0 2
4-Input OR/NOR Gate		•			MC911	601,606	–	–	4	60		6.0/3.5 2
Half-Adder		•			MC912	601,606	–	–	4	66		11.5/5.5 2
Type D-Flip-Flop		•			MC913	601,606	–	–	3	75		17.5/13.5
Dual 2-Input NOR Gate	•				MC914	601,606	16	5	–	12		38/10 2
Dual 3-Input NOR Gate	•		MC815	646,632	MC915	603,606	16	5	–	12	55/15 2	38.10 2
J.K. Flip-Flop	•		MC816	646,632	MC916	601,606	10	3	–	30	91/79 3	62 54 3
Quad 2-Input NOR Gate		•	MC817	646,632	MC917	607	–	–	4	27	20/5.0 2	16.2 5 2
Dual 3-Input NOR Gate		•	MC818	646,632	MC918	603,606	–	–	4	27	12/2.5 2	9.5 1 0 2
Dual 4-Input NOR Gate		•	MC819	646,632	MC919	607	–	–	4	27	13/2.5 2	11 1 0 2
J.K. Flip-Flop		•			MC920	601,606	–	–	2	50		15 5 10 3
Dual 2-Input Gate Expander		•			MC921	601,606	–	–	–	27		3 0 – 2
J.K. Flip-Flop		•	MC822	646,632	MC922	603,606	–	–	4	70	24/20 3	17 5 10 3
Quad 2-Input NOR Gate	•		MC824,A	646,632	MC924	607	16	5	–	12	100/30 2	76 20 2
Dual 4-Input NOR Gate	•		MC825	646,632	MC925	607	16	5	–	12	60/15 2	38 10 2

Functions	MRTL	mW MRTL	Type 1 MC800 Series 0 to +75°C	MC800 Series Case	Type 1 MC900 Series −55 to +125°C	MC900 Series Case	Loading Factors Each Output: MRTL With mW MRTL	Loading Factors Each Output: MRTL With MRTL	Loading Factors Each Output: mW MRTL With mW MRTL	tp ns typ	Power Dissipation: MC800 P&L Series	Power Dissipation: MC900 F&G Series
J.K. Flip-Flop	•		MC826	646,632	MC926	603,606	16	5	–	35	100/86 3	130/65 3
Wuad Inverter	•				MC927	603,606	16	5	–	12		76/20 2
5-Input NOR Gate		•			MC928	601,606	–	–	4	27		6.5/0.5 2
5-Input NOR Gate	•				MC929	601,606	16	5	–	12		19/5 2
Dual Exclusive (OR/NOR Gate)		•	MC864	646,632	–		–	–	4	–	25	
Quad Latch		•	MC867,A	648,620	–		–	–	9	50	110	
BCD to Decimal Decoder		•	MC870	648,620	–		–	–	7	36	100/–	
Quad Exclusive OR Gate	•		MC871	646,632	MC971	607	16	5	–	12	72	28
J.K. Flip-Flop	•				MC974	601,606	16	5	–	35		130/65 3
Dual Half-Adder	•		MC875	646,632	MC975	607	16	5	2	20	120	90
Dual J.K. Flip-Flop		•	MC876	646,632	MC976	607	–	–	–	50	41/29 3	31/20 3
Binary Up Counter	•		MC877	646,632	–		10	3	–	–	180	
Dual Type D Flip-Flop		•	MC878	646,632	MC978	607	–	–	3	60	48/35 5	35/26 5
1 J.K. Flip-Flop, 1 (Expander, 2 Buffers)	•		MC879	646,632	–		–	–	–	–	141/124 4	
Decade Up Counter	•		MC880	646,632	–		10	3	–	–	250	
Dual Buffer		•			MC891	601,606	–	–	30	57		11/32 2
J.K. Flip-Flop		•			MC982	601,606	–	–	2	80		15/13 3
Dual Half-Shift Register	•		MC883	646,632	MC983	607	13	4	–	22	140	110
Dual Half-Shift Register (w/Inverter)	•		MC884	646,632	MC984	607	13	4	–	22	100	75
Quad 2-Input Expander	•		MC885,A	646,632	MC985	607	–	–	–	12	20/– 2	17/– 2
Dual 4-Input Expander	•		MC886	646,632	MC986	607	–	–	–	12	20/– 2	17/– 2
1 J.K. Flip-Flop, 1 Inverter (2, Buffers	•		MC887	646,632	–		–	–	–	–	138/132 4	
Dual 3-Input Buffer (Non-Inverting)	•		MC888	646,632	MC988	607	80	25	–	24	145/56 2	128/42 2
Hex Inverter	•		MC889,A	646,632	MC989	607	16	5	–	12	130/15 2	76/20 2
Dual J.K. Flip-Flop	•		MC890	646,632	MC990	607	10	3	–	35	182/158 3	124/108 3
Dual J.K. Flip-Flop	•		MC891	646,632	MC991	607	16	5	–	40	190/160 3	155/130 3
Triple 3-Input NOR Gate	•		MC892	646,632	MC992	607	16	5	–	12	82/24 2	57/15 2
Triple 3-Input NOR Gate		•	MC893	646,632	MC993	607	–	–	4	27	18/3.5 2	14/2.0 2
Serial-Parallel Shift Register	•		MC894	646,632	–		16	5	–	55	225	
Dual Full Adder	•		MC896	646,632	MC996	607	16	5	–	60	225	190
Dual Full Subtractor	•		MC897	646,632	MC997	607	16	5	–	60	225	190
Dual 2-Input Buffer		•	MC898	646,632	MC998	607	–	–	30	57	14/46 2	11/32 2
Dual Buffer	•		MC899	646,632	MC999	603, 606	80	25	–	15	50/90 2	32/90 2
Dual 4-Channel (Data Selector)	•		MC9801	648,620	–		16	5	–	25	100	
Dual J.K. Flip-Flop	•		MC9802	646,632	–		10	3	–	35	182/158 3	
4-Bit Parallel Full Adder	•		MC9804	648,620	–		6	2	–	125	265	
Dual 4-Channel (Data Distributor)	•		MC9807	648,620	–		16	5	–	25	150	
Quad Schmitt Trigger	•		MC9809	646,632	–		16	5	–	30	95	
Quad 2-Input AND Gate	•		MC9813	646,632	–		16	5	–	28	100	
Quad 2-Input NAND Gate	•		MC9814	646,632	–		16	5	–	35	145	
Quad 2-Input OR Gate	•		MC9815	646,632	–		16	5	–	40	28/100 2	
Hex Inverter		•	MC9818	646,632	–		–	–	4	27	7.0/3.0 2	
Hex Expander	•		MC9819,A	646,632	–		–	–	–	12	13/– 2	
Hex Expander		•	MC9820	646,632	–		–	–	–	12	30/– 2	
Quad 2-Input Expander		•	MC9821	646,632	–		–	–	–	27	20/– 2	
Dual J.K. Flip-Flop		•	MC9822	646,632	–		–	–	4	75	24/– 3	
Quad 2-Input AND Gate		•	MC9823	646,632	–		–	–	4	50	12 6	
Quad 2-Input NAND Gate		•	MC8924	646,632	–		–	–	4	50	20/5.0 2	
Quad 2-Input OR Gate		•	MC9825	646,632	–		–	–	4	50	–/7.0 2	

"A" Suffix devices have insured capability to drive at least one MTTL load or two MDTL loads.

1 G suffix denotes Metal, F suffix Flat Package, P suffix denotes Plastic Package, L suffix denotes dual inline Ceramic Package.

2 Inputs High/Inputs Low unless otherwise noted.

3 Only clock inputs High/Input Low.

4 Only clock inputs high on Flip-Flop, other elements High/Inputs Low.

5 Direct Set & Direct Clear Low, all other inputs high/all inputs low.

6 One input high/one input low.

V_{CC} = 3.0V ± 10% for MC900 Series devices.

V_{CC} = 3.6V ± 10% for MC800 Series devices.

Power Dissipation and t_p typicals at T_A = 25

INSTRUCTIONS FOR USE OF PACKAGE INFORMATION TABLE

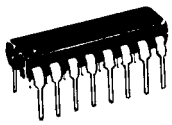
MC900 and MC800 Series Low-Power mW MRTL devices are available in the packages pictured in the following table as indicated on the line following each device type number. Plastic packaged devices are available in the MC800 Series only.

Pin numbers for any of the following devices and packages may be determined by:

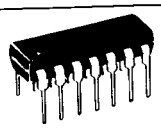
1. Locate the device as shown in the logic diagrams appearing on the preceding pages (grouped by function). Note the alpha pin designations for the device.
2. Find the device type number in the left hand columns of the "Package Information Table".
3. The letters in the columns following the type number and below the drawing of the desired package indicate the correct pin numbers for the specific package by their numbered positions beneath the package drawing. (These letters are the same as indicated on the logic diagram for the device.)
4. Notes: Blanks in an area following the type number and directly beneath a package indicate the device is not available in that package.
   A dash indicates this pin or lead is not connected nor otherwise utilized for this device and package.
   * indicates this pin number is the ground connection for this device and package.
   # indicates this pin number is the V_{CC} connection for this device and package.

PACKAGE INFORMATION TABLE

L OR P SUFFIX
CERAMIC & PLASTIC PACKAGES



CASE 620 (L)
CASE 648 (P)
(16 pin)



CASE 632 (L)
CASE 646 (P)
(14 pin)

Type No.	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	MC908																
	MC909																
	MC910																
	MC911																
	MC912																
	MC913																
MC817	MC917	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC818	MC918	–	b	c	*	e	f	–	–	i	j	#	l	m	–		
MC819	MC919	–	b	c	*	e	f	g	–	i	j	#	l	m	n		
	MC920																
	MC921																
MC822	MC922	–	b	c	*	–	f	–	–	i	j	#	l	m	–		
	MC928																

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MC864	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC867	a	b	c	*	e	f	g	h	i	j	k	–	#	n	p	q
MC870	a	b	c	*	e	f	g	h	i	j	k	l	#	n	p	q
MC876	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC878	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC981																
MC982																
MC893	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC898	–	b	c	*	e	f	–	–	i	j	#	l	m	–		
MC9818	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9820	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9821	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9822	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9823	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9824	a	b	c	*	e	f	g	h	i	j	#	l	m	n		
MC9825	a	b	c	*	e	f	g	h	i	j	#	l	m	n		

F SUFFIX
CERAMIC PACKAGES

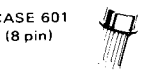
CASE 607
(14 pin)

CASE 606
TO-91
(10 pin)

1	2	3	4	5	6	7	8	9	10	11	12	13	14
a	b	–	d	*	f	g		i	#				
a	b	–	d	*	–	g	–	–	#				
a	b	–	d	*	f	g	–	i	#				
a	b	–	d	*	f	g	–	i	#				
a	b	–	d	*	f	g	–	i	#				
a	b	–	d	*	f	g	–	i	#				
a	b	c	f	g	e	*	h	i	j	n	l	m	#
b	l	m	e	*	f	i	j	c	#				
l	b	c	–	m	n	*	e	f	g	–	i	j	#
a	b	–	d	*	f	g	–	i	#				
a	b	–	d	*	f	g	–	i	#				
l	m	b	c	*	–	f	i	j	#				
a	b	–	d	*	f	g	–	i	#				
1	2	3	4	5	6	7	8	9	10	11	12	13	14
l	m	n	a	b	c	*	e	f	g	h	i	j	#
l	m	n	a	b	c	*	e	f	g	h	i	j	#
a	b	–	c	*	e	f	–	g	#				
a	b	–	c	*	e	f	–	g	#				
a	b	f	g	h	e	*	i	j	l	m	c	n	#
l	m	–	–	b	c	*	e	j	–	–	i	f	#

G SUFFIX
METAL PACKAGES

CASE 603
(10 pin)



CASE 601
(8 pin)

1	2	3	4	5	6	7	8	9	10
a	b	d	*	f	g	i	#		
a	b	d	*	–	g	–	#		
a	b	d	*	f	g	i	#		
a	b	d	*	f	g	i	#		
a	b	d	*	f	g	i	#		
a	b	d	*	f	g	i	#		
b	l	m	c	*	e	f	i	j	#
a	b	d	*	f	g	i	#		
a	b	d	*	f	g	i	#		
l	m	b	c	*	–	f	i	j	#
a	b	d	*	f	g	i	#		
1	2	3	4	5	6	7	8	9	10
a	b	c	*	e	f	g	#		
a	b	c	*	e	f	g	#		

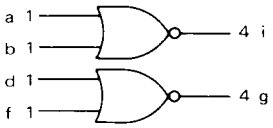
MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Input Voltage	–	+4	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)	–	+6	Vdc
Operating Temperature Range MC900 Series MC800 Series	T_A	 –55 to +125 0 to +75	°C
Storage Temperature Range Metal Packages, Flat Packages Plastic Packages	T_{stg}	 –65 to +150 –55 to +125	°C

The numbers at the end of the terminals indicate loading factors for low-power mW MRTL devices. Pin numbers vary with the package types. The alpha pin designations shown on the logic diagrams, used in conjunction with the Package Information Table (following the logic diagrams), make it possible to ascertain pin numbers for a specific device and package.

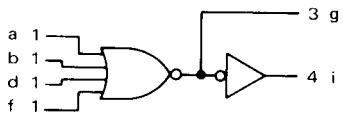
GATES

MC910
Dual 2-Input NOR Gate



$i = \overline{a + b}$

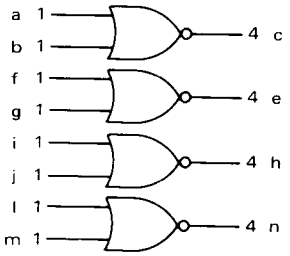
MC911
4-Input OR/NOR Gate



$g = \overline{a + b + d + f}$

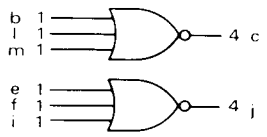
$i = a + b + d + f$

MC817, MC917
Quad 2-Input NOR Gate



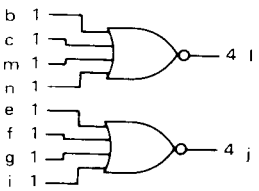
$c = \overline{a + b}$

MC818, MC918
Dual 3-Input NOR Gate



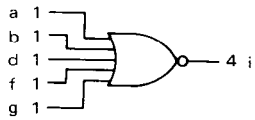
$c = \overline{b + l + m}$

MC819, MC919
Dual 4-Input NOR Gate



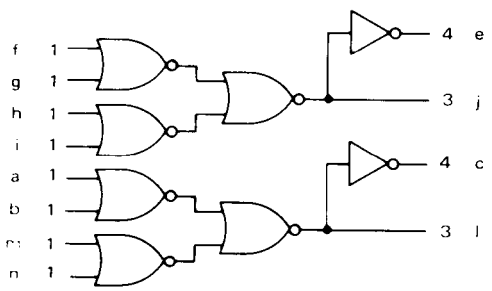
$l = \overline{b + c + m + n}$

MC928
5-Input NOR Gate



$i = \overline{a + b + d + f + g}$

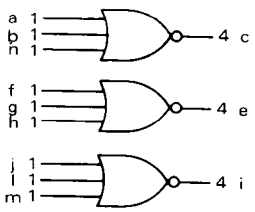
MC864
Dual Exclusive OR-NOR Gate



$l = (a + b) \cdot (m + n)$

$c = \bar{a} \cdot \bar{b} + \bar{m} \cdot \bar{n}$

MC893, MC993
Triple 3-Input NOR Gate

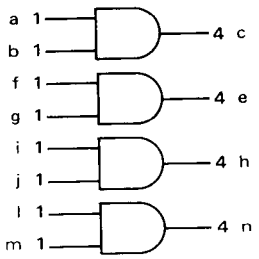


$c = \overline{a + b + n}$

(continued)

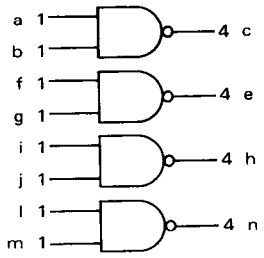
GATES (continued)

MC9823
Quad 2-Input AND Gate



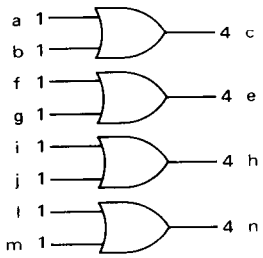
$c = a \cdot b$

MC9824
Quad 2-Input NAND Gate



$c = \overline{a \cdot b}$

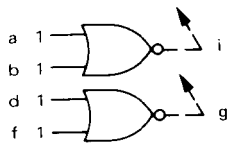
MC9825
Quad 2-Input OR Gate



$c = a + b$

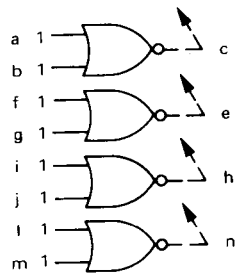
EXPANDERS

MC921
Dual 2-Input Expander



$i = \overline{a + b}$

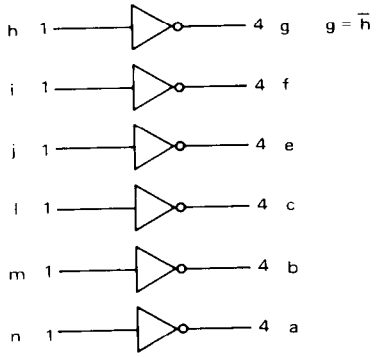
MC9821
Quad 2-Input Expander



$c = \overline{a + b}$

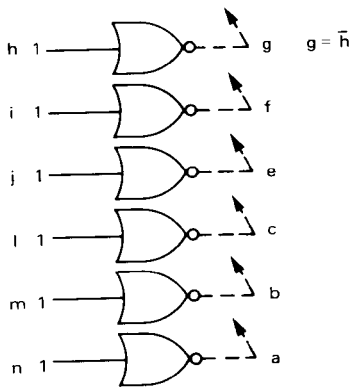
INVERTER

MC9818
Hex Inverter



$g = \overline{h}$

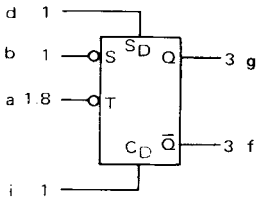
MC9820
Hex Expander



$g = \overline{h}$

FLIP-FLOPS

MC913
Type D Flip-Flop



DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

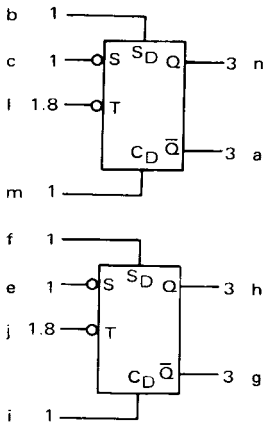
CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

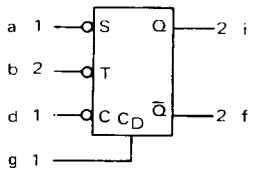
1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse

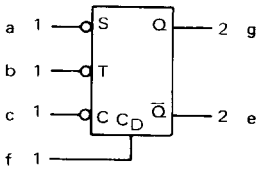
MC878, MC978
Dual Type D Flip-Flop



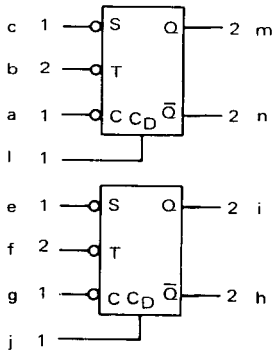
MC920
J-K Flip-Flop



MC982
J-K Flip-Flop



MC876, MC976
Dual J-K Flip-Flop



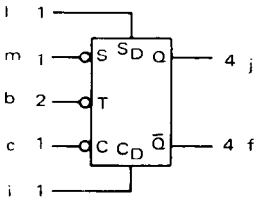
CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

Direct input (C_D) must be low.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse.
t_{n+1} = time period subsequent to negative transition of clock pulse.
Q_n = state of Q output in time period t_n.

NOTE:
Clock pulse fall time must be within the range of 10 ns to 100 ns on all J-K Flip-Flops.

MC822, MC922
J-K Flip-Flop



DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

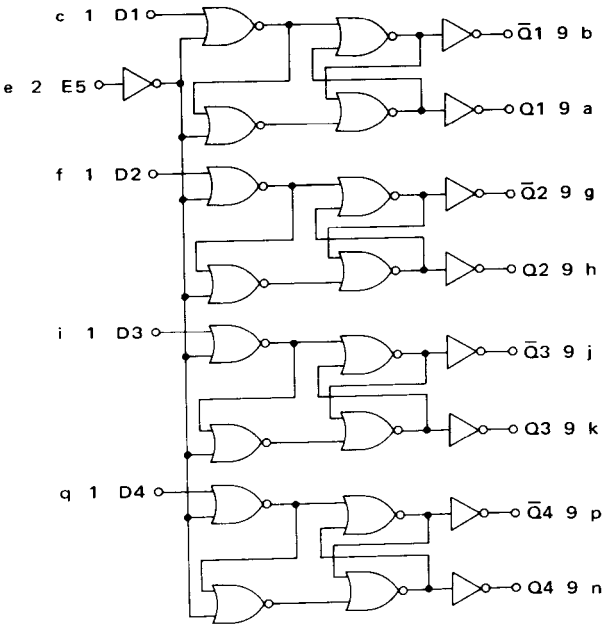
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

(continued)

– FLIP-FLOPS (continued)

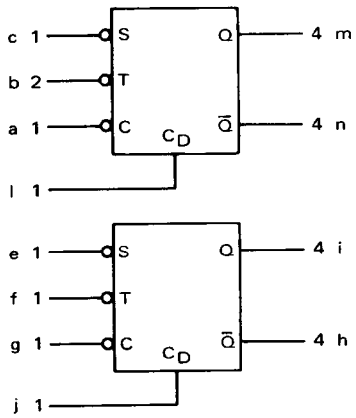
MC867
Quad Latch



TRUTH TABLE

E	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	$\bar{Q}_n$
0	1	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

MC9822
Dual J-K Flip-Flop



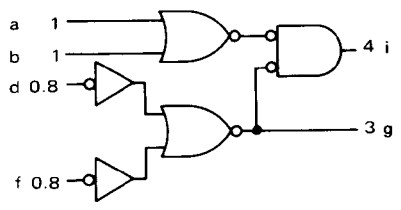
CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

HALF ADDERS

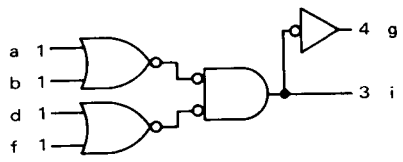
MC908
Half Adder



$i = (a + b)(\bar{d} + \bar{f})$

$g = \overline{\bar{d} + \bar{f}}$

MC912
Half Adder



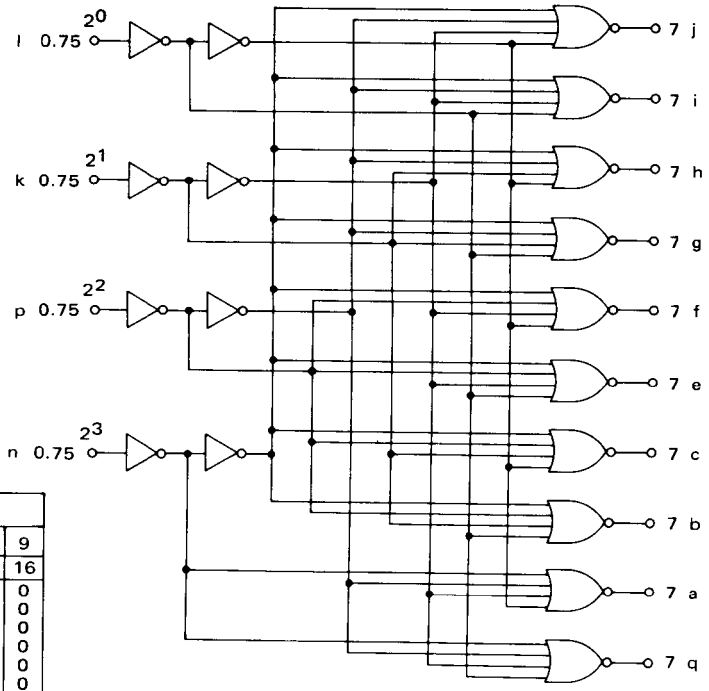
$g = \bar{a} \bullet \bar{b} + \bar{d} \bullet \bar{f}$

$i = (a + b)(d + f)$

mW MRTL LOGIC DIAGRAMS

DECODER

MC870
BCD-to-Decimal Decoder

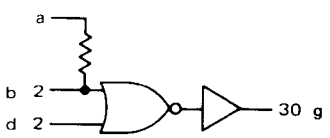


TRUTH TABLE

	INPUT (BCD)				OUTPUT (DECIMAL)									
Value	2^3	2^2	2^1	2^0	0	1	2	3	4	5	6	7	8	9
Pin No.	14	15	11	12	10	9	8	7	6	5	3	2	1	16
Logic Level	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	1	0	0	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	0	0	1	0	0	0	0	0
	0	1	0	1	0	0	0	0	0	1	0	0	0	0
	0	1	1	0	0	0	0	0	0	0	1	0	0	0
	0	1	1	1	0	0	0	0	0	0	0	1	0	0
	1	0	0	0	0	0	0	0	0	0	0	0	1	0
	1	0	0	1	0	0	0	0	0	0	0	0	0	1
	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0	0	0	0	0

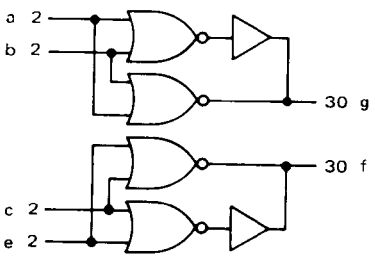
BUFFERS

MC909
Buffer



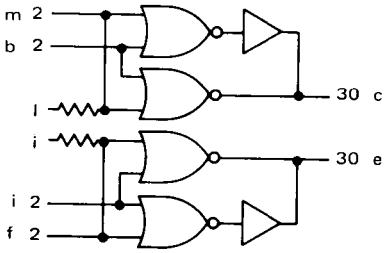
$g = \overline{b + d}$

MC981
Dual Buffers



$g = \overline{a + b}$

MC898, MC998
Dual Buffers

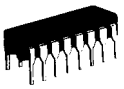


$c = \overline{b + m}$

PACKAGE INFORMATION TABLE

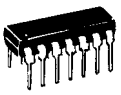
(See instructions on preceding page.)

L OR P SUFFIX
CERAMIC & PLASTIC PACKAGES



CASE 620 (L)
CASE 648 (P)
(16 pin)

CASE 632 (L)
CASE 646 (P)
(14 pin)



F SUFFIX
CERAMIC PACKAGES

CASE 607
(14 pin)

CASE 606
(10 pin)

G SUFFIX
METAL PACKAGES

CASE 603
TO 100
(10 pin)

CASE 601
(8 pin)

Type No.	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	MC900																
	MC901																
	MC902																
	MC903																
	MC904																
	MC905																
	MC906																
	MC907																
	MC914																
MC815	MC915		b	c	•	e	f				i	j	#	l	m	n	
MC816	MC916		b	c	•	e	–	–			i	j	#	l			
MC824	MC924	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC825	MC925		b	c	•	e	f	g			i	j	#	l	m	n	
MC826	MC926		b	c	•		f				i	j	#	l	n		

Type No.	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	MC927																
	MC929																
MC871	MC971	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
	MC974																
MC875	MC975	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC877				c	•	e	f	g	h	i	j	#	l	m	n		
MC879		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC880				c	•	e	f	g	h	i	j	#	l	m	n		
MC883	MC983	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC884	MC984	a	b	c	•	e	f	g	h		j	#	l		n		
MC885	MC985	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC886	MC986		b	c	•	e	f	g		i	j	#	l	m	n		
MC887		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC888	MC988	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC889	MC989	a	b	c	•	e	f	g	h	i	j	#	l	m	n		

Type No.	Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MC890	MC990	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC891	MC991	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC892	MC992	a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC894		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC896	MC996		b	c	•	e	f		h	i	j	#	l	m	n		
MC897	MC997		b	c	•	e	f		h	i	j	#	l	m	n		
MC899	MC999		b	c	•	e	f	–		i	j	#	l	m	–		
MC9801		a	b	c	•	e	f	g	h	i	j	k	l	#	n	p	q
MC9802		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC9804		a	b	c	•	e	f	g	h	i	j	k	l	#	n	p	q
MC9807		a	b	c	•	e	f	g	h	i	j	k	l	#	n	p	q
MC9809		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC9813		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC9814		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC9815		a	b	c	•	e	f	g	h	i	j	#	l	m	n		
MC9819		a	b	c	•	e	f	g	h	i	j	#	l	m	n		

1	2	3	4	5	6	7	8	9	10	11	12	13	14
	b		d	•		g	–	i	#				
	a	**b**	**c**	•	–	**e**	–	**g**	**#**				
	a	–	**c**	•	–	**e**	–	**g**	**#**				
	b	c	d	•			h	–	#				
	b	c	d	•	–	g	h	i	#				
–	b	c	d	•		g	h	i	#				
	b	c	d	•		g	–	i	#				
	b	c	d	•		g	h		#				
	b	c	d	•	–	g	h	i	#				
b	l	m	c	•	e	f	i	j	#				
–	l	b	c	•	–	e	i	j	#				
a	b	c	f	g	e	•	h	i	j	n	l	m	#
l	b	c		m	n	•	e	f	g	–	i	j	#
i	m	b	c	•		f	i	j	#				

1	2	3	4	5	6	7	8	9	10	11	12	13	14
a	b	c	d	•	f	g	h	i	#				
	b	c	d	•		g	h	i	#				
a	b	c	f	g	e	•	h	i	j	n	l	m	#
–	**a**	**b**	**c**	**•**	**–**	**e**	**f**	**g**	**#**				
i	n	a	n	b	c	•	g	h	e	f	j	i	#
n	m	i	c	b	a	•	e	f	g	j	i	h	#
l		n	a	b	c	•	e	f	g	j	–	h	#
a	b	c	f	g	e	•	h	i	j	n	l	m	#
i	b	c	–	m	n	•	e	f	g	–	i	j	#
l	m	n	a	b	c	•	e	f	g	h	i	j	#
h	i	j	e	f	g	•	a	b	c	l	m	n	#

1	2	3	4	5	6	7	8	9	10	11	12	13	14
l	m	n	a	b	c	•	e	f	g	h	i	j	#
l	m	n	a	b	c	•	e	f	g	h	i	j	#
l	m	a	b	n	c	•	e	f	g	h	i	j	#
j	i	h		f	c	•	e	b	–	n	m	l	#
l	m	n		b	c	•	e	f	–	h	i	j	#
i	f	j	e	•	c	m	l	b	#				

1	2	3	4	5	6	7	8	9	10
b	–	d	•	g	–	i	#		
a	b	c	•	e	–	g	#		
a	–	c	•	e	–	g	#		
b	c	d	•	–	h	–	#		
b	c	d	•	g	h	i	#		
b	c	d	•	g	h	i	#		
b	c	d	•	g	–	i	#		
b	c	d	•	g	h	–	#		
b	c	d	•	g	h	i	#		
b	l	m	c	•	e	f	i	j	#
l	b	c	•	e	i	j	#		
l	m	b	c	•	–	f	i	j	#

1	2	3	4	5	6	7	8	9	10
a	b	c	d	•	f	g	h	i	#
b	c	d	•		g	h	i	#	
a	b	c	•	e	f	g	#		

1	2	3	4	5	6	7	8	9	10
i	f	j	e	•	c	m	l	b	#

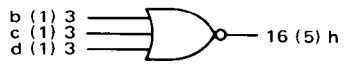
MRTL LOGIC DIAGRAMS

MOTOROLA

The numbers in parenthesis indicate loading factors for medium-power MRTL devices. The numbers at the end of the terminals indicate the normalized loading factors used for compatability with the low-power mW MRTL devices when mixing the two power levels in a system. Pin numbers vary with the package types. The alpha pin designations shown on the logic diagrams, used in conjunction with the Package Information Table (following the logic diagrams), make it possible to ascertain pin numbers for a specific device and package.

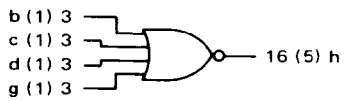
GATES

MC903
3-Input NOR Gate



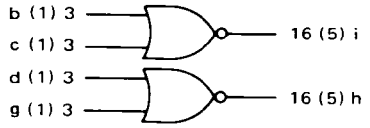
$h = \overline{b + c + d}$

MC907
4-Input NOR Gate



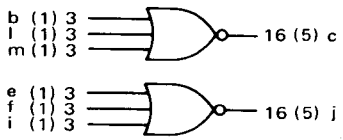
$h = \overline{b + c + d + g}$

MC914
Dual 2-Input NOR Gate



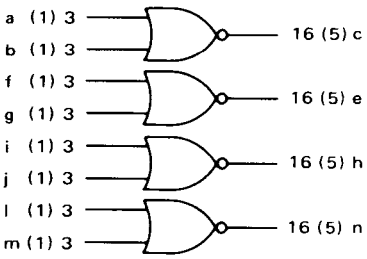
$i = \overline{b + c}$

MC815, MC915
Dual 3-Input NOR Gate



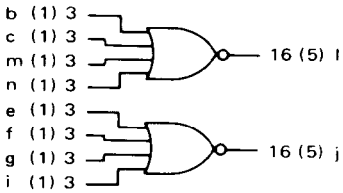
$c = \overline{b + l + m}$

A, MC824,A, MC924
Quad 2-Input NOR Gate



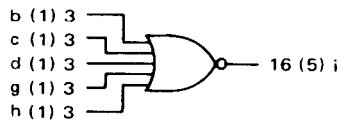
$c = \overline{a + b}$

MC825, MC925
Dual 4-Input NOR Gate



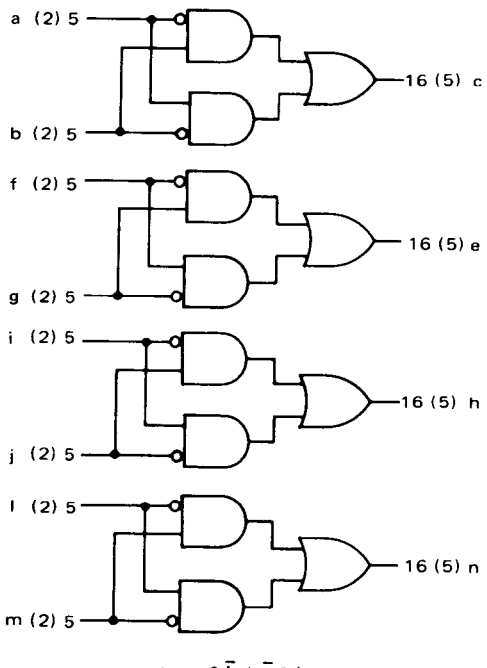
$l = \overline{b + c + m + n}$

MC929
5-Input NOR Gate



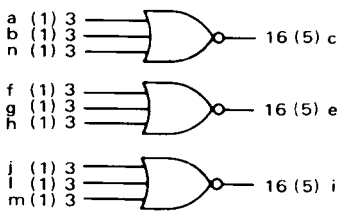
$i = \overline{b + c + d + g + h}$

MC871, MC971
Quad Exclusive OR Gate



$c = a \bullet \bar{b} + \bar{a} \bullet b$

MC892, MC992
Triple 3-Input NOR Gate

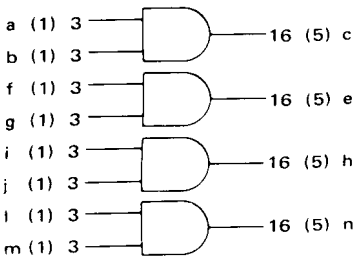


$c = \overline{a + b + d}$

(continued)

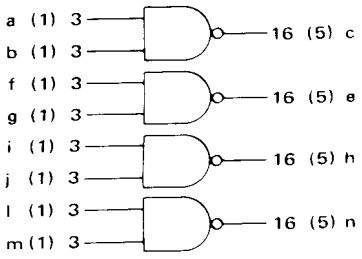
GATES (continued)

MC9813
Quad 2-Input AND Gate



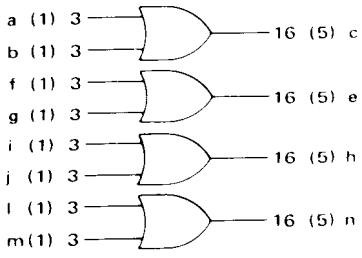
$c = a \bullet b$

MC9814
Quad 2-Input NAND Gate



$c = \overline{a \bullet b}$

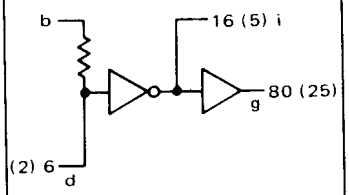
MC9815
Quad 2-Input OR Gate



$c = a + b$

BUFFERS

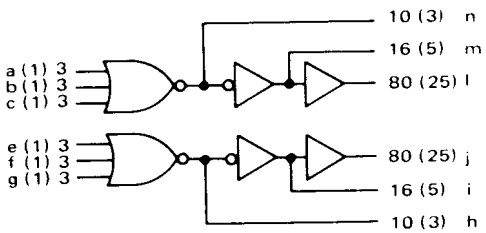
MC900
Buffer



$i = \overline{d}$

$g = \overline{d}$

MC888/MC988
Dual 3-Input Buffer

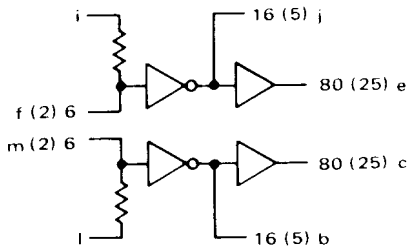


$n = \overline{a + b + c}$

$m = a + b + c$

$l = a + b + c$

MC899/MC999
Dual Buffer

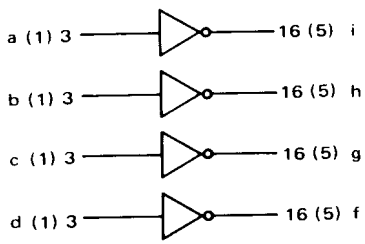


$j = \overline{f}$

$e = \overline{f}$

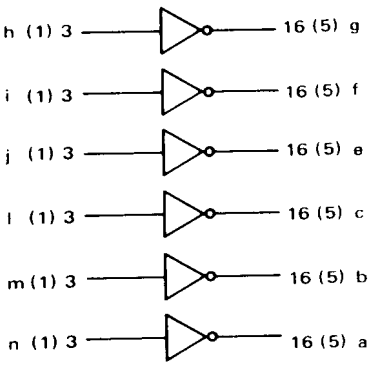
INVERTERS

MC927
Quad Inverter



$i = \overline{a}$

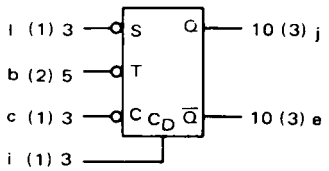
MC889, MC989
Hex Inverter



$a = \overline{n}$

FLIP-FLOPS

MC816, MC916
J-K Flip-Flop

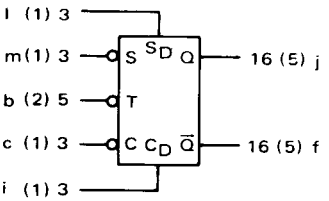


CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

MC826, MC926
J-K Flip-Flop



CLOCKED INPUT OPERATION①

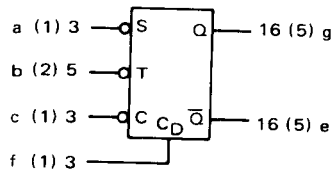
t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

DIRECT INPUT OPERATION④

S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	1	1

1. Direct inputs (C_D and S_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.

MC974
J-K Flip-Flop



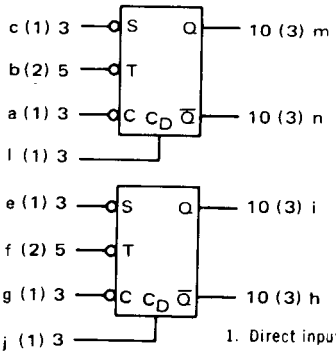
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NOTE:
Clock pulse fall time must be within the range of 10 ns to 100 ns on all J-K Flip-Flops except MC926, MC826F, and MC826G which have a range of 10 ns to 200 ns.

MC890, MC990
Dual J-K Flip-Flop

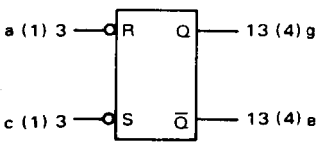


CLOCKED INPUT OPERATION①
(each Flip-Flop)

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

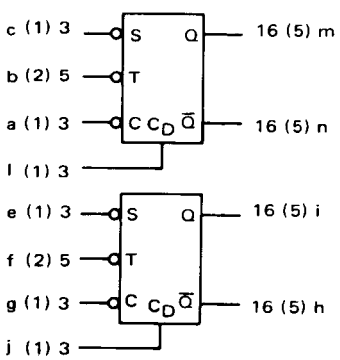
1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

MC902
R-S Flip-Flop



R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	0

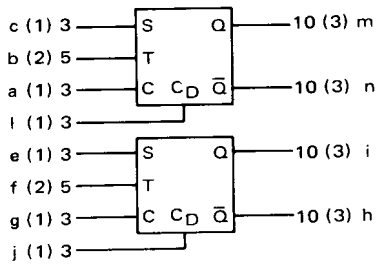
MC891, MC991
Dual J-K Flip-Flop



(continued)

FLIP-FLOPS (continued)

MC9802
Dual J-K Flip-Flop



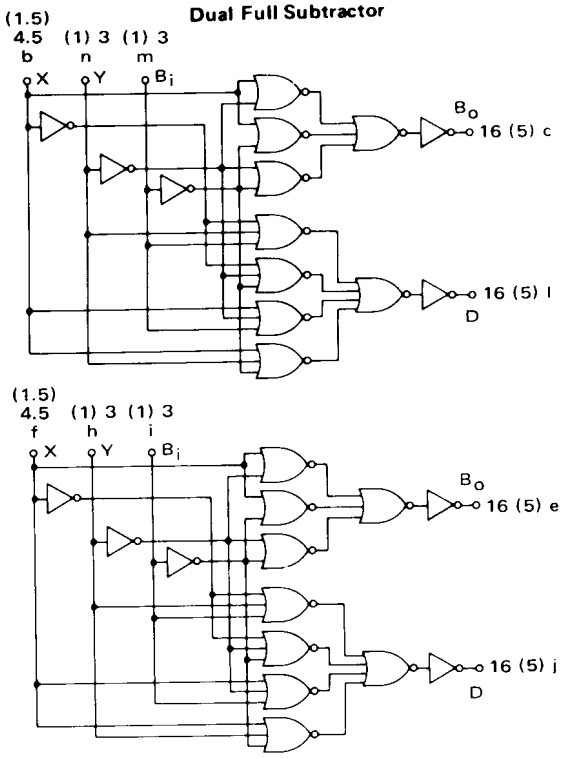
CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Preclear input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be <100 ns.

FULL SUBTRACTOR

MC897, MC997
Dual Full Subtractor



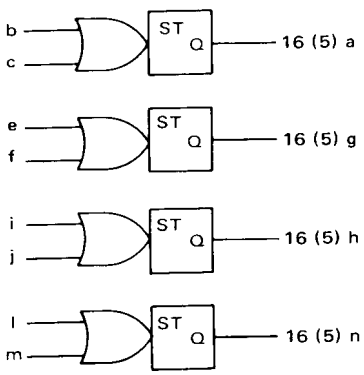
TRUTH TABLE

Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D = YXB_i + \bar{Y}X\bar{B}_i + Y\bar{X}\bar{B}_i + \bar{Y}\bar{X}B_i$
$B_o = \bar{Y}\bar{X}B_i + \bar{Y}X\bar{B}_i + Y\bar{X}B_i + YXB_i$

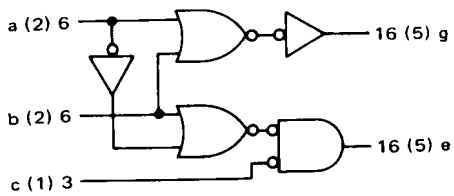
SCHMITT TRIGGER

MC9809
Quad Schmitt Trigger



COUNTER ADAPTER

MC901
Counter Adapter

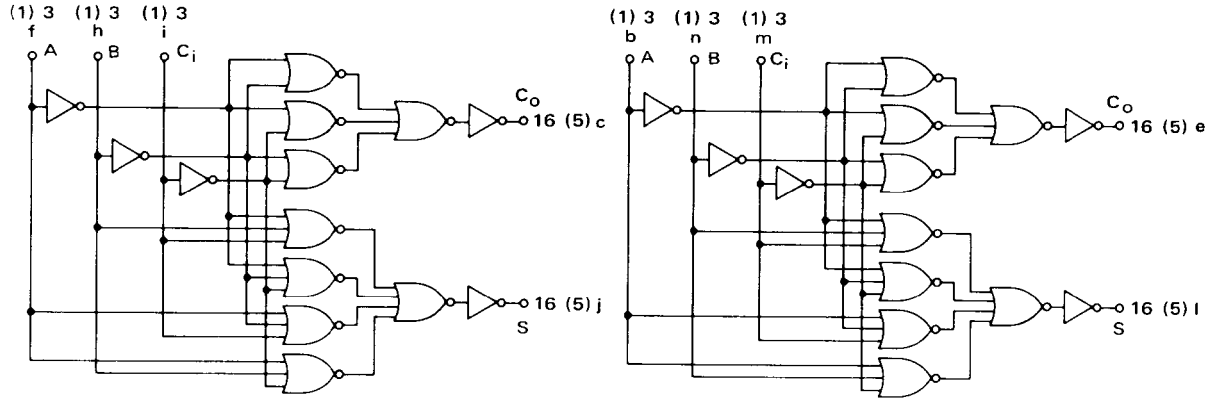


$g = a + b$
$e = (\bar{a} + b)\,\bar{c}$

MRTL LOGIC DIAGRAMS

FULL ADDERS

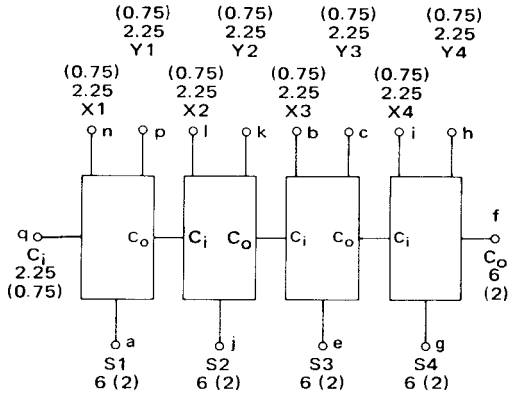
MC896, MC996
Dual Full Adder



$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$

$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}BC_i + \bar{A}\bar{B}C_i$

MC9804
4-Bit Parallel Full Adder

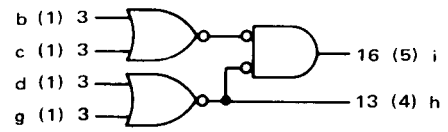


TRUTH TABLE

Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

HALF ADDERS

MC904
Half Adder



$i = (b + c)\ (d + g)$

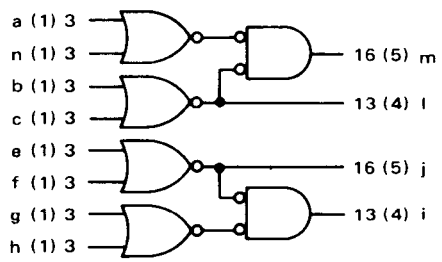
$h = \overline{d + g}$

IF: $d = \bar{b}$, & $g = \bar{c}$

THEN: $h = b \cdot c$

$i = b \cdot \bar{c} + \bar{b} \cdot c$

MC875, MC975
Dual Half Adder

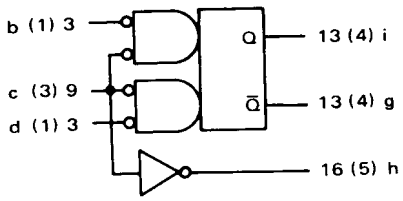


IF: $b = \bar{a}$, & $c = \bar{n}$

THEN: $l = a \cdot n$, & $m = a \cdot \bar{n} + \bar{a} \cdot n$

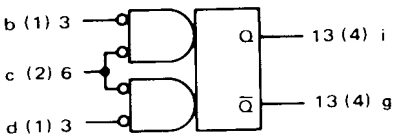
SHIFT REGISTERS

MC905
Half-Shift Register



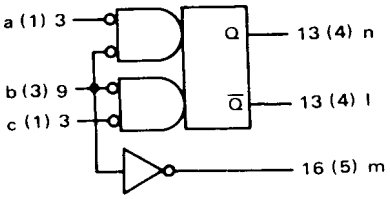
$i = \overline{g}\,(b + c)$
$g = \overline{i}\,(c + d)$

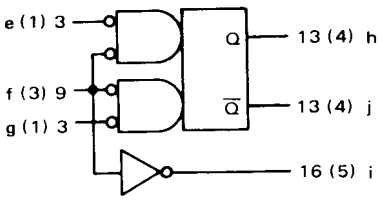
MC906
Half-Shift Register
(without inverter)



$i = \overline{g}\,(b + c)$
$g = \overline{i}\,(c + d)$

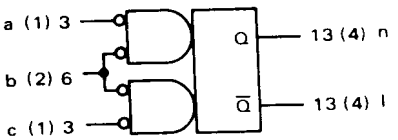
MC883, MC983
Dual Half-Shift Register

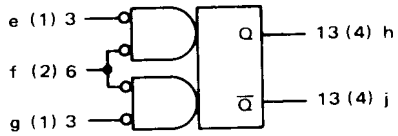




$n = \overline{l}\,(a + b)$
$l = \overline{n}\,(c + b)$

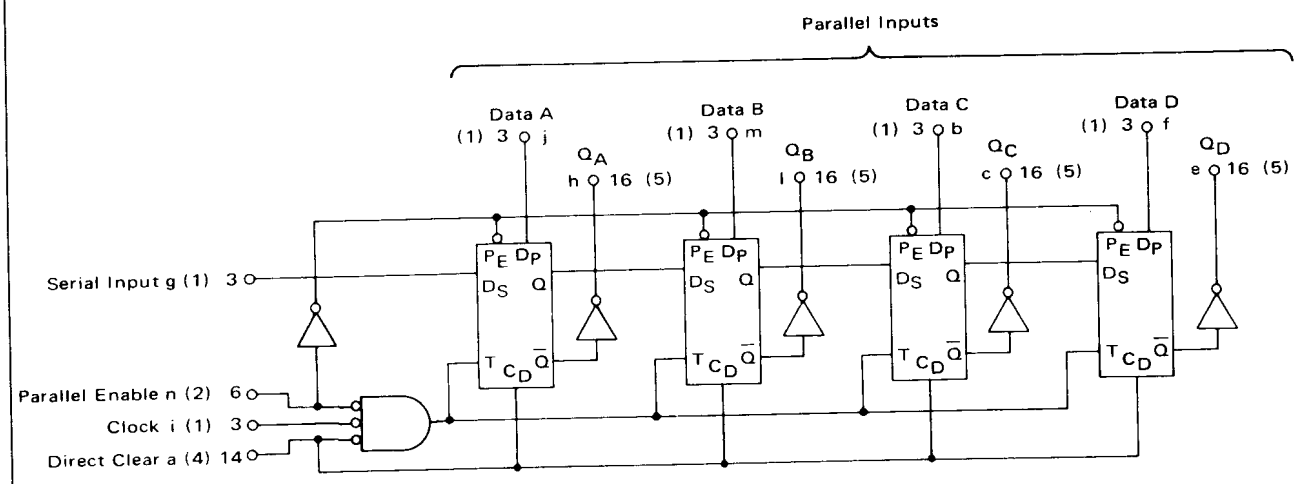
MC884, MC984
Dual Half-Shift Register
(without inverter)





$n = \overline{l}\,(a + b)$
$l = \overline{n}\,(c + b)$

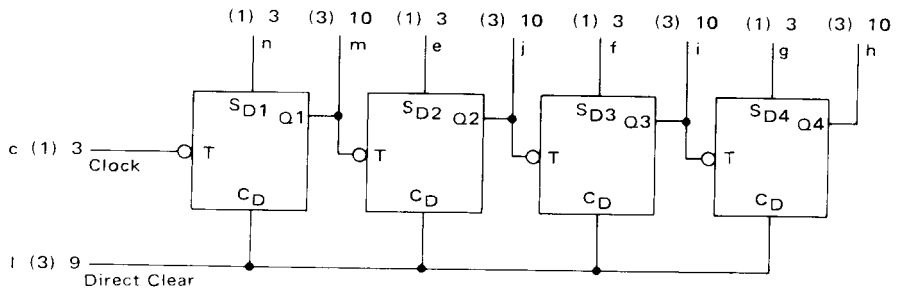
MC894
Serial-Parallel Shift Register



MRTL LOGIC DIAGRAMS

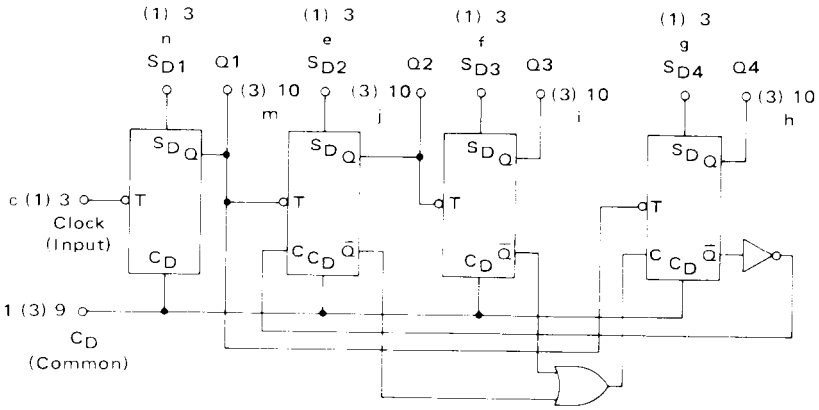
COUNTERS

MC877
Binary Up Counter



DECODING LOGIC	
0	$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$
1	$A\,\overline{B}\,\overline{C}\,\overline{D}$
2	$\overline{A}\,B\,\overline{C}\,\overline{D}$
3	$A\,B\,\overline{C}\,\overline{D}$
4	$\overline{A}\,\overline{B}\,C\,\overline{D}$
5	$A\,\overline{B}\,C\,\overline{D}$
6	$\overline{A}\,B\,C\,\overline{D}$
7	$A\,B\,C\,\overline{D}$
8	$\overline{A}\,\overline{B}\,\overline{C}\,D$
9	$A\,\overline{B}\,\overline{C}\,D$
10	$\overline{A}\,B\,\overline{C}\,D$
11	$A\,B\,\overline{C}\,D$
12	$\overline{A}\,\overline{B}\,C\,D$
13	$A\,\overline{B}\,C\,D$
14	$\overline{A}\,B\,C\,D$
15	$A\,B\,C\,D$

MC880
Decade Up Counter

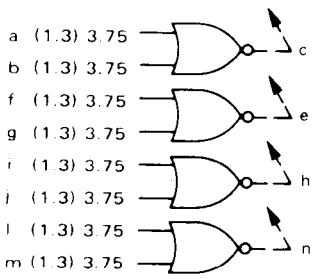


DECODING LOGIC

0	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$
1	A	$\overline{B}$	$\overline{C}$	$\overline{D}$
2	$\overline{A}$	B	$\overline{C}$	$\overline{D}$
3	A	B	$\overline{C}$	$\overline{D}$
4	$\overline{A}$	$\overline{B}$	C	$\overline{D}$
5	A	$\overline{B}$	C	$\overline{D}$
6	$\overline{A}$	B	C	$\overline{D}$
7	A	B	C	$\overline{D}$
8	$\overline{A}$	$\overline{B}$	$\overline{C}$	D
9	A	$\overline{B}$	$\overline{C}$	D

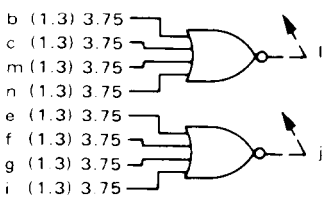
EXPANDERS

MC885, MC985
Quad 2-Input Expander



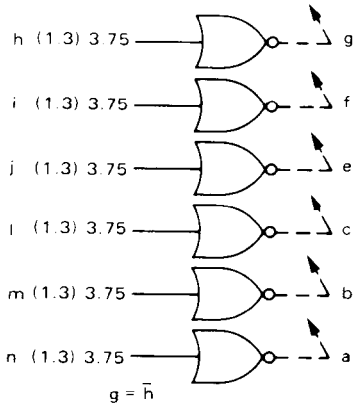
$c = \overline{a + b}$

MC886, MC986
Dual 4-Input Expander



$l = \overline{b + c + m + n}$

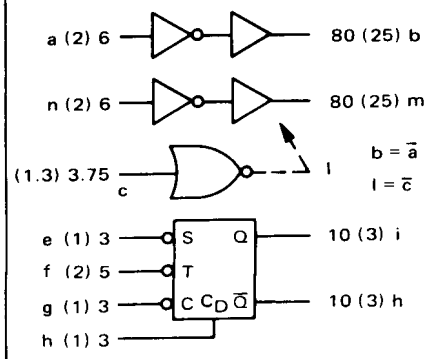
MC9819
Hex Expander



$g = \overline{h}$

MULTIFUNCTION DEVICES

MC879
(1 J-K Flip-Flop, 1 Expander, 2 Buffers)

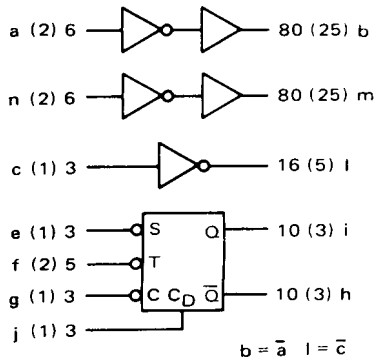


CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

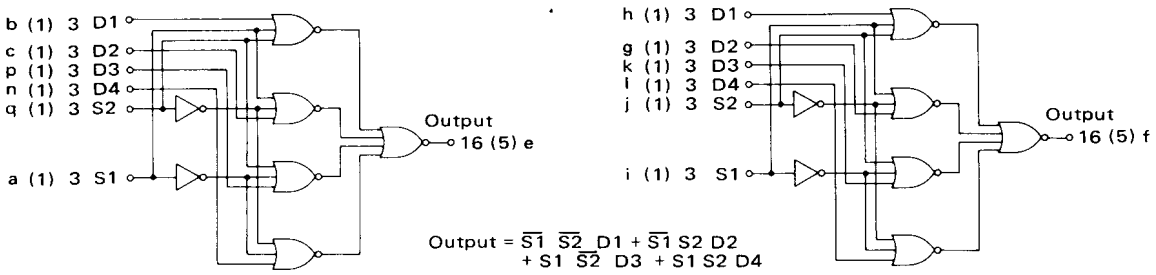
1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

MC887
(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)



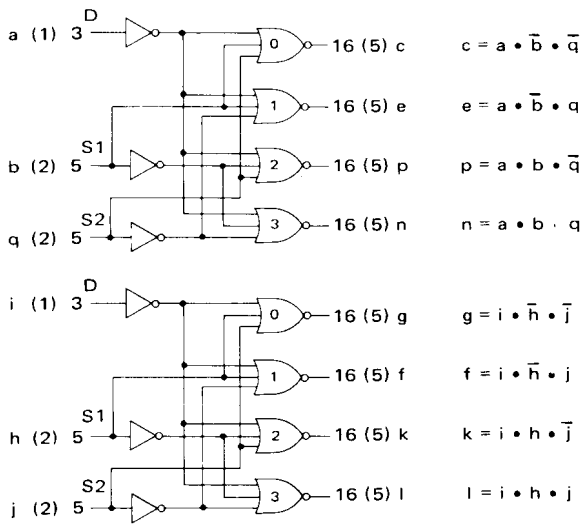
DATA ROUTING FUNCTIONS

MC9801
Dual 4-Channel Data Selector



Output = $\bar{S1}\ \bar{S2}$ D1 + $\bar{S1}$ S2 D2 + S1 $\bar{S2}$ D3 + S1 S2 D4

MC9807
Dual 4-Channel Date Distributor



TRUTH TABLE

Input Select		Data Line
S1	S2	Selected
0	0	D1
0	1	D2
1	0	D3
1	1	D4

TRUTH TABLE

	INPUTS			OUTPUTS			
	D	S1	S2	0	1	2	3
Pin Numbers	a i	b h	q j	c g	e f	p k	n l
Level	0	*	*	0	0	0	0
	1	0	0	1	0	0	0
	1	0	1	0	1	0	0
	1	1	0	0	0	1	0
	1	1	1	0	0	0	1

*Either state.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Input Voltage	–	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)		+6	Vdc
Operating Temperature Range MC900 Series MC800P Series	T_A	 −55 to +125 0 to +75	°C
Storage Temperature Range Metal Can, Flat Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

INSTRUCTIONS FOR USE OF PACKAGE INFORMATION TABLE

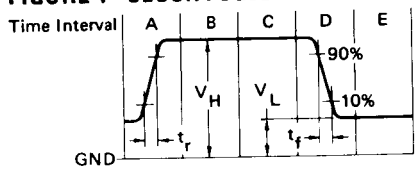
MC900 and MC800 Series Medium-Power MRTL devices are available in the packages pictured in the following table as indicated on the line following each device type number. Plastic and dual-in-line ceramic packaged devices are available in the MC800 Series only.

Pin numbers for any of the following devices and packages may be determined by:

1. Find the device among the logic diagrams appearing on the preceding pages (grouped by function). Note the alpha pin designations for the device.
2. Find the device type number in the left hand columns of the "Package Information Table".
3. The letters in the columns following the type number and below the drawing of the desired package indicate the correct pin numbers for the specific package by their numbered positions beneath the package drawing. (These letters are the same as indicated on the logic diagram for the device.)
4. Notes: Blanks in an area following the type number and directly beneath a package indicate the device is not available in that package.
   A dash indicates this pin or lead is not connected nor otherwise utilized for this device and package.
   * indicates this pin number is the ground connection for this device and package.
   # indicates this pin number is the V_{CC} connection for this device and package.

TYPICAL OPERATING CHARACTERISTICS FOR mW MRTL J-K FLIP-FLOPS

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

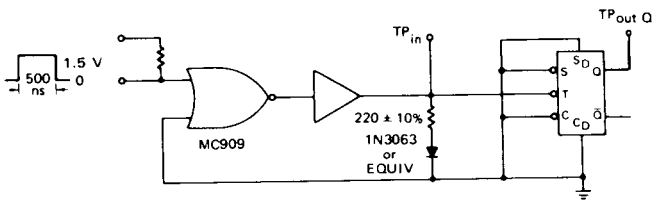
MC800 Series

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

MC900 Series

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz
Duty Cycle = 25% to 75%
t_r & t_f < 10 ns

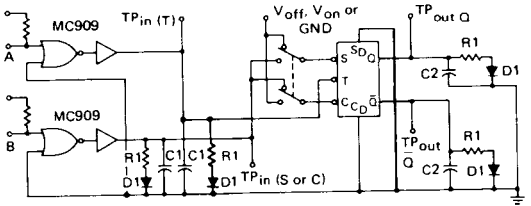
NOTE:
Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

SWITCHING TIMES

Test	Figure No. 3	Maximum (ns)
t_{T-Q-}	3B	150
$t_{T-\bar{Q}-}$	3B	150
t_{T-Q+}	3B	100
$t_{T-\bar{Q}+}$	3B	100
t_{S+T-}	3C	50
t_{S-T-}	3C	30
t_{C+T-}	3C	50
t_{C-T-}	3C	30
t_{T-S+}	3C	0
t_{T-S-}	3C	+5
t_{T-C+}	3C	0
t_{T-C-}	3C	+5
$t_{C_D+\bar{Q}-}$	4	140
t_{C_D+Q+}	4	70
$t_{S_D+\bar{Q}+}$	4	70
t_{S_D+Q-}	4	140

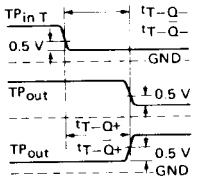
SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

FIGURE 3A - SET-UP, RELEASE AND SWITCHING TIMES TEST CIRCUIT



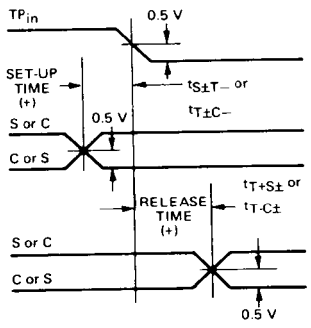
C1 = 20 pF Including Jig and Probe
C2 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or Equivalent

FIGURE 3B - SWITCHING TIME WAVEFORMS



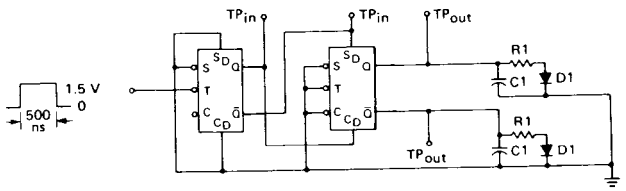
NOTE: Whichever input pin (S or C) is tied to MC909 Buffer on input pin B is at virtual ground when the input is tied to V_{BOT}.

FIGURE 3C - SET-UP AND RELEASE TIME



FOR DEFINITIONS OF SET-UP AND RELEASE TIMES, SEE GENERAL INFORMATION SECTION.

FIGURE 4 - DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY TIME



f = 1.0 MHz
t_r & t_f < 10 ns

C1 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or EQUIVALENT