MCCF1741
MCCF1741C

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC FLIP-CHIP OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

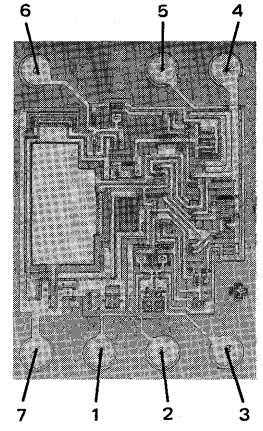
The MCCF1741 and MCCF1741C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 95-5 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

FLIP-CHIP

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MCCF1741C	MCCF1741	
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal	V_{ID}	±30		Volts
Common Mode Input Swing (Note 1)	V_{IC}	+15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Junction Temperature Range	T_J	-65 to +150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

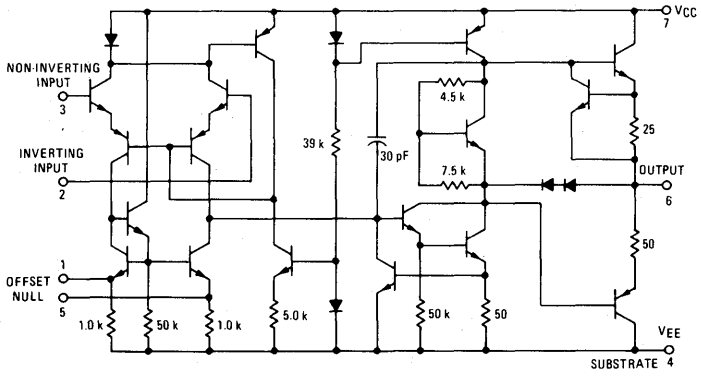
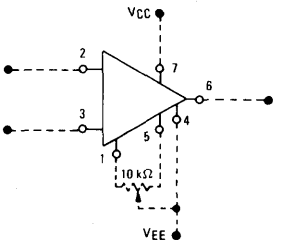


FIGURE 2 – OFFSET ADJUST CIRCUIT

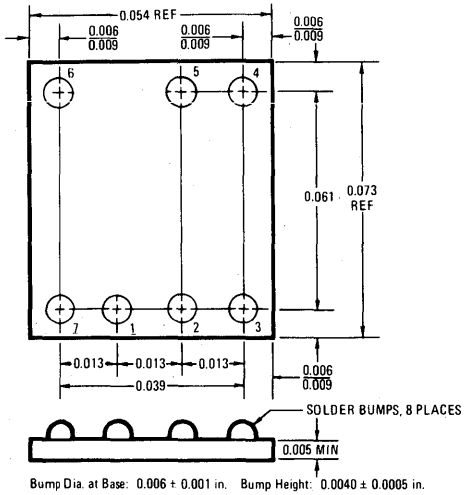


ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MCCF1741 Min	MCCF1741 Typ	MCCF1741 Max	MCCF1741C Min	MCCF1741C Typ	MCCF1741C Max	Unit
Open Loop Voltage Gain (R_L = 2.0 kΩ) (V_O = ±10 V)	A_{vol}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_{in}	–	1.0	–	–	1.0	–	Meg Ω
Output Voltage Swing (R_L = 10 kΩ)	V_O	±12	±14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{IC}	–	±13	–	–	±13	–	V_{peak}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	–	90	–	–	90	–	dB
Input Bias Current	I_{IB}	–	0.2	0.5	–	0.2	0.5	μA
Input Offset Current	$\|I_{IO}\|$	–	0.03	0.2	–	0.03	0.2	μA
Input Offset Voltage (R_S = ≦ 10 kΩ)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mV
Step Response Gain = 100	t_{THL}	–	29	–	–	29	–	μs
	t_d	–	8.5	–	–	8.5	–	μs
	dV_O/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 10	t_{THL}	–	3.0	–	–	3.0	–	μs
	t_d	–	1.0	–	–	1.0	–	μs
	dV_O/dt ①	–	1.0	–	–	1.0	–	V/μs
Gain = 1	t_{THL}	–	0.6	–	–	0.6	–	μs
	t_d	–	0.38	–	–	0.38	–	μs
	dV_O/dt ①	–	0.8	–	–	0.8	–	V/μs
Power Supply Current	I_{DCC}	–	1.67	2.83	–	1.67	2.83	mA
	I_{DEE}	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation (Power Supply = ± 15 V, V_O = 0)	P_D	–	50	85	–	50	85	mW
Positive Supply Sensitivity (V_{EE} constant)	S^+	–	30	150	–	30	150	μV/V
Negative Supply Sensitivity (V_{CC} constant)	S^-	–	30	150	–	30	150	μV/V

① dV_O/dt = Slew Rate See current MC1741/1741C data sheet for additional information.

MCCF1741/MCCF1741C BONDING DIAGRAM AND DEVICE DIMENSIONS



Bump Dia. at Base: 0.006 ± 0.001 in. Bump Height: 0.0040 ± 0.0005 in.
Each bump centerline to be located within 0.001 in. of its true position with respect to any other bump centerline.

PACKAGING AND HANDLING

The popular 1741 type operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.