MC Devices®

MCD2926

18MHz-650MHz Dual Frequency Synthesizer

General Description

The MCD2926 is a high performance dual frequency synthesizer with high frequency prescaler for RF operation frequency from 18MHz to 650MHz. The MCD2926 contains two dual modulus prescalers, three programmable counters, one crystal oscillator, two phase detectors and two programmable charge pumps, one MCU serial interface. The on-chip prescalers and dividers consist of a completed phase-lock-loop (PLL), which is combined with on board VCO and LPF. Users can lock any targeted frequency by setting proper division with an external MCU. It has been proven that MCD2926 can work stably within the range of -40 to +85 degrees.

Typical Applications

- FRS, PCS, Cordless phones
- Portable wireless systems and other wireless
- communication systems

Features

- Operating Frequency: 18MHz~650MHz
- Operating Voltage Range: 2.2 ~ 5.5V (3.3V Typical)
- Operating Power Consumption:
  Single channel: 7.5mA @3.3V
  Dual channel: 14mA @3.3V
- Power down Consumption: < 1uA
- The reference crystal oscillator supports 4~25MHz crystal
- Dual modulus prescaler: 64/66
- No dead-zone PFD
- Digital Lock Detect Signal: when loop locked, LD outputs high level.
- Programmable charge pump current: 200uA, 400uA, or 800uA
- 0.35um CMOS process
- Package: TSSOP-16

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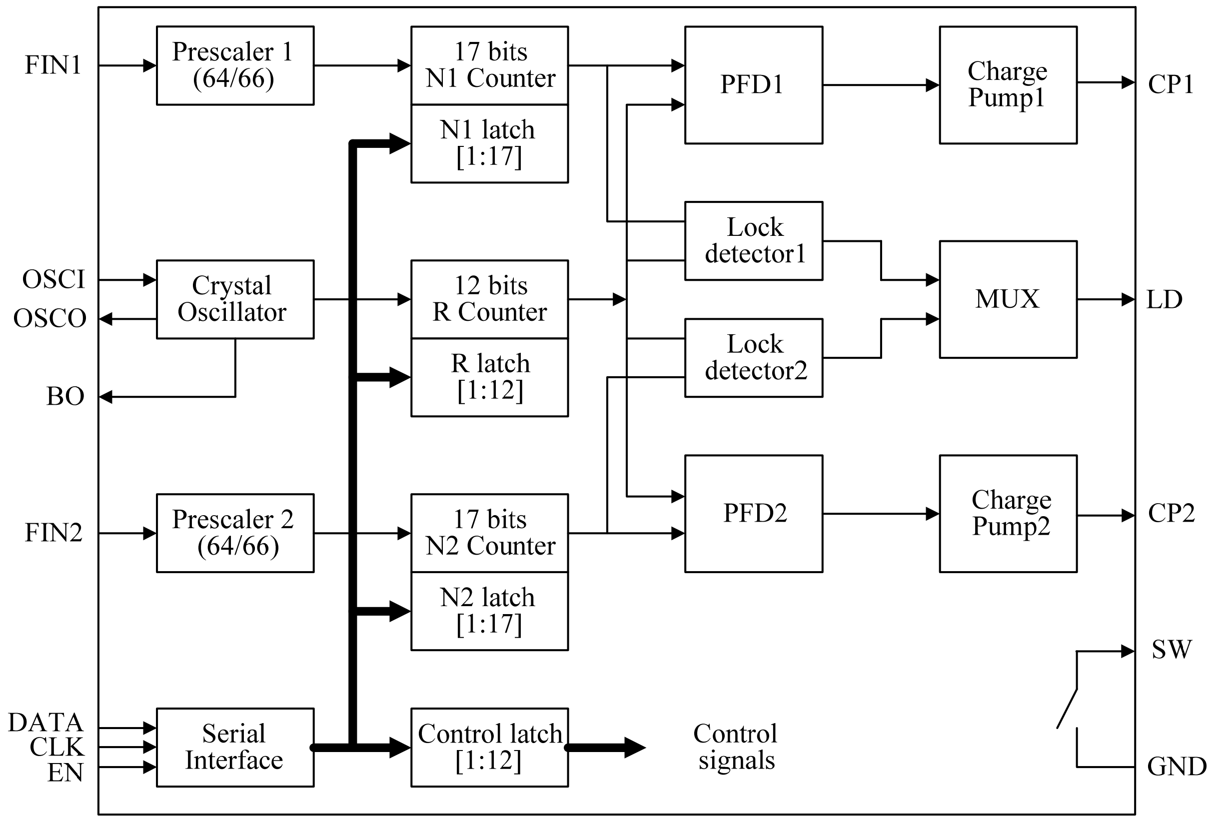
Version History

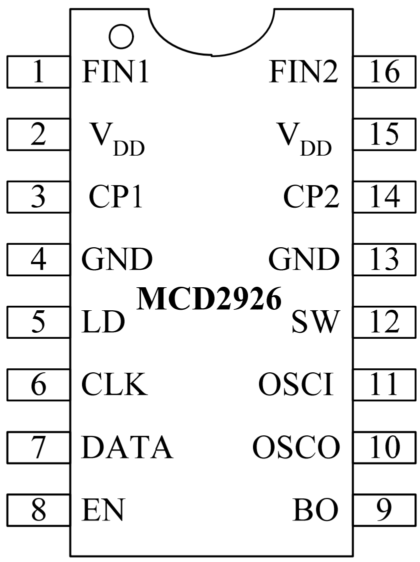
Version	Issued time	Notes
V1.0	Jun.18, 2006	First version created.
V1.1	Sep.6, 2006	Update the test parameter.
V1.2	Dec.1, 2008	Modify the format.
V2.0	Mar 05, 2009	Add packaging process and Soldering temperature profile
V2.5	April 26, 2010	Change the maximum voltage to 5.5V, remove 1600uA chargepump option.

516 Bld4, National Software Base, Kejizhong 2 Rd, Shenzhen Hi-Tech Park, Shenzhen, China Tel: (86-755)8618 5088 Fax: (86-755)8618 5000

Function Block Diagram



Pin Assignment and Description



Pin#	Pin Name	I/O	Description
1	FIN1	I	Prescaler1 input. RF signal from VCO.
2,15	V_{DD}	I	Power supply voltage input (2.2V-5.5V). Pin2 and Pin15 should be connected together externally. Bypass capacitors should be placed as close as possible to these pins and be connected directly to the ground plane.
3	CP1	O	Output terminal of channel 1 charge pump. Connected to the loop filter to drive the voltage control input of the VCO.
4,13	GND	-	Terminal of GND. Pin4 and Pin13 should be shorted externally.
5	LD	O	Lock detection output. It is a CMOS output.
6	CLK	I	Clock input of the serial interface. Data is clocked in on the rising edges of the clock, into the 19-bit shift register in the serial interface.
7	DATA	I	Serial data input. LSB is entered first and the last two bits are the control bits.
8	EN	I	Load enable input. Data stored in the shift register is loaded into one of the 4 internal latches (depending on the control bits) when EN is high.
9	BO	O	Buffered output of the crystal oscillator frequency. It is a CMOS output.
10	OSCO	O	Output terminal of the local oscillator. It is connected to the crystal if the reference frequency is generated by the local oscillator. When the reference clock is provided externally, OSCO should be connected to V_{DD} to power down the local oscillator for power saving.
11	OSCI	I	Input terminal of local oscillator. It is connected to the crystal when the reference frequency is generated by the local oscillator. It also can be driven by an external clock.
12	SW	I/O	Switch-over terminal for the time constant of loop filter. It is an open drain output.
14	CP2	O	Output terminal of channel 2 charge pump. Connected to the loop filter to drive the voltage control input of the VCO.
16	FIN2	I	Prescaler2 input. RF signal from the VCO.

Absolute Maximum Ratings (Note 1)

Parameters	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}			6.0	V
Storage Temperature Range	T_S	-55		150	℃
Lead Temp (solder 4 sec)	T_L			260	℃
ESD-Human Body Model	V_{ESD}		2000		V

Recommended Operating Conditions (Note 2)

Parameter	Symbol	Value			Unit
		Min	Typical	Max	
Power Supply Voltage	V_{DD}	2.2	3.3	5.5	V
Operating Temperature	T_A	-40	27	+85	℃

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur.
Note 2: "Recommended Operating Conditions" indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. Electrical Characteristics document specific minimum and/or maximum performance values at specified test conditions and are guaranteed.

Electrical Characteristics (VDD=3.3V, -40℃≤T_A≤+85℃； except as specified)

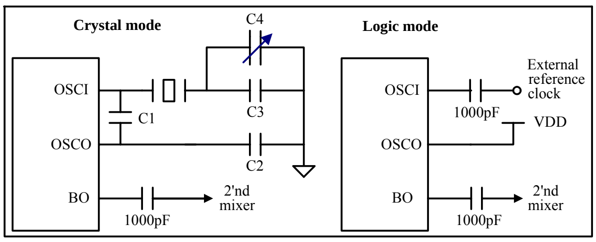
Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Operating current consumption	I_{DD}	FIN=500MHz, V_{DD}=3.3V	Single channel	7.1	7.5	8.2	mA
			Dual channel	13	14	15	
FIN operating frequency	FIN1	V_{FIN1} = V_{FIN2} = -10dBm		18		650	MHz
	FIN2			18		500	MHz
FIN input sensitivity	V_{FIN1}, V_{FIN2}	FIN1=FIN2=18MHz			-20		dBm
		FIN1=650MHz			-10		
		FIN2=500MHz			-10		
OSCI operating frequency	F_{OSC}			4	--	25	MHz
OSCI input voltage	V_{OSCI}			0	4	8	dBm
CLK, DATA, EN input high voltage	V_{IH}			V_{DD} -0.4		V_{DD}	V
CLK, DATA, EN input low voltage	V_{IL}			-0.4		0.4	V
Charge pump output current	I_{CP1}	CP1=0, CP2=1 V_{CP}=V_{DD}/2			±0.2		mA
	I_{CP2}	CP1=1, CP2=0 V_{CP}=V_{DD}/2			±0.4		
	I_{CP3}	CP1=1, CP2=1 V_{CP}=V_{DD}/2			±0.8		
Charge pump leakage	ICPL	Standby mode, V_{CP}=V_{DD}/2		-1	--	+1	uA

1. Function Description

The MCD2926 is a dual frequency synthesizer based on the PLL (phase-lock-loop) principle, it consists of a high-accuracy crystal oscillator, two phase/frequency detectors, two charge pumps, one programmable reference frequency divider and two programmable feedback frequency dividers. The dual synthesizer、two external VCOs and two passive loop filters consist of two completed separated PLL. The targeted frequencies can be phase and frequency locked through the PLL when an external MCU properly programme the divide ratio of the reference frequency divider and feedback frequency divider.

1.1 Reference Oscillator

The reference frequency for PLL is obtained by two methods. First method is to input an external clock to OSCIN pin with OSCO pin tied to V_{DD}. Second way is to apply an external crystal and few capacitors across the OSCI pin and OSCO pin. External capacitors C1, C2, C3 and C4 are required to set the proper crystal's load capacitance and oscillation frequency, local oscillation signal is buffered and output through the BO pin which can be applied to the 2^{nd} mixer input.



1.2 Reference Divider (R Counter)

The reference divider provides reference frequency for PFD, it includes a fixed 1/2 divider and a 12-bit programmable divider. The 12-bit divider can program the division ratio between 3 and 4095. Due to the fixed 1/2 divider, the total divide ratio for reference divider would range from 6 to 8190. See the programming description section for details.

1.3 Feedback Divider (N Counter)

The channel1 and channel2 N counters are clocked by the small signal FIN1 and FIN2, respectively. The input of FIN1 and FIN2 should be AC coupled signal through external capacitors. FIN1 and FIN2 are biased at $0.6V_{DD}$. An N counter consists of a 5-bit swallow counter with a divide ratio 0<A<31 and a 12-bit pulse counter with a divide ratio 3<B<4095. In conjunction with the 64/66 prescaler, the total divide ratio can range from 192 to 262142 on a feedback channel. For the proper operation of the prescaler, the pulse counter division ratio B should be always equal to or greater than the swallow counter division ratio A. See the programming description section for details.

1.4 Prescaler

The prescaler of MCD2926 consists of a pre-amplifier, a CML (current mode logic) 1/2 divider and a CMOS 32/33 dual modulus divider. The prescaler clocks the subsequent CMOS N counter.

1.5 Phase/Frequency Detector (PFD)

The channel1 and channel2 phase/frequency detectors (PFD) are driven by their respective N counters and R counter. PFD compares frequency and phase of two inputs from reference counter and N counter, outputs control logic to charge pump. The polarity of the pump-up or pump-down control is programmable according to VCO characteristics. The phase detector receives a feedback signal from charge pump in order to eliminate dead zone.

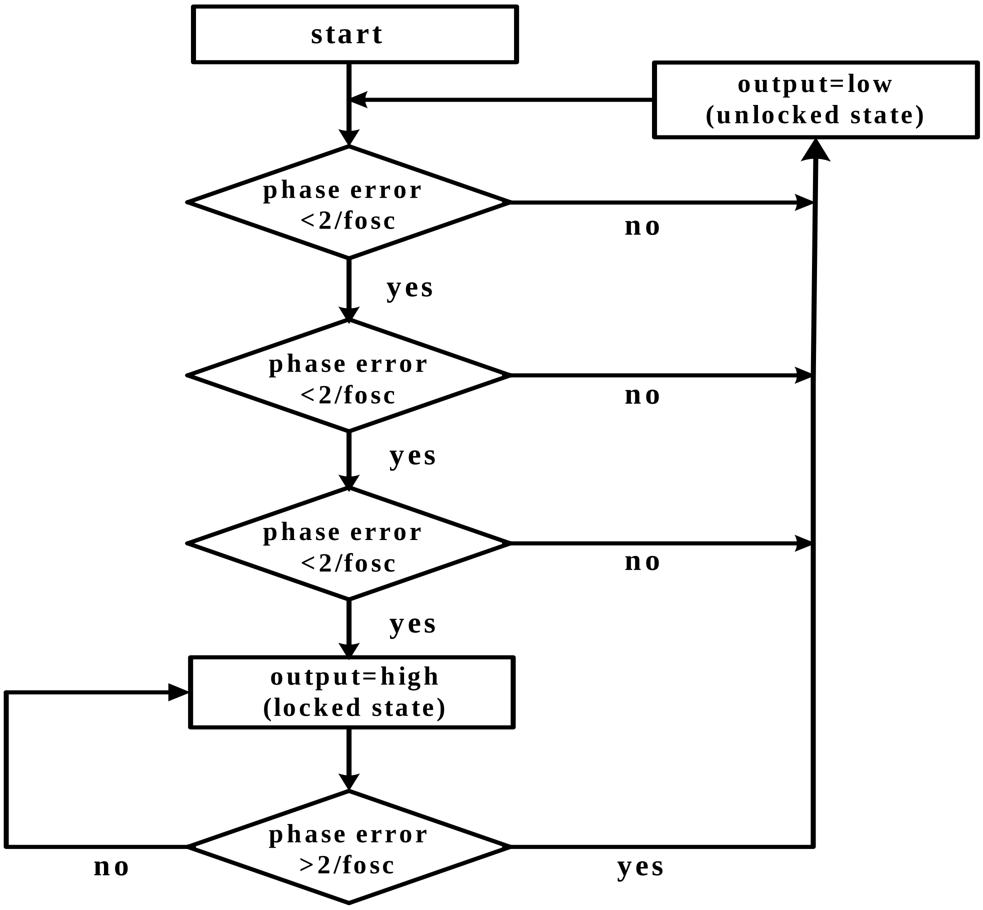
1.6 Charge Pump

The charge pump pumps up or pumps down current from an external loop filter is according to the polarity control of it's PFD outputs. The loop filter converts the charge into VCO's control voltage

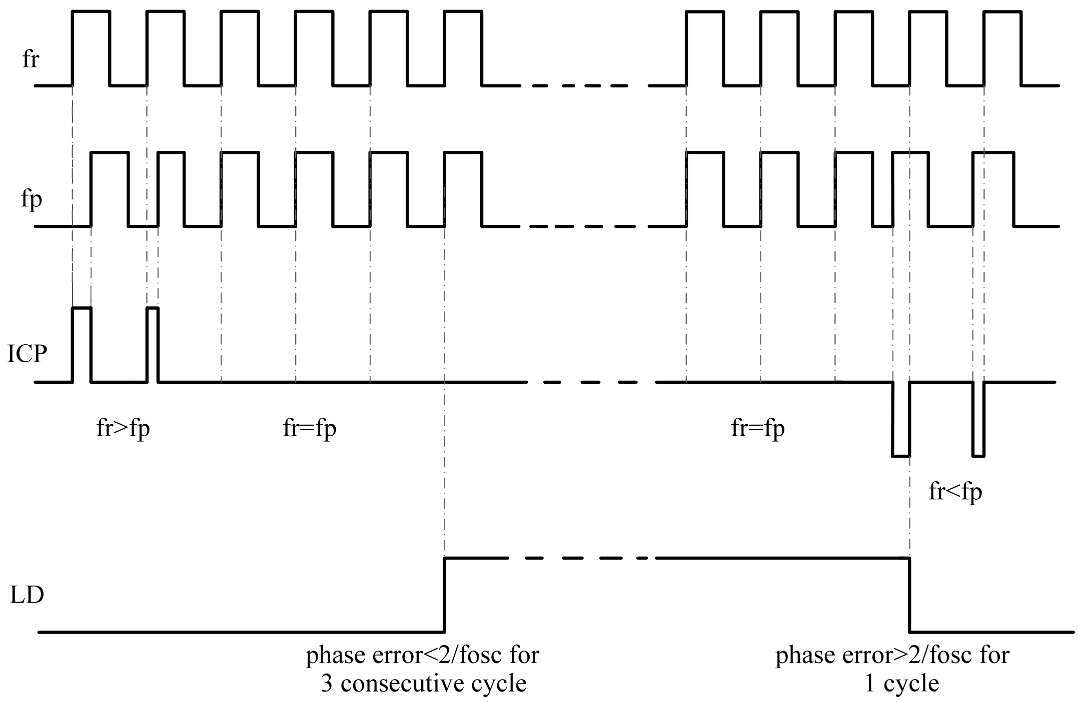
The charge pump steers the charge pump output CP1 or CP2 to VDD (pump-up) or GND (pump-down). Under the locked condition, CP1 or CP2 is primarily in a tri-state mode with small corrections. The charge pump current magnitude can be selected as 200uA, 400uA, or 800uA.

1.7 Lock Detector

Phase/frequency detector produces a logic level output at LD through an internal digital filter. When phase error between PFD inputs is less than 2/fosc for 3 consecutive comparison cycles, the LD output is high to indicate a phase-locked condition. Under phase-locked condition, if phase error between PFD inputs is greater than 2/fosc for one comparison cycle, the LD output drops to low to indicate a fail-locked condition. The lock detect output is always low when the PLL is power down. Fosc is crystal frequency.



Typical lock detect timing (positive VCO characteristics):

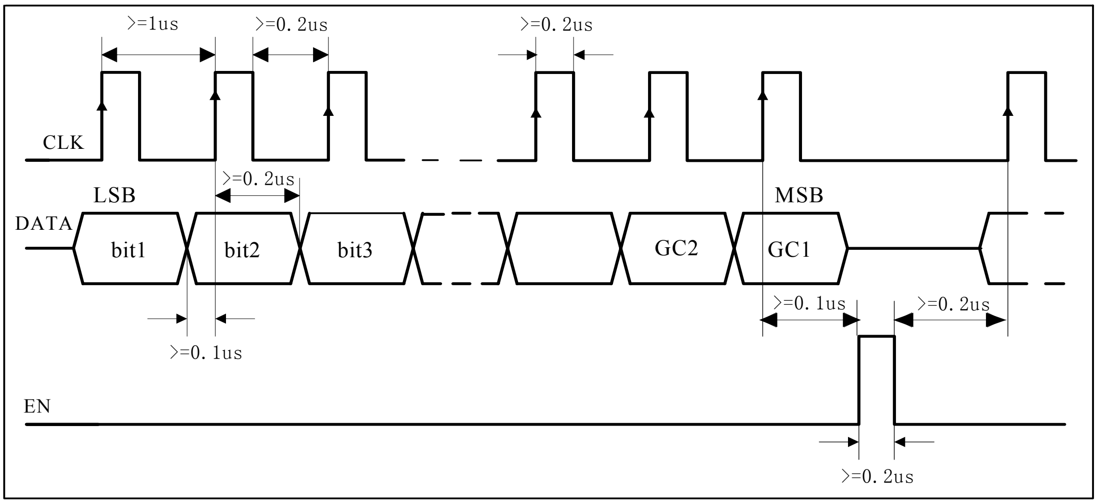


2. Programmable Description

2.1 Serial Interface

The 4 latches (N1, N2, R and control latches) of the MCD2926 are configured through the serial interface CLK, DATA and EN. The data is shifted into the shift register on the rising edges of the clock CLK with the LSB first. The last two bits (group code) are the address of the 4 latches. On the rising edge of EN, the data entered into the shift register is loaded to the appropriate latch according to the group code.

The timing of CLK、Data and EN is shown in following figure.



Notes: (1) LSB data shifted in first.

(2) When power down MCD2926, CLK, DATA, EN should be pulled low.

(3) When power up, Control latch should be configured first, then R counter, N1 and N2 counters usually are configured at last.

2.2 Latch and Group Code

There are four latches in MCD2926:

(1) Control Latch

(2) Channel1 N Latch

(3) Channel2 N Latch

(4) OSC R Latch

The last two bits of each configuration word indicate the address where data should be loaded.

GROUP CODE		LOCATION
GC1 (MSB)	GC2 (MSB-1)	
0	0	Control Latch
0	1	N1 Latch
1	0	N2 Latch
1	1	R Latch

2.3 Programming Control Latch

LSB Configuration word MSB

T	CP	CP11	CP12	SB1	CP21	CP22	SB2	SBR	LD1	LD2	SW	GC2=0	GC1=0

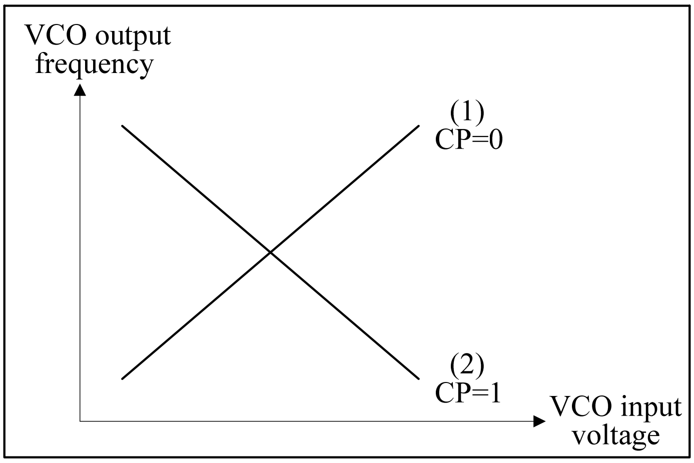
Bit description

Bit No.	Name	Description
Bit1 (LSB)	T	T=1, test mode; T= 0, normal mode
Bit2	CP	Charge pump output polarity
Bit3	CP11	Channel1 charge pump current
Bit4	CP12	
Bit5	SB1	Channel1 standby
Bit6	CP21	Channel2 charge pump current
Bit7	CP22	
Bit8	SB2	Channel2 standby
Bit9	SBR	Reference frequency divider standby
Bit10	LD1	Lock detector control
Bit11	LD2	
Bit12	SW	Filter switch
Bit13	GC2 (0)	Group code
Bit14 (MSB)	GC1 (0)	

2.3.1 Charge Pump Output Polarity (CP)

Depending on the VCO characteristics, CP should be set according to following characteristics:

If VCO characteristics are positive as line (1), CP should be set low; If VCO characteristics are negative as line (2), CP should be set high.



2.3.2 Charge Pump Output Current (CP11, CP12, CP21, CP22)

The charge pump output current is programmable by the control bits CP11, CP12, CP21 andCP22. CP11 and CP12 control the charge pump current of the channel 1, while CP21 and CP22 control the charge pump current of the channel 2.

Control bit		Charge Pump Output Current
CP11 (CP21)	CP12 (CP22)	
0	1	±200uA
1	0	±400uA
1	1	±800uA

2.3.3 Test Mode and Lock Detector Output (T, LD1, LD2)

T=0, normal operation mode, LD output is controlled by the bits SB1, SB2, LD1 and LD2.

T=1, test mode, LD is for test.

T	SB1	SB2	LD1	LD2	LD output
0	0	0	0	0	Low
			0	1	Channel 2 lock detect
			1	0	Channel 1 lock detect
			1	1	Channel 1 AND Channel2 lock detect
		1	0	0	Low
			0	1	High
			1	0	Channel 1 lock detect

			1	1	Channel 1 lock detect
	1	0	0	0	Low
			0	1	Channel 2 lock detect
			1	0	High
			1	1	Channel 2 lock detect
		1	0	0	Low
			0	1	High
			1	0	High
			1	1	High

2.3.4 Programmable Standby Mode (SB1, SB2, SBR)

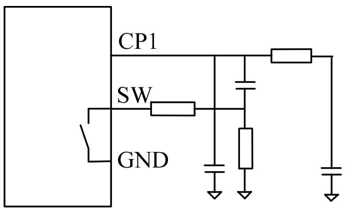
Standby mode is controlled by three control bits SB1, SB2 and SBR. SB1、SB2 control the standby mode of channel1 and channel2. The SBR control the ON/OFF state of reference divider.

Control bits			Mode state			
SB1	SB2	SBR	Channel1 divider	Channel2 divider	Reference divider	Mode status
0	0	0	ON	ON	ON	2 channels lock mode
0	1	0	ON	OFF	ON	Channel1 lock mode
1	0	0	OFF	ON	ON	Channel2 lock mode
1	1	0	OFF	OFF	ON	2 channels standby, Reference divider ON
1	1	1	OFF	OFF	OFF	Chip standby mode

2.3.5 Filter Switch Control (SW)

The output type of SW pin is an open drain output. It is used for switching the time constant of the loop filter.

SW	Operation mode
0	Normal lock mode
1	High lock mode



2.4 Programmable Reference Counter

The reference divider provides reference frequency for PLL. It includes a fixed 1/2 divider and a 12-bit programmable divider. The 12-bit divider can program the division ratio between 3 and 4095. Due to the fixed 1/2 divider, the total divide ratio for reference divider would range from 6 to 8190.

LSB Configuration word MSB

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	GC2=1	GC1=1

Divide ratio of the programmable 12bit counter:

Division ratio (R)	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

$R = R1x2^0 + R2x2^1 + \ldots + R12x2^{11}$ $(R \geq 3)$

The total division ratio range: 6 to 8190

2.5 Programmable Channel 1 and Channel 2 N Counters

These programmable dividers are composed of a 5-bit swallow counter and a 12-bit pulse counter, in conjunction with the 64/66 prescaler to provide divide ratio range from 192 to 262142.

2.5.1 Channel1 configuration word

LSB MSB

N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	GC2=1	GC1=0

|----*swallow counter*----|-------------------------------*pulse counter*------------------------|--*group code*-|

2.5.2 Channel2 configuration word

LSB MSB

N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	GC2=0	GC1=1

|------*swallow counter*------|------------------------------*pulse counter*-----------------------------------| --*group code*---|

2.5.3 Swallow counter division ratio (A)

Division ratio (A)	N5	N4	N3	N2	N1
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

$A = N1x2^0 + N2x2^1 + \ldots + N5x2^4$

Division ratio range: 0 to 31

2.5.4 Pulse counter divide ratio (B)

Division ratio (B)	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

$B = N6x2^0 + N7x2^1 + \ldots + N17x2^{11}$

Division ratio range: 3 to 4095 $(B \geq A)$

2.5.5 Channel1 and Channel2 programmable N counter total divide ratio

N = 2x(32xB + A)   (B≥A)

Division ratio range: 192 to 262142

3. Configuration Examples

3.1 Example A: Control latch configuration

- Condition: normal mode, CP set as low, SW set as normal lock mode, channel1 is active with 400uA charge pump current, channel2 is disable with 800uA charge pump current, LD1 and LD2 output channel1 lock detect.
- Configuration word   "00100111011000"

LSB (first in)   MSB

0	0	1	0	0	1	1	1	0	1	1	0	0	0

3.2 Example B: To get a 12.5KHz reference frequency from a 21.25MHz crystal

- Total division ratio   2R = 21.25MHz÷12.5KHz = 1700
- Programmable division ratio   R = 1700÷2 = 850
- Binary format (12bit)   R=001101010010
- Group code   "11"
- Configuration word(14bit)   "11001101010010"

LSB (first in)   MSB

0	1	0	0	1	0	1	0	1	1	0	0	1	1

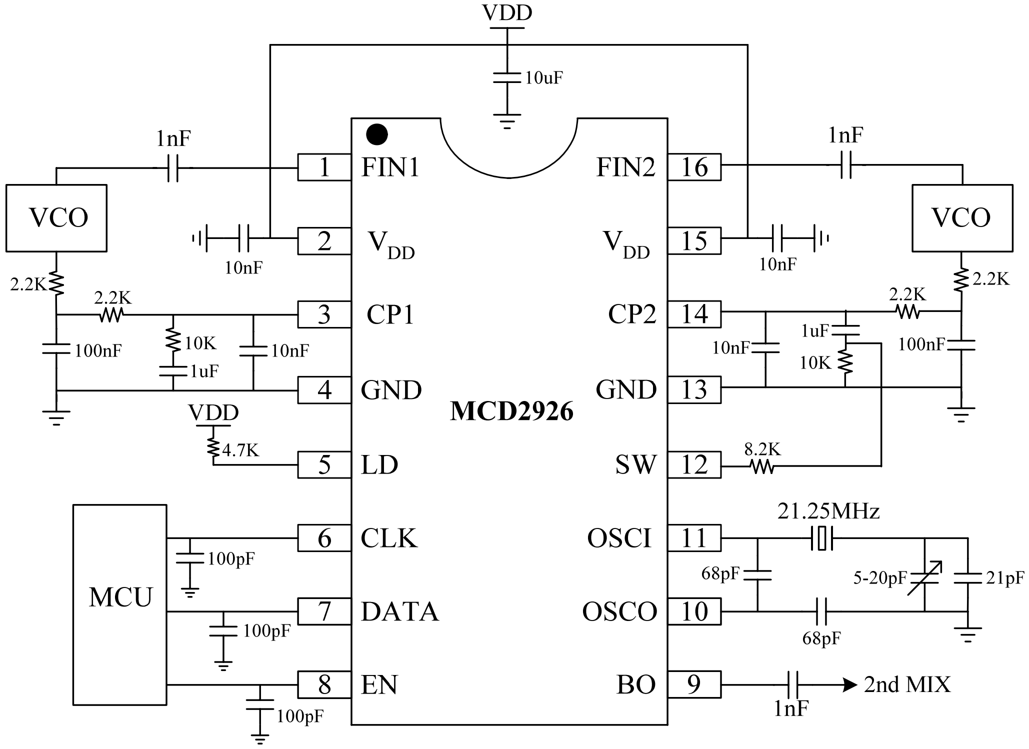
3.3 Example C: To synthesize a 453MHz frequency from a 12.5KHz reference frequency (Channel 1)

- Reference frequency   12.5KHz (see Example A)
- Total division ratio   2x(32xB + A) = 453MHz÷12.5KHz = 36240
- 32*B+A=18120
- Pulse counter division ratio   B = Int (18120÷32) = 566
- Binary format (12bit)   B = 001000110110
- Swallow counter division ratio   A = 18120 - 32*566 = 8
- Binary format (5bit)   A=01000
- Group code   "01"
- Configuration word(19bit)   "0100100011011001000"

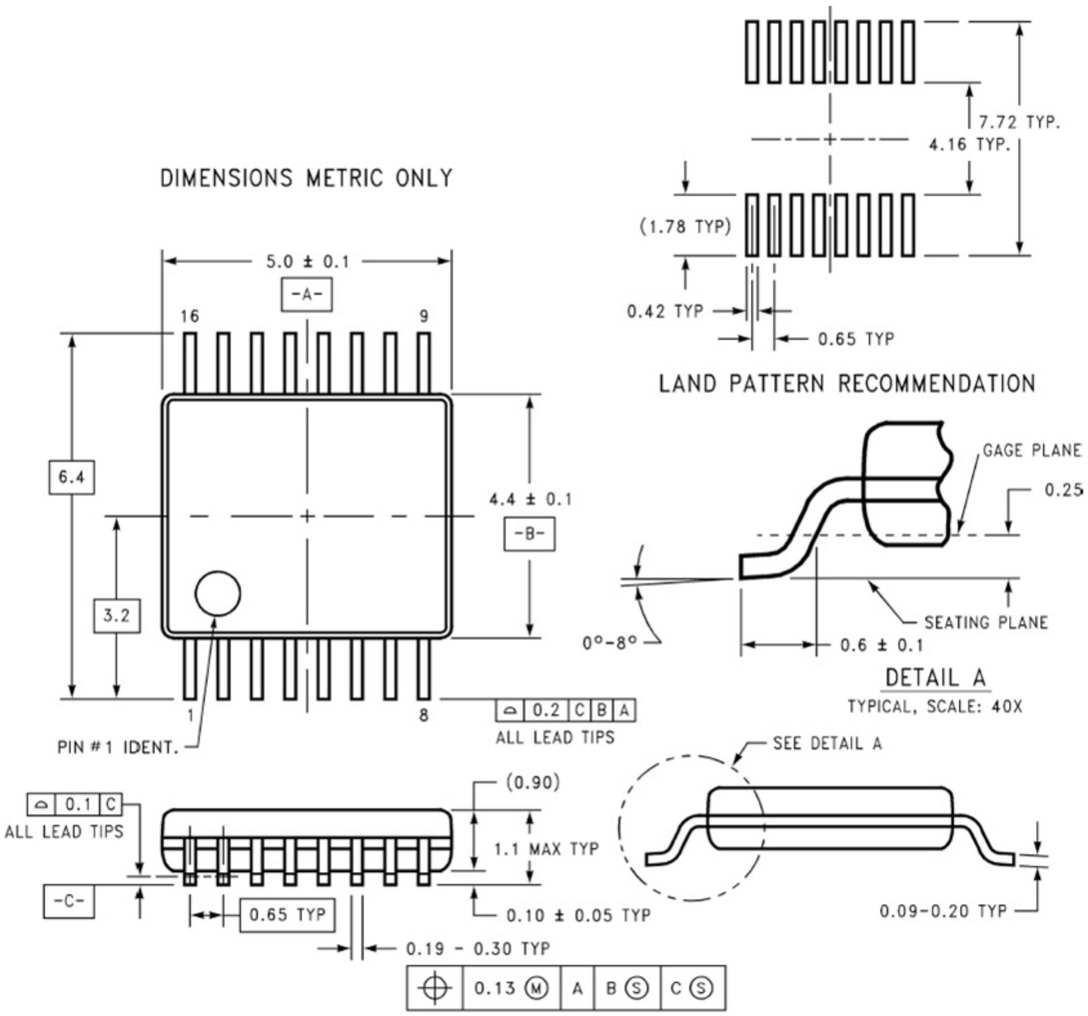
LSB (first in)   MSB

0	0	0	1	0	0	1	1	0	1	1	0	0	0	1	0	0	1	0

4. Typical Application Circuit



5. Package Dimensions: TSSOP-16 (Unit: millimetre; unless otherwise noted)



Dimensions are in millimeters.

16-Pin TSSOP Package

5.1 Packaging Method

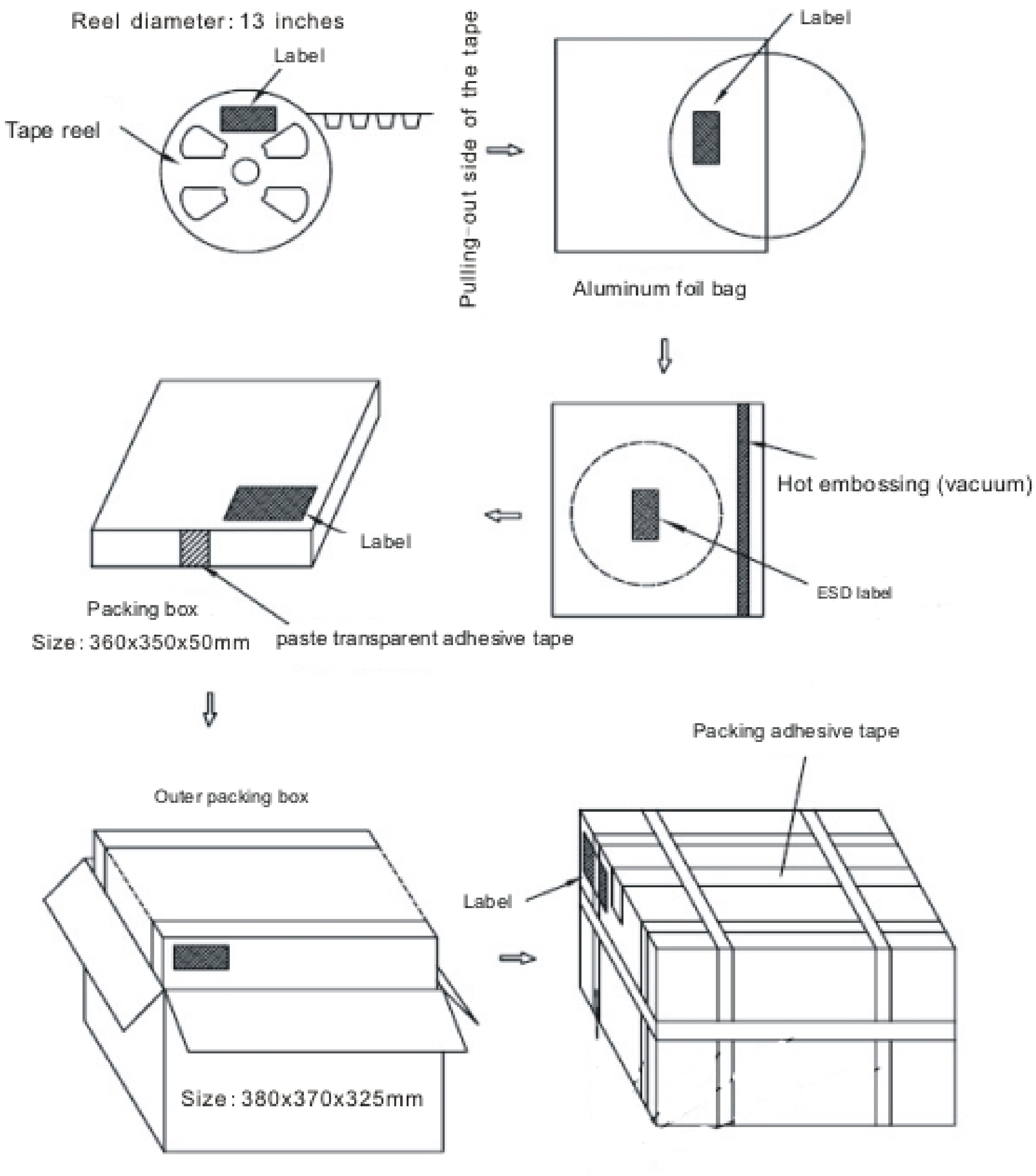
5.1.1. Tube packaging process:

Packaging Type	Pcs/Tube	Pcs/Box	Pcs/Case
TSSOP16 (Tube)	60	7200	43200

No.	Packaging example	Packaging description
1		1. Make the first pin toward the non-white cork (the other side of the tube is white cork). 2. The direction is as Figure 1, please make the direction of all products the same. 3. 60pcs chips in each tube.
2		1. Tie plastic tubes with the same direction. 2. 20 tubes for each buddle, 1200pcs chips altogether.
3		1. Place tubes in small packaging boxes. 2. 7200pcs chips in each box.
4		1. Cover small boxes, and stick the product label in the middle of right side.
5		Place small boxes with the same direction in cartoon boxes.
6		1. Cover cartoon boxes, and seal with transparent adhesive tape. 2. Stick product label in top left corner of cartoon boxes. 3. 43200pcs chips in each box.
7		Product label on cartoon boxes

5.1.2. Tape packaging process:

Packaging Type	Pcs/ Reel	Pcs /Box	Pcs / Case
TSSOP16 (Tape)	3,000	3,000	18,000



6. Comparison of MCD2926 and similar PLL ICs and Application Notes:

6.1 Comparison of MCD2926 and similar PLL ICs

Parameter \ Type		MCD2926 (MC Devices)	MCD8825B (MC Devices)	TB31202 (Toshiba)	S1T8825 (Samsung)	GP214D (Gaintech)
I_{DD}	single ~ dual channel (Typ. V_{DD}) (Amplitude)	7.5~14mA (3.3V) (-5dBm)	3.9~5.9mA (3.0V) (-5dBm)	6~12mA (2.2V) (0dBm)	5.5~9.5mA (3.0V) (-5dBm)	7.0~14.5mA (3.0V) (-5dBm)
Supply Voltage(V)		2.2~5.5	2.2~3.6	2.0~5.5	2.2~5.5	2.4~5.0
Frequency range (MHz)		18~650	200~1300	200~520	200~1300	100~1400
Charge pump current (uA)		200、400、800	200、400、800、1600	100、200、400、800	200、400、800、1600	200、400、800、1600

Note: The chips in above table are functional same ICs, and they are pin to pin compatible.

6.2 Application notes of MCD2926:

(1) The software of MCD2926 is completely compatible with MCD8825B、TB31202、S1T8825's. It is compatible with GP214D except pin 12.

(2) The pin2 and pin5 have to short each other and connect to power supply at anytime.

(3) The best operation voltage is 3.3V.

(4) When operation voltage is 5.5V, to apply a transient voltage suppressor on power supply is recommended to avoid chip damage.

(5) The input amplitude of Pin1(Fin1) and Pin16(Fin2) are required to be larger than -10dBm to guarantee the loop lock stably.

(6) The selection of charge pump current: the higher CP current, the shorter lock time, the larger power consumption and the worse low frequency noise; vice versa.

(7) The bias voltages of Pin1(Fin1)、Pin16(Fin2) and Pin11(Oscin) depend on I/O resistance, usually are 05~0.7 VDD.

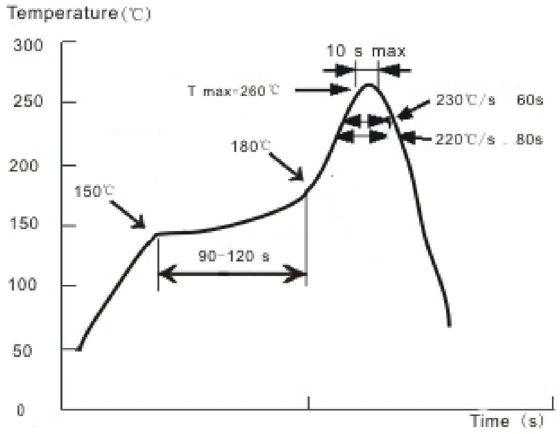
(8) When single channel applied, to short the unused Fin to GND is recommended for improving noise performance.

(9) When dual channel applied, the software control should follow the sequence:

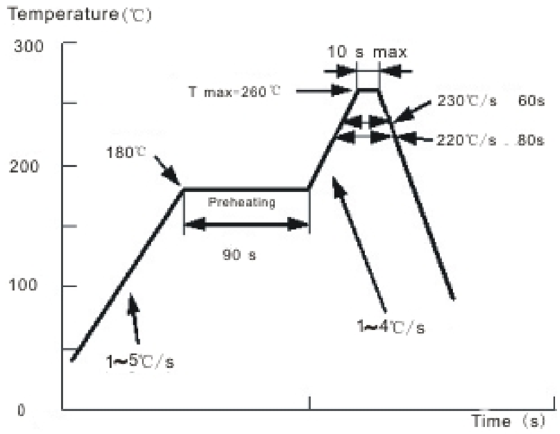
Firstly, configure the R counter; secondly, configure the N counter. At last, configure the control latch. Keep the data interval as 5 times of CLK period.

(10) Please refer to reflow soldering temperature profile as below:

7. Soldering temperature profile:



Wave-soldering temperature profile



Reflow soldering temperature profile

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美芯集成电路（深圳）有限公司
中国深圳高新区科技中二路软件园一期四栋 516 室
电话：（86）755-8618-5088
传真：（86）755-8618-5000
Email：sales@mcdevices.com
网址：www.mcdevices.com

MC DEVICES Co., Ltd
516 Bld. 4, National Software Park, 2 Kejizhong Rd., Shenzhen Hi-Tech Park,
Shenzhen, Guangdong, China
Tel: 86-755-8618-5088
Fax:86-755-8618-5000
Email: sales@mcdevices.com
http://www.mcdevices.com