Freescale

P-Channel 32-V (D-S) MOSFET

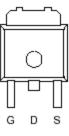
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY	
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V _{DS} (V)	$r_{\mathrm{DS(on)}} m(\Omega)$	I _D (A)
-32	$59 @ V_{GS} = -10V$	24
-32	$95 @ V_{GS} = -4.5V$	19





TO-252

Top View

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter			Maximum	Units
Drain-Source Voltage			-32	V
Gate-Source Voltage			±25	v
Continuous Drain Current ^a	T _A =25°C	I _D	24	А
Pulsed Drain Current ^b			±40	A
Continuous Source Current (Diode Conduction) ^a		Is	-30	А
Power Dissipation ^a	$T_A=25^{\circ}C$	P _D	50	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	°C/W	
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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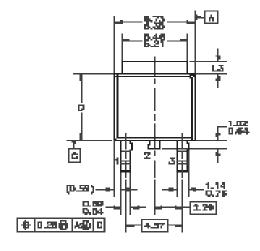
Parameter	Symbol	Symbol Test Conditions		Limits		Unit	
r ar ameter	Symbol	Test Conditions	Min	Тур	Max		
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-1				
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -24 V, V_{GS} = 0 V$ $V_{DS} = -24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			-1 -5	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 V, V_{GS} = -10 V$	-41			А	
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -24 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -19 \text{ A}$			59 95	mΩ	
Forward Tranconductance ^A	g _{fs}	$V_{DS} = -15 \text{ V}, I_D = -24 \text{ A}$		31		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = -41$ A, $V_{\rm GS} = 0$ V		-0.7		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = -15 V, V_{GS} = -4.5 V,$		6.4			
Gate-Source Charge	Q _{gs}	$v_{DS} = -15 v, v_{GS} = -4.5 v,$ $I_D = -24 A$		1.9		nC	
Gate-Drain Charge	Q _{gd}	$I_{\rm D} = -27$ A		2.5			
Input Capacitance	C _{iss}			520			
Output Capacitance	C _{oss}	VDS=-15V, VGS=0V, f=1MHz		130		pF	
Reverse Transfer Capacitance	C _{rss}			70			
Switching							
Turn-On Delay Time	t _{d(on)}			10			
Rise Time	t _r	V_{DD} = -15 V, R_L = 15 Ω , ID = -24		2.8		nS	
Turn-Off Delay Time	t _{d(off)}	A, VGEN = -10 V, $RG = 6\Omega$		53.6		115	
Fall-Time	t _f			46			

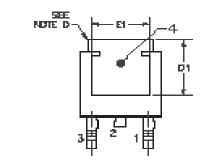
Notes

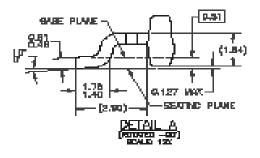
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

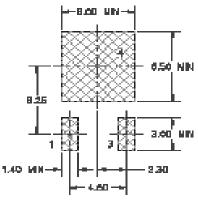
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Package Information

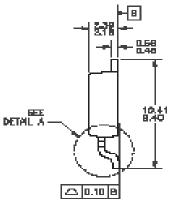








LAND PATTERN RECOMMENDATION



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