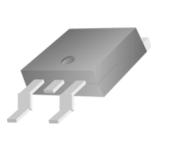
P-Channel 40-V (D-S) MOSFET

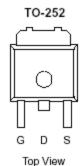
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

V _{DS} (V)	$r_{\mathrm{DS}(\mathrm{on})} \mathrm{m}(\Omega)$	I _D (A)
-40	$69 @ V_{GS} = -10V$	22
	$106 @ V_{GS} = -4.5V$	18

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)				
Parameter			Maximum	Units
Drain-Source Voltage			-4 0	V
Cate-Source Voltage			±20	V
Continuous Drain Current ^a	T _A =25°C	I_D	22	A
Pulsed Drain Current ^b		I_{DM}	±72	Α
Continuous Source Current (Diode Conduction) ^a			-30	Α
Power Dissipation ^a	T _A =25°C	P_{D}	50	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	$R_{ heta JA}$	50	°C/W	
Maximum Junction-to-Case	$R_{ heta JC}$	3.0	°C/W	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

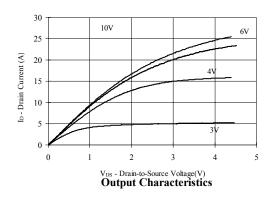
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Davidana Asar	Ch al	Symbol Test Conditions		Limits			
Parameter	Symbol			Тур	Max	Unit	
Static			•				
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \text{ uA}$	-1				
Gate-Body Leakage	Igss	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1		
Zero Gate Voltage Diam Current	IDSS	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-41			A	
D i G G D i A		$V_{GS} = -10 \text{ V}, I_D = -22 \text{ A}$			69		
Drain-Source On-Resistance ^A	fDS(on)	$V_{GS} = -4.5 \text{ V}, I_D = -18 \text{ A}$			106	mΩ	
Forward Tranconductance ^A	$g_{ m fs}$	$V_{DS} = -15 \text{ V}, I_D = -22 \text{ A}$		31		S	
Diode Forward Voltage	V _{SD}	$I_S = -41 \text{ A}, V_{GS} = 0 \text{ V}$		-0.7		V	
Dynamic ^b	•				-	•	
Total Gate Charge	Qg	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -22 \text{ A}$		10			
Gate-Source Charge	Q_{gs}			2.2		nC	
Gate-Drain Charge	Qgd			2.5]	
Switching	•				•	•	
Turn-On Delay Time	t _{d(on)}			10			
Rise Time	$t_{\rm r}$	V_{DD} = -15 V, R_L = 15 Ω , ID = -24 A,		2.8		nS	
Turn-Off Delay Time	t _{d(off)}	VGEN = -10 V, $RG = 6\Omega$		53.6		ns	
Fall-Time	t_{f}			46		Ī	

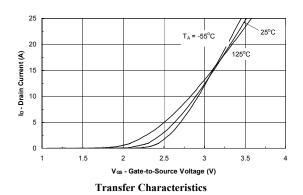
Notes

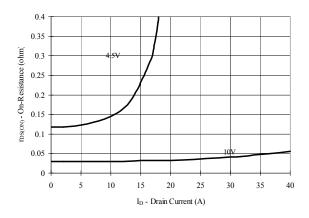
- a. Pulse test: $PW \le 300us duty cycle \le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics







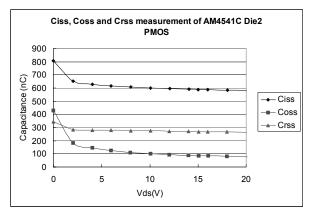
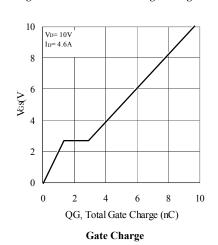
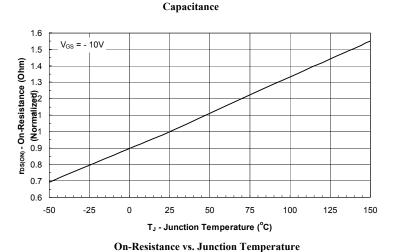


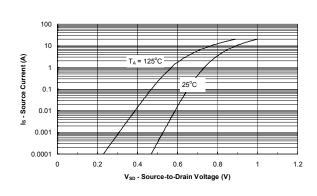
Figure 3. On Resistance Vs Vgs Voltage

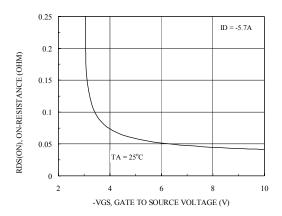




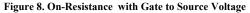
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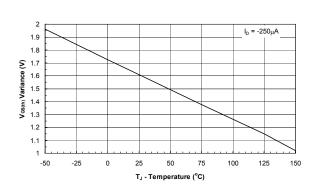
Typical Electrical Characteristics

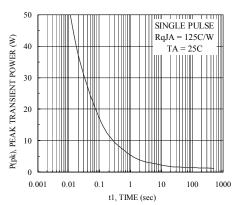




Source-Drain Diode Forward Voltage







Threshold Voltage

Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

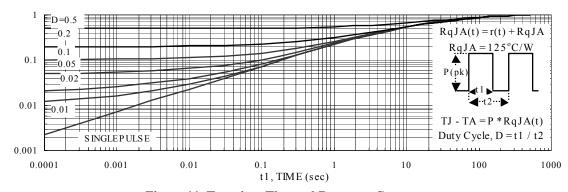
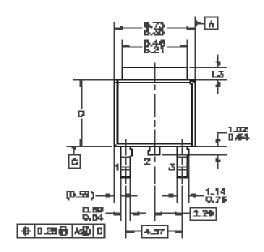
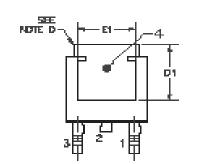
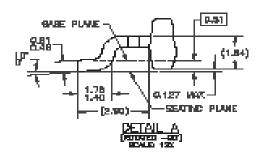


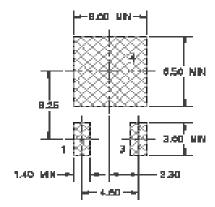
Figure 11. Transient Thermal Response Curve

Package Information

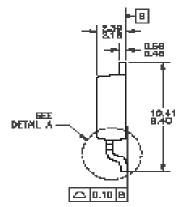








LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- ALL DIVERSIONS ARE IN NULLWETERS.
- THIS PACIONE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AN IN RE, DATED NOW 1989. DIMENSIONIC AND TOLERANCING PER
- MENE Y14,041—1884.
 HEAT SHIK TOP EDGE COULD BE IN CHANFERED
 CORPLETS OR EDGE PROTEVOICH.
 DIMENSIONS L3,D,E1&D1 TABLE:

DE -1.27	1.63-7.79
	8.44-8.40
4.42	3.01 MH
341 104	4.37