Ordering number : ENN7199

P-Channel Silicon MOSFET

MCH3319

Ultrahigh-Speed Switching Applications

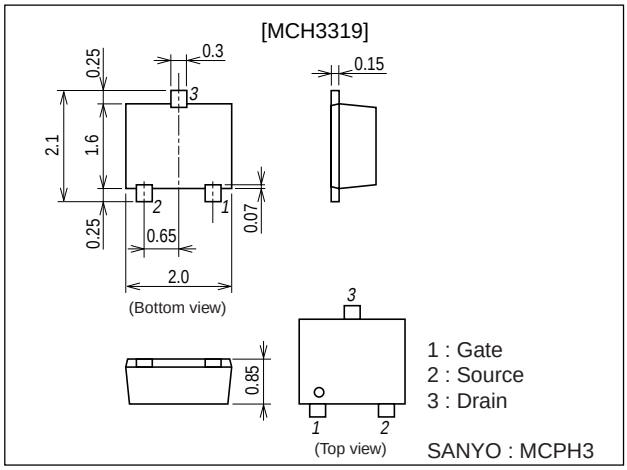
Features

- Low ON-resistance.
- Ultrahigh-speed switching.
- 1.8V drive.

Package Dimensions

unit : mm

2167A



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−12	V
Gate-to-Source Voltage	V_{GSS}		±8	V
Drain Current (DC)	I_D		−2.6	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−10.4	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (900mm²×0.8mm)	1.0	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0	−12			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−12V, V_{GS}=0			−10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±6.4V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−6V, I_D=−1mA	−0.3		−1.0	V
Forward Transfer Admittance	|yfs|	V_{DS}=−6V, I_D=−1.3A	2.9	4.2		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−1.3A, V_{GS}=−4.5V		75	98	mΩ
	R_{DS}(on)2	I_D=−0.7A, V_{GS}=−2.5V		110	155	mΩ
	R_{DS}(on)3	I_D=−0.3A, V_{GS}=−1.8V		150	255	mΩ

Marking : JU

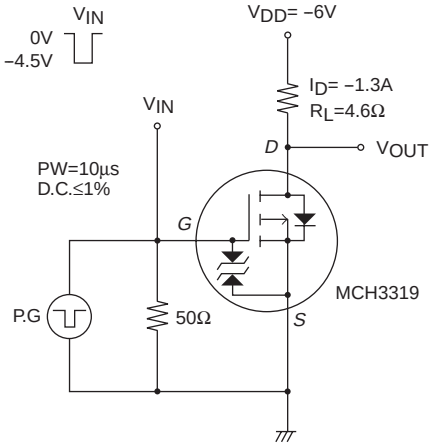
Continued on next page.

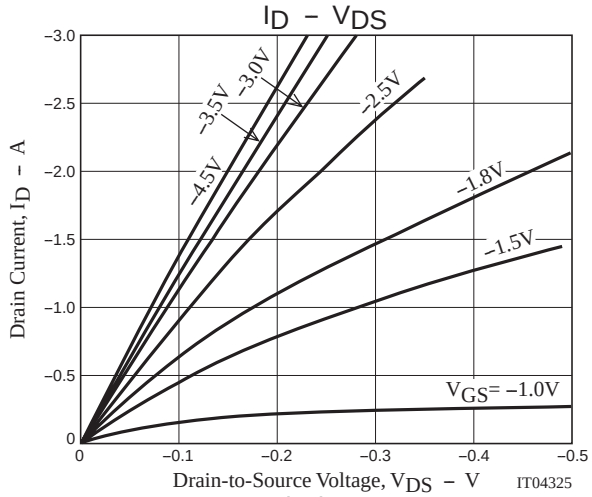
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

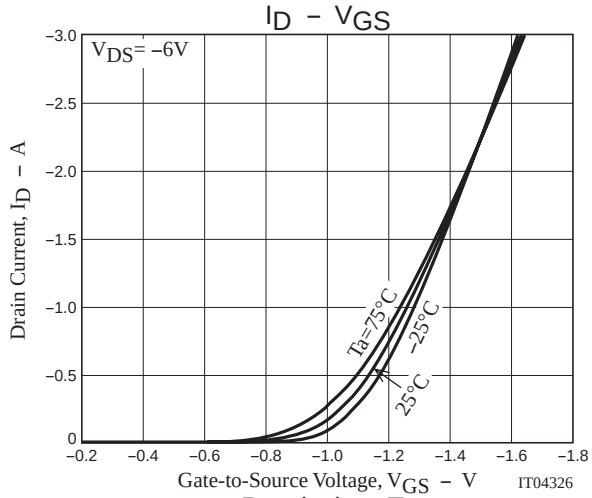
Continued from preceding page.

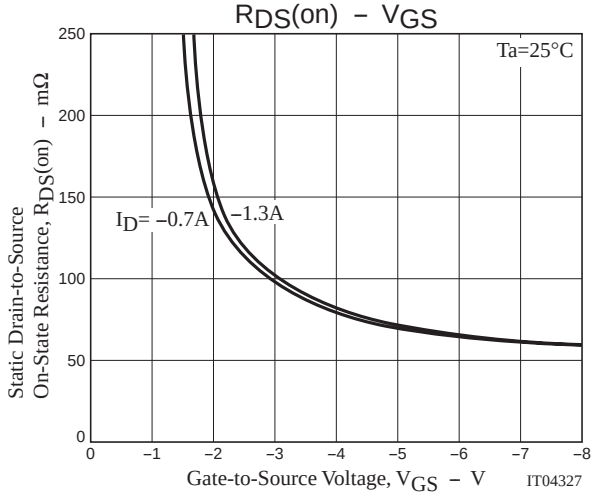
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=-6V, f=1MHz		450		pF
Output Capacitance	Coss	V_{DS}=-6V, f=1MHz		100		pF
Reverse Transfer Capacitance	Crss	V_{DS}=-6V, f=1MHz		85		pF
Turn-ON Delay Time	t_{d}(on)	See specified Test Circuit.		15		ns
Rise Time	t_{r}	See specified Test Circuit.		70		ns
Turn-OFF Delay Time	t_{d}(off)	See specified Test Circuit.		65		ns
Fall Time	t_{f}	See specified Test Circuit.		50		ns
Total Gate Charge	Qg	V_{DS}=-6V, V_{GS}=-4.5V, I_{D}=-2.6A		6.5		nC
Gate-to-Source Charge	Qgs	V_{DS}=-6V, V_{GS}=-4.5V, I_{D}=-2.6A		0.8		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=-6V, V_{GS}=-4.5V, I_{D}=-2.6A		2.0		nC
Diode Forward Voltage	V_{SD}	I_{S}=-2.6A, V_{GS}=0		-0.87	-1.5	V

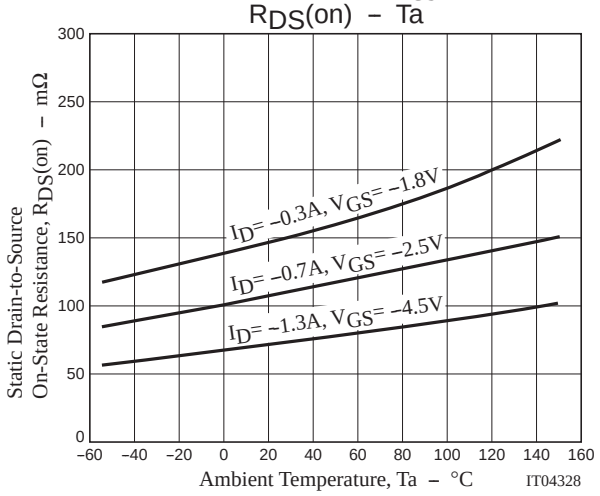
Switching Time Test Circuit

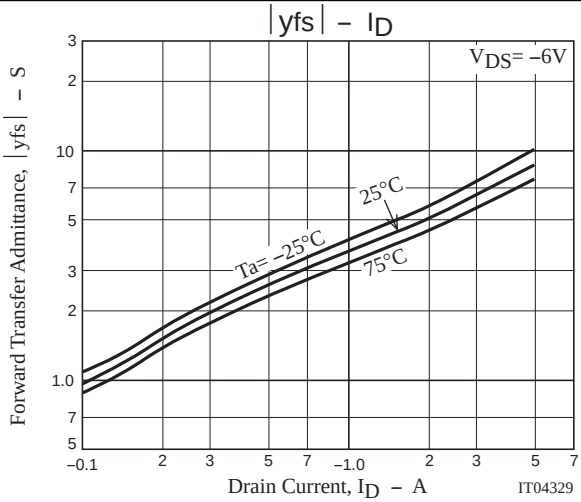


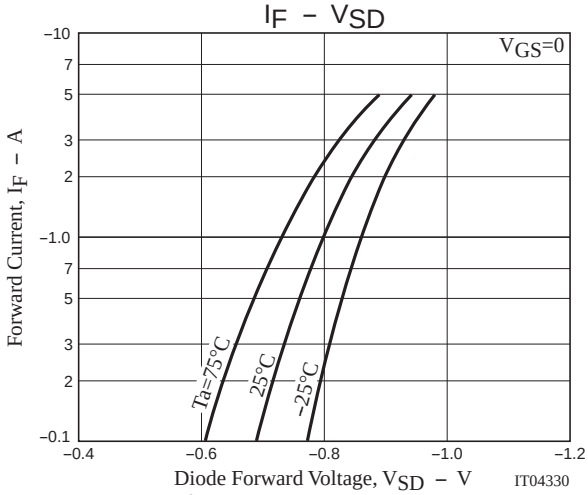


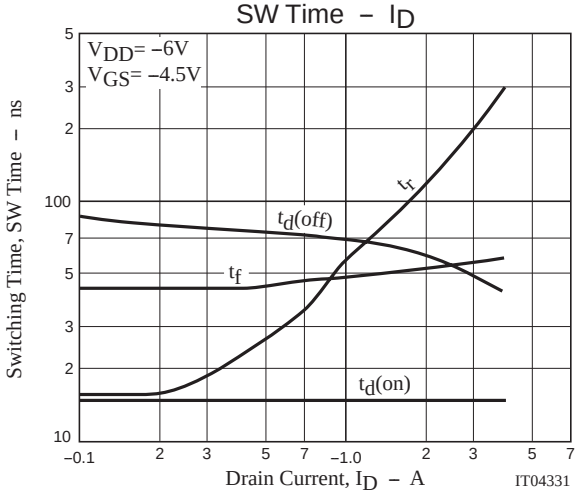


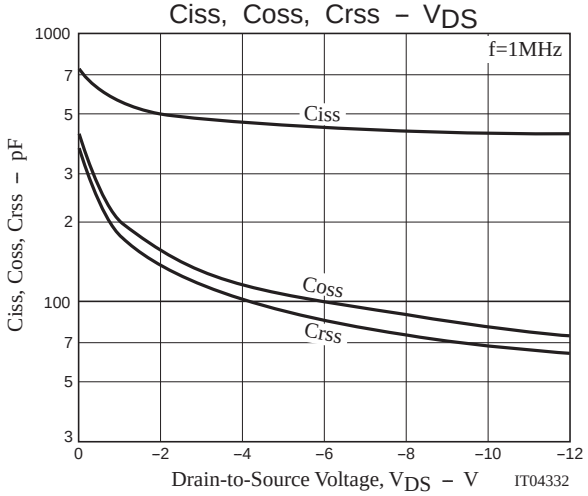


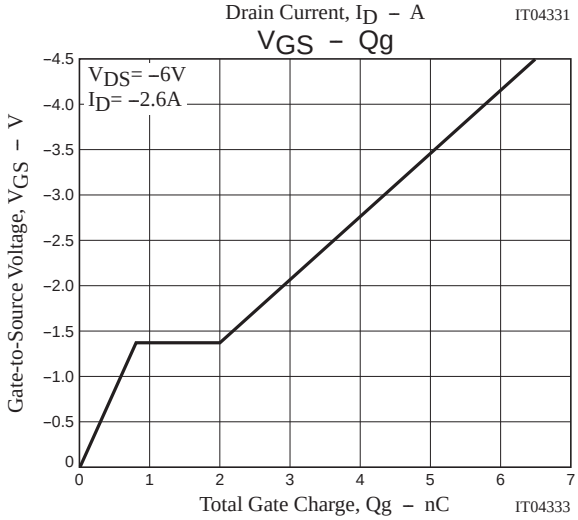


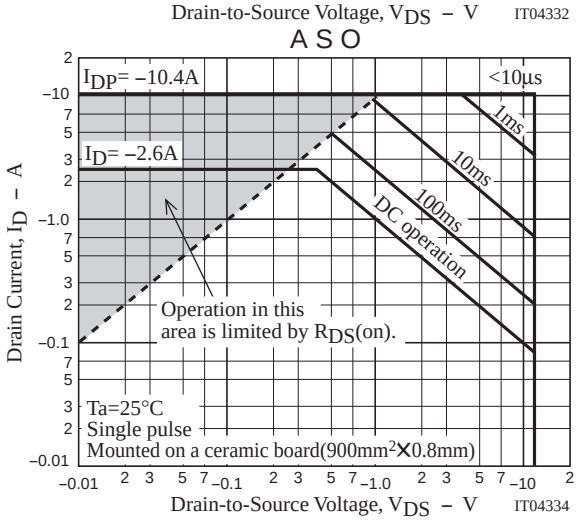

|yfs| – ID
VDS= –6V
25°C
Ta= –25°C
75°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT04329

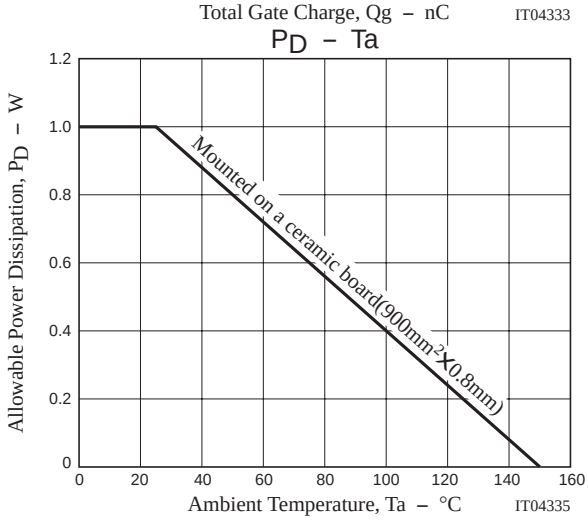

IF – VSD
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT04330


SW Time – ID
VDD= –6V
VGS= –4.5V
tr
td(off)
tf
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT04331


Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT04332


VGS – Qg
VDS= –6V
ID= –2.6A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT04333


A S O
IDP= –10.4A
<10μs
1ms
10ms
100ms
DC operation
ID= –2.6A
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board(900mm²X0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT04334


PD – Ta
Mounted on a ceramic board(900mm²X0.8mm)
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT04335

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