Data Sheet

M-5 CHANNEL ADAPTER

SILICON REVISION A0

M5CAA0-DS
Rev 02 PRODUCTION

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Data Sheet

M-5 CHANNEL ADAPTER
SILICON REVISION A0

M5CAA0-DS
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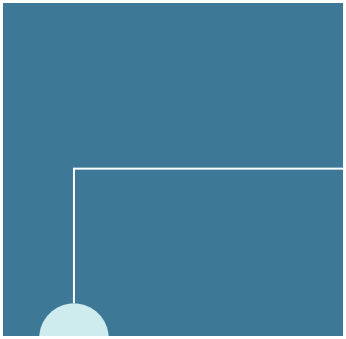


ABOUT THIS GUIDE

Guide Overview

The M-5™ Channel Adapter (CA) Data Sheet describes hardware layout specifications including pinouts, memory configuration guidelines, timing diagrams, power and power sequencing guidelines, thermal design guidelines and mechanical specifications. Motorola reserves the right to change the detail specifications as may be required to permit improvements in the design of its products. Motorola reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

The guide covers the following topics:

- Functional Description
- Signal Descriptions
- Electrical Specifications
- Mechanical Specifications

Data Sheet Classifications

Table 1 describes the Data Sheet classifications of Advance, Preliminary, and Production.

Table 1 Data Sheet Classifications

CLASSIFICATION	DESCRIPTION
Advance Information	Used to advise customers of the proposed addition to the product line. This document will typically contain some useful information including interfacing with the user's system and some specifications. The goal of this document is to allow customers to begin designs but with expectation of changes. Specification details may be changed later without notice.
Preliminary Information	Describes pre-production or first production devices and is usually indicative of production stage performance. Minor changes should be expected as characteristic spreads become better controlled. Specification details may be changed slightly without notice, but the customer can design their product based on this data sheet.
Production Data	Defines the long-term specified production limits based on fully characterized data. It includes a disclaimer to allow improvements in specifications and modifications that do not affect form, fit or function in original applications; if absolute maximum ratings are changed, they should improve rather than downgrade.

Using C-Port Electronic Documents

C-Port electronic documents are provided as PDF files. Open and view them using the Adobe® Acrobat® Reader application, version 3.0 or later. If necessary, download the Acrobat Reader from the Adobe Systems, Inc. web site:

http://www.adobe.com/prodindex/acrobat/readstep.html

Each provided PDF file offers several ways for moving among the document's pages, as follows:

To move quickly from section to section within the document, use the *Acrobat bookmarks* that appear on the left side of the Acrobat Reader window. The bookmarks provide an expandable outline view of the document's contents. To display the document's Acrobat bookmarks, press the "Display both bookmarks and page" button on the Acrobat Reader tool bar.

To move to the referenced page of an entry in the document's Contents or Index, click on the entry itself, each of which is hyperlinked.

To follow a cross-reference to a heading, figure, or table, click the blue text.

To move to the beginning or end of the document, to move page by page within the document, or to navigate among the pages you displayed by clicking on hyperlinks, use the Acrobat Reader navigation buttons shown in this figure:

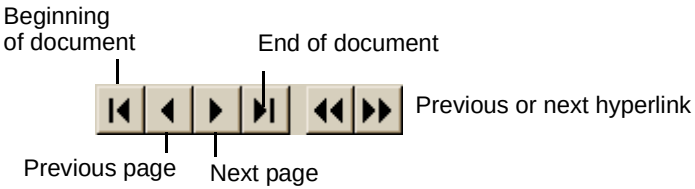


Table 2 summarizes how to navigate within a C-Port electronic document.

Table 2 Navigating Within a PDF Document

TO NAVIGATE THIS WAY	CLICK THIS
Move from section to section within the document.	A bookmark on the left side of the Acrobat Reader window
Move to an entry in the Table of Contents.	The entry itself
Move to an entry in the Index.	The page number
Move to an entry in the List of Figures or List of Tables.	The Figure or Table number
Follow a cross-reference (highlighted in blue text).	The cross-reference text
Move page by page.	The appropriate Acrobat Reader navigation buttons
Move to the beginning or end of the document.	The appropriate Acrobat Reader navigation buttons
Move backward or forward among a series of hyperlinks you have selected.	The appropriate Acrobat Reader navigation buttons

Guide Conventions

The following visual elements are used throughout this guide, where applicable:

This icon and text designates information of special note.

Warning: *This icon and text indicate a potentially dangerous procedure. Instructions contained in the warnings must be followed.*

Warning: *This icon and text indicate a procedure where the reader must take precautions regarding laser light.*

This icon and text indicate the possibility of electro-static discharge (ESD) in a procedure that requires the reader to take the proper ESD precautions.

Related Product Documentation

Table 3 lists the C-Port Family silicon documentation. These documents can be found either on the Motorola web site (motorola.com/networkprocessors) or on the password-protected C-Port Family Support site (motorola.cportcorp.com/support).

Table 3 C-Port Silicon Documentation Set

DOCUMENT NAME	PURPOSE	DOCUMENT ID
C-5e/C-3e Network Processor Architecture Guide	Describes the full architecture of the C-5e and C-3e network processors.	C5EC3EARCH-RM
C-5e Network Processor Data Sheet	Describes hardware design specifications for the C-5e network processor.	C5ENPB0-DS
C-3e Network Processor Data Sheet	Describes hardware design specifications for the C-3e network processor.	C3ENPB0-DS
C-5 Network Processor to C-5e Network Processor Comparison	Describes key architectural features of the C-5e, and highlights main differences between C-5 and C-5e.	C5C5EDELTA-RM
M-5 Channel Adapter Architecture Guide	Describes the full architecture of the M-5 channel adapter.	M5CAARCH-RM
M-5 Channel Adapter Data Sheet	Describes hardware design specifications for the M-5 channel adapter.	M5CAA0-DS

Revision History

Table 4 shows the revision history for this data sheet, providing a description of the changes.

Table 4 M-5 CA Data Sheet Revision History

REVISION	CHANGE
02	Chapter 1, restructured and enhanced. Chapter 2, added details for eight signal types. Chapter 2, condensed the signals listed by pin number table. Chapter 3, added description and specifications for Low Speed Serial Bus t_{sp} characteristics. Chapter 4, added more detail information about Reflow.
01	New document - no changes

Chapter 1

FUNCTIONAL DESCRIPTION

Chapter Overview

This chapter covers the following topic:

- M-5 Channel Adapter (CA) Overview

M-5 Channel Adapter (CA) Overview

In general, the M-5 CA accepts a mix of PDU rates (OC-1, OC-3c, OC-12c, OC-48 and OC-48c) for both packet and cell applications. Basically, the M-5 CA is a multiplexor. It can be used with the C-5e's CPs and/or with the C-5e's FP based upon your application needs.

In more detail, the M-5 Channel Adapter (CA), is used with the C-5e NP to provide the required PDU ordering for both packet and cells for both the front ports (CPs) and back port (FPTx only under certain configurations). In addition, it provides bus translation from multi-physical layer (MPHY), 32bit UTOPIA Level 3 (UTOPIA-L3) to the C-5e front ports (CPs) and back port (FP), as well as, bus translation from Saturn POS-PHY Level 3 (POS-PHY-L3) to the C-5e front ports (CPs) and back port (FP), thus allowing OC-48c bandwidths. Additionally, the front ports (CPs) use a Gigabit Media Independent Interface (GMII) that can be modified to provide flow control that interfaces with the SDPs.

The method that the M-5 uses to provide PDU ordering is called *Sequence Numbers*. Sequencer numbers are 13bits long and are included as part of the enqueue and dequeue operations. Sequence Numbers are used whenever a flow is spread across more than one cluster in the case of the front ports (CPs). The FPRx does not need sequence numbers since it maintains strict ordering internally. However, the FPTx does require sequence numbers *only* when *virtual queueing* is used in the configuration.

For a detailed description of potential M-5 CA configurations, refer to the C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM), section entitled "C-5e NP System Configuration Overview".

Throughout this manual Channel Processors (CPs) are referred to as "Front Port" and Fabric Processor (FP) is referred to as "Back Port". This simply refers to the location of theses ports on the C-5e NP.

General M-5 CA Features

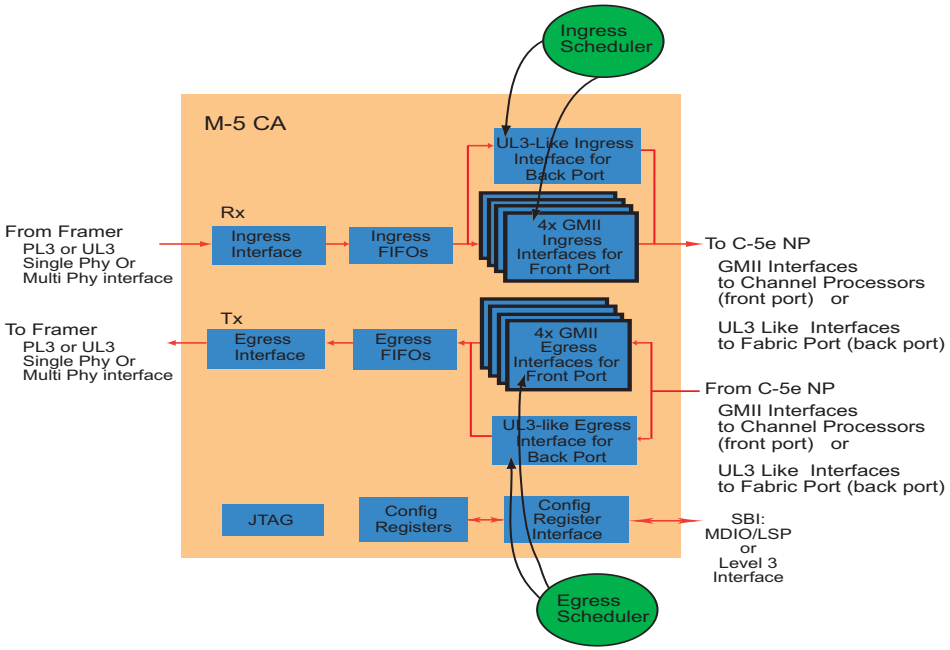
The M-5 CA coprocessor provides the following features.

- Supports ATM 52Byte cells
- Supports packets from 5Bytes to 9216Bytes
- Provides buffering of cells or packets between the framer and the C-5e NP
- Provides two (2) low pin count Serial Bus Interface (SBI) protocols:
  - High-speed protocol Management Data input/output (MDIO) *or*
  - Low-Speed Protocol (LSP) slave

  Both provide configuration, control and status monitoring functions. The M-5 CA MDIO is compatible with the C-5e NP MDIO. And the M-5 CA LSP is compatible with the C-5e NP's Level3 master serial interface.
- Provides a standard five signal IEEE 1149.1 JTAG interface
- BIST (Built In Self Test) provided for all internal RAMs.
- Low power 1.8 V CMOS device with 3.3V TTL compatible digital inputs and 3.3 V CMOS/TTL compatible outputs
- 324-pin TBGA
- Industrial Temperature Range (-40° to 85°C) ambient

Block Diagram The block diagram of the M-5 CA is shown in Figure 1 on page 10.

Figure 1 M-5 CA Functional Block Diagram



M-5 CA System Overview

Based on the particular application, a framer to M-5 CA set may be used in three (3) possible configurations: on the front of the C-5e NP that feeds into its Channel Processors (CP0 to CP15), on the back of the C-5e NP that feeds into its Fabric Processor (FP), or on both the front and back of the C-5e NP.

Figure 2 on page 11 and show the two (2) bridging configurations of the M-5 CA. Also shown in Figure 2 on page 11 are the four (4) allowed interfaces of the C-5 CA system. The M-5 CA may have two (2) framer interfaces (noted as 1 & 2) and two (2) NP interfaces (noted as 3 & 4). In addition, Table 5 on page 12 provides a list of each interface and its description.

Figure 2 M-5 CA System Overview Block Diagram

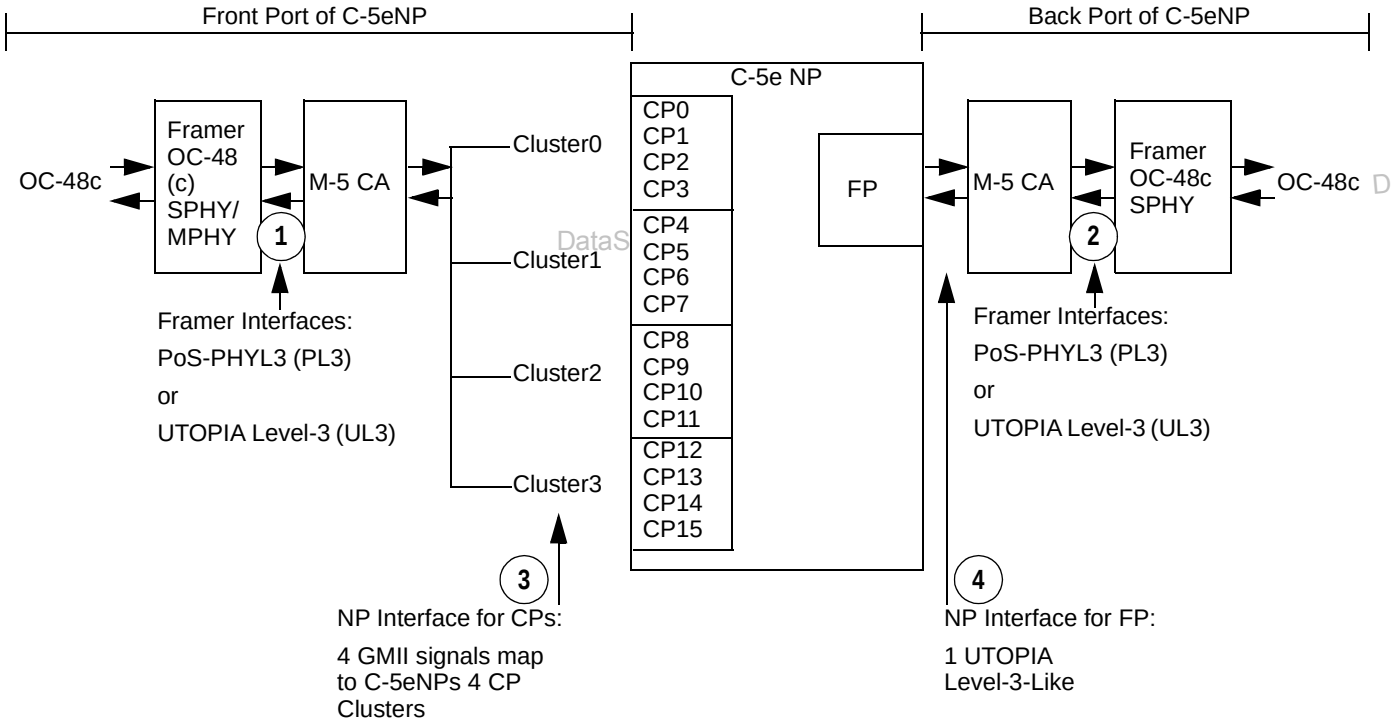


Table 5 Summary of Interfaces Supported by the M-5 CA

ITEM	DESCRIPTION
Framer Interface	In general, the framer interface supports a variety of framers with an aggregate data rate of OC-48c. Specifically, it provides bridging function from Framer to C-5e NPs Channel Processors (CPs) on the Front Ports *and* on the C-5e NPs Fabric Port (FP) on the Back Port. Two (2) framer protocols are supported: • Provides a 32bit UL3 (UTOPIA Level 3) framer interface operating from 66 to 104MHz with optional parity for ATM (Asynchronous Transfer Mode) applications. The M-5 CA is the UL3 master, or • Provides a 32bit PL3 (SATURN PoS-PHY Level 3) framer interface operating from 66 to 104MHz with optional parity and packet level transfer control for Packet Over SONET (PoS), HDLC or ATM applications. Word level transfer control (PL3 specification refers to this as Byte level transfer control) is not supported. The M-5 CA is the PL3 master. Both direct status (single Phy only, OC-48c) and polling (single Phy (OC-48c) or multi Phy (OC-1, OC-3, OC-12)) modes are supported for both UTOPIA Level3 and PoS Level3.
C-5e NP Channel Processors (CPs) Front Port Interface	Provides bridging function from the framer to the C-5e NP's Channel Processor (CP) interface. One type of protocol is supported: • Provides four (4) 8bit Gigabit Media Independent Interfaces (GMII) to the C-5e's front port operating from approximately 66 to 104MHz with optional Cyclic Redundancy Check (CRC)-16. GMII protocol maps from the M-5 CA to the C-5e NP CP *Clusters*, of which their are four (4), and *not* to the C-5e NP individual sixteen (16) CP ports.
C-5e NP Fabric Processor (FP) Back Port Interface	Provides a bridging function from an OC-48c Framer to the C-5e NP's Fabric Processor (FP) interface. One type of protocol is supported: • Provides a 32bit UL3-like (UTOPIA Level 3) interface to the C-5e's back port operating from 66 to 104 MHz. Only direct status mode is supported. The M-5 CA is the UL3-Like master.

Possible Framer Configurations for C-5e NP (CPs) and (FP)

Framer configurations for the C-5e NP CPs and the C-5e NP FP. In addition, the M-5 CA to C-5e NP CP mapping is provided.

C-5e NP CPs to Framer Configurations

Table 6 on page 13 gives some of the possible framer configurations that are supported by the M-5 CA when bridging the framer to the C-5e NP's Channel Processor (CPs). The various mix configurations are made up of legal mixtures of OC-1, OC-3 and OC-12 channels with a combination data rate less than or equal to OC-48c.

Table 6 Framer to C-5e NP (CP) Configurations Supported by the M-5 CA

FRAMER PORT CONFIGURATION	AGGREGATED DATA RATE	NUMBER OF FRAMER CHANNELS
16 ports x OC-3c	OC-48	16
4 ports x OC-12c	OC-48	4
1 port x OC-48c	OC-48	1
Various Mix of OC-1, OC-3c and OC-12c	OC-48	Configurable. See Table 7 on page 13 for details

Table 7 Some of the Various Mix Configurations Supported

# OF OC-1 CHANNELS	# OF OC-3C CHANNELS	# OF OC-12C CHANNELS	TOTAL AGGREGATED DATA RATE
48	0	0	OC-48
0	16	0	OC-48
0	0	4	OC-48
3	3	3	OC-48
12	12	0	OC-48

Table 7 on page 13 *provides some of the possible OC-48 channel configurations supported. Not all supported channel configurations are listed.*

M-5 CA to C-5e NP CP Mapping

The M-5 CA provides the mapping function between the framer that has from 1 to 48 channels to the 16 channel processors of the C-5e NP. Table 8 on page 14 describes this mapping.

Table 8 M-5 CA to C-5e NP CP Mapping

DATA RATE	FRAMER CHANNEL TO C-5e NP CHANNEL PROCESSOR MAPPINGS
OC-1	Three OC-1 channels map to a single C-5e NP channel processor
OC-3c	One OC-3c channel maps to a single C-5e NP channel processor
OC-12c	One OC-12c channel maps to one C-5e NP cluster, a cluster is comprises four (4) channel processors. Note: Clusters mapping is only required when using GMII protocol.
OC-48c	One OC-48c channel maps to all 16 C-5e NP channel processors

C-5e NP FP to Framer Configuration

Table 9 on page 14 gives the framer channel configuration supported by the M-5 CA when bridging the framer to the C-5e NP's back port.

Table 9 Framer to C-5e NP (FP) Configuration Supported by the M-5 CA

FRAMER PORT CONFIGURATION	AGGREGATED DATA RATE	NUMBER OF FRAMER CHANNELS
1 port x OC-48c	OC-48	1

Chapter 2

SIGNAL DESCRIPTIONS

Signal Summary

The M-5 CA contains 324 pins that are organized into ten (10) signal groups as listed below:

- Framer Interface — 94 pins (see Table 10 on page 17)
- C-5e NP Interface — 76 pins (see Table 11 on page 19)
- Serial Bus Interface — 2 pins (see Table 13 on page 24)
- Clock Interface — 9 pins (see Table 14 on page 24)
- Phase Lock Loop (PLL) — 3 pins (see Table 15 on page 24)
- Test Access Port (TAP) — 5 pins (see Table 16 on page 25)
- Scan Mode — 1 pin (see Table 17 on page 25)
- Reset — 1 pin (see Table 18 on page 25)
- Power and Ground — 109 pins (see Table 19 on page 26)
- No Connection — 24 pins (see Table 20 on page 26)

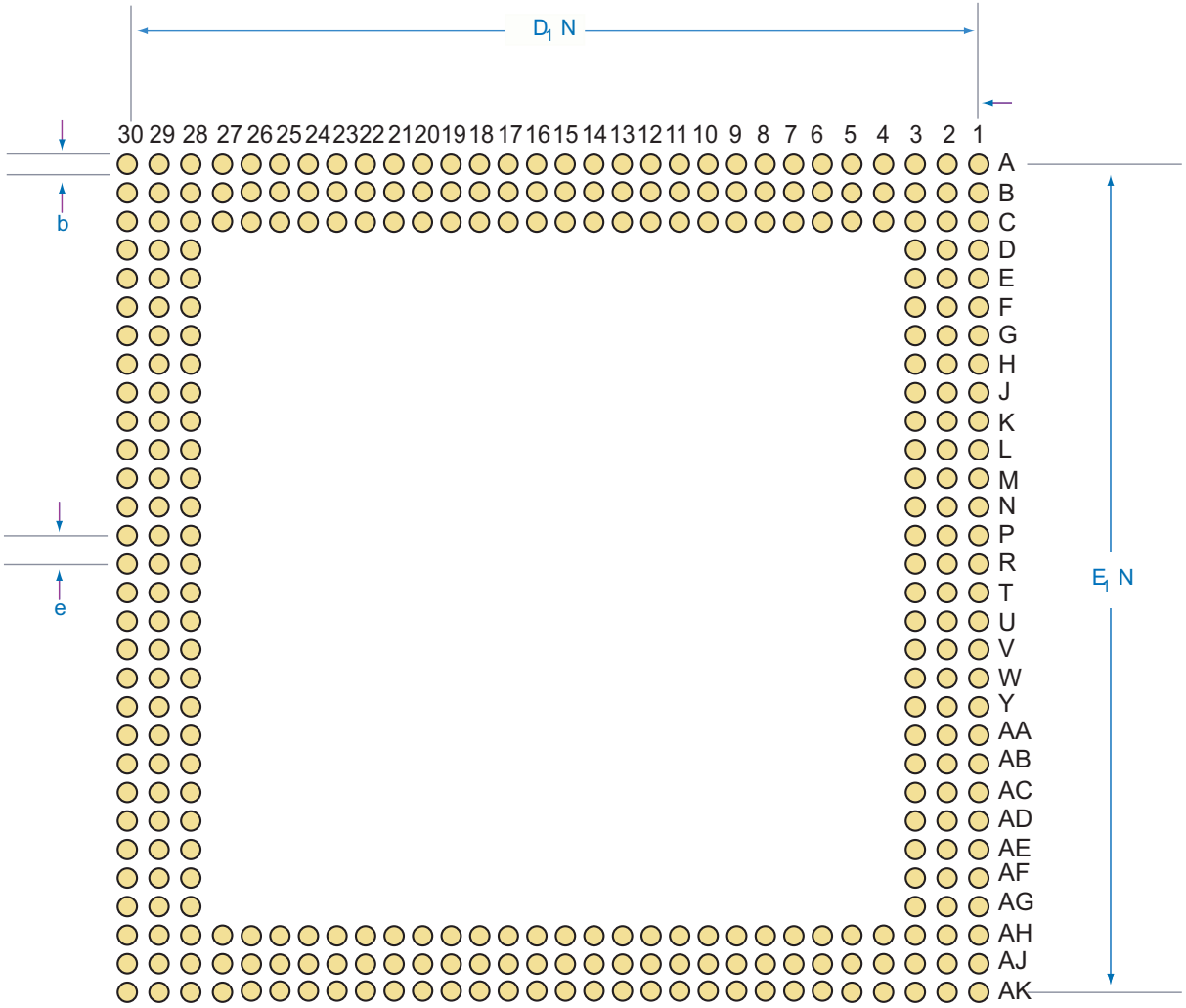
For proper clock configurations, refer to the M-5 Channel Adapter Architecture Guide (part number M5CAARCH-RM).

All pins are LVTTL type.

Pinout Diagram

Figure 3 on page 16 and Table 23 on page 31 describe the M-5 CA Pin Assignments. These pin numbers are referenced throughout the remaining chapter.

Figure 3 M-5 CA Pinout Diagram



M-5 CA I/O Interface Signals

Table 10 describes the M-5 CA's I/O interfaces to UTOPIA and POS-PHY framers. Table 11 describes the M-5 CA's I/O interfaces to the C-5e NP's front and back ports.

Table 10 M-5 CA Framer I/O

	FRAMER INTERFACES						
M-5 SIGNAL	**PL3 SIGNAL**	**PL3 FUNCTION**	**UL3 SIGNAL**	**UL3 FUNCTION**	**TOTAL**	**I/O**	**PIN # (MSB - LSB)**
TADR[5:0]	TADR[5:0]	PL3 Framer Interface Transmit Address	TxAddr[5:0]	UL3 Framer Interface Transmit Address	6	O	A13, B13, A12, B12, A11, A10
TPA_TCA	PTPA or DTPA	PL3 Framer Interface Polled-PHY Transmit Packet Available (MPHY) or Direct-PHY Transmit Packet Available (SPHY)	TxClav	UL3 Framer Interface Polled-PHY Transmit Cell Available (MPHY) or Direct-PHY Transmit Cell Available (SPHY)	1	I	A15
TENB	TENB	PL3 Framer Interface Transmit Enable	TxEnb	UL3 Framer Interface Transmit Enable	1	O	B14
TSOP_TSOC	TSOP	PL3 Framer Interface Transmit Start of Packet	TxSOC	UL3 Framer Interface Transmit Start of Cell	1	O	A17
TDAT[31:0]	TDAT[31:0]	PL3 Framer Interface Transmit Data	TxData[31:0]	UL3 Framer Interface Transmit Data	32	O	L30, K30, J30, J29, H30, H29, G30, F30, F29, E30, D30, D29, B30, A29, B28, A28, A27, B27, A26, A25, B25, A24, B24, A23, B23, A22, B22, A21, B21, A20, B20, A19
TPRTY	TPRTY	PL3 Framer Interface Transmit Parity	TxPrty	UL3 Framer Interface Transmit Parity	1	O	B18
TSX	TSX	PL3 Framer Interface Transmit Start of Transfer	unused		1	O	B17

Table 10 M-5 CA Framer I/O (continued)

	FRAMER INTERFACES						
M-5 SIGNAL	**PL3 SIGNAL**	**PL3 FUNCTION**	**UL3 SIGNAL**	**UL3 FUNCTION**	**TOTAL**	**I/O**	**PIN # (MSB - LSB)**
TEOP	TEOP	PL3 Framer Interface Transmit End of Packet	unused		1	O	B16
TMOD[1:0]	TMOD[1:0]	PL3 Framer Interface Transmit Modulo	unused		2	O	B15, A14
TERR	TERR	PL3 Framer Interface Transmit Error	unused		1	O	A18
RADDR[5:0]	unused		RxAddr[5:0]	UL3 Framer Interface Receive Address	6	O	T1,U1,W1,W2,Y1,Y2
RVAL_RCA	RVAL	PL3 Framer Interface Receive Data Valid	RxClav	UL3 Framer Interface Receive Cell Available	1	I	R1
RENB	RENB	PL3 Framer Interface Receive Enable	RxEnb	UL3 Framer Interface Receive Enable	1	O	R2
RSOP_RSOC	RSOP	PL3 Framer Interface Receive Start of Packet	RxSOC	UL3 Framer Interface Receive Start of Cell	1	I	M1
RDAT[31:0]	RDAT[31:0]	PL3 Framer Interface Receive Data	RxData[31:0]	UL3 Framer Interface Receive Data	32	I	A9, B9, A8, B8, A7, B7, A6, B6, A5, B5, A4, B4, A3, A2, B3, B1, C1, C2, D2, D1, E1, E2, F2, F1, G1, H2, H1, J1, J2, K2, K1, L1,
RPRTY	RPRTY	PL3 Framer Interface Receive Parity	RxPrty	UL3 Framer Interface Receive Parity	1	I	L2
RSX	RSX	PL3 Framer Interface Receive Start of Transfer	unused		1	I	N2

Table 10 M-5 CA Framer I/O (continued)

	FRAMER INTERFACES						
M-5 SIGNAL	**PL3 SIGNAL**	**PL3 FUNCTION**	**UL3 SIGNAL**	**UL3 FUNCTION**	**TOTAL**	**I/O**	**PIN # (MSB - LSB)**
REOP	REOP	PL3 Framer Interface Receive End of Packet	unused		1	I	M2
RMOD[1:0]	RMOD[1:0]	PL3 Framer Interface Receive Modulo	unused		2	I	P2, P1
RERR	RERR	PL3 Framer Interface Receive Error	unused		1	I	N1
TOTAL PINS					**94**		

Table 11 M-5 CA C-5e NP I/O

	C-5e INTERFACES						
M-5 SIGNAL	**FRONT PORT MODE (GMII)**	**GMII FUNCTION**	**BACK PORT MODE (UL3)**	**UL3 LIKE FUNCTION**	**TOTAL**	**I/O**	**PIN # (MSB - LSB)**
FPI_TDATA[31:24]	GMII3_RXD[7:0]	C5 Channel Processor Cluster3 Interface (GMII3) Receive Data [7:0]	FPI_TDATA[31:24]	C5 Fabric Processor Interface Transmit Data [31:24]	8	O	R29, R30, T30, T29, U30, V30, W29, W30
FPI_TDATA[23:16]	GMII2_RXD[7:0]	C5 Channel Processor Cluster2 Interface (GMII2) Receive Data [7:0]	FPI_TDATA[23:16]	C5 Fabric Processor Interface Transmit Data [23:16]	8	O	AA29, AB30, AC30, AC29, AD30, AD29, AE30, AE29
FPI_TDATA[15:8]	GMII1_RXD[7:0]	C5 Channel Processor Cluster1 Interface (GMII1) Receive Data [7:0]	FPI_TDATA[15:8]	C5 Fabric Processor Interface Transmit Data [15:8]	8	O	AH29, AJ30, AK29, AJ28, AK28, AJ27, AK27, AJ26

Table 11 M-5 CA C-5e NP I/O (continued)

	C-5e INTERFACES						
M-5 SIGNAL	**FRONT PORT MODE (GMII)**	**GMII FUNCTION**	**BACK PORT MODE (UL3)**	**UL3 LIKE FUNCTION**	**TOTAL**	**I/O**	**PIN # (MSB - LSB)**
FPI_TDATA[7:0]	GMII0_RXD[7:0]	Output - C5 Channel Processor Cluster0 Interface (GMII0) Receive Data [7:0] Input - Serial bus configuration sampled on POR	FPI_TDATA[7:0]	Output - C5 Fabric Processor Interface Transmit Data [7:0] Input - Serial bus configuration sampled on POR	8	I/O	AJ24, AK24, AJ23, AK23, AJ22, AK22, AJ21, AK21
FPI_TPRTY	GMII0_COL	C5 Channel Processor Cluster0 Interface (GMII0) Transmit Flow Control	FPI_TPRTY	C5 Fabric Processor Interface Transmit Parity	1	O	AK20
FPI_TENB	GMII1_COL	C5 Channel Processor Cluster1 Interface (GMII1) Transmit Flow Control	FPI_TENB	C5 Fabric Processor Interface Transmit Enable	1	O	AJ25
FPI_TCA	GMII1_TXEN	C5 Channel Processor Cluster1 Interface (GMII1) Transmit Enable	FPI_TCA	C5 Fabric Processor Interface Transmit Segment Available	1	I	AF1
GMII0_RXDV	GMII0_RXDV	C5 Channel Processor Cluster0 Interface (GMII0) Receive Data Valid	unused		1	O	AJ19

Table 11 M-5 CA C-5e NP I/O (continued)

M-5 SIGNAL	C-5e INTERFACES				TOTAL	I/O	PIN # (MSB - LSB)
	FRONT PORT MODE (GMII)	GMII FUNCTION	BACK PORT MODE (UL3)	UL3 LIKE FUNCTION			
GMII1_RXDV	GMII1_RXDV	C5 Channel Processor Cluster1 Interface (GMII0) Receive Data Valid	unused		1	O	AK25
GMII2_RXDV	GMII2_RXDV	C5 Channel Processor Cluster2 Interface (GMII0) Receive Data Valid	unused		1	O	AH30
FPI_TSOC	GMII3_RXDV	C5 Channel Processor Cluster3 Interface (GMII3) Receive Data Valid	FPI_TSOC	C5 Fabric Processor Interface Transmit Start of Segment	1	O	AA30
FPI_RDATA[31:24]	GMII3_TXD[7:0]	C5 Channel Processor Cluster3 Interface (GMII3) Transmit Data[7:0]	FPI_RDATA[31:24]	C5 Fabric Processor Interface Receive Data [31:24]	8	I	AJ14, AK13, AJ13, AK12, AJ12, AK11, AJ11, AK10
FPI_RDATA[23:16]	GMII2_TXD[7:0]	C5 Channel Processor Cluster2 Interface (GMII2) Transmit Data[7:0]	FPI_RDATA[23:16]	C5 Fabric Processor Interface Receive Data [23:16]	8	I	AJ9, AK8, AJ8, AK7, AJ7, AJ6, AK6, AK5
FPI_RDATA[15:8]	GMII1_TXD[7:0]	C5 Channel Processor Cluster1 Interface (GMII1) Transmit Data[7:0]	FPI_RDATA[15:8]	C5 Fabric Processor Interface Receive Data [15:8]	8	I	AJ4, AK3, AJ3, AK2, AJ1, AH2, AG1, AG2

Table 11 M-5 CA C-5e NP I/O (continued)

M-5 SIGNAL	C-5e INTERFACES				TOTAL	I/O	PIN # (MSB - LSB)
	FRONT PORT MODE (GMII)	GMII FUNCTION	BACK PORT MODE (UL3)	UL3 LIKE FUNCTION			
FPI_RDATA[7:0]	GMII0_TXD[7:0]	C5 Channel Processor Cluster0 Interface (GMII0) Transmit Data[7:0]	FPI_RDATA[7:0]	C5 Fabric Processor Interface Receive Data [7:0]	8	I	AE1, AE2, AD2, AD1, AC1, AC2, AB2, AB1
FPI_RENB	GMII2_COL	C5 Channel Processor Cluster2 Interface (GMII2) Transmit Flow Control	FPI_RENB	C5 Fabric Processor Interface Receive Enable	1	O	AG29
GMII3_COL	GMII3_COL	C5 Channel Processor Cluster3 Interface (GMII3) Transmit Flow Control	unused		1	O	Y29
FPI_RPRTY	GMII0_TXEN	C5 Channel Processor Cluster0 Interface (GMII0) Transmit Enable	FPI_RPRTY	C5 Fabric Processor Interface Receive Parity	1	I	AA2
GMII2_TXEN	GMII2_TXEN	C5 Channel Processor Cluster2 Interface (GMII2) Transmit Enable	unused		1	I	AK4
FPI_RSOC	GMII3_TXEN	C5 Channel Processor Cluster3 Interface (GMII3) Transmit Enable	FPI_RSOC	C5 Fabric Processor Interface Receive Start of Segment	1	I	AK9
TOTAL PINS					**76**		

Serial Interface Signals

The Serial Bus interface is a general purpose bi-directional, two-wire serial bus and I/O port. The serial bus allows a master (C-5e NP or other) to modify and read registers in the M-5 CA. It allows the M-5 CA to support two (2) standard protocols.

- The high-speed protocol (MDIO) uses a 16bit data format (though the M-5 CA only uses the lower 8bits; the upper 8bits are ignored) with 10bits of addressing, and supports transfers at up to 25 MHz (the M5CLK must run more than 3 times faster than the SICL).
- The low-speed protocol (LSP) uses an 8bit data format followed by an acknowledge bit and supports transfers at up to 400kbps. The serial bus interface is configured by pulling up or pulling down a set of pins that the M-5 CA samples during power on reset.

Refer to Table 12 on page 23 for the SBI configuration pins and Table 13 on page 24 for the SBI signals.

Table 12 Serial Interface Configuration Pins

PIN NAME	CONFIGURATION NAME	PULLED LOW	PULLED HIGH
FPI_TDATA[0]	MDIO mode	LSP Used	MDIO Protocol Used
FPI_TDATA[6:1]	Slave Address[5:0]	Serial Bus Slave Address	
FPI_TDATA[7]	MDIO Preamble Suppression	Full Preamble Required (32 cycle)	Two Cycle Preamble Required
FPI_TDATA[8]	MDIO Two Bit Turnaround	MDIO uses 1 TA cycle during reads	MDIO always uses 2 TA cycles

The protocol to be used is selected by pulling up or pulling down the FPI_TDATA[0] pin, which the M-5 CA samples during power on reset. The M-5 CA is always a slave in both protocols.

Both SIDA and SICL are bi-directional lines that are connected (via an external pull-up resistor) to the positive supply voltage. The M-5 CA never drives the SICL line when in MDIO mode. When the bus is free, both lines are HIGH. In Low Speed Protocol (LSP) mode, the output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism. The bus supports collision detection and arbitration in LSP mode.

Table 13 Serial Interface Signals

SIGNAL NAME	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
SICL	Serial Clock line	1	I_{PD}/O	Y5
SIDA	Serial Data line	1	I_{PD}/O	Y6
TOTAL PINS		**2**		

Table 14 Clocks Interfaces

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
M5CLK	M-5 Clock	1	I	AK15
GTX_CLK[0:3]	C-5e NP Forwarded GMII Transmit Clock	4	I	AA1, AF2, AJ5, AJ10
RXCLK{0:3]	M-5 Forwarded GMII Receive Clock	4	O	AJ20, AK26, AG30, Y30
TOTAL PINS		**9**		

Table 15 Phase Lock Loop

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
TPA_ANA	Analog PLL Test Pin	1	O	AK17
VDDANA_1	Analog VDD	1	Power Pad	AK16
GNDANA_1	Ground	1	Gnd	AK18
TOTAL PINS		**3**		

Table 16 Test Access Port

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
TCK	Test Logic Clock	1	I	N30
TMS	Tap mode control input	1	I_{PD}	L29
TDI	Serial test instruction/data input	1	I_{PD}	M30
TRSTB	Asynchronous test controller reset. In normal system operation, this should be connected to RESETB.	1	I_{PD}	N29
TDO	Serial test instruction/data output	1	O	P30
TOTAL PINS		**5**		

Table 17 Scan Mode

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
SCAN	Scan enable	1	I	AJ15
TOTAL PINS		**1**		

Table 18 Reset

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
RESETB	Reset	1	I	AK14
TOTAL PINS		**1**		

Table 19 Power and Ground Signals

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
VDDCORE	Core Supply Voltage (1.8V Input)	31	P	C3, AB3, AD3, AF3, AH6, AH15, AH26, AE28, AC28, AB28, AA28, E3, W28, T28, P28, N28, K28, J28, G28, F28, C27, C19, G3, C13, C6, J3, L3, N3, R3, V2, Y3
VDDPAD	I/O Supply Voltage (3.3V Input)	20	P	AH27, P29, C11, AH24, H28, B26, AH21, E28, B19, AH18, C30, B11, AH3, C24, AF28, C23, V28, C18, U3, C15
GND	Ground	58	P	AK30, AH19, AC3, U29, M28, F3, C17, A30, AK1, AH17, AB29, U28, M3, E29, C14, A1, AJ29, AH7, AA3, U2, L28, D28, C12, AJ17, AG3, Y28, T3, K29, D3, C10, AJ2, AF30, W3, T2, K3, C29, C4, AH28, AF29, V29, R28, H3, C26, B29, AH25, AE3, V3,P3, G29, C22, B10, AH22, AD28, V1, M29, G2, C20, B2
TOTAL PINS		**109**		

Table 20 No Connection Pins

M5 SIGNAL	FUNCTION	TOTAL	I/O	PIN # (MSB - LSB)
NC[0:23]	Reserved for future functionality	24	N/A	A16, AH10, AH23 C21, AG28, AH11, AJ16, C25, AH1, AH12, C5, C28, AH4, AH13, C7, AH5, AH14, C8, AH8, AH16, C9, AH9, AH20, C16
TOTAL PINS		**24**		

M-5 CA to C-5e NP Signal Connections

Table 21 and Table 22 show the mapping of M-5 CA signals to C-5e NP signals.

Table 21 M-5 CA to C-5e NP Channel Processor s (CPs) (Front Port) Connections

M-5 CA PIN FUNCTION	C-5e NP PIN FUNCTION	GMII SIGNAL NAME	PIN # (MSB - LSB)
FPI_TDATA [31:24]	CPF_5, CPF_4, CPF_3, CPF_2, CPE_5, CPE_4, CPE_3, CPE_2	GMII3 RXD [7:0]	R29, R30, T30, T29, U30, V30, W29, W30
FPI_TSOC	CPE_6	GMII3 RX_DV	AA30
RX_CLK3	CPE_1	GMII3 RX_CLK	Y30
FPI_TDATA [23:16]	CPB_5, CPB_4, CPB_3,CPB_2, CPA_5, CPA_4, CPA_3, CPA_2	GMII2 RXD [7:0]	AA29, AB30, AC30, AC29, AD30, AD29, AE30, AE29
GMII2_RXDV	CPA_6	GMII2 RX_DV	AH30
RX_CLK2	CPA_1	GMII2 RX_CLK	AG30
FPI_TDATA [15:8]	CP7_5, CP7_4, CP7_3, CP7_2, CP6_5, CP6_4, CP6_3, CP6_2	GMII1 RXD [7:0]	AH29, AJ30, AK29, AJ28, AK28, AJ27, AK27, AJ26
GMII1_RXDV	CP6_6	GMII1 RX_DV	AK25
RX_CLK1	CP6_1	GMII1 RX_CLK	AK26
FPI_TDATA [7:0]	CP3_5, CP3_4, CP3_3, CP3_2, CP2_5, CP2_4, CP2_3, CP2_2	GMII0 RXD [7:0]	AJ24, AK24, AJ23, AK23, AJ22, AK22, AJ21, AK21
GMII0_RXDV	CP2_6	GMII0 RX_DV	AJ19
RX_CLK0	CP2_1	GMII0 RX_CLK	AJ20
FPI_RDATA [31:24]	CPD_5, CPD_4, CPD_3, CPD_2, CPC_5, CPC_4, CPC_3, CPC_2	GMII3 TXD [7:0]	AJ14, AK13, AJ13, AK12, AJ12, AK11, AJ11, AK10
GMII3_COL	CPD_1	GMII3 COL	Y29
FPI_RSOC	CPC_6	GMII3 TX_EN	AK9
GTX_CLK3	CPC_0	GMII3 GTX_CLK	AJ10

Table 21 M-5 CA to C-5e NP Channel Processor s (CPs) (Front Port) Connections (continued)

M-5 CA PIN FUNCTION	C-5e NP PIN FUNCTION	GMII SIGNAL NAME	PIN # (MSB - LSB)
FPI_RDATA [23:16]	CP9_5, CP9_4, CP9_3, CP9_2, CP8_5, CP8_4, CP8_3, CP8_2	GMII2 TXD [7:0]	AJ9, AK8, AJ8, AK7, AJ7, AJ6, AK6, AK5
FPI_RENB	CP9_1	GMII2 COL	AG29
GMII2_TXEN	CP8_6	GMII2 TX_EN	AK4
GTX_CLK2	CP8_0	GMII2 GTX_CLK	AJ5
FPI_RDATA [15:8]	CP5_5, CP5_4, CP5_3, CP5_2, CP4_5, CP4_4, CP4_3, CP4_2	GMII1 TXD [7:0]	AJ4, AK3, AJ3, AK2, AJ1, AH2, AG1, AG2
FPI_TENB	CP5_1	GMII1 COL	AJ25
FPI_TCA	CP4_6	GMII1 TX_EN	AF1
GTX_CLK1	CP4_0	GMII1 GTX_CLK	AF2
FPI_RDATA [7:0]	CP1_5, CP1_4, CP1_3, CP1_2, CP0_5, CP0_4, CP0_3, CP0_2	GMII0 TXD [7:0]	AE1, AE2, AD2, AD1, AC1, AC2, AB2, AB1
FPI_TPRTY	CP1_1	GMII0 COL	AK20
FPI_RPRTY	CP0_6	GMII0 TX_EN	AA2
GTX_CLK0	CP0_0	GMII0 GTX_CLK	AA1

Table 22 M-5 CA to C-5e NP Fabric Processor (Back Port) Connections

M-5 CA PIN FUNCTION	C-5e NP PIN FUNCTION	UL3-LIKE SIGNAL NAME	PIN # (MSB - LSB)
FPI_TDATA [31:0]	FIN[31:0]	UL3L RxData[31:0]	R29, R30, T30, T29, U30, V30, W29, W30, AA29, AB30, AC30, AC29, AD30, AD29, AE30, AE29, AH29, AJ30, AK29, AJ28, AK28, AJ27, AK27, AJ26, AJ24, AK24, AJ23, AK23, AJ22, AK22, AJ21, AK21
FPI_TSOC	FRXCTL2	UL3L RxSOC	AA30
FPI_TENB	FRXCTL0	UL3L RxEnb	AJ25
FPI_TCA	FRXCTL1	UL3L RxClav	AF1
FPI_TPRTY	FRXCTL6	UL3L RxPrty	AK20
FPI_RDATA [31:0]	FOUT[31:0]	UL3L TxData[31:0]	AJ14, AK13, AJ13, AK12, AJ12, AK11, AJ11, AK10, AJ9, AK8, AJ8, AK7, AJ7, AJ6, AK6, AK5, AJ4, AK3, AJ3, AK2, AJ1, AH2, AG1, AG2, AE1, AE2, AD2, AD1, AC1, AC2, AB2, AB1
FPI_RSOC	FTXCTL2	UL3L TxSOC	AK9
FPI_RENB	FTXCTL0	UL3L TxEnb	AG29
FPI_RPRTY	FTXCTL6	UL3L TxPrty	AA2

Signals Listed by Pin Number

Table 23 lists M-5 CA signals organized by their corresponding pin number by row.

Table 23 M-5 CA Pin Assignments

ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION
A	A1	GND	B	B1	RDAT_16	C	C1	RDAT_15
	A2	RDAT_18		B2	GND		C2	RDAT_14
	A3	RDAT_19		B3	RDAT_17		C3	VDDCORE
	A4	RDAT_21		B4	RDAT_20		C4	GND
	A5	RDAT_23		B5	RDAT_22		C5	No Connect
	A6	RDAT_25		B6	RDAT_24		C6	VDDCORE
	A7	RDAT_27		B7	RDAT_26		C7	No Connect
	A8	RDAT_29		B8	RDAT_28		C8	No Connect
	A9	RDAT_31		B9	RDAT_30		C9	No Connect
	A10	TADR_0		B10	GND		C10	GND
	A11	TADR_1		B11	VDDPAD		C11	VDDPAD
	A12	TADR_3		B12	TADR_2		C12	GND
	A13	TADR_5		B13	TADR_4		C13	VDDCORE
	A14	TMOD_0		B14	TENB		C14	GND
	A15	TPA_TCA		B15	TMOD_1		C15	VDDPAD
	A16	No Connect		B16	TEOP		C16	No Connect
	A17	TSOP_TSOC		B17	TSX		C17	GND
	A18	TERR		B18	TPRTY		C18	VDDPAD
	A19	TDAT_0		B19	VDDPAD		C19	VDDCORE
	A20	TDAT_2		B20	TDAT_1		C20	GND
	A21	TDAT_4		B21	TDAT_3		C21	No Connect
	A22	TDAT_6		B22	TDAT_5		C22	GND
	A23	TDAT_8		B23	TDAT_7		C23	VDDPAD
	A24	TDAT_10		B24	TDAT_9		C24	VDDPAD
	A25	TDAT_12		B25	TDAT_11		C25	No Connect
	A26	TDAT_13		B26	VDDPAD		C26	GND
	A27	TDAT_15		B27	TDAT_14		C27	VDDCORE
	A28	TDAT_16		B28	TDAT_17		C28	No Connect
	A29	TDAT_18		B29	GND		C29	GND
	A30	GND		B30	TDAT_19		C30	VDDPAD

Table 23 M-5 CA Pin Assignments (continued)

ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION
D	D1	RDAT_12	J	J1	RDAT_4	P	P1	RMOD_0
	D2	RDAT_13		J2	RDAT_3		P2	RMOD_1
	D3	GND		J3	VDDCORE		P3	GND
	D28	GND		J28	VDDCORE		P28	VDDCORE
	D29	TDAT_20		J29	TDAT_28		P29	VDDPAD
	D30	TDAT_21		J30	TDAT_29		P30	TDO
E	E1	RDAT_11	K	K1	RDAT_1	R	R1	RVAL_RCA
	E2	RDAT_10		K2	RDAT_2		R2	RENB
	E3	VDDCORE		K3	GND		R3	VDDCORE
	E28	VDDPAD		K28	VDDCORE		R28	GND
	E29	GND		K29	GND		R29	FPI_TDATA_31
	E30	TDAT_22		K30	TDAT_30		R30	FPI_TDATA_30
F	F1	RDAT_8	L	L1	RDAT_0	T	T1	RADDR_5
	F2	RDAT_9		L2	RPRTY		T2	GND
	F3	GND		L3	VDDCORE		T3	GND
	F28	VDDCORE		L28	GND		T28	VDDCORE
	F29	TDAT_23		L29	TMS		T29	FPI_TDATA_28
	F30	TDAT_24		L30	TDAT_31		T30	FPI_TDATA_29
G	G1	RDAT_7	M	M1	RSOP_RSOC	U	U1	RADDR_4
	G2	GND		M2	REOP		U2	GND
	G3	VDDCORE		M3	GND		U3	VDDPAD
	G28	VDDCORE		M28	GND		U28	GND
	G29	GND		M29	GND		U29	GND
	G30	TDAT_25		M30	TDI		U30	FPI_TDATA_27
H	H1	RDAT_5	N	N1	RERR	V	V1	GND
	H2	RDAT_6		N2	RSX		V2	VDDCORE
	H3	GND		N3	VDDCORE		V3	GND
	H28	VDDPAD		N28	VDDCORE		V28	VDDPAD
	H29	TDAT_26		N29	TRSTB		V29	GND
	H30	TDAT_27		N30	TCK		V30	FPI_TDATA_26

Table 23 M-5 CA Pin Assignments (continued)

ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION
W	W1	RADDR_3	AC	AC1	FPI_RDATA_3	AG	AG1	FPI_RDATA_9
	W2	RADDR_2		AC2	FPI_RDATA_2		AG2	FPI_RDATA_8
	W3	GND		AC3	GND		AG3	GND
	W28	VDDCORE		AC28	VDDCORE		AG28	No Connect
	W29	FPI_TDATA_25		AC29	FPI_TDATA_20		AG29	FPI_RENB
	W30	FPI_TDATA_24		AC30	FPI_TDATA_21	AH	AH1	No Connect
Y	Y1	RADDR_1	AD	AD1	FPI_RDATA_4		AH2	FPI_RDATA_10
	Y2	RADDR_0		AD2	FPI_RDATA_5		AH3	VDDPAD
	Y3	VDDCORE		AD3	VDDCORE		AH4	No Connect
	Y28	GND		AD28	GND		AH5	No Connect
	Y29	GMII3_COL		AD29	FPI_TDATA_18		AH6	VDDCORE
	Y30	RXCLK3		AD30	FPI_TDATA_19		AH7	GND
AA	AA1	GTX_CLK0	AE	AE1	FPI_RDATA_7		AH8	No Connect
	AA2	FPI_RPRTY		AE2	FPI_RDATA_6		AH9	No Connect
	AA3	GND		AE3	GND		AH10	No Connect
	AA28	VDDCORE		AE28	VDDCORE		AH11	No Connect
	AA29	FPI_TDATA_23		AE29	FPI_TDATA_16		AH12	No Connect
	AA30	FPI_TSOC		AE30	FPI_TDATA_17		AH13	No Connect
AB	AB1	FPI_RDATA_0	AF	AF1	FPI_TCA		AH14	No Connect
	AB2	FPI_RDATA_1		AF2	GTX_CLK1		AH15	VDDCORE
	AB3	VDDCORE		AF3	VDDCORE		AH16	No Connect
	AB28	VDDCORE		AF28	VDDPAD		AH17	GND
	AB29	GND		AF29	GND		AH18	VDDPAD
	AB30	FPI_TDATA_22		AF30	GND		AH19	GND

Table 23 M-5 CA Pin Assignments (continued)

ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION	ROW	PIN #	FUNCTION
AH	AH20	No Connect	AJ	AJ20	RXCLK0	AK	AK20	FPI_TPRTY
	AH21	VDDPAD		AJ21	FPI_TDATA_1		AK21	FPI_TDATA_0
	AH22	GND		AJ22	FPI_TDATA_3		AK22	FPI_TDATA_2
	AH23	No Connect		AJ23	FPI_TDATA_5		AK23	FPI_TDATA_4
	AH24	VDDPAD		AJ24	FPI_TDATA_7		AK24	FPI_TDATA_6
	AH25	GND		AJ25	FPI_TENB		AK25	GMII1_RXDV
	AH26	VDDCORE		AJ26	FPI_TDATA_8		AK26	RXCLK1
	AH27	VDDPAD		AJ27	FPI_TDATA_10		AK27	FPI_TDATA_9
	AH28	GND		AJ28	FPI_TDATA_12		AK28	FPI_TDATA_11
	AH29	FPI_TDATA_15		AJ29	GND		AK29	FPI_TDATA_13
	AH30	GMII2_RXDV		AJ30	FPI_TDATA_14		AK30	GND
AJ	AJ1	FPI_RDATA_11	AK	AK1	GND			
	AJ2	GND		AK2	FPI_RDATA_12			
	AJ3	FPI_RDATA_13		AK3	FPI_RDATA_14			
	AJ4	FPI_RDATA_15		AK4	GMII2_TXEN			
	AJ5	GTX_CLK2		AK5	FPI_RDATA_16			
	AJ6	FPI_RDATA_18		AK6	FPI_RDATA_17			
	AJ7	FPI_RDATA_19		AK7	FPI_RDATA_20			
	AJ8	FPI_RDATA_21		AK8	FPI_RDATA_22			
	AJ9	FPI_RDATA_23		AK9	FPI_RSOC			
	AJ10	GTX_CLK3		AK10	FPI_RDATA_24			
	AJ11	FPI_RDATA_25		AK11	FPI_RDATA_26			
	AJ12	FPI_RDATA_27		AK12	FPI_RDATA_28			
	AJ13	FPI_RDATA_29		AK13	FPI_RDATA_30			
	AJ14	FPI_RDATA_31		AK14	RESETB			
	AJ15	SCAN		AK15	M5CLK			
	AJ16	No Connect		AK16	VDDANA			
	AJ17	GND		AK17	TPA_ANA			
	AJ18	SICL		AK18	GNDANA			
	AJ19	GMII0_RXDV		AK19	SIDA			

Chapter 3

ELECTRICAL SPECIFICATIONS

DC Electrical Characteristics

The figures and tables in this section describe the DC electrical characteristics of the M-5 CA.

Table 24 Absolute Maximum Ratings

SYMBOL	CHARACTERISTIC[1]	MIN	MAX	UNIT
V_{DD}	Core Supply Voltage	-0.3	2.2	V
AV_{DD}	PLL Supply Voltage	-0.3	2.2	V
OV_{DD}	LVTTL I/O Supply Voltage	-0.3	4.0	V
V_{in}	LVTTL Input Voltage[2, 3]	-0.3	4.3	V
T_{stg}	Storage Temperature Range	-55	150	°C
ESD_{tol}	ESD Tolerance[4]	2,000	-	V

1 Functional and tested operating conditions are given in Table 25. Absolute maximum ratings are stress ratings only, and functional operation at the maximums are not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 Caution: LVTTL V_{in} must not exceed OV_{DD} by more than 0.3V at any time, including during power-up.

3 Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.2V at any time, including during power-up.

4 ESD tolerance is stated for Human Body Model, all pins.

Table 25 Recommended Operating Conditions

SYMBOL	CHARACTERISTIC[1]	MIN	MAX	UNIT
V_{DD}	Core Supply Voltage[2]	1.65	1.95	V
AV_{DD}	PLL Supply Voltage	1.65	1.95	V
OV_{DD}	LVTTL I/O Supply Voltage	3.0	3.6	V
V_{in}	LVTTL Input Voltage	0	3.6	V
T_J	Junction Temperature	-40	105	°C

1 These are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 Recommended supply power-up order is V_{DD}, AV_{DD},, OV_{DD} , however, any order is acceptable as long as Absolute Maximum Ratings are not exceeded.

Table 26 DC Electrical Specifications

SYMBOL	CHARACTERISTIC[1]	MIN	MAX	UNIT
V_{IH}	LVTTL Input High Voltage	2.0	-	V
V_{IL}	LVTTL Input Low Voltage	-	0.8	V
I_{IH}	LVTTL Input Leakage Current, V_{in}=V_{DD}	-	5	µA
I_{IL}	LVTTL Input Leakage Current, V_{in}=GND	-	5	µA
C_{in}	LVTTL Input Capacitance	-	10	pF
V_{hys}	Schmitt Trigger Hysteresis	500	-	mV
V_{OH}	LVTTL Output High Voltage, I_{OH}= -8 mA	2.4	-	V
V_{OL}	LVTTL Output Low Voltage, I_{OL}= 8 mA	-	0.4	V
P_{DCore}	Core Supply Power Dissipation	-	2.7	W
P_{DPLL}	PLL Supply Power Dissipation	-	0.2	W
P_{DIO}	LVTTL I/O Supply Power Dissipation	-	0.7	W

1 V_{DD} = AV_{DD} = 1.8 + 0.15V dc, OV_{DD} = 3.3 + 0.3V dc, GND = 0V dc, -40 < T J < 105 °C.

Table 27 Thermal Specifications

SYMBOL	CHARACTERISTIC		VALUE	UNIT
$R_{\theta JA}$	Junction to Ambient Natural Convection[1,2]		18.4	°C/W
$R_{\theta JMA}$	Junction to Ambient Natural Convection[1,3]	Four layer board (2s2p)	13.0	°C/W
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min)[1,3]	Single layer board (1s)	13.0	°C/W
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min)[1,3]	Four layer board (2s2p)	9.7	°C/W
$R_{\theta JB}$	Junction to Board[4]		6.2	°C/W
$R_{\theta JC}$	Junction to Case[5]		1.1	°C/W
Ψ_{JT}	Junction to Package Top[6]	Natural Convection	1.1	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3 Per JEDEC JESD51-6 with the board horizontal.
4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate used for case temperature.
6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

AC Electrical Characteristics

The figures and tables in this section describe the AC electrical characteristics of the M-5 CA. All of the input and outputs of the M-5 CA are 3.3V LVTTL compatible. The MDIO/low speed serial interface signals have Schmitt triggered inputs. Specifications are stated for T_j = -40 °C to 105 °C, V_{DD} = AV_{DD} =1.8 + 0.15V dc, OV_{DD} = 3.3+0.3V dc, and rise and fall time of 1.5 ns of all input signals; except where explicitly counter indicated.

M-5 CA Reference Clock Timing Specification

See Figure 4. The M-5 CA Reference Clock is the master clock of the device and is used to drive the M-5 CA PLL. The UL3 (UTOPIA Level 3), PL3 (SATURN POS-PHY Level 3 and a UL3L (UTOPIA Level 3 - Like) (UL3/PL3/UL3L) interface timing is specified relative to this clock input.

Figure 4 M-5 CA Reference Clock

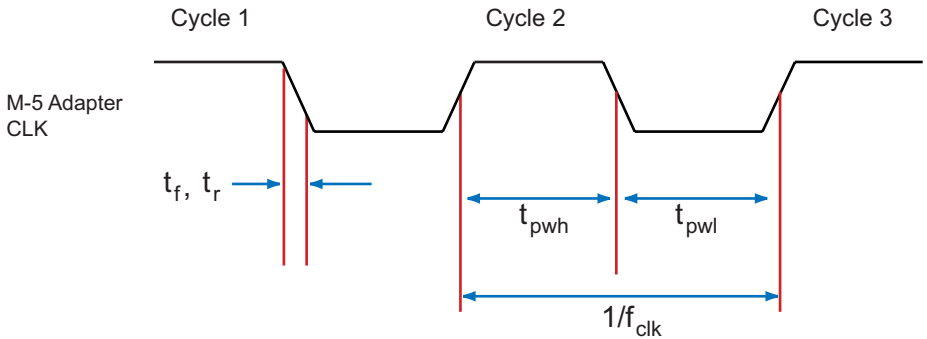


Table 28 M-5 CA Reference Clock AC Specification

SYMBOL	CHARACTERISTIC	MIN	MAX
f_{clk}	Clock Frequency	66 MHz	104 MHz
t_{pwh}/t_{pwl}	Clock Pulse Width High/Low[1]	3.85 ns	-
t_r/t_f	Clock Rise/Fall Time[2]	-	2.0 ns
t_{lock}	PLL Lock Time[3]	-	2048 clocks + 50 µs

1 Measured between 50-50% points.
2 Measured between 10-90% points.
3 Lock time after compliant M5CLK signal applied.

UTOPIA Level 3, SATURN POS-PHY Level 3 and UTOPIA Level 3-Like (PL3/UL3/UL3L)

See Figure 5. The M-5 CA supports UL3 (UTOPIA Level 3) and PL3 (SATURN POS-PHY Level 3) framer interfaces and a UL3L (UTOPIA Level 3-Like) C-5e NP system interface. These interfaces have identical timing attributes with the only exception being the output load at which timing is specified. The more demanding load of 30pF is used for specification.

Figure 5 PL3/UL3/UL3L Interface

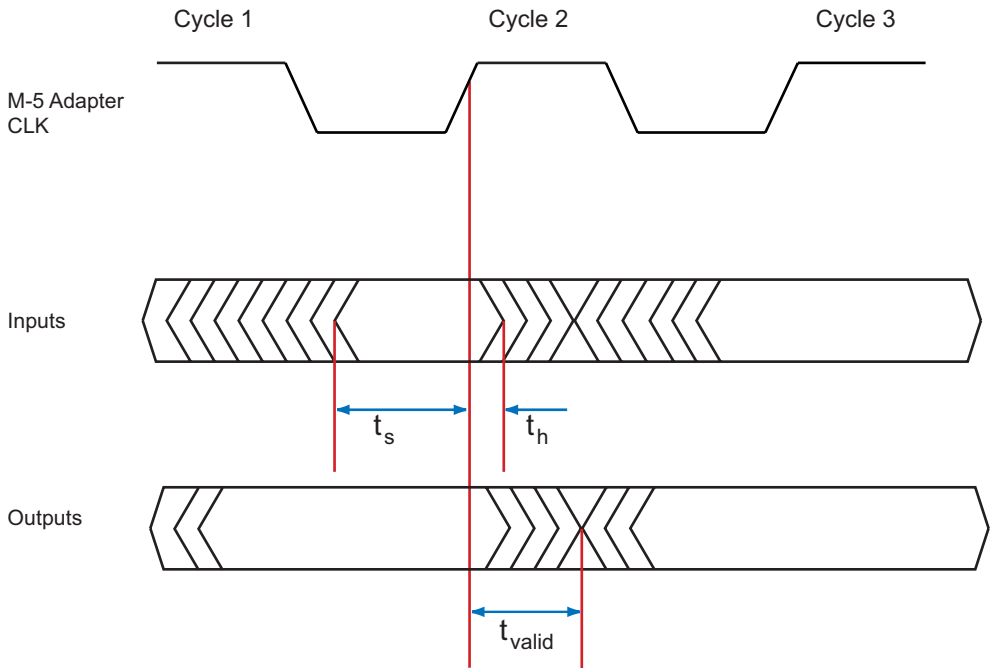


Table 29 PL3/UL3/UL3L AC Specification

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_s	Input setup time to rising edge of M5CLK[1]	2.0	-	ns
t_h	Input hold time to rising edge of M5CLK[1]	0.5	-	ns
t_{valid}	Output valid time after rising edge of M5CLK[1,2,3]	1.5	6.0	ns

1 Measured between 50-50% points.
2 UL3 specification is 0 ns minimum, PL3 specification is 1.5 ns minimum which is used for M-5 CA.
3 Timing specified for 30pF output load.

Gigabit Ethernet Media Independent Interface (GMII)

See Figure 6. The M-5 CA supports a GMII C-5e NP interface. The GMII interface AC specifications do not meet the IEEE 802.3 specifications, but are rather designed to interoperate as a point-to-point interface with the C-5e NP. The RXDV, RXD and COL M-5 CA output signals are synchronous to the falling edge of the receiver interface clock, RXCLK, to meet the C-5e NP input hold time requirements. The GMII source-synchronous interfaces operate at the same frequency as the M-5 CA master clock, but have an arbitrary bounded phase relationship.

Figure 6 Gigabit Ethernet Media Independent Interface (GMII)

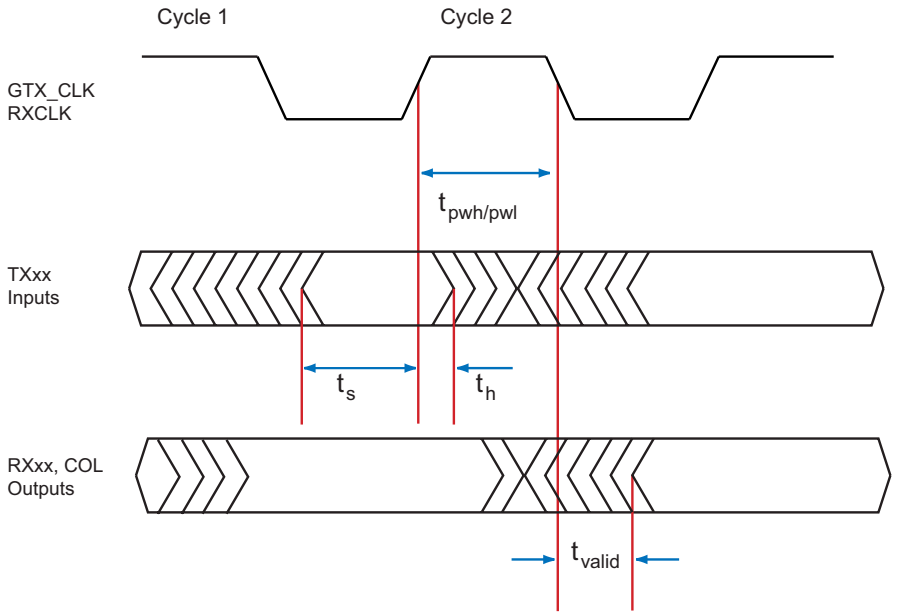


Table 30 GMII AC Specification

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{pwh}/t_{pwl}	Clock pulse width high/low[1]	3.85	-	ns
t_s	Input setup time to rising edge of GTX_CLK[1]	2.0	-	ns
t_h	Input hold time to rising edge of GTX_CLK[1]	0.0	-	ns

Table 30 GMII AC Specification (continued)

t_{valid}	Output valid time after falling edge of RXCLK[1,2,3]	-1.0	1.0	ns
Φ_{drift}	Phase drift tolerance between GTX_CLK and M5CLK[4, 5]	-360	360	degrees

1 Measured between 50-50% points.
2 Provides an equivalent output valid time of 3.8 ns min, 5.8 ns max relative to the rising edge of RXCLK at 104 MHz.
3 Timing specified for 30pF output load.
4 After compliant M5CLK signal applied and reset deasserted.
5 Not tested but guaranteed by design.

Management Data Input/Output (MDIO)

See Figure 7 on page 42. The MDIO interface follows the IEEE 802.3 Standard protocol but does not have the same AC characteristics. IEEE 802.3 specifies an interface that operates at a minimum period of 400 ns and utilizes an open-drain driver with passive pull-up. The M-5 CA MDIO must work with the C-5e NP MDIO that operates at a minimum period of 40 ns and utilizes a LVTTL three state driver. Although, the interface is compliant with IEEE 802.3 Standard AC characteristics with the exception of an external pull-up resistor and reduction of the cycle time to 40ns.

Figure 7 MDIO Interface

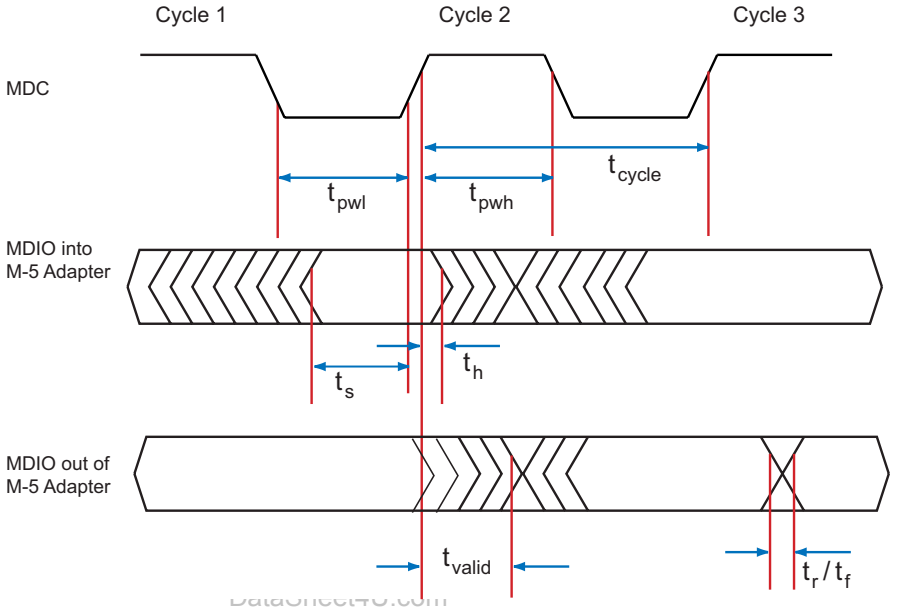


Table 31 MDIO AC Specification

SYMBOL	CHARACTERISTIC[1]	MIN	MAX	UNIT
t_{cycle}	MDC cycle time	40	-	ns
t_{pwh}/t_{pwl}	MDC pulse width high/low	16	-	ns
t_s	Input setup time to rising edge of MDC	10	-	ns
t_h	Input hold time to rising edge of MDC	0.0	-	ns
t_r/t_f	MDIO rise and fall time[2]	-	15.5	ns
t_{valid}	Output valid time after rising edge of MDC[2]	0	20	ns
t_{valid}	Output valid time after rising edge of MDC[3]	-	75	ns

1 All timing measured relative to V_{IL} and V_{IH} points.
2 Timing for minimum cycle time operation with 10pF to 100pF load.
3 Timing for IEEE 802.3 compliant load of 470pF; minimum cycle time operation is not possible. Not tested but guaranteed by design.

Low Speed Serial Bus (LSP)

Figure 8 on page 43. The M-5 CA Low Speed Serial Bus (LSB) slave interface works with the C-5e NP low speed serial bus master interface and other slave devices on the bus. Operation to 400kHz is supported.

Figure 8 LSP Interface

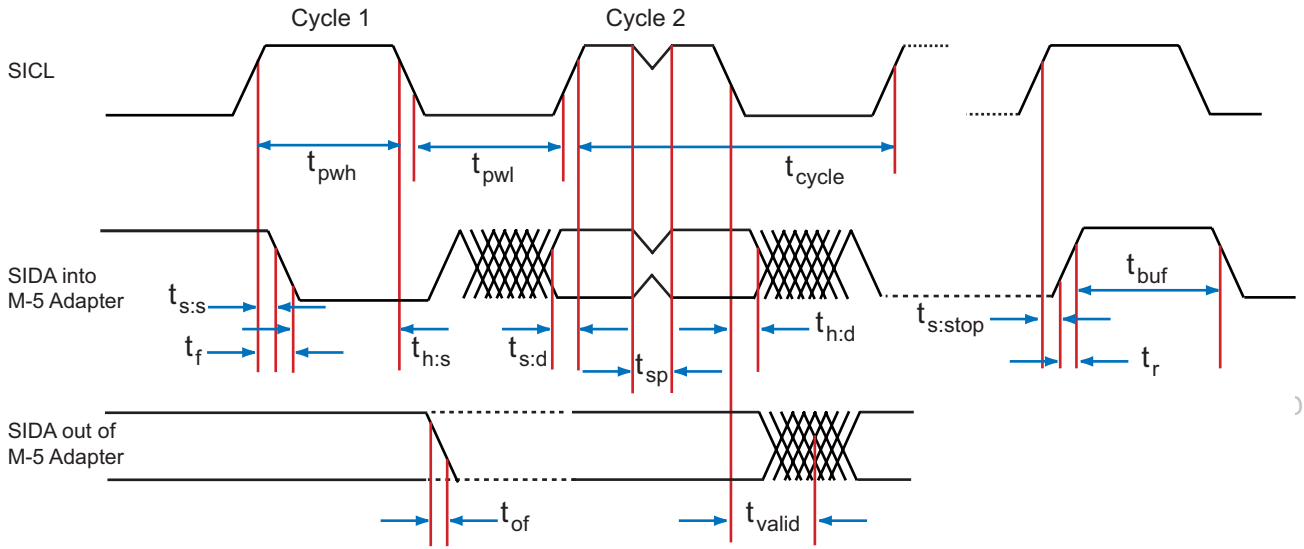


Table 32 Low Speed Serial Bus AC Specification

SYMBOL	CHARACTERISTIC[1, 2]	MIN	MAX	UNIT
t_{cycle}	SICL cycle time	2500	-	ns
t_{pwh}	SICL pulse width high	600	-	ns
t_{pwl}	SICL pulse width low	1300	-	ns
t_r/t_f	Input rise and fall time	2	300	ns
t_{of}	Output fall time[3]	2	60	ns
$t_{s:s}$	Input setup time for repeated START condition	600	-	ns
$t_{h:s}$	Input hold time for repeated START condition	600	-	ns
$t_{s:d}$	Input setup time for data	100	-	ns
t_{sp}	Pulse width of spike that must be suppressed by the input filter	0	50	ns

Table 32 Low Speed Serial Bus AC Specification (continued)

SYMBOL	CHARACTERISTIC[1, 2]	MIN	MAX	UNIT
$t_{h:d}$	Input hold time for data	0	-	ns
$t_{s:stop}$	Input setup time for STOP condition	600	-	ns
t_{buf}	Bus free time between a STOP and START condition	1250	-	ns
t_{valid}	Output valid time	0	350	ns

1 All timing measured relative to V_{IL} and V_{IH} points.
2 Timing with 10pF to 400pF output load (C_L).
3 M-5 CA does not meet the slew-controlled Min fall time equal to 20+0.1*C_L.

JTAG See Figure 9. The M-5 CA has an IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture compliant implementation.

Figure 9 JTAG Interface

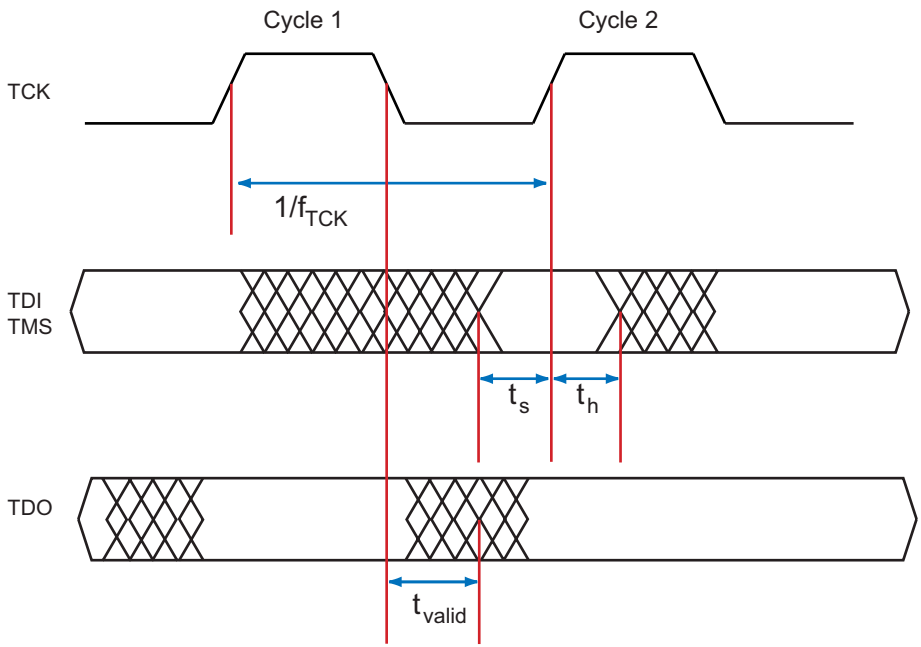


Table 33 JTAG AC Specification

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{valid}	Output valid time after falling edge of TCK[1,2]	1.0	8.0	ns
t_s	Setup time to rising edge of TCK[1]	15.0	-	ns
t_h	Hold time to rising edge of TCK[1]	15.0	-	ns
f_{TCK}	TCK frequency	-	20	MHz
f_D	TCK duty cycle	35	65	%
R_{PU}	Pull-up impedance to OV_{DD}[3]	74	135	kΩ

1 Measured between 50-50% points.
2 Timing specified for 10pF output load.
3 Internal pull-ups on TDI, TMS and TRSTB.

Chapter 4

MECHANICAL SPECIFICATIONS

Package Views

The M-5 CA is an adapter ISA 324 pin Tape Ball Grid Array (TBGA). Figure 10 and Figure 11 and Table 34 show the package measurements.

Figure 10 M-5 CA TBGA Package Side View

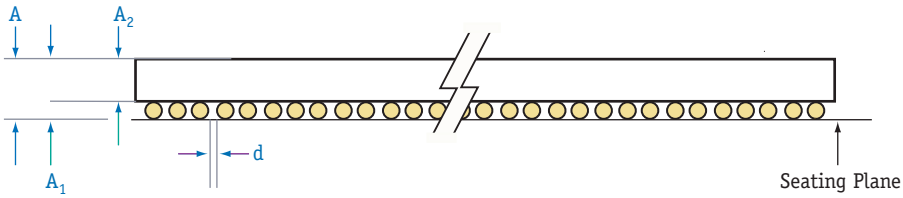
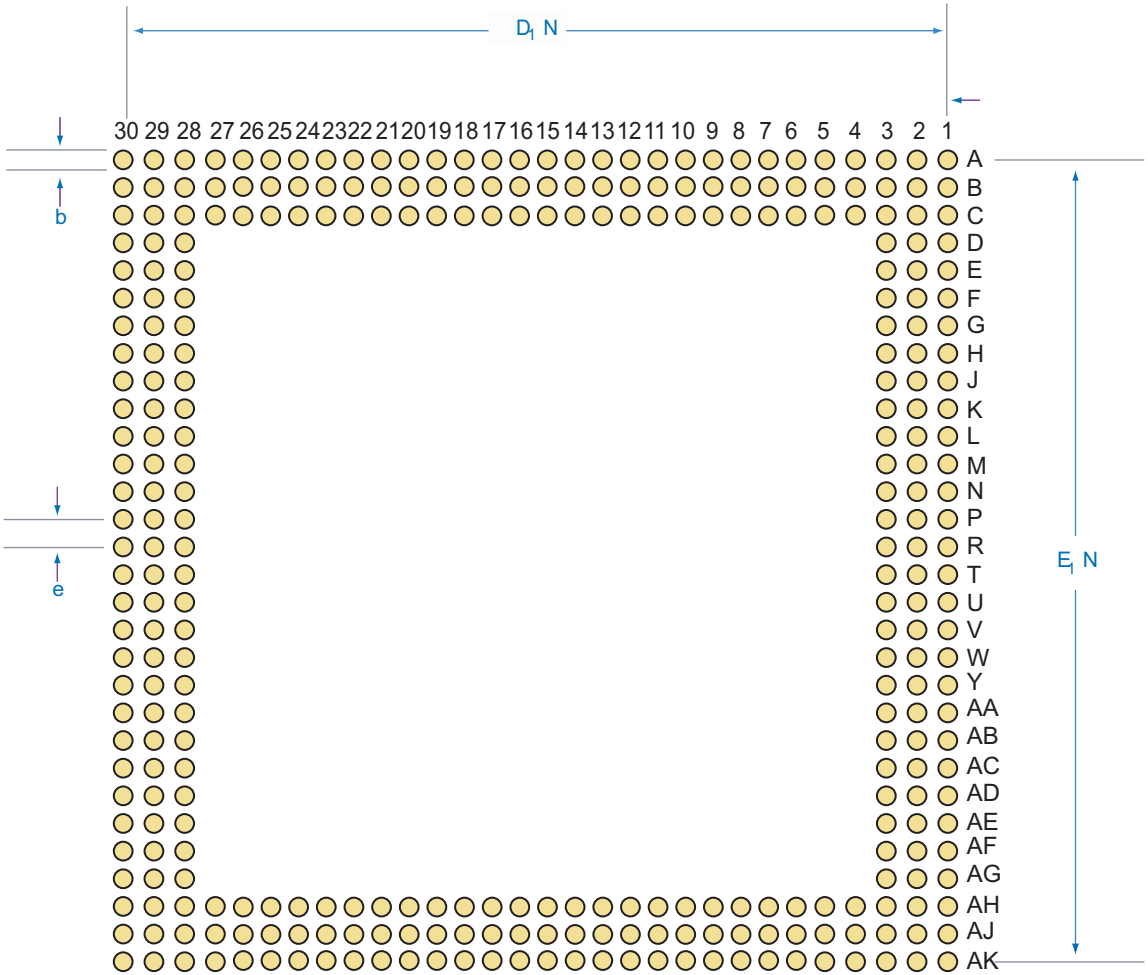


Figure 11 M-5 CA TBGA Package (Bottom View)



Package Measurements

Table 34 defines the M-5 CA package measurements, providing nominal, minimum, and maximum sizes where appropriate. See Figure 10 and Figure 11 for Symbols.

Table 34 M-5 CA Package Measurements

SYMBOL	DEFINITION	NOM. (MM)	MIN. (MM)	MAX. (MM)
A	Overall	1.65	1.20	
A_1	Ball height	0.60	0.40	
A_2	Body thickness	1.05	0.80	
b	Ball diameter	0.63	0.50	0.70
D	Body size	31		
D_1	Ball footprint (X)	29		
e	Ball pitch	1.00		
E	Body size	31		
E_1	Ball footprint (Y)	29		
N	Ball Matrix	30 x 30		

Marking Codes

Table 35 explains the marking on the M-5 CA.

Table 35 M-5 CA Marking Codes

MARKING (EXPLANATION OF CODES)	
Top	Logo/Part#/Country of Origin/Date Code
Bottom	N/A
Pin 1 Marking	Pin 1 has a solid dot in the A1 ball location marked on the package.

Reflow

Typical Reflow Profile for the M-5 CA is described below.

- No minimum solder paste volume is required since the solder ball melts during reflow.
- TBGA has a high thermal mass and should be carefully profiled.
- Suggested profile (somewhat flux-dependent):
  - Qualified to a maximum reflow temperature of 220°C -0/+5.
  - Raise temperature of the joints to 100°C in 50 secs or less.
  - Peak component temperature typically between 205 and 220°C.
  - Desirable dwell time above 183°C between 50 and 80 secs.

This is a general guideline and should be modified as needed by the reflow vendor.

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MOTOROLA

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