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## Stand-Alone USB Type-C™ Power Delivery 3.1 Controller

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### Features

- Programmable USB Type-C™ (1) Power Delivery (PD) Solution for Source-only, Sink-only, Dual Role Power, and Dual Role Data Applications
  - Companion device for USB Power Delivery Stack (PDS)
  - Fully Customizable Software
  - Standard Power Delivery Power Profiles (15/27/45/60/100W) Supported with No Software Modification
  - USB Power Delivery 3.1 Compliant MAC
  - USB Type-C™ Connector Support with Connection Detection and Control
  - Integrated Analog Discrete Components Reduce Bill of Materials and Design Footprint
  - Easily Supports One Additional Power Delivery Port via MCP22350 Add-on
  - Industrial Temperature Support
- 32-bit ARM Cortex-M0+ CPU
    - 64 KB Flash, 8 KB RAM
  - Optional Two Port Solution via External MCP22350
    - SPI for external MCP22350 communication
    - Power delivery firmware controls all ports
  - Integrated Analog Discrete Components
    - VCONN FETs with Rp/Rd switching
    - Dead battery Rd termination (MCP22301-2 Only)
    - Programmable current sense for overcurrent conditions
    - Voltage sense for overvoltage conditions
  - USB Power Delivery MAC
    - Compliant with USB Power Delivery Specification Revision 3.1
    - Power Delivery Packet Framing
    - CRC Checking/Generation
    - 4B/5B Encoding/Decoding
    - BMC Encoding/Decoding
    - EOP/SOP Generation for PD Frames
    - SOP Detection and SOP Header Processing
    - Separate RX/TX FIFOs
    - Automatic GoodCRC Message Generation
    - Automatic Retry Generation
    - Error Handling
    - Low Standby Power Support
  - USB Type-C Cable Detect Logic
    - Auto Cable Attach and Orientation Detection
    - Routes Baseband Communication to Respective CC Pin per Detected Orientation
    - VCONN Supply Control for Active Cable
    - Charging Current Capability Detection
  - Power and I/Os
    - Integrated 1.8V Voltage Regulator
    - 10 Configurable General Purpose I/O Pins
  - Package
    - 40-VQFN (6.0 mm × 6.0 mm)
  - Environmental
    - Industrial Temperature Range (-40°C to +85°C)

### Target Applications

- Point-of-Sale Terminals
- Charging Lockers
- IoT Products and Sensors
- Smart Speakers and Monitors
- Conference Systems
- Power Tools
- Multi-port Charging Docks

### Key Benefits

- Fully Customizable Power Delivery Firmware
  - Industry standard MPLABX development and programming environment
  - Supports all standard power delivery profiles (15/27/45/60/100W) and custom profiles
  - Supports Dual Role Port (DRP) operation
  - Supports Alternate Mode operation
  - Power Delivery Stack (PDS) enables customized PD applications

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1. USB Type-C™ and USB-C™ are trademarks of USB Implementers Forum.

# MCP22301

## 1.0 PREFACE

### 1.1 Glossary of Terms

**TABLE 1-1: GLOSSARY OF TERMS**

Term	Definition
<b>BCI</b>	Baseband CC interface
<b>Billboard</b>	USB Billboard Device. A required USB device class for UFPs which support Alternate Modes in order to provide product information to the USB Host.
<b>BIST</b>	Built-in Self Test
<b>BMC</b>	Bi-phase Mark Coding
<b>Byte</b>	8 bits
<b>CC</b>	Generic reference to USB Type-C™ Cable / Connector CC1/CC2 Pins
<b>CSR</b>	Control and Status Register
<b>DFP</b>	Downstream Facing Port (USB Type-C™ Specification Definition)
<b>DP</b>	DisplayPort (a VESA standard interface)
<b>DRP</b>	Dual-role Power
<b>ESD</b>	Electro-static Discharge
<b>FIFO</b>	First-in, First-out buffer
<b>GPIO</b>	General Purpose Input/Output
<b>Host</b>	External System (includes processor, application software, etc.)
<b>HBM</b>	Human Body Model (simulates ESD from humans)
<b>HS</b>	High-speed
<b>LDO</b>	Linear Drop-out Regulator
<b>MAC</b>	Media Access Controller
<b>Microchip</b>	Microchip Technology Incorporated
<b>N/A</b>	Not Applicable
<b>NC</b>	No Connect (pin)
<b>OCS</b>	Over-current Sense
<b>PD / UPD</b>	USB Power Delivery
<b>PDO</b>	Power Delivery Object (USB PD Specification definition). PDOs enable the port to indicate its Port Partner supported combinations of Voltage/Current or Power as well as the type of supply (Fixed, Variable, Battery) in Source Role or Sink Role.
<b>PIO</b>	General Purpose I/O
<b>POR</b>	Power-on Reset
<b>Port Partner</b>	Remote port which is connected to the MCP22301's local port
<b>PRBS</b>	Pseudo Random Binary Sequence
<b>Source Role</b>	USB Type-C port sinking power from its Port Partner
<b>Source-only Operation</b>	Operation exclusively in USB Type-C / Power Delivery Source Role as defined in the USB Type-C and Power-Delivery specifications. In this mode of operation, USB Type-C Dual-Role Power Operation is not supported, and there is no support for USB Power Role Swap.
<b>SPI</b>	Serial Peripheral Interface
<b>SS</b>	SuperSpeed
<b>Stand-alone Mode</b>	Chip operation without the control or configuration by an external MCU. Policy is defined locally by the MCP22301 firmware. Configuration is achieved by use of configuration straps.
<b>UFP</b>	Upstream-facing Port (USB Type-C™ specification definition)
<b>USB</b>	Universal Serial Bus

TABLE 1-1: GLOSSARY OF TERMS (CONTINUED)

Term	Definition
<b>USB Power Delivery Operation</b>	Port is operating using USB Power Delivery protocols in conformance to the USB PD Specification.
<b>USB Power Role Swap</b>	Message sequence as defined in the USB PD Specification, enabling a transition between Source Role and Sink Role during USB Power Delivery Operation
<b>USB Type-C™</b>	USB Type-C™ Cable / Connector

## 1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input
IS	Schmitt-triggered Input
O2	Output with 2 mA sink and 2 mA source
OD2	Open-drain output with 2 mA sink and 2 mA source
O8	Output with 8 mA sink and 8 mA source
PD	200 kΩ (typical) internal pull-down. <b>Note:</b> Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog Input
AO	Analog Output
AIO	Analog Bi-directional
P	Power Pin

**Note:** Refer to [Section 5.4, "DC Characteristics," on page 28](#) for the electrical characteristics of the various buffers.

## 1.3 References

- Microchip MCP22350 data sheet: <https://ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/MCP22350-Integrated-Small-Form-Factor-USB-Type-C-Data-Sheet-DS20006885.pdf>
- Microchip SAM D20 device family data sheet: [http://ww1.microchip.com/downloads/en/DeviceDoc/SAM\\_D20\\_%20Family\\_Datasheet\\_DS60001504\\_C.pdf](http://ww1.microchip.com/downloads/en/DeviceDoc/SAM_D20_%20Family_Datasheet_DS60001504_C.pdf)
- USB Power Delivery documents: <https://www.usb.org/document-library/usb-power-delivery>
- USB Type-C™ Specification: <https://www.usb.org/usb-type-cr-cable-and-connector-specification>

# MCP22301

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## 2.0 INTRODUCTION

### 2.1 General Description

The MCP22301 is a stand-alone, small form factor USB Type-C™ Power Delivery (PD) Port Controller designed to adhere to the *USB Type-C™ Cable and Connector Specification* and *USB Power Delivery 3.1 Specification*. The MCP22301 provides stand-alone operation for a wide range of PD applications, enabling cable plug orientation and detection for a USB Type-C receptacle, and implementing baseband communication with a partner USB Type-C device via the integrated USB Power Delivery 3.1 MAC.

The MCP22301 is an integrated PD solution with SAMD20 (32-bit ARM Cortex-M0+) microcontroller and MCP22350 PD MAC/PHY functionality. The embedded 32-bit ARM Cortex-M0+ can execute the USB Power Delivery Stack (PDS). Optionally, a second PD port is supported via SPI connection of additional external Microchip MCP22350 devices. The MCP22301 devices are shipped blank and require programming with compiled application specific code before operation.

Additionally, the MCP22301 integrates many of the analog discrete components required for USB Type-C PD applications, including two VCONN FETs with Rp/Rd switching and current/voltage sense circuitry for over-voltage/current detection. By integrating the PD firmware and many of the analog discrete components required for USB Type-C PD applications, the MCP22301 provides a low cost, stand-alone, fast time-to-market solution for consumer and industrial applications.

The Microchip MCP22301 family includes the following devices:

- MCP22301-1, without dead battery support in hardware
- MCP22301-2, with dead battery support in hardware

The MCP22301 is available in industrial temperature range.

### 2.2 USB Power Delivery Stack (PDS)

The PDS firmware stack allows for a wide range of USB Power Delivery applications, including but not limited to: Single or Multi-Port source Only applications, Bus-Powered Sink applications, Battery-Powered Sink applications, and Dual Role Data / Dual Role Power applications such as PD-based docking stations or PD-based dongles.

The PDS firmware stack is continuously deployed. Not all features that are able to be supported by the MCP22301 device are necessarily supported by PDS. The supported features may be expanded over time. The PDS firmware stack can be downloaded from the

MCP22301 product page. Refer to the MCP22301 product page and PDS Online code repository for details on the currently supported feature set and future development road-map. Additional feature development may be requested through Microchip support channels.

### 2.3 Example Applications

The MCP22301 has been designed for multiple applications, including:

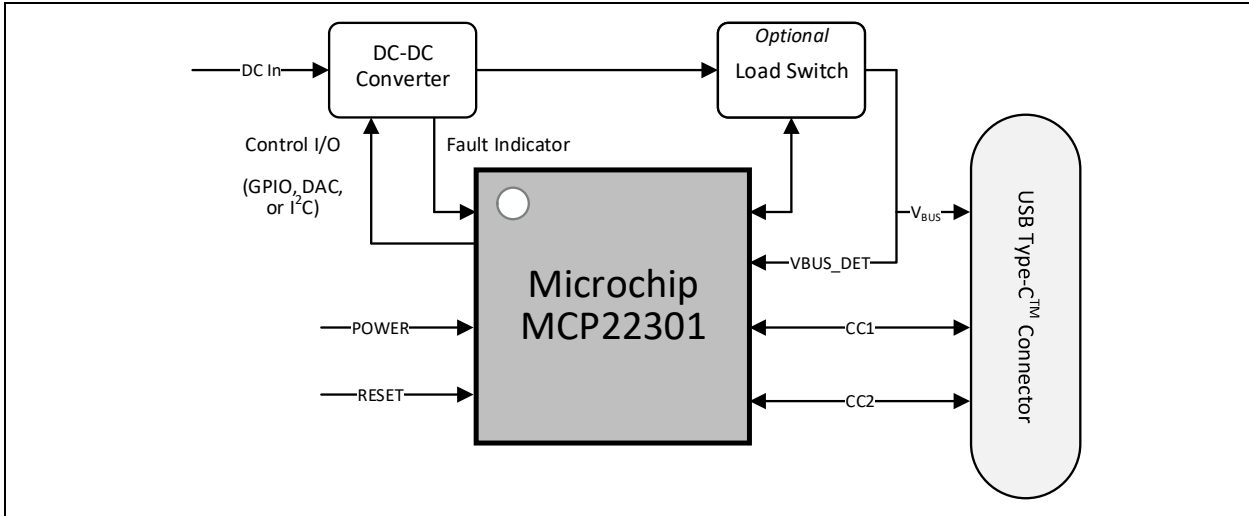
- [Source-Only Applications \(E.G., Charging Ports\)](#)
- [Two-Port Source-Only Applications](#)
- [Bus-Powered or Battery Powered Sink-Only Applications](#)
- [Dual Role Power/Data Application \(5V Source, High Voltage Sink\)](#)
- [Dual Role Power/Data Application \(High Voltage Source, 5V @ 0A Sink\)](#)
- [2-Port Dual Role Power/Data Application 'Charge-Through Adapter'](#)

#### 2.3.1 SOURCE-ONLY APPLICATIONS (E.G., CHARGING PORTS)

The simplest MCP22301 application is a power source (Source-Only), as shown in [Figure 2-1](#). The MCP22301 control I/O configures the DC-DC converter, selecting the output voltage, and controls the load switch to regulate and protect the output voltage. The load switch can also be replaced by discrete FETs and over-current / over-voltage protection circuits.

Additional notes on Source-Only Charging Port Applications:

- Supporting USB data is not required for a Charging Port.
- A Power Source Load Switch is optional for Source-Only ports. Source-Only ports are permitted to maintain a large bulk capacitance on VBUS at all times, even when the port is in the detached state.
- USB3 operation is optional for PD docking ports.

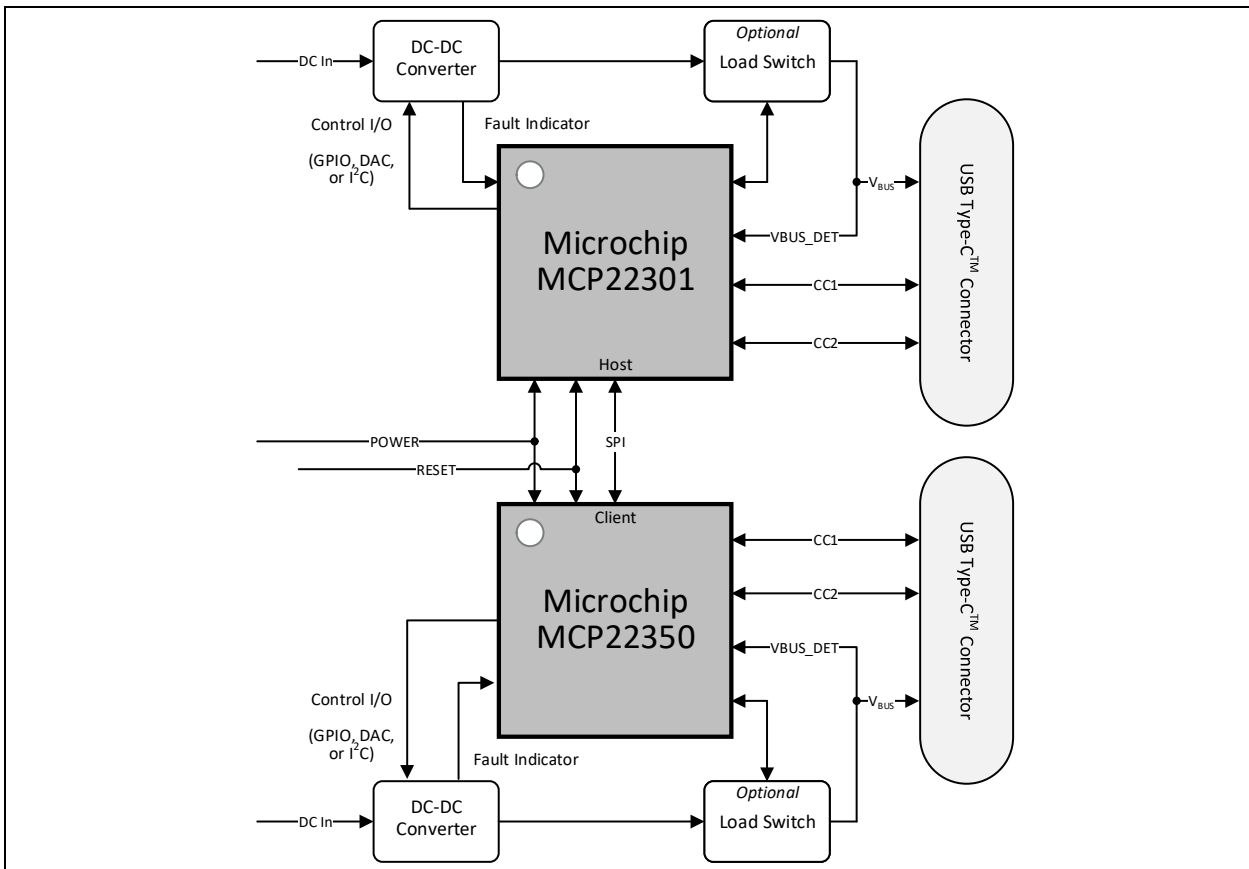


**FIGURE 2-1:** System Block Diagram - Source-Only Application.

### 2.3.2 TWO-PORT SOURCE-ONLY APPLICATIONS

Some applications may need multiple USB Type-C™ power delivery ports. These ports can be implemented by connecting a MCP22301 and a MCP22350 via the

SPI interface, as shown in [Figure 2-2](#). The MCP22301 will execute the stack for the MCP22350. The two-port implementation supports dynamic power allocation (e.g., go-to power min based on an external input).



**FIGURE 2-2:** System Block Diagram - Two-Port Application.

# MCP22301

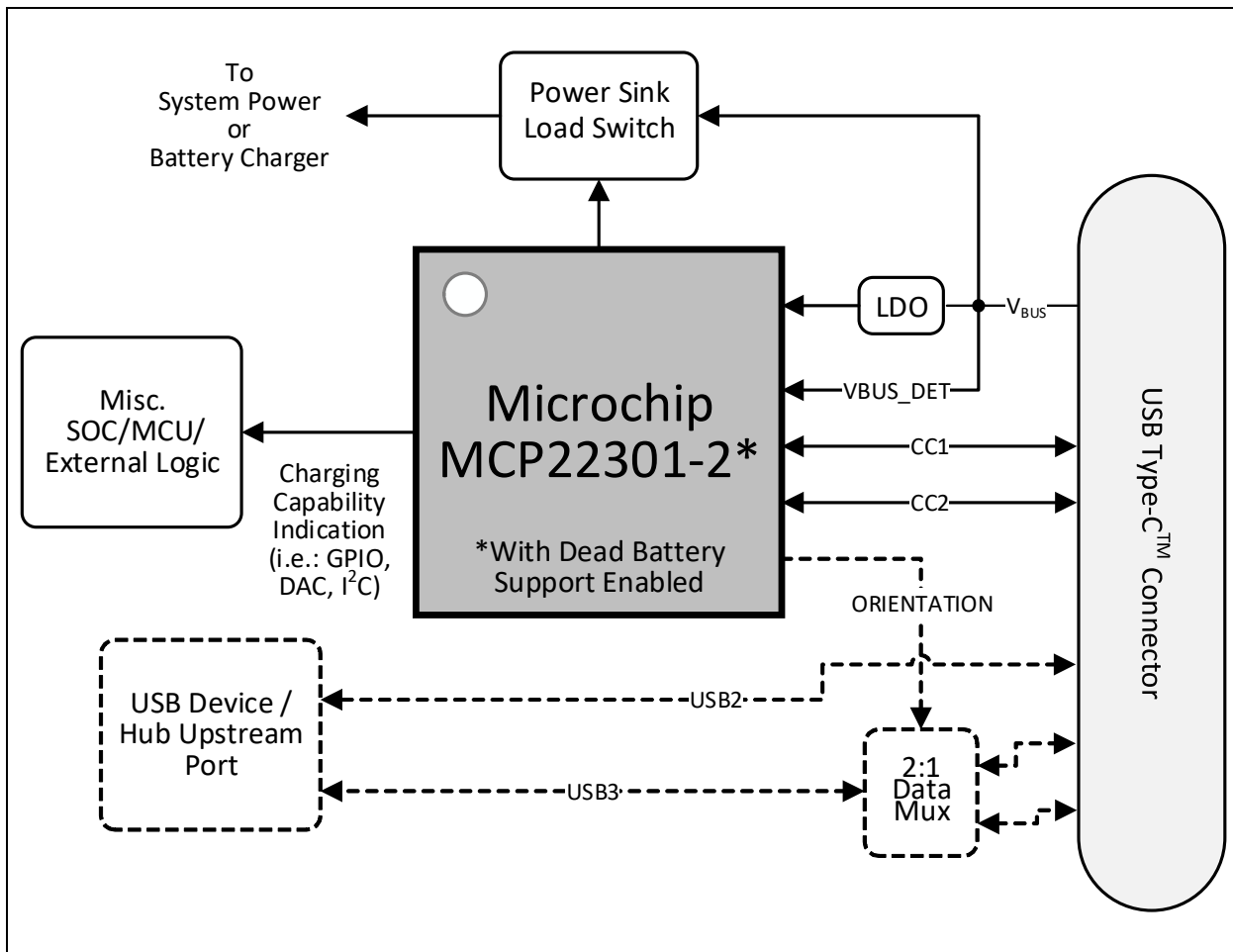
## 2.3.3 BUS-POWERED OR BATTERY POWERED SINK-ONLY APPLICATIONS

An example of a bus powered power sink (Sink-Only) application is shown in Figure 2-3. A bus powered Sink-Only application derives all power from the upstream VBUS connection and does not have any other power source. The MCP22301-2 device with dead battery support should be selected for all Sink-Only devices. The dead battery Rp terminations allow the Sink-Only device to be detected and powered from an attached DFP port when connected in an unpowered state.

Additional notes on Bus-Power or Battery Powered Sink-Only Applications:

- USB data support is optional.
- If USB3 data is supported, a 2:1 multiplexer may be required to handle Type-C cable insertion reversibility. Device controllers and hubs specifically designed to support USB Type-C may also integrate the reversibility functionality.

- USB Alternate Modes may also be supported in Sink-Only applications.
- DisplayPort support is optional for mobile device ports.
- USB2 signals may be connected directly to the Type-C connector; a multiplexer is not necessary as long as the USB2 signal layout is carefully managed to keep branches at a minimum.



**FIGURE 2-3:** System Block Diagram - Sink-Only Application.

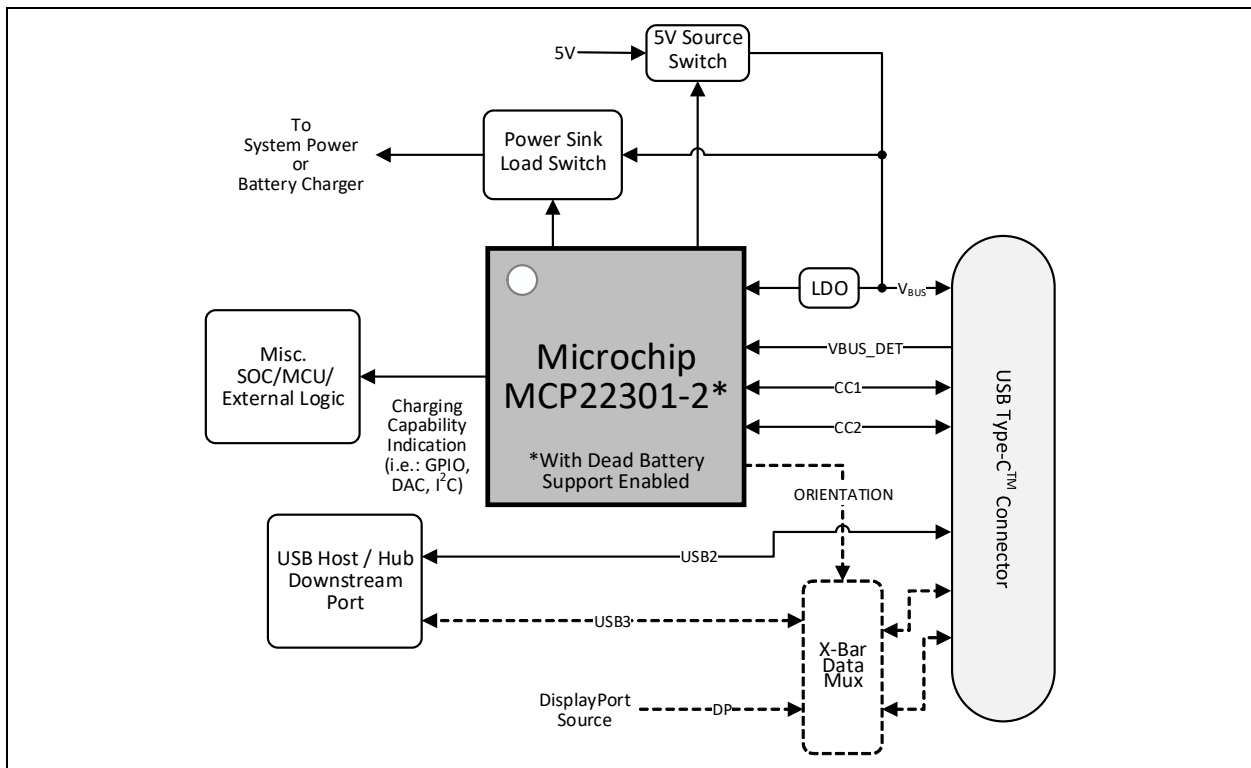
## 2.3.4 DUAL ROLE POWER/DATA APPLICATION (5V SOURCE, HIGH VOLTAGE SINK)

An example of a mobile device port is shown in Figure 2-4. In this example a mobile device, such as a notebook, smart-phone, or tablet, is capable of operating as a USB host (and device if the processor is capable of OTG operation), receiving a charge, and driving an external video display through a single Type-C connection. A cross-bar switch is shown for routing DisplayPort Alternate Mode and USB3 data to the connector, allowing port expansion and video display.

Additional notes on Dual Role Power/Data (5V Source, High Voltage Sink) Applications:

- A typical mobile device will limit the power sourcing capability to 5V only in order to preserve battery life. This is not explicitly required and a mobile device may optionally provide up to the maximum 100W capability if the system supports it.

- When the port is operating as a power sink/data UFP, the USB Host / Hub Downstream Port block is not required to support USB Device / Hub Upstream Port operation.
- A 5V Source Load Switch device must be tolerant of the maximum supported sinking voltage.
- USB3 operation is optional for mobile device ports.
- DisplayPort support is optional for mobile device ports.
- If both USB3 and DisplayPort operation are omitted, the crossbar data switch is not necessary.
- USB2 signals may be connected directly to the Type-C connector; a multiplexer is not necessary as long as the USB2 signal layout is carefully managed to keep branches to a minimum.



**FIGURE 2-4:** System Block Diagram - Dual Role Power/Data Application (5V Source, High Voltage Sink).

# MCP22301

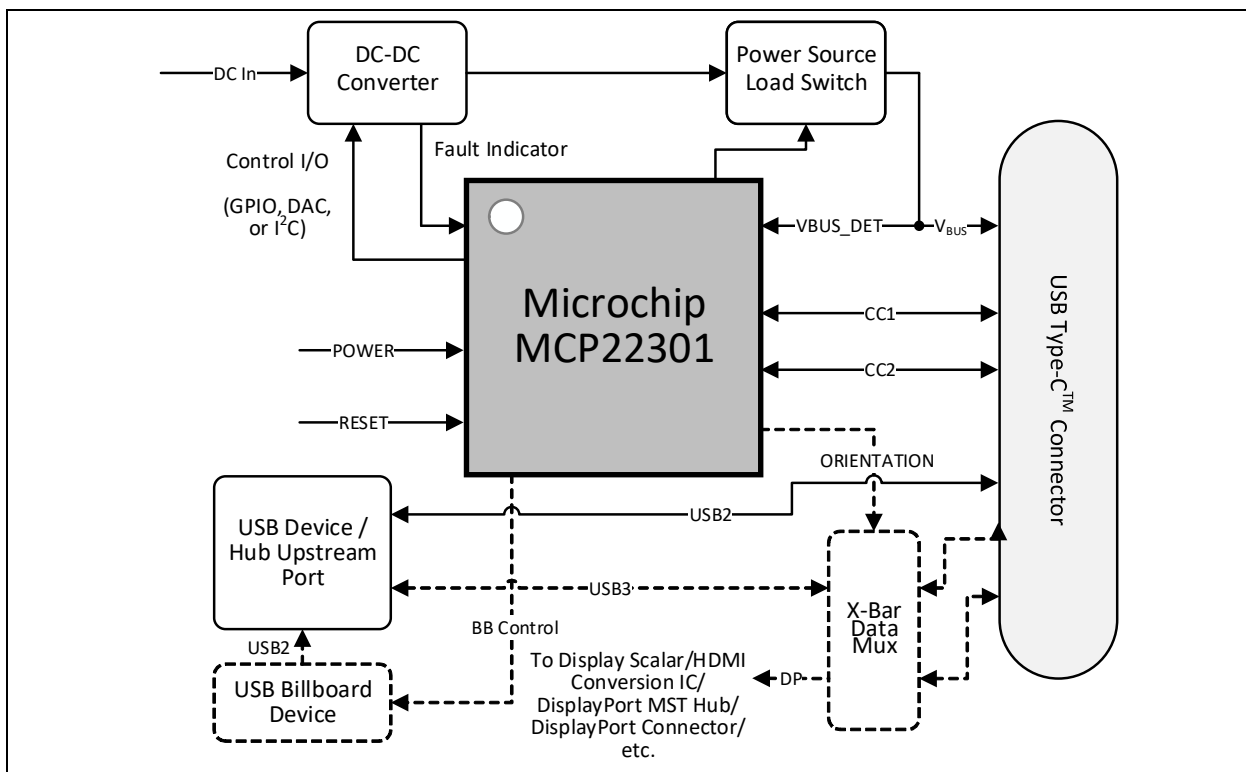
## 2.3.5 DUAL ROLE POWER/DATA APPLICATION (HIGH VOLTAGE SOURCE, 5V @ 0A SINK)

An example of a PD docking port is shown in [Figure 2-5](#). In this example a battery powered mobile device, such as a notebook, smart-phone, or tablet may connect to the docking PD port and receive a charge, access the USB device tree, and drive an external video display through a single Type-C connection. A cross-bar switch is shown for routing DisplayPort Alternate Mode and USB3 data to the connector, allowing port expansion and video display.

Additional notes on Dual Role Power/Data (High Voltage Source, 5V @ 0A Sink) Applications:

- While a PD docking port may technically resolve into a power sink role, a typical PD dock will not attempt to sink any power while operating as a power sink. This type of operation may be referred to a “5V @ 0A Sink”.
- When the port is operating as a power sink/data UFP, the USB Device/Hub Upstream Port block is not required to support USB Host/Hub Downstream Port operation.

- A Power Source Load Switch device is necessary, as the DC-DC converters bulk capacitance must be isolated from VBUS when the port is operating as a 5V @ 0A Sink.
- USB3 operation is optional for PD docking ports.
- DisplayPort support is optional for PD docking ports.
- If an Alternate Mode such as DisplayPort is supported, a Billboard device must also be included within the system and be exposed following an Alternate Mode negotiation failure (A Billboard device may optionally be connected at all times and communicate a successful Alternate Mode connection, but this is optional).
- If both USB3 and DisplayPort operation are omitted, the crossbar data switch is not necessary.
- USB2 signals may be connected directly to the Type-C connector; a multiplexer is not necessary as long as the USB2 signal layout is carefully managed to keep branches to a minimum.



**FIGURE 2-5:** System Block Diagram - Dual Role Power/Data Application (High Voltage Source, 5V @ 0A Sink).

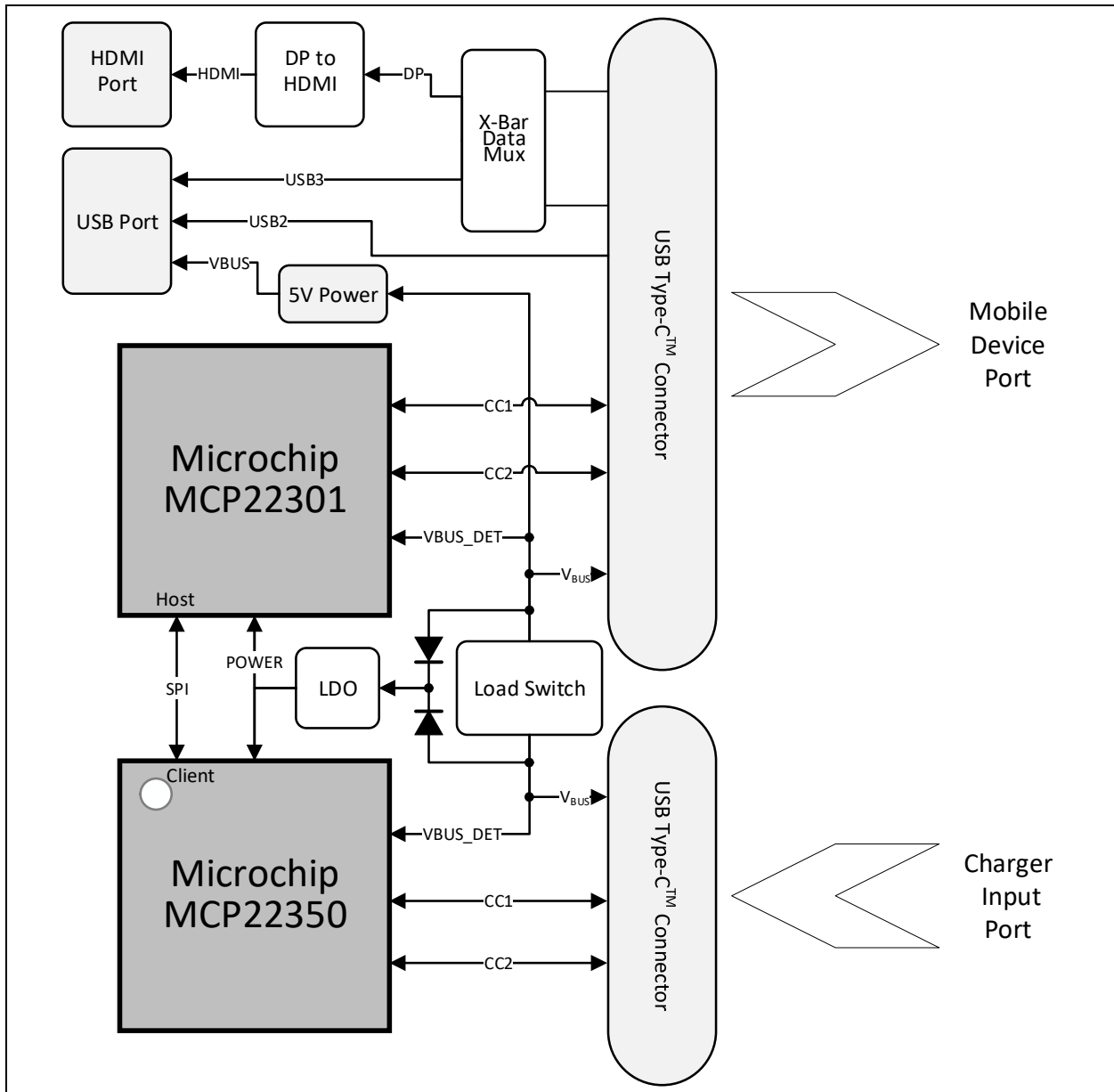


## 2.3.6 2-PORT DUAL ROLE POWER/DATA APPLICATION 'CHARGE-THROUGH ADAPTER'

An example of a charge through adapter/mobile dock device is shown in [Figure 2-6](#). In this example, the 'Charger Input Port' may pass a high voltage power profile through the system to an attached mobile device. If a charger is not inserted into the 'Charger Input Port', then the mobile device may power the adapter with 5V power.

A cross-bar switch is shown for routing DisplayPort Alternate Mode and USB3 data to the connector, allowing port expansion and video display.

An LDO is shown connected to a power OR circuit to ensure power to the system is available regardless of which Type-C port is supplying power to the system. The LDO should be selected to operate at the maximum supported charge-through voltage.



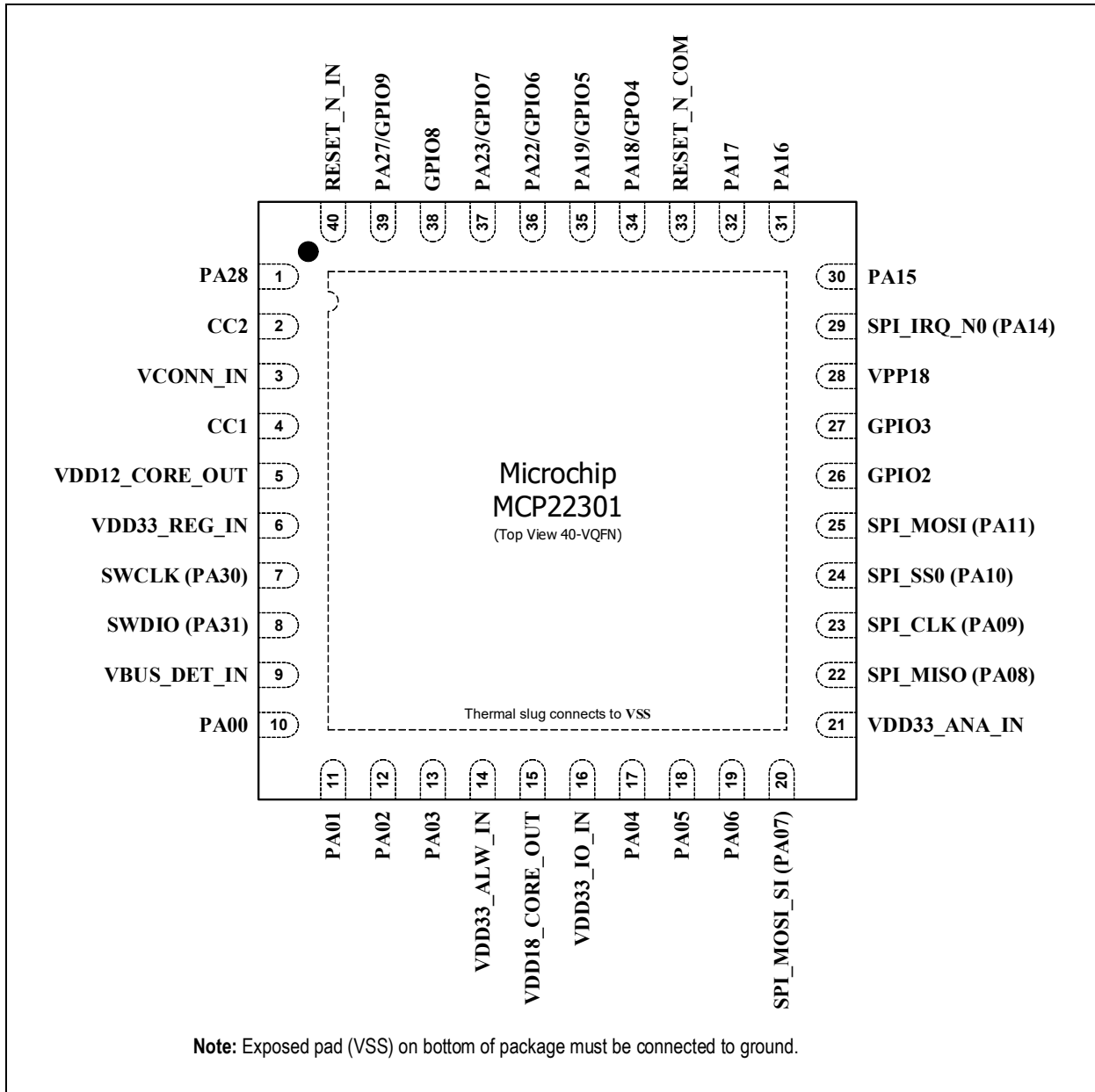
**FIGURE 2-6:** System Block Diagram - 2-Port Dual Role Power/Data Application 'Charge-Through Adapter'.

# MCP22301

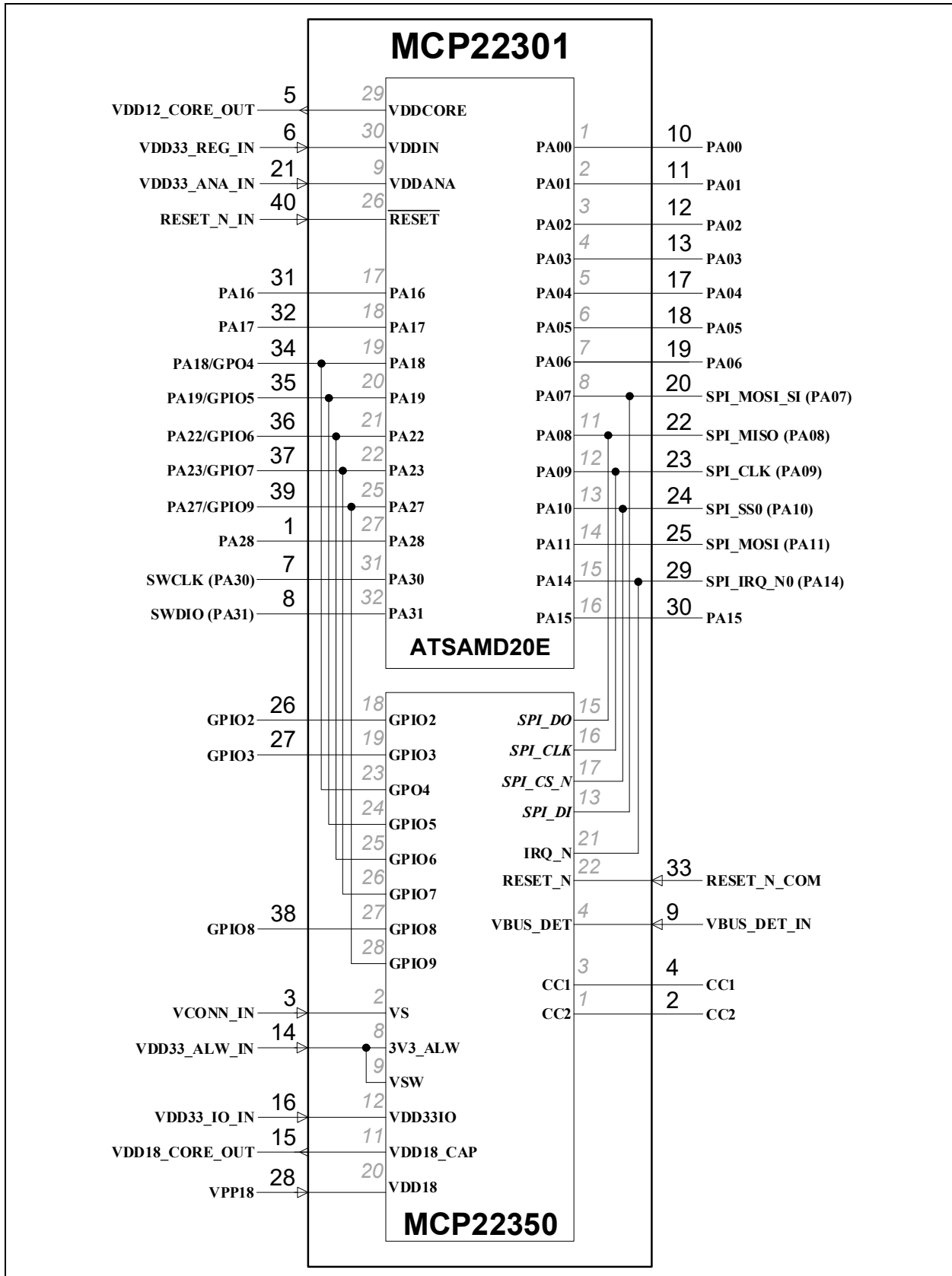
## 3.0 PIN DESCRIPTIONS AND CONFIGURATION

### 3.1 Pin Assignments

The device pin diagram for the MCP22301 can be seen in [Figure 3-1](#). [Table 3-1](#) provides a MCP22301 pin assignment table. The internal bonding diagram (simplified) is shown in [Figure 3-2](#). Pin descriptions are provided in [Section 3.2, "Pin Descriptions"](#).



**FIGURE 3-1:** MCP22301 Pin Assignments (Top View).



**FIGURE 3-2:** Simplified Internal Bonding Diagram.

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**TABLE 3-1: MCP22301 PIN ASSIGNMENTS**

Pin	Pin Name	Bond to SAMD20E	Bond to MCP22350
1	PA28	PA28	-
2	CC2	-	CC2
3	VCONN_IN	-	VS
4	CC1	-	CC1
5	VDD12_CORE_OUT	VDDCORE	-
6	VDD33_REG_IN	VDDIN	-
7	SWCLK (PA30)	PA30	-
8	SWDIO (PA31)	PA31	-
9	VBUS_DET_IN	-	VBUS_DET
10	PA00	PA00	-
11	PA01	PA01	-
12	PA02	PA02	-
13	PA03	PA03	-
14	VDD33_ALW_IN	-	3V3_ALW & VSW
15	VDD18_CORE_OUT	-	VDD18_CAP
16	VDD33_IO_IN	-	VDD33IO
17	PA04	PA04	-
18	PA05	PA05	-
19	PA06	PA06	-
20	SPI_MOSI_SI (PA07)	PA07	SPI_DI
21	VDD33_ANA_IN	VDDANA	-
22	SPI_MISO (PA08)	PA08	SPI_DO
23	SPI_CLK(PA09)	PA09	SPI_CLK
24	SPI_SS0 (PA10)	PA10	SPI_CS_N
25	SPI_MOSI (PA11)	PA11	-
26	GPIO2	-	GPIO2
27	GPIO3	-	GPIO3
28	VPP18	-	VDD18
29	SPI_IRQ_N0 (PA14)	PA14	IRQ_N
30	PA15	PA15	-
31	PA16	PA16	-
32	PA17	PA17	-
33	RESET_N_COM	-	RESET_N
34	PA18/GPO4 (Note 1)	PA18	GPO4
35	PA19/GPIO5 (Note 1)	PA19	GPIO5
36	PA22/GPIO6 (Note 1)	PA22	GPIO6
37	PA23/GPIO7 (Note 1)	PA23	GPIO7
38	GPIO8	-	GPIO8
39	PA27/GPIO9 (Note 1)	PA27	GPIO9
40	RESET_N_IN	RESET	-

Exposed Pad (VSS) must be connected to ground.

**Note 1:** This pin is double bonded to the internal SAMD20E and MCP22301 and should not be simultaneously driven by both sources under normal use cases.

## 3.2 Pin Descriptions

This section details the functions of the various device signals.

**TABLE 3-2: PIN DESCRIPTIONS**

Name	Symbol	Buffer Type	Description
<b>USB Type-C™</b>			
Configuration Channel 1	CC1	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable. ( <i>CC1 in MCP22350</i> )
Configuration Channel 2	CC2	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable. ( <i>CC2 in MCP22350</i> )
VBUS Detection	VBUS_DET_IN	AIO	Scaled down version of VBUS input used for VBUS detection. Tie this signal to VBUS via a resistor divider. ( <i>VBUS_DET in MCP22350</i> )
<b>SPI Interface</b>			
SPI Clock	SPI_CLK	IS	SPI clock. The maximum supported SPI clock frequency is 8 MHz. ( <i>SPI_CLK in MCP22350 and PA09 in SAMD20</i> )
SPI Data Host In / Client Out	SPI_MISO	I/O8	SPI data host in, client out. ( <i>SPI_DO in MCP22350 and PA08 in SAMD20</i> )
SPI Data Host Out / Client In	SPI_MOSI	O2	SPI data host out / client in. This pin must be connected to <b>SPI_MOSI_SI</b> for proper operation. ( <i>PA11 in SAMD20</i> )
SPI Data Client In	SPI_MOSI_SI	IS	SPI data client in. This pin must be connected to <b>SPI_MOSI</b> for proper operation. ( <i>SPI_DI in MCP22350 and PA07 in SAMD20</i> )
SPI Chip Enable 0	SPI_SS0	IS	Active low SPI chip enable input for MCP22301. ( <i>SPI_CS_N in MCP22350 and PA10 in SAMD20</i> )
SPI Interrupt 0	SPI_IRQ_N0	I	SPI interrupt indicating request for service from optional external MCP22350. ( <i>IRQ_N in MCP22350 and PA14 in SAMD20</i> )
<b>Serial Wire Debug Interface</b>			
Serial Wire Debug Clock	SWCLK	IS	Serial wire debug clock. ( <i>PA30 in SAMD20</i> )
Serial Wire Debug Data	SWDIO	I/O	Serial wire debug bidirectional data. ( <i>PA31 in SAMD20</i> )
<b>Miscellaneous</b>			
System Reset Input	RESET_N_IN	I	Active low SAMD20 system reset input. This reset is used for reset of the SAMD20 portion of the MCP22301 by a companion MCU. ( <i>RESET in SAMD20</i> )
System Reset Common	RESET_N_COM	IS	Active low MCP22350 system reset input. This reset is used for reset of the MCP22350 portion of the MCP22301 by a companion MCU. ( <i>RESET_N in MCP22350</i> )
<b>General Purpose I/Os</b>			
Misc. SAMD20E I/O	PA00, PA01, PA02, PA03, PA04, PA05, PA06, PA15, PA16, PA17, PA18, PA19, PA22, PA23, PA27, PA28	I/O	Refer to SAMD20E Datasheet for pin function, peripheral detail, and characteristics. ( <i>PAxx in SAMD20</i> )  <b>Note:</b> PA18, PA19, PA22, PA23, and PA27 are multiplexed with MCP22350 GPIOs. Refer to <a href="#">Table 3-1</a> for more information.

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**TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)**

Name	Symbol	Buffer Type	Description
MCP22350 GPIO	GPIO2, GPIO3, GPO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9	I/O	Refer to MCP22350 Datasheet for pin function, peripheral detail, and characteristics. ( <i>GPIOx, GPO4 in MCP22350</i> )  <b>Note:</b> GPO4, GPIO5, GPIO6, GPIO7, and GPIO9 are multiplexed with SAMD20 GPIOs. Refer to <a href="#">Table 3-1</a> for more information.
<b>Power/Ground</b>			
+5V Port Power Switch Input	VCONN_IN	P	+5V VCONN FET power source. ( <i>VS in MCP22350</i> )
+3.3V I/O Power Supply Input	VDD33_IO_IN	P	+3.3V I/O power supply input. ( <i>VDD33IO in MCP22350</i> )
+3.3V Analog Power Supply Input	VDD33_ANA_IN	P	+3.3V analog power supply input. ( <i>VDDANA in SAMD20</i> )
+3.3V Always Supply Input	VDD33_ALW_IN	P	+3.3V always supply input. ( <i>3V3_ALW &amp; VSW in MCP22350</i> )  <b>Note:</b> This pin must be connect to a 2.2 uF capacitor to ground.
+3.3V Regulator Power Supply Input	VDD33_REG_IN	P	+3.3V regulator power supply input. ( <i>VDDIN in SAMD20</i> )
+1.8V Core Voltage Power Supply Input	VPP18	P	+1.8V core voltage power supply input. ( <i>VDD18 in MCP22350</i> )
+1.8V Digital Core Power Supply Output	VDD18_CORE_OUT	P	+1.8V digital core power supply output. This signal must be connected to a 1uF capacitor to ground for proper operation. ( <i>VDD18_CAP in MCP22350</i> )
+1.2V Core Power Supply Output	VDD12_CORE_OUT	P	+1.2V core power supply output. This signal must be connected to a 1uF capacitor to ground for proper operation. ( <i>VDDCORE in SAMD20</i> )
Ground	VSS	P	Ground pins.

NOTES:

# MCP22301

## 4.0 FUNCTIONAL DESCRIPTIONS

This section provides functional descriptions of the following:

- [Serial Peripheral Interface \(SPI\)](#)
- [Power States](#)
- [Cable Plug Orientation and Detection](#)
- [Baseband CC Interface \(BCI\)](#)
- [Power Delivery MAC](#)
- [The BIST RX block contains a PRBS generator and bit error detection logic. BIST RX is used only during the BIST Receiver Test.](#)

### 4.1 Serial Peripheral Interface (SPI)

The MCP22301 integrates a SPI host/client controller which includes the following features:

- Full-duplex, four-wire interface ([SPI\\_MISO](#), [SPI\\_MOSI](#), [SPI\\_SCK](#), [SPI\\_SS](#))
- Single-buffered transmitter, double-buffered receiver
- Supports all four SPI modes of operation
- Single data direction operation allows alternate function on [SPI\\_MISO](#) or [SPI\\_MOSI](#) pin
- Selectable LSB- or MSB-first data transfer
- Host operation:
  - Serial clock speed,  $f_{SCK}=1/t_{SCK}$  ([Note](#))
  - 8-bit clock generator

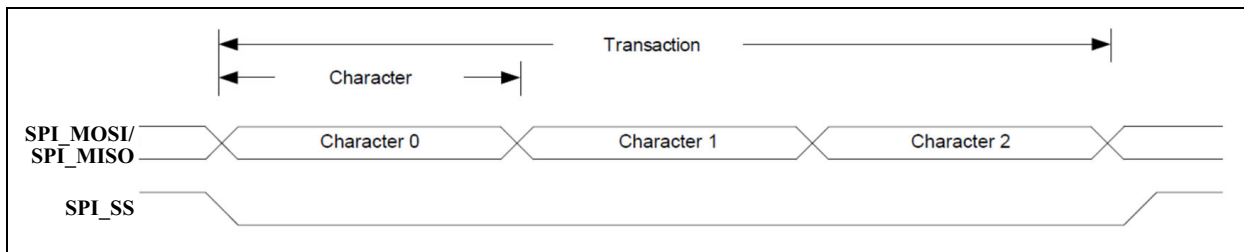
- Client operation:
  - Serial clock speed,  $f_{SCK}=1/t_{SSCK}$  ([Note](#))
  - Optional 8-bit address match operation
  - Operation in all sleep modes

**Note:** For  $t_{SCK}$  and  $t_{SSCK}$  values, refer to [Section 5.5.2, "SPI Timing"](#).

The SPI is a high-speed synchronous data transfer interface which allows high-speed communication between the device and peripheral devices. The SPI can operate as a host or client. As a host, the SPI initiates and controls all data transactions. The SPI is single buffered for transmitting and double buffered for receiving.

When transmitting data, a Data register is loaded with the next character to be transmitted during the current transmission. When receiving, the data is transferred to the two-level receive buffer, and the receiver is ready for a new character.

The SPI transaction format is shown in [Figure 4-1](#). Each transaction can contain one or more characters. The character size is configurable, and can be either 8 or 9 bits.



**FIGURE 4-1:** SPI Transaction Format.

The SPI host pulls the client select line ([SPI\\_SS](#)) of the desired client low to initiate a transaction. The host and client prepare data to send via their respective shift registers, and the host generates the serial clock on the [SPI\\_SCK](#) line.

Data is always shifted from host to client on the Host Output Client Input line ([SPI\\_MOSI](#)); data is shifted from host to client on the Host Input Client Output line ([SPI\\_MISO](#)).

Each time character is shifted out from the host, a character will be shifted out from the client simultaneously. To signal the end of a transaction, the host will pull the [SPI\\_SS](#) line high.



## 4.2 Power States

The device supports the following power states, as defined in their respective sub-sections:

- [STANDBY](#)
- [ATTACHED IDLE \(FRS Enabled\)](#)
- [ATTACHED IDLE \(FRS Disabled\)](#)
- [ACTIVE](#)

### 4.2.1 STANDBY

STANDBY is the lowest power functional state of the device. The majority of the device is powered off in this state. The internal CC comparator and 20 KHz oscillator are enabled in this state as well as requisite analog components (1.8V LDO, PORs, Biases, etc).

The CC lines are constantly monitored for an attach condition which shall result in an interrupt assertion to the host. If an attachment has been made, this state can detect a change in the partner's advertisement as well as a detach.

STANDBY is the power state that the MCP22301 device will be in when in USB Type-C™ Unattached.SRC.

### 4.2.2 ATTACHED IDLE (FRS ENABLED)

In this state, a USB Type-C™ device is connected and the USB PD bus is idle (no USB packets in transit). The CC signals are constantly being monitored for packet transmission and Fast Role Swap (FRS) signal detection is enabled.

### 4.2.3 ATTACHED IDLE (FRS DISABLED)

In this state, a USB Type-C™ device is connected and the USB PD bus is idle (no USB packets in transit). The CC signals are constantly being monitored for packet transmission and Fast Role Swap (FRS) signal detection is disabled.

### 4.2.4 ACTIVE

This state defines the condition of the device after an attachment occurred. In this state, Power Delivery communication is supported. This state is also used for any condition in which the 48 MHz Relaxation Oscillator must be enabled, such as when it is desired to debounce a GPIO within the micro-second range.

When transmitting a Power Delivery packet, an additional 5 mA may be consumed. Additional power consumption results from enabling the OCS comparator, VBUS comparator and other modules. When VCONN FETs are enabled, there is an additional 70 mW of power consumption.

This section details the functions that control and monitor the CC pins, monitor the **VBUS\_DET** pin, control the VCONN FETs, and sample the **CFG\_SEL** pin.

## 4.3 Cable Plug Orientation and Detection

### 4.3.1 CC COMPARATOR

The device integrates a comparator and DAC circuit to implement Type-C attach and detach functions. It supports up to eight programmable thresholds for attach detection between UFP and DFP. When operating as a UFP, the device supports detecting changes in the DFP's advertised thresholds to determine current sourcing capability. The default nominal values for the thresholds detected by the CC comparators are:

- 0.20 V
- 0.40 V
- 0.66 V
- 0.80 V
- 1.23 V
- 1.60 V
- 2.60 V
- 3.0 V Proprietary Mode

**TABLE 4-1: CABLE DETECT SUMMARY**

Parameter	Threshold CSR	Description	Min	Typ	Max
DFP_ACT_DEF	CC_THR0	Detecting an active cable when configured as DFP and advertising default USB current.	—	0.20 V	—
UFP_DFP_DEF	CC_THR0	Detecting DFP attach when configured as UFP and DFP is advertising default USB current.	—	0.20 V	—
DFP_ACT_1A5	CC_THR1	Detecting an active cable when configured as DFP and advertising 1.5A.	—	0.40 V	—
UFP_DFP_1A5	CC_THR2	Detecting DFP attach when configured as UFP and DFP is advertising 1.5A.	—	0.66 V	—
DFP_ACT_3A0	CC_THR3	Detecting an active cable when configured as DFP and advertising 3.0A.	—	0.80 V	—

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**TABLE 4-1: CABLE DETECT SUMMARY (CONTINUED)**

Parameter	Threshold CSR	Description	Min	Typ	Max
UFP_DFP_3A0	CC_THR4	Detecting DFP attach when configured as UFP and DFP is advertising 3.0A.	—	1.23 V	—
DFP_UFP_DEF	CC_THR5	Detecting UFP attach when configured as DFP advertising default USB current.	—	1.60 V	—
DFP_UFP_1A5	CC_THR5	Detecting UFP attach when configured as DFP advertising 1.5A.	—	1.60 V	—
DFP_UFP_3A0	CC_THR6	Detecting UFP attach when configured as DFP advertising 3.0A.	—	2.60 V	—

The following tables summarizes the expected thresholds to be matched for various configurations.

**TABLE 4-2: DFP CC MATCH SUMMARY**

CC State	CC THR0	CC THR1	CC THR2	CC THR3	CC THR4	CC THR5	CC THR6	CC THR7
Advertise Default USB Current and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 1.5 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 3.0 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise Default USB Current and connected to UFP	1	0	0	0	0	0	0	0
Advertise 1.5 A and connected to UFP	0	1	0	0	0	0	0	0
Advertise 3.0 A and connected to UFP	0	0	0	1	0	0	0	0
Advertise Default USB Current and no connect (vOpen)	1	0	0	0	0	1	0	0
Advertise 1.5 A and no connect (vOpen)	0	1	0	0	0	1	0	0
Advertise 3.0 A and no connect (vOpen)	0	0	0	1	0	0	1	0
Proprietary Mode and no connect (vOpen)	0	0	0	0	0	0	0	1

**TABLE 4-3: UFP CC MATCH SUMMARY**

CC State	CC THR0	CC_THR1	CC THR2	CC THR3	CC THR4	CC THR5	CC THR6	CC THR7
Powered cable detected.	0	0	0	0	0	0	0	0
No Connect (SNK.Open)	0	0	0	0	0	0	0	0
DFP Connected and advertising default USB current	1	0	0	0	0	0	0	0
DFP Connected and advertising 1.5 A	1	0	1	0	0	0	0	0
DFP Connected and advertising 3.0 A	1	0	1	0	1	0	0	0
DFP Connected and advertising proprietary current	1	0	1	0	1	0	0	1

### 4.3.2 DFP OPERATION

The device implements current sources to advertise current charging capabilities on both CC pins when operating as a DFP.

When a UFP connection is established, the current driven across the CC pins creates a voltage across the UFP's Rd pull-down that can be detected by the

integrated CC comparator. The voltages monitored are summarized in [Table 4-4](#). When connected to an active cable, an alternative pull-down (Ra) appears on the CC pin.

The DFP also integrates two 5V FETs for implementing the VCONN function. This is further discussed in [Section 4.3.9, "VCONN Operation"](#).

**TABLE 4-4: SOURCE DETECTION**

CC1	CC2	Connection State	CC Comparator State	VBUS	VCONN
Open	Open	Nothing Attached	Monitor both CC pins for attach	Off	Off
Rd	Open	UFP Attached	Monitor CC1 for detach	On	Off
Open	Rd	UFP Attached	Monitor CC2 for detach	On	Off
Ra	Open	Powered Cable, No UFP attached	Monitor CC2 for UFP attach. Monitor CC1 for cable detach.	Off	Off
Open	Ra	Powered Cable, No UFP attached	Monitor CC1 for UFP attach. Monitor CC2 for cable detach.	Off	Off
Ra	Rd	Powered Cable, UFP attached	Monitor CC2 for UFP detach. CC1 is not monitored for detach.	On	On
Rd	Ra	Powered Cable, UFP attached	Monitor CC1 for UFP detach. CC2 is not monitored for detach.	On	On
Rd	Rd	Debug accessory mode attached	Monitor both CC pins for detach	Off	Off
Ra	Ra	Audio accessory mode attached.	Monitor both CC pins for detach	Off	Off

### 4.3.3 RP CURRENT SOURCES

In order to advertise the current charging capabilities of the device via the integrated port power controller or external power circuit, Rp current sources are used.

The current source can be selected by software. [Table 4-5](#) summarizes the values supported by the current sources in regards to the programmed value.

**TABLE 4-5: RP CURRENT SOURCES**

DFP Advertisement	Current source (1.7V to 5.5V)	RPx Value
Disabled		00b
Default USB Power	80 $\mu$ A +/-20%	01b
1.5A @ 5V	180 $\mu$ A +/-8%	10b
3.0A @ 5V	330 $\mu$ A +/-8%	11b

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The current source coupled with the CC pins for RP advertisement is also used for sampling the CFG\_SEL pin. When the CFG\_SEL pin is sampled, current is steered away from the CC pins and no RP value is advertised.

## 4.3.4 UFP OPERATION

When operating as a UFP, the device applies an Rd pull-down on both CC lines and waits for a DFP connection from the assertion of VBUS. The CC comparator is used to determine the advertised current charger capabilities supported by the DFP.

## 4.3.5 DRP OPERATION (LEGACY)

In this configuration, software utilizes the device to alternate between a Source and Sink advertisement with an interval of tDRP per the USB Type-C™ Specification.

## 4.3.6 DRP OFFLOAD

DRP offload enables the device to manage the DRP toggle. This is beneficial as it allows the host CPU to remain in a low power state until a connection is detected.

DRP offload toggles between Source and Sink advertisement by alternating between enabling Rp current sources and Rd pull-downs for a period of tDRP (DRP Time Register). The duty cycle between Source and Sink advertisement is determined by the DRP Duty Cycle Register. The DRP Time Register may be written by firmware or generated automatically via a pseudo random number generator. The latter approach should be used to reduce the probability of collisions when connecting. It is selectable whether the DRP cycle shall first advertise UFP or DFP.

A connection is detected after a successful debounce for a period defined by the Match Debounce Register. VBUS is checked to be below vSafe0v for the DFP case. This results in IRQ\_N assertion and automatic disablement of the DRP toggle. Firmware must further debounces for the period tPDDebounce before determining if a valid match is present. If a match has not occurred, firmware will enable DRP again.

A pseudo random number generator, implemented via a LFSR, is utilized to generate the DRP period. The LFSR operates off of the 20 KHz clock and updates every 100 μs when enabled.

Hardware limits the total DRP period to be between 50 ms and 100 ms in order to comply with the USB Type-C™ specification.

## 4.3.7 COLLISION AVOIDANCE

An alternative mode of operation is required to enable the CC detection circuit to facilitate software implementation of collision detection which was incorporated into version 3.0 of the USB PD Specification.

In order to avoid message collisions due to asynchronous Messaging (AMS) sent from the Sink, the Source sets Rp to SinkTxOk (3A@5V) to indicate to the Sink that it is OK to initiate an AMS. When the Source wishes to initiate an AMS it sets Rp to SinkTxNG (1.5A@5V). When the Sink detects that Rp is set to SinkTxOk it may initiate an AMS. When the Sink detects that Rp is set to SinkTxNG it shall not initiate an AMS and shall only send Messages that are part of an AMS the Source has initiated.

When operating as a Sink, a mechanism is required for quickly determining whether the Source is advertising SinkTxNG or SinkTxOK on Rp.

A collision avoidance mechanism exists to enable software to instruct the device to sample only a single threshold on a single CC pin. This results in a cycle through both thresholds taking only 100 μs, making it easier for software to meet the timing constraints mandated by SinkTxOk in the specification.

## 4.3.8 FAST ROLE SWAP (FRS)

This feature is used to detect when a partner source has lost power. Upon detection of FRS signaling, the “Old Sink” transitions to be a Source and begins supplying VBUS.

When operating as a Sink, the FRS mode of operation enables detection of FRS signaling. Detection results in IRQ\_N assertion and this event may also be mapped as a PIO override source. When operating as a Source, upon detection of loss of power, the device will transmit FRS signaling. This is initiated by either assertion of a selected PIO or a CSR write.

The following FRS related features are supported:

- Ability to detect reception of FRS signaling
- High bandwidth and current boost mode for CC comparator to increase sampling frequency
- Interrupt, and PIO, assertion upon FRS detection
- PIO override support for FRS detection as a source
- Ability to initiate FRS signaling via GPIO assertion or register write.
- Control 5 Ohm (Rsw) pull-down resistor

### 4.3.8.1 FRS Sink Operation

When operating as a Sink, the device is configured to detect FRS signaling by setting FRS Detect Enable (FRS\_DET\_EN) in FRS Control Register. The CC detection logic is programmed to detect three thresholds (SinkTxOK, SinkTXNG, FRSWAP) and samples each threshold in round robin fashion. The sampling rate is determined by CC Sample Clock Register.

When a match is detected on FRSWAP threshold, the CC detection logic will “park” at this threshold and continue monitoring the output of the comparator. While “parked” the output of the CC comparator will be

sampled at an increased rate of 12 MHz. This higher sampling rate will prevent PD messages from inadvertently looking like FRS signaling which will happen on occasion when the sampling rate is similar or slower than the ~270 kbps rate of PD messages.

It will continue debouncing for the amount of time specified in FRS CC Debounce Register. The FRSWAP threshold is indicated by FRS Threshold Select Register.

If the debounce is successful, then the FRS\_RCV\_STS interrupt is asserted and the CC detection logic resumes sampling all enabled thresholds. If the FRS debounce fails, the CC detection logic resumes sampling all enabled thresholds.

In this mode of operation the CC Comparator operates at a faster rate in order to minimize the FRS detection latency. This is enabled by placing this the comparator into a high bandwidth mode.

After detecting the FRS signaling, the “old Sink” must start supplying vSafe5V at USB Type-C™ current VBUS no later than tSrcFRSwap (150 μs) after VBUS has dropped below vSafe5V. This must be accomplished via circuitry external to the device.

**Note:** The upper threshold used for vSafe5V should be used for determining when VBUS has dropped below vSafe5v to help meet tSrcFRSwap requirement.

**Note:** Matching of a VBUS threshold may be selected as a source to a PIO override. Additionally, VBUS threshold match ANDed with FRS signal detect may also be used as a PIO override source.

### 4.3.8.2 FRS Source Operation

The initial Source shall signal a FRS request by driving the CC pin to ground with a resistance of less than 5 Ohms for a period defined by FRS Transmission Length Register. The FRS request signaling is initiated by either a CSR write or GPIO assertion.

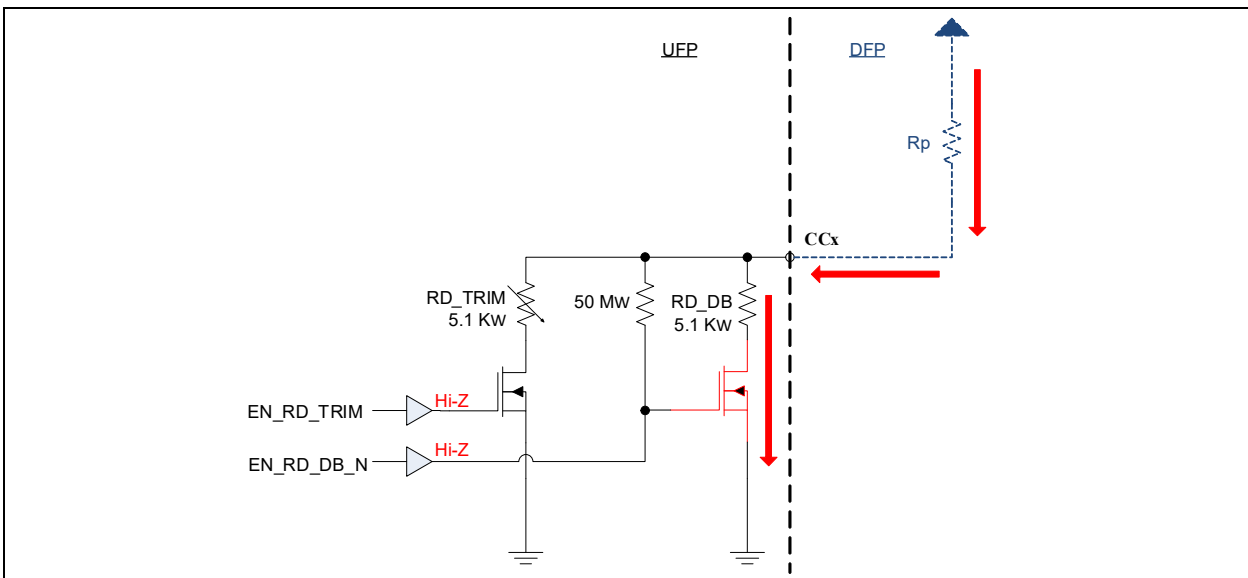
The former case is implemented by setting the FRS Request (FRS\_REQ\_EN) bit in FRS Control Register. This bit self clears after the FRS request is transmitted. For the latter case, the PIO is selected by the FRS Request PIO (FRS\_REQ\_PIO) field in FRS Control Register.

Transmission of FRS signaling will take precedence over PD MAC TX communication. The FRS PD resistor is enabled in tandem on the CC pin determined by FRS CC Select (FRS\_CC\_SEL) in FRS Control Register. This configuration remains until FRS transmission has completed.

### 4.3.8.3 Dead Battery (MCP22301-2 Only)

The MCP22301-2 device includes two variations of the Rd resistor implementation: Rd (Dead Battery) and Rd (Trimmed). The CC pins are configured to present either Hi-Z or an untrimmed Rd pull-down resistance when connected to a DFP advertising a pull-up resistance.

Figure 4-2 illustrates the configuration for supporting dead battery cases. The UFP pull-up activates the FET in series with RD\_DB and enables the untrimmed dead battery pull-down.

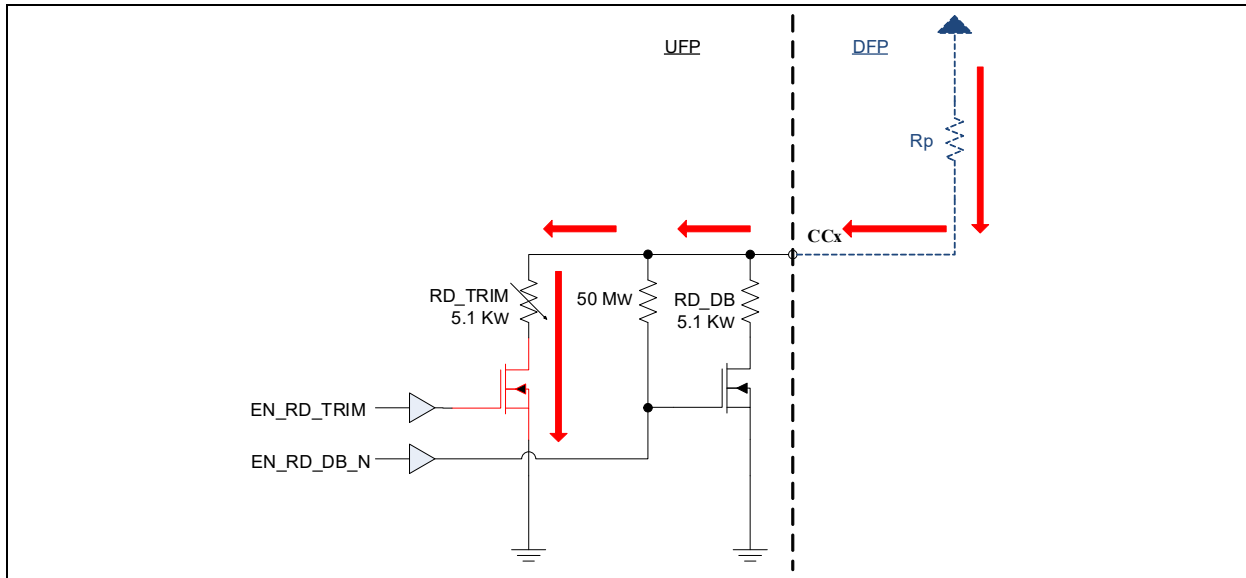


**FIGURE 4-2:** CC RD (Dead Battery).

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Figure 4-3 illustrates operation after the UFP has been powered over VBUS by the DFP. After the device is powered, EN\_RD\_DB asserts by default to keep the RD\_DB pull-down activated.

Upon powering the host CPU, software simultaneously deasserts EN\_RD\_DB and asserts EN\_RD\_TRIM. Going forward the device presents RD\_TRIM.



**FIGURE 4-3:** CC RD (Trim).

The Rd resistor presented, trimmed or untrimmed, is controlled by the CC1 and CC2 Pull-Down Values in the CC Control Register (CC\_CTL). These register fields serve the basis for the EN\_RD\_TRIM and EN\_RD\_DB\_N control signals depicted.

### 4.3.9 VCONN OPERATION

VCONN is a 5V supply that is used to power circuitry in the USB Type-C™ plug, which is required to implement Electronically Marked Cables. By default, the DFP always sources VCONN when connected to an active cable. However, this may be changed by software.

The VCONN FETs are enabled/disabled by software via the VCONN1 Control and VCONN2 Control control bits in the CC Control Register (CC\_CTL).

**Note:** It is not envisioned to ever enable both FETs simultaneously.

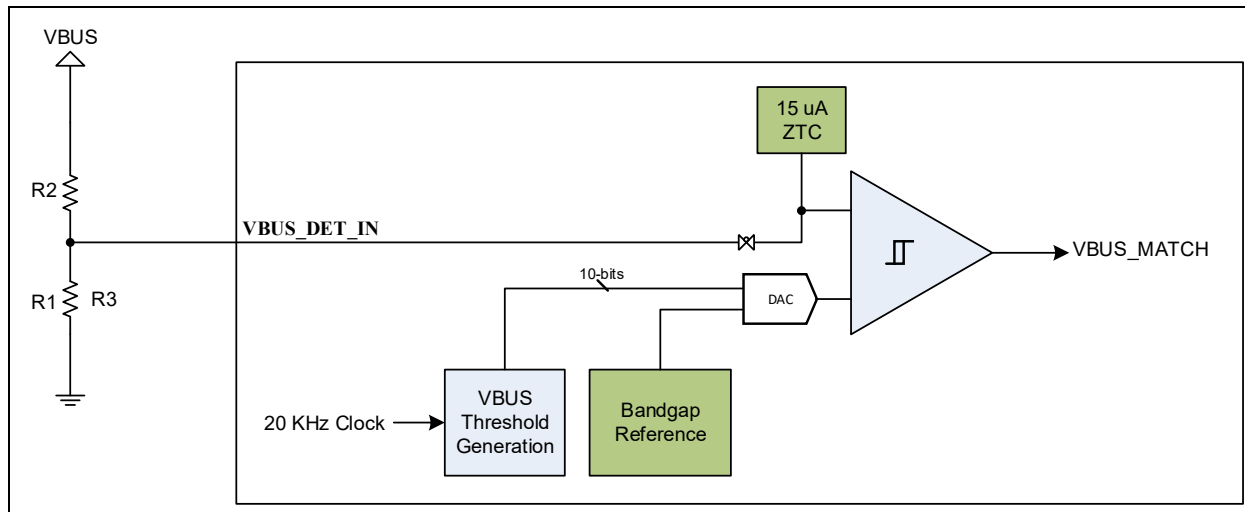
VCONN is monitored for an over current condition via an internal monitoring circuit. A VCONN over current condition is recognized when the event persists for a time longer than specified. When an over-current VCONN event is detected, an interrupt asserts. The device may be configured to automatically disable the VCONN FET upon detection of a CC1/CC2 Back-Drive Error or VCONN Discharge Error. In the event of the detection of a debounced over-current VCONN event, the enabled VCONN FET will be disabled.

### 4.3.10 VBUS DETECTION

The device implements a comparator for determining when VBUS is within a programmed range, vSafe5V, or vSafe0v. VBUS is divided down externally via a 1:9 resistor divider to generate VBUS\_DET\_IN. VBUS\_DET\_IN is compared with an 8-bit threshold generated by an integrated DAC. The comparator is also shared by the CFG\_SEL pin which is sampled automatically after a system reset.

Figure 4-4 illustrates the VBUS\_DET\_IN circuit. In a typical use case, VBUS\_DET\_IN thresholds are programmed to track the following voltage ranges as defined in Table 4-5.

**Note:** Table 4-5 illustrates the values of VBUS\_DET\_IN utilizing +/-1% accurate resistors where R1 is 10 kΩ and R2 is 90 kΩ.



**FIGURE 4-4:** VBUS\_DET\_IN Comparator.

For a DFP, the VBUS comparator is useful to detect when VBUS is within the desired range per PD negotiations. This is the case when VBUS is generated by a source external to the device.

For a UFP, the VBUS comparator is required to determine when a DFP is attached or detached. It may also use the comparator to determine when VBUS is within a new voltage range negotiated via PD.

If supported, the ranges 8V, 12V and 20V may be programmed in VBUS Threshold 2 and VBUS Threshold 3 registers. Likewise 5V range, vSafe5v, can be programmed in VBUS Threshold 0 and VBUS Threshold 1 registers.

The threshold for vSafe0V is programmable.

VBUS\_DET\_IN monitoring logic operates off of the 20 KHz oscillator which cycles through each threshold. Including vSafe0v, a total of five values are compared.

The VBUS Match Register (VBUS\_MATCH) indicates when the value on VBUS\_DET\_IN is higher than the corresponding programmed threshold and can therefore be used to determine if VBUS is in the desired range.

A change in the state of the VBUS match may trigger assertion of the IRQ\_N pin if appropriately configured.

#### 4.4 Baseband CC Interface (BCI)

The device integrates a Baseband CC Interface (BCI) to facilitate USB Power Delivery communication. This module bridges between the PD MAC/BMC and the analog front end. Baseband communication is initiated by the PD MAC, which interfaces to the BCI. The BCI implements the digital functions required to control TX baseband components.

##### 4.4.1 BASEBAND TX DATA-FLOW

The key responsibility of the BCI is to generate the wave form required for baseband communication. To this end, the BMC has a group of eight registers that define the Lo-Hi and Hi-Lo transitions for the generated BMC signal.

When instructed to transition from Lo-Hi, the BCI steps through all BB TX Rise Registers. Likewise when instructed to transition from Hi-Lo, the BCI steps through all BB TX Fall Registers.

**Note:** The user may replicate values if it is desired to use less than twelve unique values for this purpose.

##### 4.4.2 BASEBAND RX DATA-FLOW

Baseband RX data is received by the BCI from the RX analog front end where it is compared to a threshold programmed by software. The CC RX DAC Value defines the trip point used for reception of baseband data. The field shall be programmed to be 175 mV below the RX Eye center, as defined in the PD Specification for the mode in which the device is operating (Sourcing Power, Sinking Power, Power Neutral).

#### 4.5 Power Delivery MAC

The PD MAC implements certain features of the protocol layer and physical layer of the Universal Serial Bus Power Delivery Specification. On one end the PD MAC interfaces to the software implementing the bulk of protocol and higher level layers and on the other end it interfaces to a BMC encoder / decoder module.

In addition to the normal TX and RX functions, the PD MAC implements the test mode logic defined in the USB PD specification (BIST).

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The PD MAC supports the following features:

- Automatic TX Mode for packet framing and CRC32 insertion.
- Raw TX Mode for bit level packet control.
- Automatic GoodCRC response to received messages.
- Automatic BIST Error Count Message in BIST RX Mode.
- GoodCRCTimer implementation.
- Automatic retries with programmable retry count.
- Redundant receive packets automatically dropped in auto response mode.
- 74 byte TX queue.
- 128 byte RX queue.
- Programmable TX Bit-time. Allows for changing operating frequency.
- Programmable preamble length.
- BIST TX and RX logic.
- Programmable TX and RX queue modes - buffer mode and FIFO mode.
- CRC32 generator for TX.
- CRC32 calculator and comparator for RX.

## 4.5.1 PD MAC TRANSMITTER

The PD MAC transmitter is comprised of three major blocks:

- **TX Queue:**  
The TX Queue is where software loads the message to be transmitted.
- **TX Control:**  
The TX Control implements the necessary control logic. It is responsible for reading the data from the TX queue and based on the data processing mode (automatic or raw), processing the data to make it suitable (nibbles with control information) for use by the TX Comm. It is also responsible for generating packet framing and terminating the packet in automatic mode, and generating messages for automatic response (GoodCRC and BIST Error Count). TX Control also handles the selection of the SOP type that is to be transmitted.
- **TX Comm:**  
The TX Comm is comprised of a TX CRC generator, a 4b5b encoder, serializer, preamble generator, and TX bit timer. It takes the nibble data, computes and inserts the CRC, 5b encodes, and generates the baseband serial data. Preamble insertion is also performed by this logic.

## 4.5.2 PD MAC RECEIVER

The PD MAC receiver is comprised of three major blocks:

- **RX Queue:**  
The RX Queue is where software reads the received messages.
- **RX Control:**  
The RX Control implements the necessary control logic. It is responsible for validating the received packet, updating the RX Queue status, and triggering automatic responses, if required.
- **RX Comm:**  
The RX Comm is comprised of the Clock and Data Recovery (CDR), RX DES (de-serializer) (serial-to-parallel converter, 4b5b decoder, and framing detector), RX CRC32 (CRC calculator, receive timer), and other logic to detect valid packet reception.

## 4.5.3 PD MAC BIST

The PD MAC incorporates BIST functions as defined in the USB PD Specification. It is comprised of a TX and RX block.

The BIST TX block contains a PRBS (Pseudo Random Binary Sequence) generator, BIST pattern generation logic, and its own bit-timing logic. The SOP type used by TX BIST Test Frames is a 20-bit static vector which is created by multiplexing between the five SOP ordered sets based on a register setting. The resultant 20-bit vector is simply bit selected when the packet is transmitted.

The BIST RX block contains a PRBS generator and bit error detection logic. BIST RX is used only during the BIST Receiver Test.



## 5.0 OPERATIONAL CHARACTERISTICS

### 5.1 Absolute Maximum Ratings †

Supply Voltage (VCONN_IN) (Note 1)	-0.3V to +6.0V
Supply Voltage (VDD33_ALW_IN, VDD33_IO_IN) (Note 1)	0V to +6.0V
Supply Voltage (VDD33_REG_IN, VDD33_ANA_IN) (Note 1)	0V to +3.8V
Supply Voltage (VPP18) (Note 1)	0V to +7.75V
Pin voltage with respect to ground (Note 2)	VSS-0.6V to VDD33_REG_IN+0.6V
Pin voltage with respect to ground (VBUS_DET_IN)	-0.5V to +3.96V
Pin voltage with respect to ground (CC1, CC2, SPI_MOSI_SI, EN_VBUS, RESET_N_COM, VBUS_DIS)	-0.5V to +6.0V
Storage Temperature	-55°C to +150°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020
HBM ESD Performance	+/-2 kV

† **Notice:** Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 5.2, "Operating Conditions ‡", Section 5.4, "DC Characteristics", or any other applicable section of this specification is not implied.

**Note 1:** When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

**2:** This rating does not apply to the following pins: VBUS\_DET\_IN, CC1, CC2, SPI\_MOSI\_SI, EN\_VBUS, RESET\_N\_IN, VBUS\_DIS.

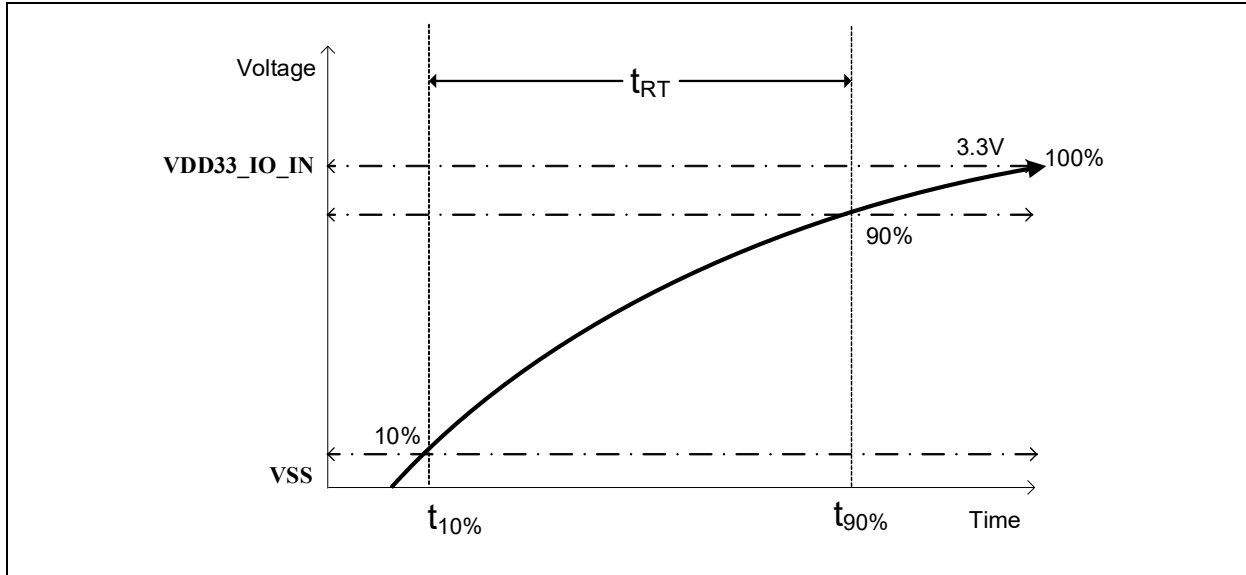
### 5.2 Operating Conditions ‡

Supply Voltage (VCONN_IN)	+4.75V to +5.25V
Supply Voltage (VDD33_ALW_IN, VDD33_IO_IN)	+2.97V to +3.63V
Supply Voltage (VDD33_REG_IN, VDD33_ANA_IN)	+2.97V to +3.63V
Supply Voltage (VPP18)	+1.62V to +1.98V
Pin voltage with respect to ground (Note 1)	0V to +2.00V
Positive pin voltage with respect to ground (VBUS_DET_IN)	VDD33_IO_IN-0.3V to VDD33_IO_IN+0.3V
Negative pin voltage with respect to ground (VBUS_DET_IN)	-0.33V to -0.27V
Positive pin voltage with respect to ground (CC1, CC2, SPI_MOSI_SI, EN_VBUS, RESET_N_COM, VBUS_DIS)	+2.97V to +3.63V
Negative pin voltage with respect to ground (CC1, CC2, SPI_MOSI_SI, EN_VBUS, RESET_N_COM, VBUS_DIS)	-0.33V to -0.27V
Power Supply Rise Time Max (T <sub>RT</sub> ) (VDD33_IO_IN) (Figure 5-1)	100 ms
Power Supply Rise Rate Max (VDD33_ANA_IN, VDD33_REG_IN)	0.1 V/μs
Ambient Operating Temperature in Still Air (T <sub>A</sub> )	-40°C to +85°C

‡ **Notice:** Proper operation of the device is assured only within the ranges specified in this section.

**Note 1:** This rating does not apply to the following pins: VBUS\_DET\_IN, CC1, CC2, SPI\_MOSI\_SI, EN\_VBUS, RESET\_N\_COM, VBUS\_DIS.

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**FIGURE 5-1:** Supply Rise Time Model.

## PACKAGE THERMAL SPECIFICATIONS

Parameter	Symbol	°C/W
Thermal Resistance Junction to Ambient (@ 0 air flow)	$\Theta_{JA}$	36.6
Thermal Resistance Junction to Top of Case	$\Theta_{JC}$	9.2
Thermal Resistance Junction to Board	$\Theta_{JB}$	15.7
Thermal Resistance Junction to Bottom of Case (@ 0 air flow)	$\Psi_{JT}$	0.2

**Note 1:** Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

**TABLE 5-1: POWER DISSIPATION**

Parameter	Symbol	Max	Units
Power Dissipation	$P_{dis}$	214	mW

**Note:** This is the worst-case power dissipation as a consequence of maximum loading (before current-limiting protections take effect) upon the VCONN power switch, 3.3V power-ORing switch, analog blocks, and core digital logic.

## 5.3 Current Consumption

**TABLE 5-2: TYPICAL DEVICE CURRENT CONSUMPTION**

Power State	3.3V Supply Current		
	Typical	Max	Units
<b>RESET</b>	1.27	—	mA
<b>STANDBY (source)</b>	7.49	—	mA
<b>ATTACHED IDLE (source)</b>	11.40	—	mA
<b>ACTIVE (with PD packet transmitting)</b>	-	23.84	mA

**Note 1:** This table details the power consumption of the MCP22301 device as measured during various modes of operation for a single port Source-Only implementation (i.e.: loading a PDS Source-only configuration and programming with default settings). The power consumption may vary significantly depending on the utilization SAMD20 MCU to handle any additional custom system-specific functions. Refer to the respective SAMD20E and MCP22350 data sheets for more details on the power consumption of these two devices under certain specific usage scenarios. Also refer to [Section 4.2, "Power States"](#) for additional information. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements. Maximum values represent very short bursts of activity over a small amount of time. Typical values represent averaged current consumption over time.

- 2:** **STANDBY** is equivalent to USB Type-C™ specification's Unattached.SRC.
- 3:** Currents measured with all 3.3V rails tied together.

# MCP22301

## 5.4 DC Characteristics

**TABLE 5-3: ELECTRICAL CHARACTERISTICS**

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>I Type Input Buffer</b>						
Low Input Level	$V_{IL}$	—	—	$0.3 \cdot V_{DD33\_REG\_IN}$	V	
High Input Level	$V_{IH}$	$0.55 \cdot V_{DD33\_REG\_IN}$	—	—	V	
Input Leakage	$I_{LEAK}$	-1	$\pm 0.015$	1	$\mu A$	
<b>IS_1 Type Input Buffer</b>						
Low Input Level	$V_{IL}$	—	—	$0.3 \cdot V_{DD33\_REG\_IN}$	V	
High Input Level	$V_{IH}$	$0.55 \cdot V_{DD33\_REG\_IN}$	—	—	V	
Input Leakage	$I_{IH}$	-1	$\pm 0.015$	1	$\mu A$	
<b>IS_2 Type Input Buffer</b>						
Low Input Level	$V_{ILI}$	-0.3	—	0.8	V	
High Input Level	$V_{IHI}$	2.0	—	3.6	V	
Negative-Going Threshold	$V_{ILT}$	1.21	1.33	1.8	V	Schmitt trigger
Positive-Going Threshold	$V_{IHT}$	1.31	1.58	1.8	V	Schmitt trigger
Schmitt Trigger Hysteresis ( $V_{IHT} - V_{ILT}$ )	$V_{HYS}$	100	133	200	mV	
Input Leakage ( $V_{IN} = V_{SS}$ or $V_{DD33\_IO\_IN}$ )	$I_{IH}$	-10	—	10	$\mu A$	Note 1
Input Capacitance		—	—	3	pF	
<b>O2 Type Output Buffer</b>						
Low Output Level	$V_{OL}$	—	$0.1 \cdot V_{DD33\_REG\_IN}$	$0.2 \cdot V_{DD33\_REG\_IN}$	V	$I_{OL} = -2$ mA
High Output Level	$V_{OH}$	$0.8 \cdot V_{DD33\_REG\_IN}$	$0.9 \cdot V_{DD33\_REG\_IN}$	—	V	$I_{OH} = 2$ mA
<b>OD2 Type Output Buffer</b>						
Low Output Level	$V_{OL}$	—	$0.1 \cdot V_{DD33\_REG\_IN}$	$0.2 \cdot V_{DD33\_REG\_IN}$	V	$I_{OL} = -2$ mA
<b>O8_1 Type Output Buffer</b>						
Low Output Level	$V_{OL}$	—	$0.1 \cdot V_{DD33\_REG\_IN}$	$0.2 \cdot V_{DD33\_REG\_IN}$	V	$I_{OL} = -8$ mA
High Output Level	$V_{OH}$	$0.8 \cdot V_{DD33\_REG\_IN}$	$0.9 \cdot V_{DD33\_REG\_IN}$	—	V	$I_{OH} = 8$ mA
<b>O8_2 Type Output Buffer</b>						
Low Output Level	$V_{OL}$	—	—	0.4	V	$I_{OL} = -8$ mA
High Output Level	$V_{OH}$	$V_{DD33\_IO\_IN} - 0.4$	—	—	V	$I_{OH} = 8$ mA

**Note 1:** This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50  $\mu A$  per-pin (typical).

**TABLE 5-4: VOLTAGE REGULATOR OPERATING RANGES**

Pin Name	Parameter	Min	Typ	Max	Units
VDD18_CORE_OUT	DC uncalibrated output voltage	1.62	1.80	1.91	V
VDD12_CORE_OUT	DC calibrated output voltage	1.10	1.23	1.30	V

**TABLE 5-5: VCONN SOURCE DC PARAMETERS**

Parameter	Symbol	Min	Typ	Max	Units	Notes
ILIM	$I_{LIM\_VCONN}$		600		mA	VCONN_IN = 5V
On Resistance	$R_{ON\_VCONN}$		270		m $\Omega$	

## 5.5 AC Characteristics and Timing

This section details the various AC timing specifications of the device.

### 5.5.1 RESET\_N TIMING

Figure 5-2 illustrates the RESET\_N timing requirements. Assertion of RESET\_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

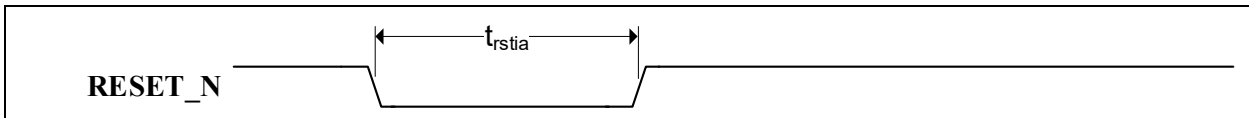


FIGURE 5-2: RESET\_N Timing.

TABLE 5-6: RESET\_N TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{rstia}$	RESET_N input assertion time	1	—	—	$\mu\text{s}$

### 5.5.2 SPI TIMING

Figure 5-3 and Figure 5-4 illustrate the SPI host and client timing requirements, respectively. Refer to Section 4.1, "Serial Peripheral Interface (SPI)" for additional information.

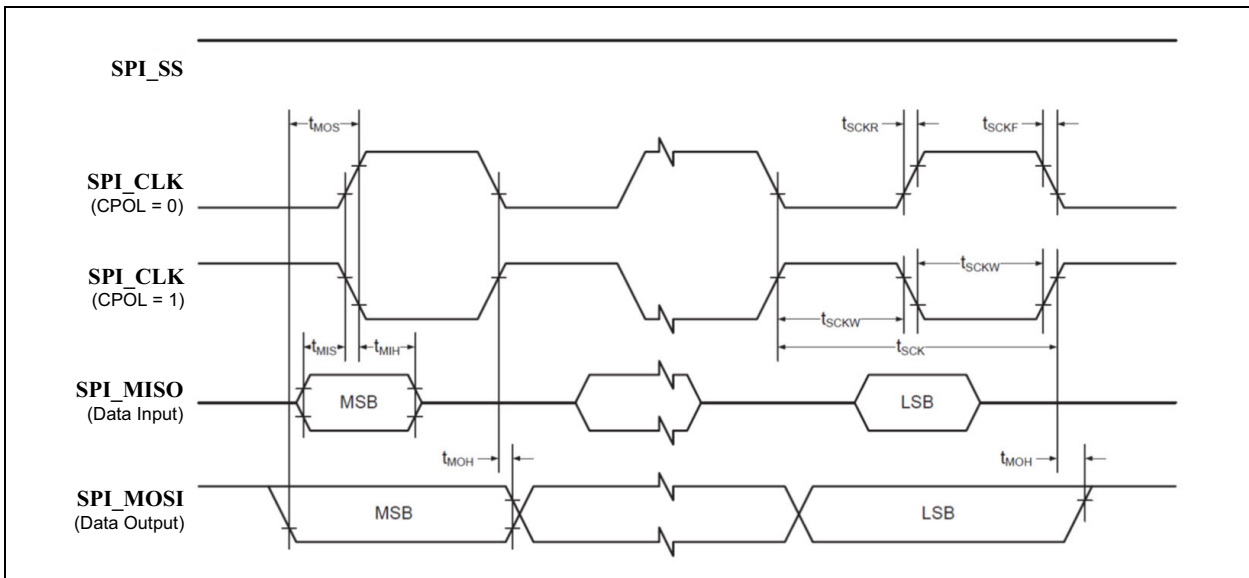
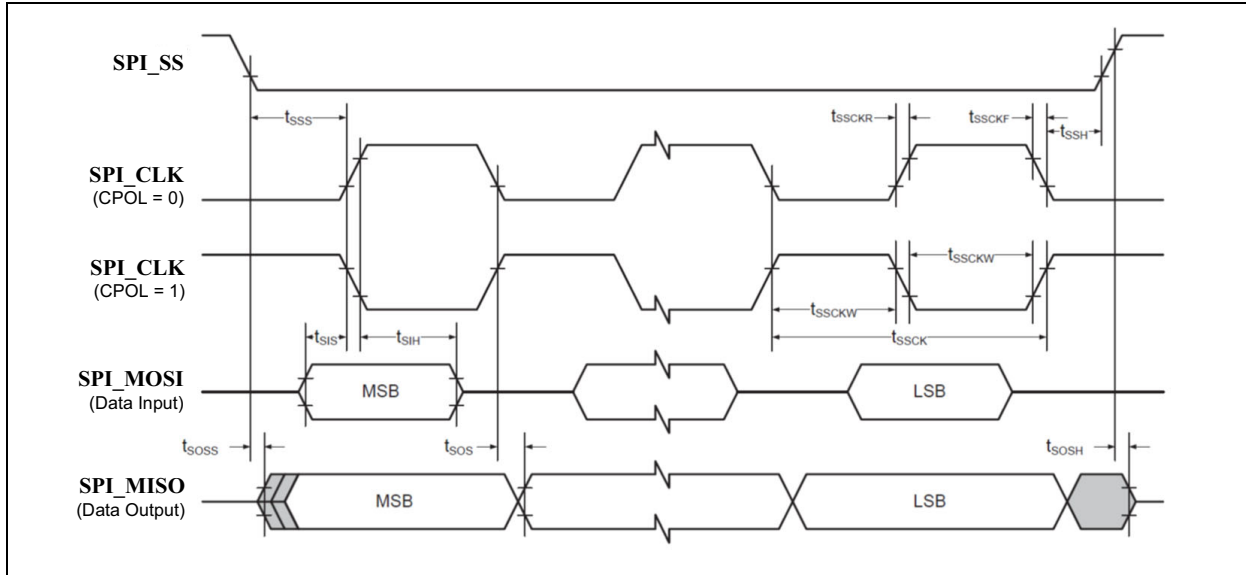


FIGURE 5-3: SPI Host Timing.

# MCP22301



**FIGURE 5-4:** SPI Client Timing.

**TABLE 5-7: SPI TIMING VALUES**

Symbol	Description	Min	Typ	Max	Units
$t_{SCK}$	SPI_CLK period (Host)	—	84	—	
$t_{SCKW}$	SPI_CLK high/low width (Host)	—	$0.5 \cdot t_{SCK}$	—	
$t_{SCKR}$	SPI_CLK rise time (Host)	—	7	—	ns
$t_{SCKF}$	SPI_CLK fall time (Host)	—	9.5	—	ns
$t_{MIS}$	SPI_MISO setup to SPI_CLK (Host)	—	29	—	ns
$t_{MIH}$	SPI_MISO hold after SPI_CLK (Host)	—	8	—	ns
$t_{MOS}$	SPI_MOSI setup to SPI_CLK (Host)	—	$t_{SCK}/2 - 16$	—	ns
$t_{MOH}$	SPI_MOSI hold after SPI_CLK (Host)	—	16	—	ns
$t_{SSCK}$	SPI_CLK period (Client)	$1 \cdot t_{CLK\_APB}$	—	—	ns
$t_{SSCKW}$	SPI_CLK high/low width (Client)	$0.5 \cdot t_{SSCK}$	—	—	ns
$t_{SSCKR}$	SPI_CLK rise time (Client)	—	7	—	ns
$t_{SSCKF}$	SPI_CLK fall time (Client)	—	9.5	—	ns
$t_{SIS}$	SPI_MOSI setup to SPI_CLK (Client)	$t_{SSCK}/2 - 19$	—	—	ns
$t_{SIH}$	SPI_MOSI hold after SPI_CLK (Client)	$t_{SSCK}/2 - 5$	—	—	ns
$t_{SSS}$	SPI_SS setup to SPI_CLK (Client, PRELOADEN=1)	$2 \cdot t_{CLK\_APB} + t_{SOS}$	—	—	ns
	SPI_SS setup to SPI_CLK (Client, PRELOADEN=0)	$t_{SOS} + 7$	—	—	ns
$t_{SSH}$	SPI_SS hold after SPI_CLK (Client)	$t_{SIH} - 4$	—	—	ns
$t_{SOS}$	SPI_MISO setup to SPI_CLK (Client)	—	$t_{SSCK}/2 - 20$	—	ns
$t_{SOH}$	SPI_MISO hold after SPI_CLK (Client)	—	20	—	ns
$t_{SOSS}$	SPI_MISO setup after SPI_SS low (Client)	—	16	—	ns
$t_{SOSH}$	SPI_MISO setup after SPI_SS high (Client)	—	11	—	ns

## 6.0 PACKAGE INFORMATION

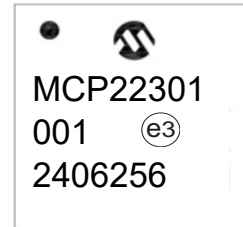
### 6.1 Package Marking Information

40-Lead VQFN (6 x 6 mm)

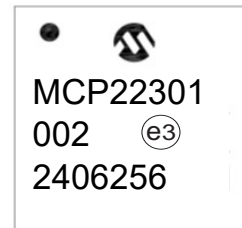


Examples

MCP22301-1



MCP22301-2

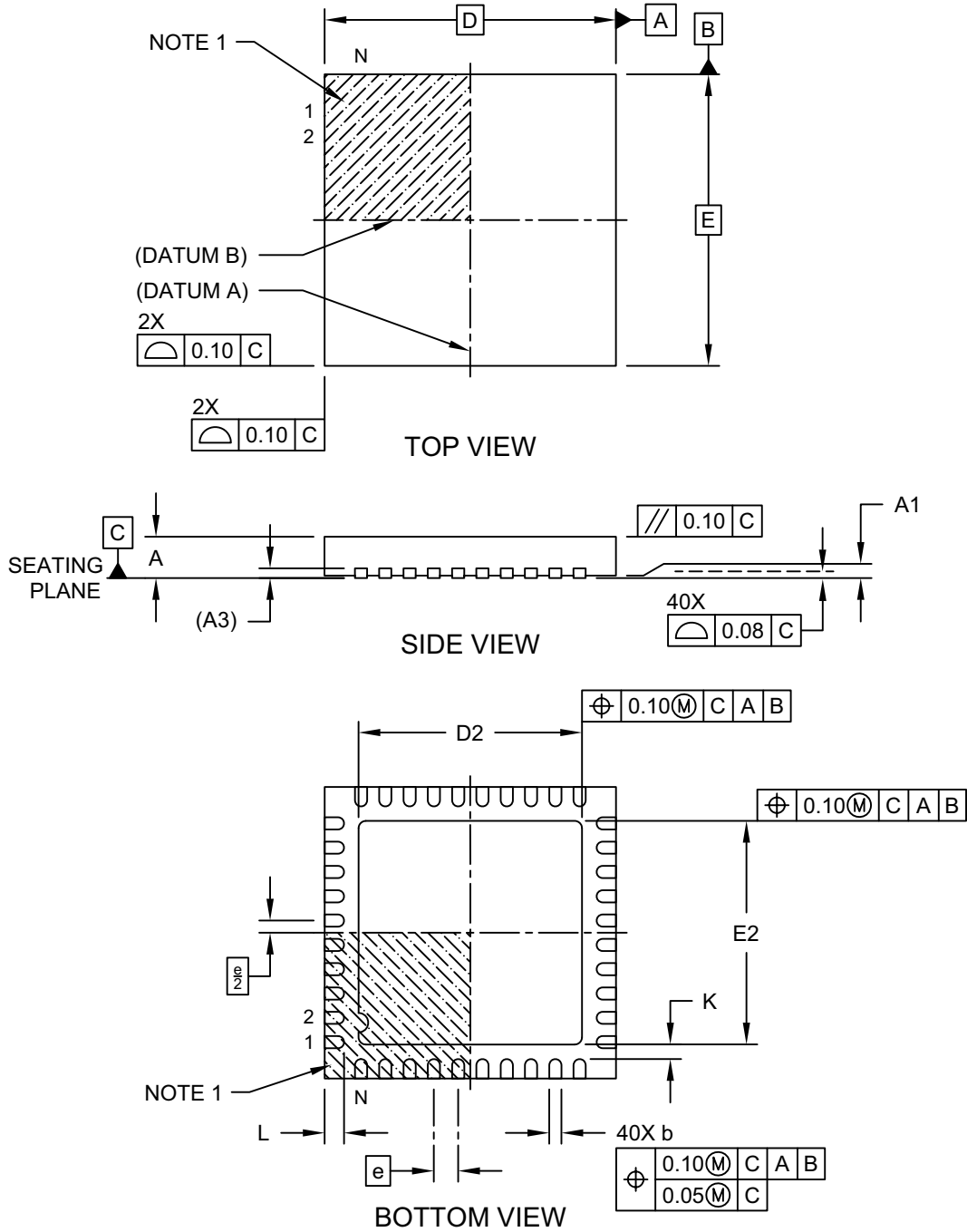


<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( ) and/or Overbar ( ) symbol may not be to scale.	

# MCP22301

## 40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

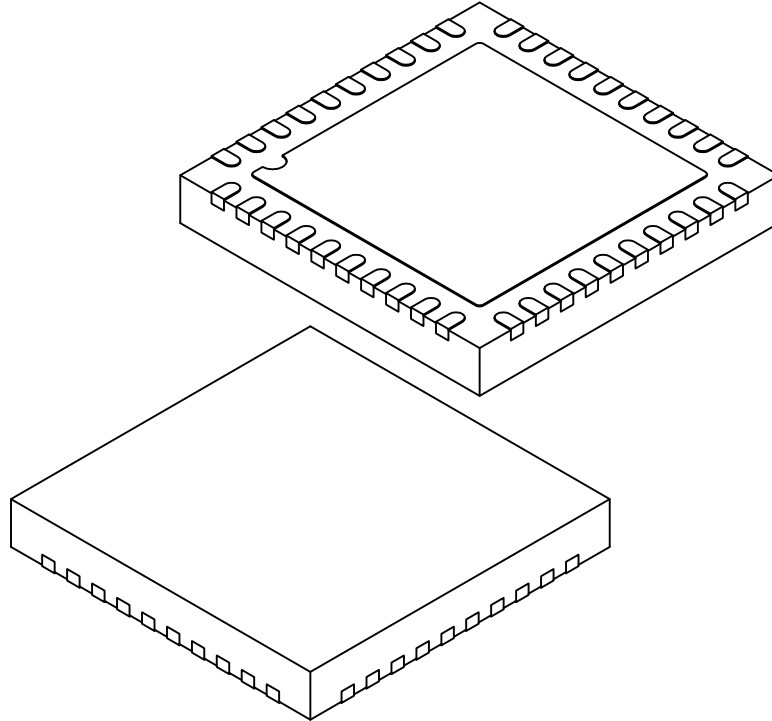


Microchip Technology Drawing C04-473 Rev. A Sheet 1 of 2



## 40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	40		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.07
Terminal Thickness	A3	0.20 REF		
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.50	4.60	4.70
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.50	4.60	4.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

**Notes:**

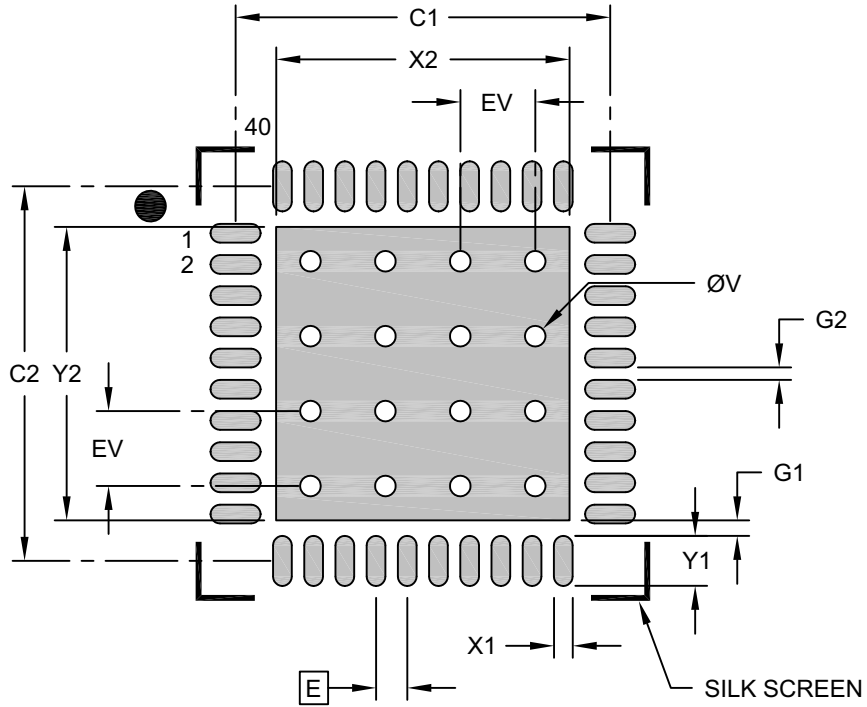
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-473 Rev. A Sheet 2 of 2

# MCP22301

## 40-Lead Very Thin Plastic Quad Flat, No Lead Package (KYX) - 6x6 mm Body [VQFN] With 4.6x4.6 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			4.70
Optional Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X40)	X1			0.30
Contact Pad Length (X40)	Y1			0.80
Contact Pad to Center Pad (X40)	G1	0.20		
Contact Pad to Contact Pad (X36)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2473 Rev. A

## APPENDIX A: REVISION HISTORY

### Revision A (May 2024)

- Initial release of this document.

# MCP22301

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>IXI</u> <sup>(1)</sup>	<u>-X</u>	<u>IXI</u>	<u>/XX</u>
Device	Tape & Reel Option	Version	Temperature Range	Package
<b>Device:</b>	MCP22301: Stand-alone USB Type-C™ Power Delivery 3.1 Controller			
<b>Tape and Reel Option:</b>	Blank = Standard packaging (Tube/Tray) T = Tape and Reel ( <a href="#">Note 1</a> )			
<b>Version:</b>	1 = No Dead Battery Support 2 = With Dead Battery Support			
<b>Temperature Range:</b>	I = -40°C to +85°C (Industrial)			
<b>Package:</b>	KYX = 40-pin 6 mm x 6 mm VQFN			

**Examples:**

- a) MCP22301-1I/KYX  
No Dead Battery Support, Standard Packaging, -40°C to +85°C, 40-pin VQFN Package
- b) MCP22301-2I/KYX  
With Dead Battery Support, Standard Packaging, -40°C to +85°C, 40-pin VQFN Package
- c) MCP22301T-1I/KYX  
No Dead Battery Support, Tape and Reel, -40°C to +85°C, 40-pin VQFN Package
- d) MCP22301T-2I/KYX  
With Dead Battery Support, Tape and Reel, -40°C to +85°C, 40-pin VQFN Package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

# MCP22301

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NOTES:

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