# MCP444X/446X

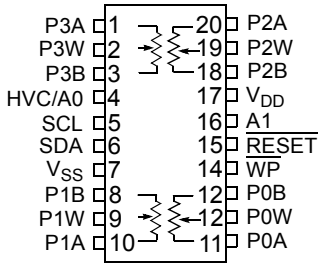
## 7/8-Bit Quad I²C Digital POT with Nonvolatile Memory

### Features

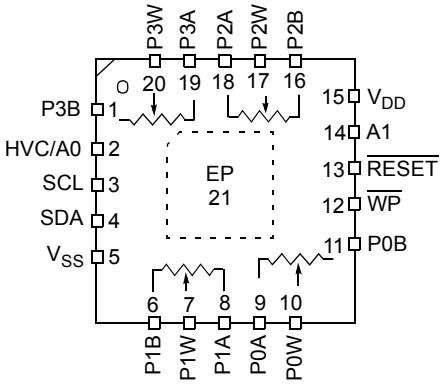
- Quad Resistor Network
- Potentiometer or Rheostat configuration options
- Resistor Network Resolution
  - 7-bit: 128 Resistors (129 Taps)
  - 8-bit: 256 Resistors (257 Taps)
- $R_{AB}$ Resistances options of:
  - 5 kΩ
  - 10 kΩ
  - 50 kΩ
  - 100 kΩ
- Zero Scale to Full Scale Wiper operation
- Low Wiper Resistance: 75 Ω (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- Nonvolatile Memory
  - Automatic Recall of Saved Wiper Setting
  - WiperLock™ Technology
  - 5 General Purpose Memory Locations
- I²C Serial Interface
  - 100 kHz, 400 kHz, and 3.4 MHz support
- Serial protocol allows:
  - High-Speed Read/Write to wiper
  - Read/Write to EEPROM
  - Write Protect to be enabled/disable
  - WiperLock to be enabled/disabled
- Resistor Network Terminal Disconnect Feature via Terminal Control (TCON) Register
- Reset input pin
- Write Protect Feature:
  - Hardware Write Protect ($\overline{WP}$) Control pin
  - Software Write Protect (WP) Configuration bit
- Brown-out reset protection (1.5V typical)
- Serial Interface Inactive current (2.5 uA typical)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Supports Split Rail Applications
- Internal weak pull-up on all digital inputs (except SCL and SDA)
- Wide Operating Voltage:
  - 2.7V to 5.5V - Device Characteristics Specified
  - 1.8V to 5.5V - Device Operation
- Wide Bandwidth (-3 dB) Operation:
  - 2 MHz (typical) for 5.0 kΩ device
- Extended temperature range (-40°C to +125°C)
- Package Types: 4x4 QFN-20, TSSOP-20 and TSSOP-14

### Package Types (Top View)

**MCP44X1** Quad Potentiometers

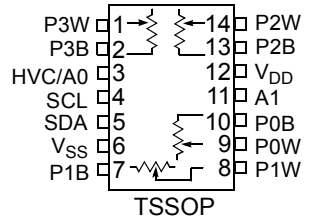



TSSOP



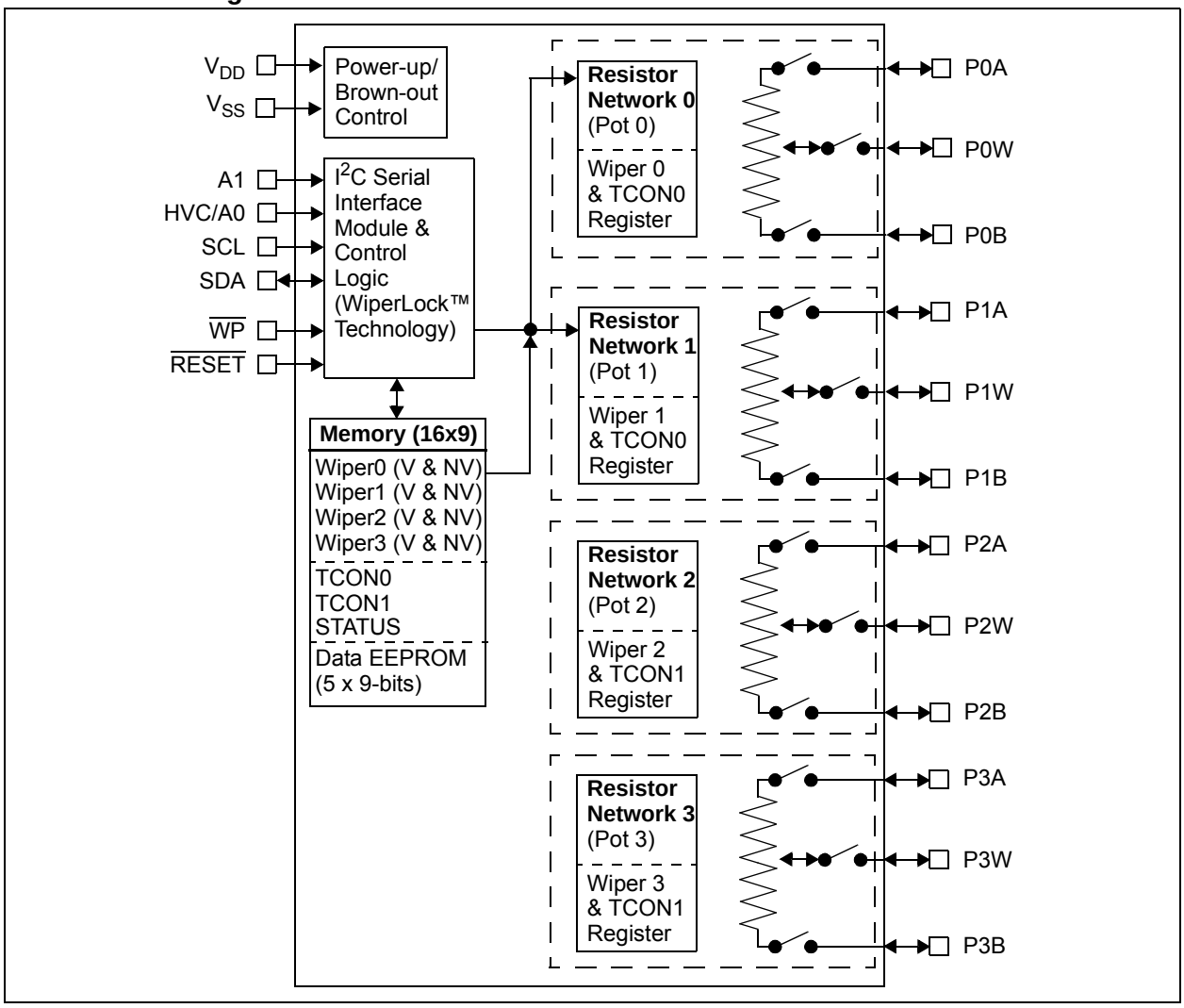

4x4 QFN

**MCP44X2** Quad Rheostat




TSSOP

## Device Block Diagram




## Device Features

| Device | # of POTs | Wiper Configuration | Control | Memory Type | WiperLock Technology | POR Wiper Setting | Resistance (typical) | | # of Taps | $V_{DD}$ Operating Range(2) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | $R_{AB}$ Options (kΩ) | Wiper - $R_W$ (Ω) | | |
| MCP4431(3) | 4 | Potentiometer (1) | I²C | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4432 (3) | 4 | Rheostat | I²C | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4441 | 4 | Potentiometer (1) | I²C | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4442 | 4 | Rheostat | I²C | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4451(3) | 4 | Potentiometer(1) | I²C | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4452(3) | 4 | Rheostat | I²C | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4461 | 4 | Potentiometer(1) | I²C | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |
| MCP4462 | 4 | Rheostat | I²C | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |

**Note 1:** Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

**2:** Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

**3:** Please check Microchip web site for device release and availability.

# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.6V to +7.0V
Voltage on HVC/A0, A1, SCL, SDA, $\overline{WP}$, and $\overline{RESET}$ with respect to $V_{SS}$ ..... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, and PxB) with respect to $V_{SS}$ ..... -0.3V to $V_{DD}$ + 0.3V
Input clamp current, $I_{IK}$ ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ ON HV pins) .....±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) .....±20 mA
Maximum output current sunk by any Output pin .....25 mA
Maximum output current sourced by any Output pin ed .....25 mA
Maximum current out of $V_{SS}$ pin .....100 mA
Maximum current into $V_{DD}$ pin .....100 mA
Maximum current into PxA, PxW & PxB pins .....±2.5 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
Package power dissipation ($T_A$ = +50°C, $T_J$ = +150°C)

- TSSOP-14.....1000 mW
- TSSOP-20.....1110 mW
- QFN-20 (4x4).....2320 mW

Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV (HBM), ..... ≥ 300V (MM)
Maximum Junction Temperature ($T_J$) .....+150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## AC/DC CHARACTERISTICS

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Supply Voltage | $V_{DD}$ | 2.7 | — | 5.5 | V | | |
| | | 1.8 | — | 2.7 | V | Serial Interface only. | |
| HVC/A0, SDA, SCL, A1, WP, RESET pin Voltage Range | $V_{HV}$ | $V_{SS}$ | — | 12.5V | V | $V_{DD} \geq$ 4.5V | The HVC/A0 pin will be at one of three input levels ($V_{IL}$, $V_{IH}$ or $V_{IHH}$). (**Note 6**) |
| | | $V_{SS}$ | — | $V_{DD}$ + 8.0V | V | $V_{DD}$ < 4.5V | |
| $V_{DD}$ Start Voltage to ensure Wiper Reset | $V_{BOR}$ | — | — | 1.65 | V | RAM retention voltage ($V_{RAM}$) < $V_{BOR}$ | |
| $V_{DD}$ Rise Rate to ensure Power-on Reset | $V_{DDRR}$ | (**Note 9**) | | | V/ms | | |
| Delay after device exits the reset state ($V_{DD}$ > $V_{BOR}$) | $T_{BORD}$ | — | 10 | 20 | µs | | |
| Supply Current (**Note 10**) | $I_{DD}$ | — | — | 600 | µA | Serial Interface Active,<br>HVC/A0 = $V_{IH}$ (or $V_{IL}$) (**Note 11**)<br>Write all 0's to volatile Wiper 0<br>$V_{DD}$ = 5.5V, $F_{SCL}$ @ 3.4 MHz | |
| | | — | — | 250 | µA | Serial Interface Active,<br>HVC/A0 = $V_{IH}$ (or $V_{IL}$) (**Note 11**)<br>Write all 0's to volatile Wiper 0<br>$V_{DD}$ = 5.5V, $F_{SCL}$ @ 100 kHz | |
| | | — | — | 575 | µA | EE Write Current (Write Cycle)<br>(Nonvolatile device only),<br>$V_{DD}$ = 5.5V, $F_{SCL}$ = 400 kHz,<br>Write all 0's to Nonvolatile Wiper 0<br>SCL = $V_{IL}$ or $V_{IH}$ | |
| | | — | 2.5 | 5 | µA | Serial Interface Inactive,<br>(Stop condition, SCL = SDA = $V_{IH}$),<br>Wiper = 0<br>$V_{DD}$ = 5.5V, HVC/A0 = $V_{IH}$ | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Resistance (± 20%) | $R_{AB}$ | 4.0 | 5 | 6.0 | kΩ | -502 devices **(Note 1)** | |
| | | 8.0 | 10 | 12.0 | kΩ | -103 devices **(Note 1)** | |
| | | 40.0 | 50 | 60.0 | kΩ | -503 devices **(Note 1)** | |
| | | 80.0 | 100 | 120.0 | kΩ | -104 devices **(Note 1)** | |
| Resolution | N | 257 | | | Taps | 8-bit | No Missing Codes |
| | | 129 | | | Taps | 7-bit | No Missing Codes |
| Step Resistance | $R_S$ | — | $R_{AB}$ / (256) | — | Ω | 8-bit | **Note 6** |
| | | — | $R_{AB}$ / (128) | — | Ω | 7-bit | **Note 6** |
| Nominal Resistance Match | (\| $R_{ABWC}$ - $R_{ABMEAN}$ \|) / $R_{ABMEAN}$ | — | 0.2 | 1.50 | % | 5 kΩ | **MCP44X1** devices only |
| | | — | 0.2 | 1.25 | % | 10 kΩ | |
| | | — | 0.2 | 1.0 | % | 50 kΩ | |
| | | — | 0.2 | 1.0 | % | 100 kΩ | |
| | (\| $R_{BWWC}$ - $R_{BWMEAN}$ \|) / $R_{BWMEAN}$ | — | 0.25 | 1.75 | % | 5 kΩ | Code = Full Scale |
| | | — | 0.25 | 1.50 | % | 10 kΩ | |
| | | — | 0.25 | 1.25 | % | 50 kΩ | |
| | | — | 0.25 | 1.25 | % | 100 kΩ | |
| Wiper Resistance (**Note 3**, **Note 4**) | $R_W$ | — | 75 | 160 | Ω | $V_{DD}$ = 5.5 V, $I_W$ = 2.0 mA, code = 00h | |
| | | — | 75 | 300 | Ω | $V_{DD}$ = 2.7 V, $I_W$ = 2.0 mA, code = 00h | |
| Nominal Resistance Tempco | $\Delta R_{AB}/\Delta T$ | — | 50 | — | ppm/°C | $T_A$ = -20°C to +70°C | |
| | | — | 100 | — | ppm/°C | $T_A$ = -40°C to +85°C | |
| | | — | 150 | — | ppm/°C | $T_A$ = -40°C to +125°C | |
| Ratiometeric Tempco | $\Delta V_{WB}/\Delta T$ | — | 15 | — | ppm/°C | Code = Midscale (80h or 40h) | |
| Resistance Tracking | $\Delta R_{TRACK}$ | **Section 2.0** | | | ppm/°C | See **Typical Performance Curves** | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Resistor Terminal Input Voltage Range (Terminals A, B and W) | $V_A, V_W, V_B$ | Vss | — | $V_{DD}$ | V | **Note 5**, **Note 6** | |
| Maximum current through A, W or B (**Note 6**) | $I_W$ | — | — | 2.5 | mA | Terminal A | $I_{AW}$, W = Full Scale (FS) |
| | | — | — | 2.5 | mA | Terminal B | $I_{BW}$, W = Zero Scale (ZS) |
| | | — | — | 2.5 | mA | Terminal W | $I_{AW}$ (W = FS) or $I_{BW}$ (W = ZS) |
| Maximum $R_{AB}$ current ($I_{AB}$) (**Note 6**) | $I_{AB}$ | — | — | 1.38 | mA | $V_B$ = 0V, $V_A$ = 5.5V, $R_{AB(MIN)}$ = 4000Ω | |
| | | — | — | 0.688 | mA | $V_B$ = 0V, $V_A$ = 5.5V, $R_{AB(MIN)}$ = 8000Ω | |
| | | — | — | 0.138 | mA | $V_B$ = 0V, $V_A$ = 5.5V, $R_{AB(MIN)}$ = 40000Ω | |
| | | — | — | 0.069 | mA | $V_B$ = 0V, $V_A$ = 5.5V, $R_{AB(MIN)}$ = 80000Ω | |
| Leakage current into A, W or B | $I_{WL}$ | — | 100 | — | nA | **MCP44X1** PxA = PxW = PxB = $V_{SS}$ | |
| | | — | 100 | — | nA | **MCP44X2** PxB = PxW = $V_{SS}$ | |
| | | — | 100 | — | nA | Terminals Disconnected<br>(R0A = R0W = R0B = 0;<br>R1A = R1W = R1B = 0;<br>R2A = R2W = R2B = 0;<br>R3A = R3W = R3B = 0) | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Full Scale Error (**MCP44X1** only) (8-bit code = 100h, 7-bit code = 80h) | $V_{WFSE}$ | -6.0 | -0.1 | — | LSb | 5 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -4.0 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -3.5 | -0.1 | — | LSb | 10 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -2.0 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.8 | -0.1 | — | LSb | 50 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | 100 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| Zero Scale Error (**MCP44X1** only) (8-bit code = 00h, 7-bit code = 00h) | $V_{WZSE}$ | — | +0.1 | +6.0 | LSb | 5 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +3.0 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +3.5 | LSb | 10 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +2.0 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.8 | LSb | 50 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | 100 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| Potentiometer Integral Non-linearity | INL | -1 | ±0.5 | +1 | LSb | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V **MCP44X1** devices only **(Note 2)** | |
| | | -0.5 | ±0.25 | +0.5 | LSb | 7-bit | | |
| Potentiometer Differential Non-linearity | DNL | -0.5 | ±0.25 | +0.5 | LSb | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V **MCP44X1** devices only **(Note 2)** | |
| | | -0.25 | ±0.125 | +0.25 | LSb | 7-bit | | |
| Bandwidth -3 dB (See Figure 2-72, load = 30 pF) | BW | — | 2 | — | MHz | 5 kΩ | 8-bit | Code = 80h |
| | | — | 2 | — | MHz | | 7-bit | Code = 40h |
| | | — | 1 | — | MHz | 10 kΩ | 8-bit | Code = 80h |
| | | — | 1 | — | MHz | | 7-bit | Code = 40h |
| | | — | 200 | — | kHz | 50 kΩ | 8-bit | Code = 80h |
| | | — | 200 | — | kHz | | 7-bit | Code = 40h |
| | | — | 100 | — | kHz | 100 kΩ | 8-bit | Code = 80h |
| | | — | 100 | — | kHz | | 7-bit | Code = 40h |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Rheostat Integral Non-linearity **MCP44X1** (**Note 4**, **Note 8**) **MCP44X2** devices only **(Note 4)** | R-INL | -1.5 | ±0.5 | +1.5 | LSb | 5 kΩ | 8-bit | 5.5V, $I_W$ = 900 µA |
| | | -8.25 | +4.5 | +8.25 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 900 µA |
| | | -6.0 | +4.5 | +6.0 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -1.5 | ±0.5 | +1.5 | LSb | 10 kΩ | 8-bit | 5.5V, $I_W$ = 450 µA |
| | | -5.5 | +2.5 | +5.5 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 450 µA |
| | | -4.0 | +2.5 | +4.0 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -1.5 | ±0.5 | +1.5 | LSb | 50 kΩ | 8-bit | 5.5V, $I_W$ = 90 µA |
| | | -2.0 | +1 | +2.0 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 90 µA |
| | | -1.5 | +1 | +1.5 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -1.0 | ±0.5 | +1.0 | LSb | 100 kΩ | 8-bit | 5.5V, $I_W$ = 45 µA |
| | | -1.5 | +0.25 | +1.5 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |
| | | -0.8 | ±0.5 | +0.8 | LSb | | 7-bit | 5.5V, $I_W$ = 45 µA |
| | | -1.125 | +0.25 | +1.125 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Rheostat Differential Non-linearity **MCP44X1** (**Note 4**, **Note 8**) **MCP44X2** devices only (**Note 4**) | R-DNL | -0.5 | ±0.25 | +0.5 | LSb | 5 kΩ | 8-bit | 5.5V, $I_W$ = 900 µA |
| | | -1.0 | +0.5 | +1.0 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 900 µA |
| | | -0.75 | +0.5 | +0.75 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 10 kΩ | 8-bit | 5.5V, $I_W$ = 450 µA |
| | | -1.0 | +0.25 | +1.0 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 450 µA |
| | | -0.75 | +0.5 | +0.75 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 50 kΩ | 8-bit | 5.5V, $I_W$ = 90 µA |
| | | -0.5 | ±0.25 | +0.5 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 90 µA |
| | | -0.375 | ±0.25 | +0.375 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 100 kΩ | 8-bit | 5.5V, $I_W$ = 45 µA |
| | | -0.5 | ±0.25 | +0.5 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 45 µA |
| | | -0.375 | ±0.25 | +0.375 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |
| Capacitance ($P_A$) | $C_{AW}$ | — | 75 | — | pF | f =1 MHz, Code = Full Scale | | |
| Capacitance ($P_w$) | $C_W$ | — | 120 | — | pF | f =1 MHz, Code = Full Scale | | |
| Capacitance ($P_B$) | $C_{BW}$ | — | 75 | — | pF | f =1 MHz, Code = Full Scale | | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| **Digital Inputs/Outputs (HVC/A0, A1, SDA, SCL, $\overline{WP}$, $\overline{RESET}$)** | | | | | | | |
| Schmitt Trigger High Input Threshold | $V_{IH}$ | 0.45 $V_{DD}$ | — | — | V | All Inputs except SDA and SCL | 2.7V ≤ $V_{DD}$ ≤ 5.5V (Allows 2.7V Digital $V_{DD}$ with 5V Analog $V_{DD}$) |
| | | 0.5 $V_{DD}$ | — | — | V | | 1.8V ≤ $V_{DD}$ ≤ 2.7V |
| | | 0.7 $V_{DD}$ | — | $V_{MAX}$ | V | SDA and SCL | 100 kHz |
| | | 0.7 $V_{DD}$ | — | $V_{MAX}$ | V | | 400 kHz |
| | | 0.7 $V_{DD}$ | — | $V_{MAX}$ | V | | 1.7 MHz |
| | | 0.7 $V_{DD}$ | — | $V_{MAX}$ | V | | 3.4 Mhz |
| Schmitt Trigger Low Input Threshold | $V_{IL}$ | — | — | 0.2$V_{DD}$ | V | All inputs except SDA and SCL | |
| | | -0.5 | — | 0.3$V_{DD}$ | V | SDA and SCL | 100 kHz |
| | | -0.5 | — | 0.3$V_{DD}$ | V | | 400 kHz |
| | | -0.5 | — | 0.3$V_{DD}$ | V | | 1.7 MHz |
| | | -0.5 | — | 0.3$V_{DD}$ | V | | 3.4 Mhz |
| Hysteresis of Schmitt Trigger Inputs | $V_{HYS}$ | — | 0.1$V_{DD}$ | — | V | All inputs except SDA and SCL | |
| | | N.A. | — | — | V | SDA and SCL | 100 kHz, $V_{DD}$ < 2.0V |
| | | N.A. | — | — | V | | 100 kHz, $V_{DD}$ ≥ 2.0V |
| | | 0.1 $V_{DD}$ | — | — | V | | 400 kHz, $V_{DD}$ < 2.0V |
| | | 0.05 $V_{DD}$ | — | — | V | | 400 kHz, $V_{DD}$ ≥ 2.0V |
| | | 0.1 $V_{DD}$ | — | — | V | | 1.7 MHz |
| | | 0.1 $V_{DD}$ | — | — | V | | 3.4 Mhz |
| High Voltage Input Entry Voltage | $V_{IHHEN}$ | 9.0 | — | 12.5 **(Note 6)** | V | Threshold for WiperLock Technology | |
| High Voltage Input Exit Voltage | $V_{IHHEX}$ | — | — | $V_{DD}$ + 0.8V **(Note 6)** | V | | |
| High Voltage Limit | $V_{MAX}$ | — | — | 12.5 **(Note 6)** | V | Pin can tolerate $V_{MAX}$ or less. | |
| Output Low Voltage (SDA) | $V_{OL}$ | $V_{SS}$ | — | 0.2$V_{DD}$ | V | $V_{DD}$ < 2.0V, $I_{OL}$ = 1 mA, | |
| | | $V_{SS}$ | — | 0.4 | V | $V_{DD}$ ≥ 2.0V, $I_{OL}$ = 3 mA | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Weak Pull-up Current | $I_{PU}$ | — | — | 1.75 | mA | Internal $V_{DD}$ pull-up, $V_{IHH}$ pull-down, $V_{DD}$ = 5.5V, $V_{HVC}$ = 12.5V | |
| | | — | 170 | — | µA | HVC pin, $V_{DD}$ = 5.5V, $V_{HVC}$ = 3V | |
| HVC Pull-up / Pull-down Resistance | $R_{HVC}$ | — | 16 | — | kΩ | $V_{DD}$ = 5.5V, $V_{HVC}$ = 3V | |
| $\overline{\text{RESET}}$ Pull-up Resistance | $R_{RESET}$ | — | 16 | — | kΩ | $V_{DD}$ = 5.5V, $V_{\overline{\text{RESET}}}$ = 0V | |
| Input Leakage Current | $I_{IL}$ | -1 | — | 1 | µA | $V_{IN}$ = $V_{DD}$ (all pins) and $V_{IN}$ = $V_{SS}$ (all pins except $\overline{\text{RESET}}$) | |
| Pin Capacitance | $C_{IN}$, $C_{OUT}$ | — | 10 | — | pF | $f_C$ = 20 MHz | |
| **RAM (Wiper, TCON) Value** | | | | | | | |
| Value Range | N | 0h | — | 1FFh | hex | 8-bit device | |
| | | 0h | — | 1FFh | hex | 7-bit device | |
| TCON POR/BOR Setting | | 1FF | | | hex | All Terminals connected | |
| **EEPROM** | | | | | | | |
| Endurance | $E_{ndurance}$ | — | 1M | — | Cycles | | |
| EEPROM Range | N | 0h | — | 1FFh | hex | | |
| Initial NV Wiper POR/BOR Setting | N | 080h | | | hex | 8-bit | WiperLock Technology = Off |
| | | 040h | | | hex | 7-bit | WiperLock Technology = Off |
| Initial EEPROM POR/BOR Setting | N | 000h | | | hex | | |
| EEPROM Programming Write Cycle Time | $t_{WC}$ | — | 3 | 10 | ms | | |
| **Power Requirements** | | | | | | | |
| Power Supply Sensitivity (**MCP44X1**) | PSS | — | 0.0015 | 0.0035 | %/% | 8-bit | $V_{DD}$ = 2.7V to 5.5V, $V_A$ = 2.7V, Code = 80h |
| | | — | 0.0015 | 0.0035 | %/% | 7-bit | $V_{DD}$ = 2.7V to 5.5V, $V_A$ = 2.7V, Code = 40h |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP44X1** only.

**4:** **MCP44X2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network.

**11:** When HVC/A0 = $V_{IHH}$, the $I_{DD}$ current is less due to current into the HVC/A0 pin. See $I_{PU}$ specification.

## 1.1 I²C Mode Timing Waveforms and Requirements

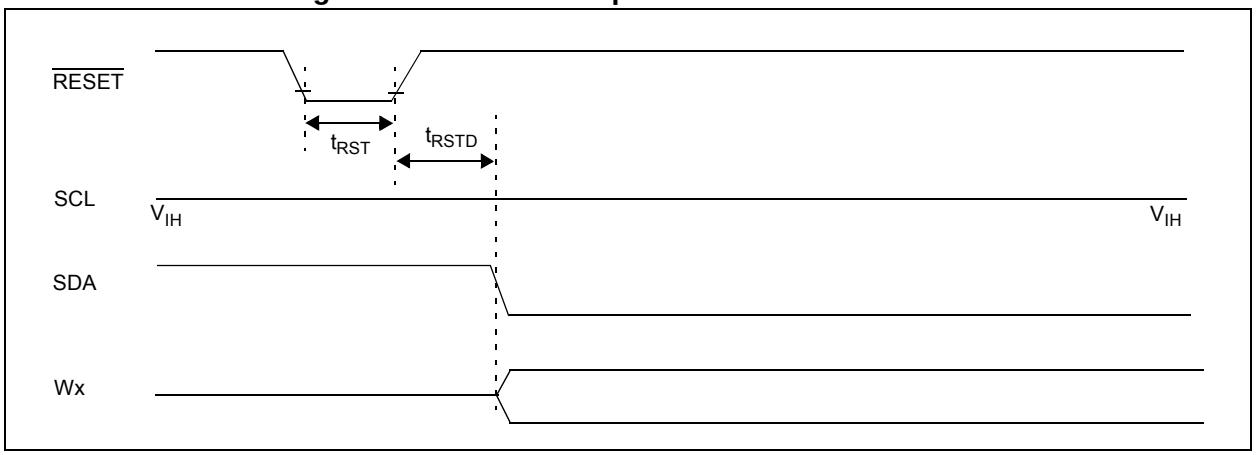



***FIGURE 1-1:*** *RESET Waveforms.*

**TABLE 1-1: RESET TIMING**

| **Timing Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| $\overline{\text{RESET}}$ pulse width | $t_{RST}$ | 50 | — | — | ns | |
| $\overline{\text{RESET}}$ rising edge normal mode (Wiper driving and I²C interface operational) | $t_{RSTD}$ | — | — | 20 | ns | |

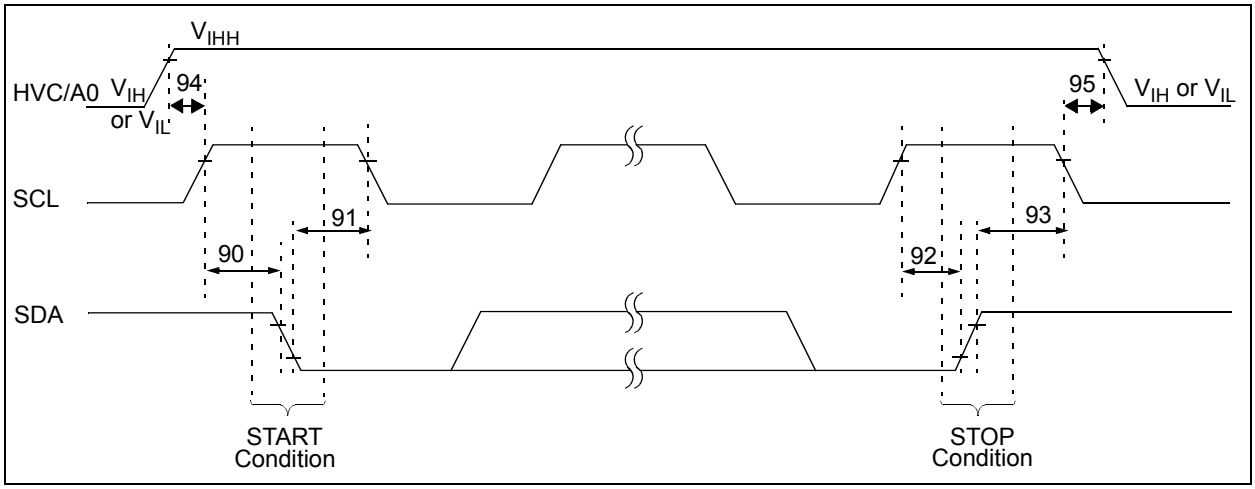



***FIGURE 1-2:*** *$I^2C$ Bus Start/Stop Bits Timing Waveforms.*

**TABLE 1-2: $I^2C$ BUS START/STOP BITS REQUIREMENTS**

| **$I^2C$ AC Characteristics** | | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage VDD range is described in **AC/DC characteristics** | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| | $F_{SCL}$ | | Standard Mode | 0 | 100 | kHz | $C_b$ = 400 pF, 1.8V - 5.5V |
| | | | Fast Mode | 0 | 400 | kHz | $C_b$ = 400 pF, 2.7V - 5.5V |
| | | | High-Speed 1.7 | 0 | 1.7 | MHz | $C_b$ = 400 pF, 4.5V - 5.5V |
| | | | High-Speed 3.4 | 0 | 3.4 | MHz | $C_b$ = 100 pF, 4.5V - 5.5V |
| D102 | Cb | Bus capacitive loading | 100 kHz mode | — | 400 | pF | |
| | | | 400 kHz mode | — | 400 | pF | |
| | | | 1.7 MHz mode | — | 400 | pF | |
| | | | 3.4 MHz mode | — | 100 | pF | |
| 90 | TSU:STA | START condition Setup time | 100 kHz mode | 4700 | — | ns | Only relevant for repeated START condition |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 91 | THD:STA | START condition Hold time | 100 kHz mode | 4000 | — | ns | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 92 | TSU:STO | STOP condition Setup time | 100 kHz mode | 4000 | — | ns | |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 93 | THD:STO | STOP condition Hold time | 100 kHz mode | 4000 | — | ns | |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 94 | $T_{HVCSU}$ | HVC to SCL Setup time | | 25 | — | uS | High Voltage Commands |
| 95 | $T_{HVCHD}$ | SCL to HVC Hold time | | 25 | — | uS | High Voltage Commands |

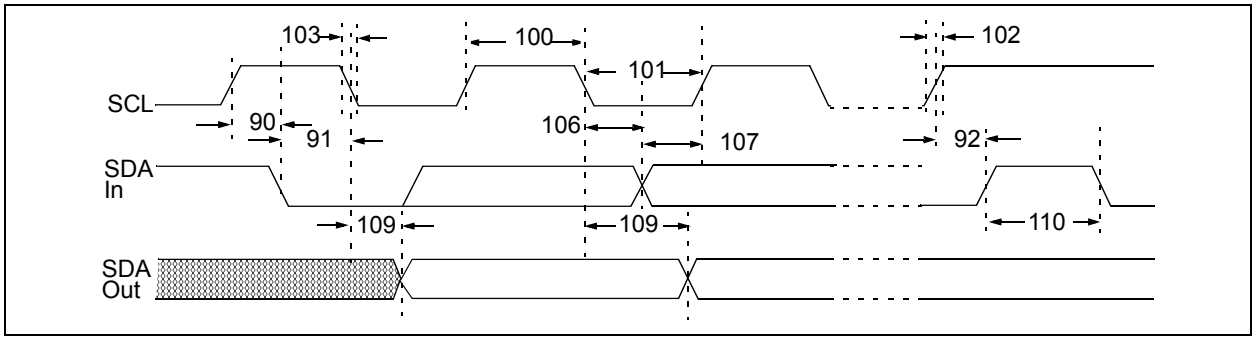



***FIGURE 1-3:*** *$I^2C$ Bus Data Timing.*

**TABLE 1-3: $I^2C$ BUS DATA REQUIREMENTS (SLAVE MODE)**

| **$I^2C$ AC Characteristics** | | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage $V_{DD}$ range is described in **AC/DC characteristics** | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| 100 | THIGH | Clock high time | 100 kHz mode | 4000 | — | ns | 1.8V-5.5V |
| | | | 400 kHz mode | 600 | — | ns | 2.7V-5.5V |
| | | | 1.7 MHz mode | 120 | | ns | 4.5V-5.5V |
| | | | 3.4 MHz mode | 60 | — | ns | 4.5V-5.5V |
| 101 | TLOW | Clock low time | 100 kHz mode | 4700 | — | ns | 1.8V-5.5V |
| | | | 400 kHz mode | 1300 | — | ns | 2.7V-5.5V |
| | | | 1.7 MHz mode | 320 | | ns | 4.5V-5.5V |
| | | | 3.4 MHz mode | 160 | — | ns | 4.5V-5.5V |

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**2:** A fast-mode (400 kHz) $I^2C$-bus device can be used in a standard-mode (100 kHz) $I^2C$-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
$T_R$ max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode $I^2C$ bus specification) before the SCL line is released.

**3:** The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between $V_{IH}$ and $V_{IL}$ of the falling edge of the SCL signal. This specification is not a part of the $I^2C$ specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**4:** Use Cb in pF for the calculations.

**5:** Not Tested.

**6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

**7:** Ensured by the $T_{AA}$ 3.4 MHz specification test.

**TABLE 1-3: $I^2C$ BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| $I^2C$ AC Characteristics | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage $V_{DD}$ range is described in **AC/DC characteristics** | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| 102A (5) | $T_{RSCL}$ | SCL rise time | 100 kHz mode | — | 1000 | ns | Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1Cb | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 80 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | After a Repeated Start condition or an Acknowledge bit |
| | | | 3.4 MHz mode | 10 | 40 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | After a Repeated Start condition or an Acknowledge bit |
| 102B (5) | $T_{RSDA}$ | SDA rise time | 100 kHz mode | — | 1000 | ns | Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1Cb | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | |
| 103A (5) | $T_{FSCL}$ | SCL fall time | 100 kHz mode | — | 300 | ns | Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1Cb | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 80 | ns | |
| | | | 3.4 MHz mode | 10 | 40 | ns | |
| 103B (5) | $T_{FSDA}$ | SDA fall time | 100 kHz mode | — | 300 | ns | Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1Cb (4) | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | |
| 106 | $T_{HD:DAT}$ | Data input hold time | 100 kHz mode | 0 | — | ns | 1.8V-5.5V, **Note 6** |
| | | | 400 kHz mode | 0 | — | ns | 2.7V-5.5V, **Note 6** |
| | | | 1.7 MHz mode | 0 | — | ns | 4.5V-5.5V, **Note 6** |
| | | | 3.4 MHz mode | 0 | — | ns | 4.5V-5.5V, **Note 6** |

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**2:** A fast-mode (400 kHz) $I^2C$-bus device can be used in a standard-mode (100 kHz) $I^2C$-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
$T_R$ max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode $I^2C$ bus specification) before the SCL line is released.

**3:** The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between $V_{IH}$ and $V_{IL}$ of the falling edge of the SCL signal. This specification is not a part of the $I^2C$ specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**4:** Use Cb in pF for the calculations.

**5:** Not Tested.

**6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

**7:** Ensured by the $T_{AA}$ 3.4 MHz specification test.

**TABLE 1-3: $I^2C$ BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| $I^2C$ AC Characteristics | | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C (Extended)<br>Operating Voltage $V_{DD}$ range is described in **AC/DC characteristics** | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| 107 | $T_{SU:DAT}$ | Data input setup time | 100 kHz mode | 250 | — | ns | **Note 2** |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1.7 MHz mode | 10 | — | ns | |
| | | | 3.4 MHz mode | 10 | — | ns | |
| 109 | $T_{AA}$ | Output valid from clock | 100 kHz mode | — | 3450 | ns | **Note 1** |
| | | | 400 kHz mode | — | 900 | ns | |
| | | | 1.7 MHz mode | — | 150 | ns | Cb = 100 pF, **Note 1**, **Note 7** |
| | | | | — | 310 | ns | Cb = 400 pF, **Note 1**, **Note 5** |
| | | | 3.4 MHz mode | — | 150 | ns | Cb = 100 pF, **Note 1** |
| 110 | $T_{BUF}$ | Bus free time | 100 kHz mode | 4700 | — | ns | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1300 | — | ns | |
| | | | 1.7 MHz mode | N.A. | — | ns | |
| | | | 3.4 MHz mode | N.A. | — | ns | |
| | $T_{SP}$ | Input filter spike suppression (SDA and SCL) | 100 kHz mode | — | 50 | ns | Philips Spec states N.A. |
| | | | 400 kHz mode | — | 50 | ns | |
| | | | 1.7 MHz mode | — | 10 | ns | Spike suppression |
| | | | 3.4 MHz mode | — | 10 | ns | Spike suppression |

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**2:** A fast-mode (400 kHz) $I^2C$-bus device can be used in a standard-mode (100 kHz) $I^2C$-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
$T_R$ max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode $I^2C$ bus specification) before the SCL line is released.

**3:** The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between $V_{IH}$ and $V_{IL}$ of the falling edge of the SCL signal. This specification is not a part of the $I^2C$ specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

**4:** Use Cb in pF for the calculations.

**5:** Not Tested.

**6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

**7:** Ensured by the $T_{AA}$ 3.4 MHz specification test.

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = +2.7V to +5.5V, $V_{SS}$ = GND. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |
| Thermal Resistance, 20L-QFN | $\theta_{JA}$ | — | 43 | — | °C/W | |
| Thermal Resistance, 20L-TSSOP | $\theta_{JA}$ | — | 90 | — | °C/W | |

**NOTES:**

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

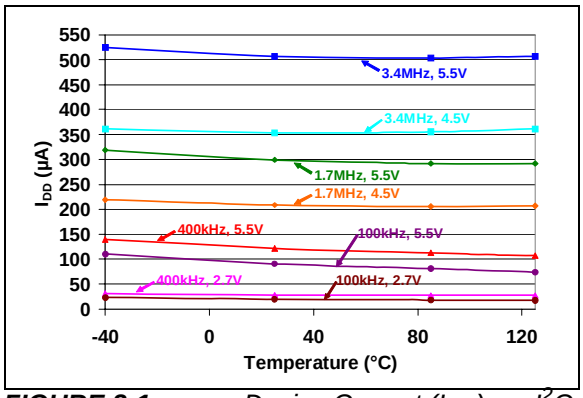



***FIGURE 2-1:*** *Device Current ($I_{DD}$) vs. $I^2C$ Frequency ($f_{SCL}$) and Ambient Temperature ($V_{DD}$ = 2.7V and 5.5V).*

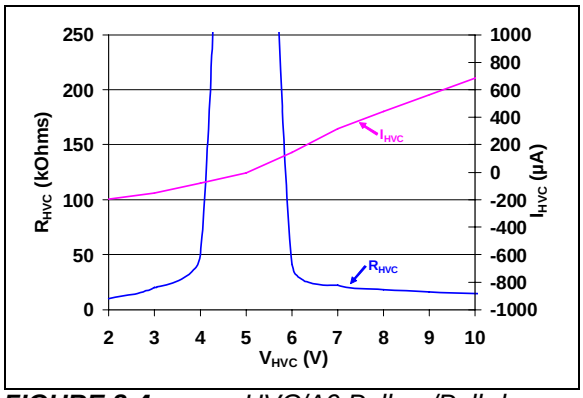



***FIGURE 2-4:*** *HVC/A0 Pull-up/Pull-down Resistance ($R_{HVC}$) and Current ($I_{HVC}$) vs. HVC/A0 Input Voltage ($V_{HVC}$) ($V_{DD}$ = 5.5V).*

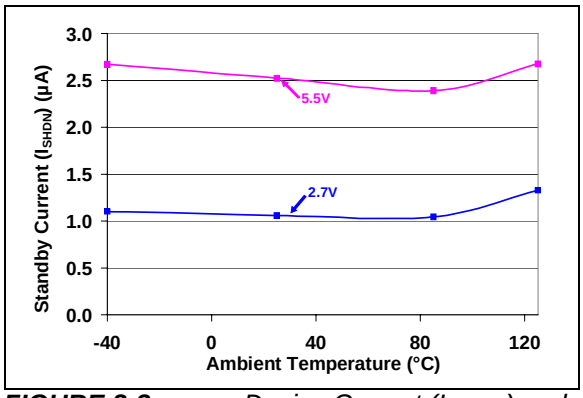



***FIGURE 2-2:*** *Device Current ($I_{SHDN}$) and $V_{DD}$. (HVC/A0 = $V_{DD}$) vs. Ambient Temperature.*

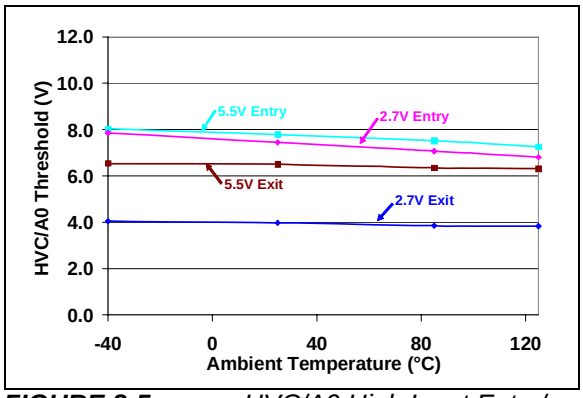



***FIGURE 2-5:*** *HVC/A0 High Input Entry/Exit Threshold vs. Ambient Temperature and $V_{DD}$.*

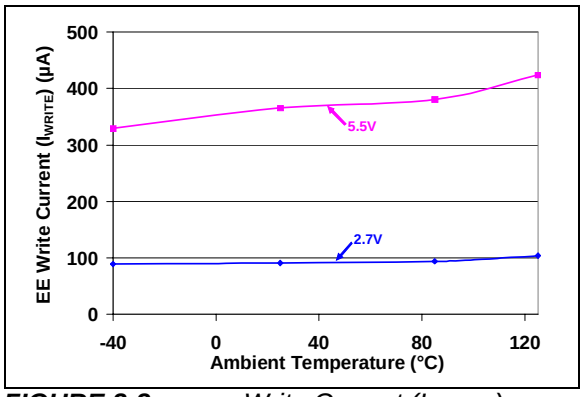



***FIGURE 2-3:*** *Write Current ($I_{WRITE}$) vs. Ambient Temperature and $V_{DD}$.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

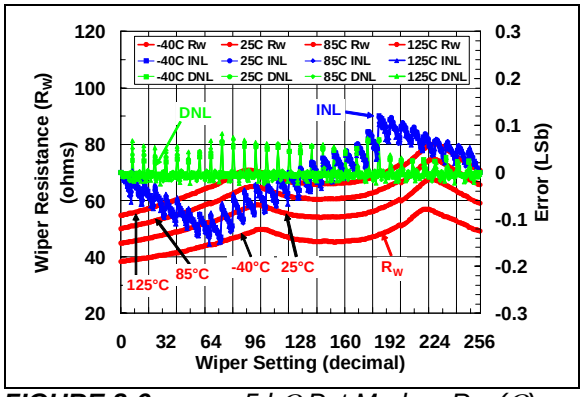



***FIGURE 2-6:*** *5 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

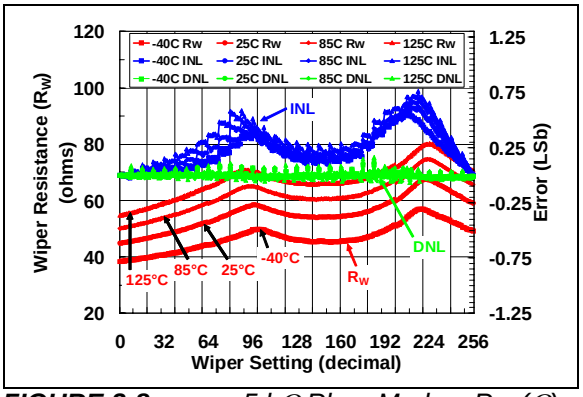



***FIGURE 2-8:*** *5 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

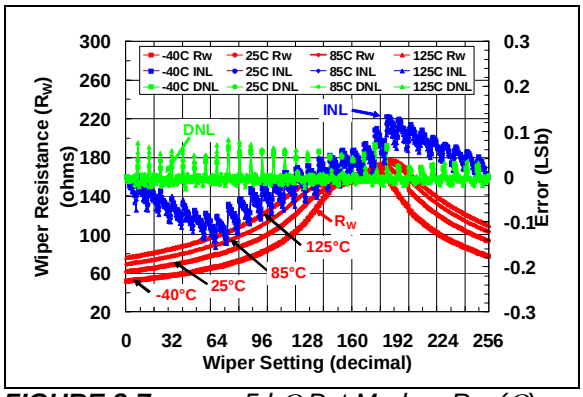



***FIGURE 2-7:*** *5 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

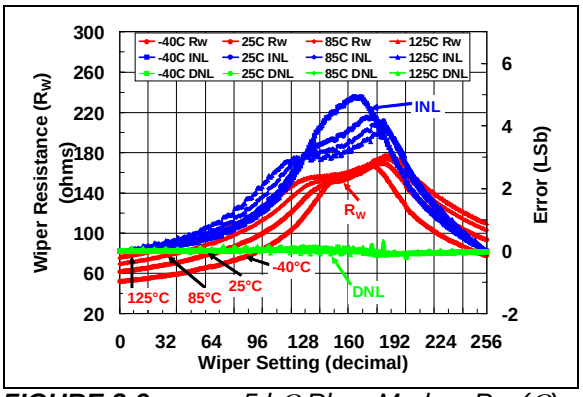



***FIGURE 2-9:*** *5 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

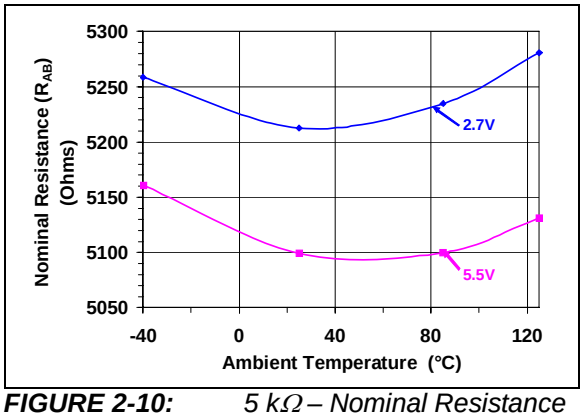



***FIGURE 2-10:*** *5 kΩ – Nominal Resistance ($R_{AB}$) (Ω) vs. Ambient Temperature and $V_{DD}$.*

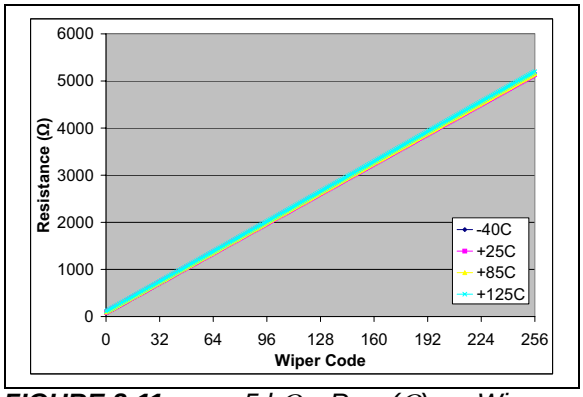



***FIGURE 2-11:*** *5 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V, $I_W$ = 190 µA).*

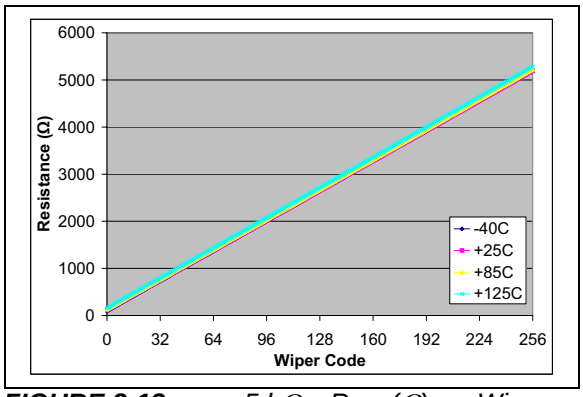



***FIGURE 2-12:*** *5 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V, $I_W$ = 190 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

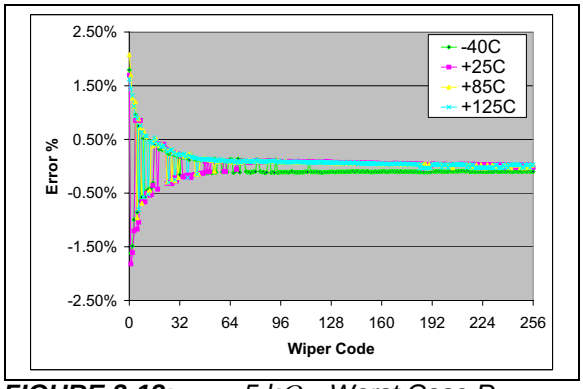



***FIGURE 2-13:*** *5 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 5.5V, $I_W$ = 190 µA).*

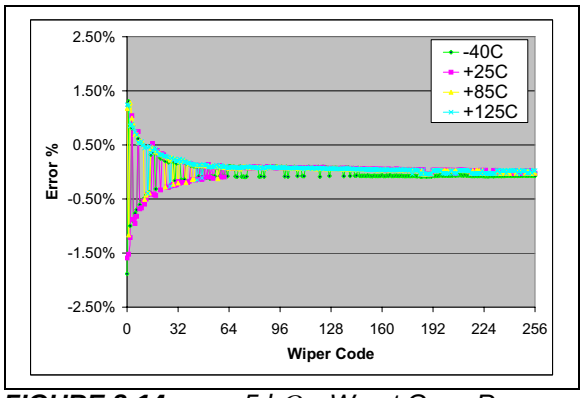



***FIGURE 2-14:*** *5 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 3.0V, $I_W$ = 190 µA).*

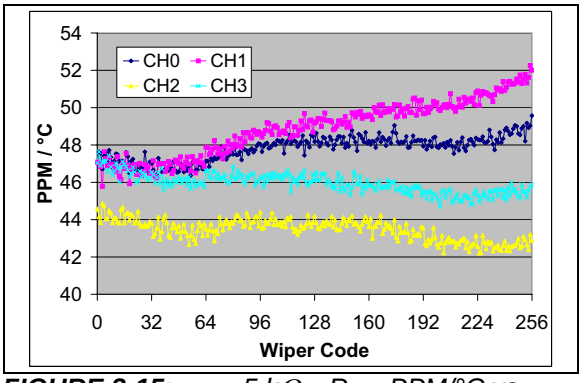



***FIGURE 2-15:*** *5 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, $I_W$ = 190 µA).*

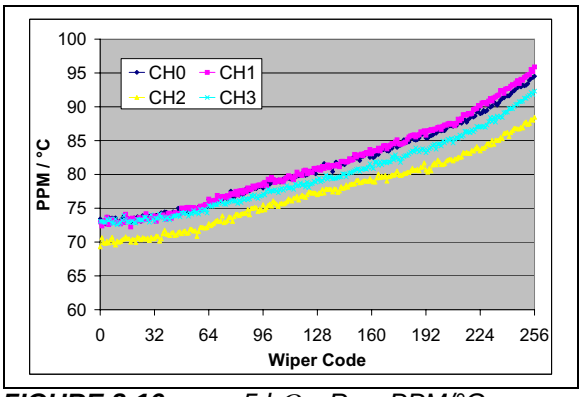



***FIGURE 2-16:*** *5 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, $I_W$ = 190 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

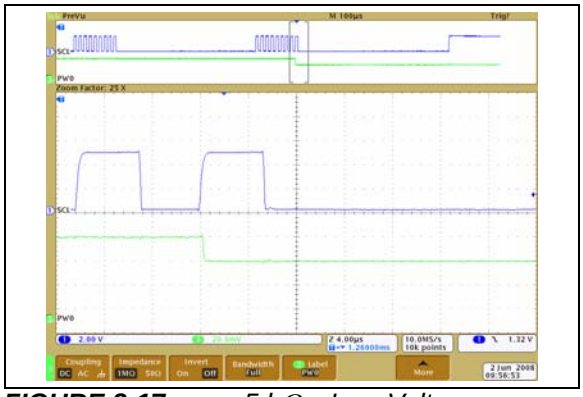


***FIGURE 2-17:*** *5 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

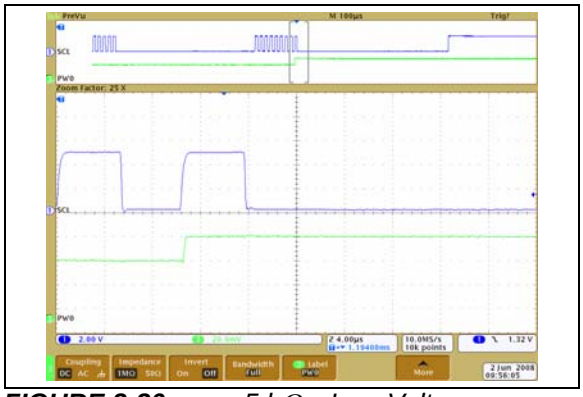


***FIGURE 2-20:*** *5 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

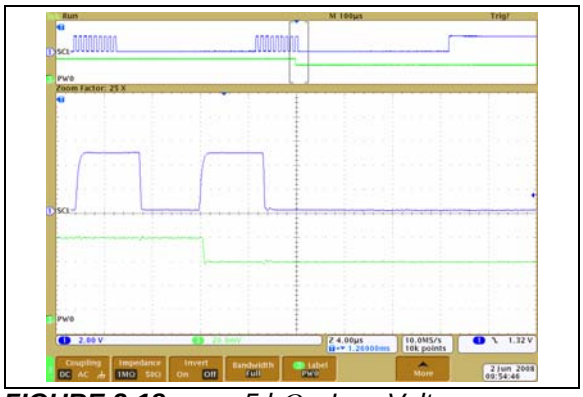


***FIGURE 2-18:*** *5 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

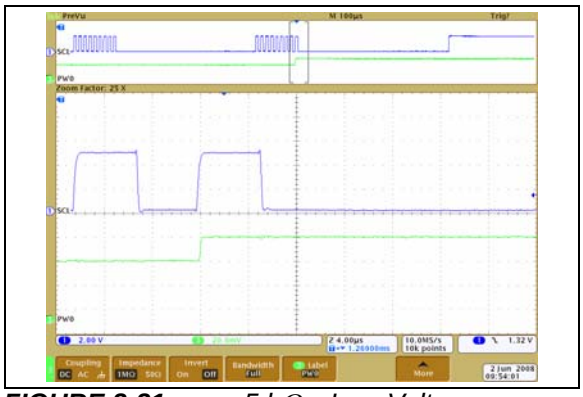


***FIGURE 2-21:*** *5 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

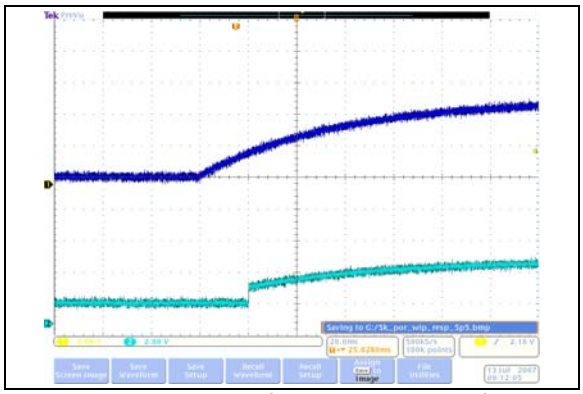


***FIGURE 2-19:*** *5 kΩ – Power-Up Wiper Response Time (20 ms/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

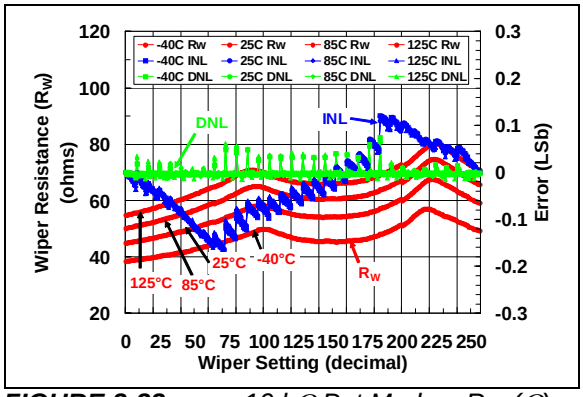



***FIGURE 2-22:*** *10 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

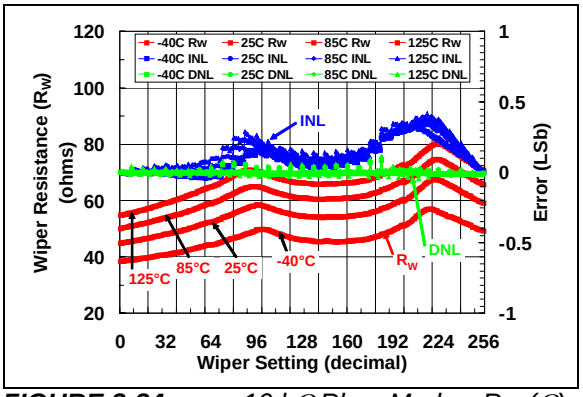



***FIGURE 2-24:*** *10 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

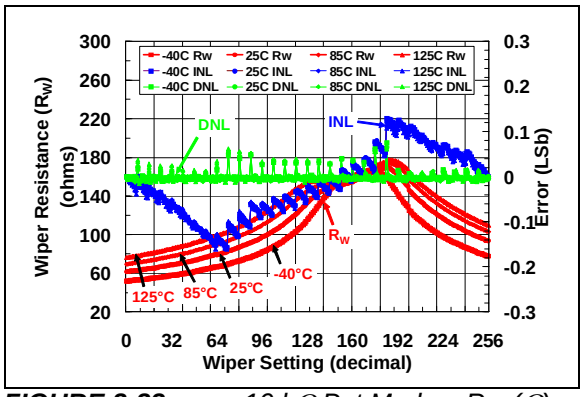



***FIGURE 2-23:*** *10 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

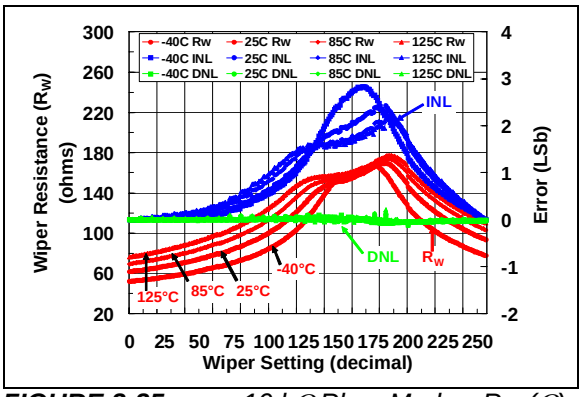



***FIGURE 2-25:*** *10 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

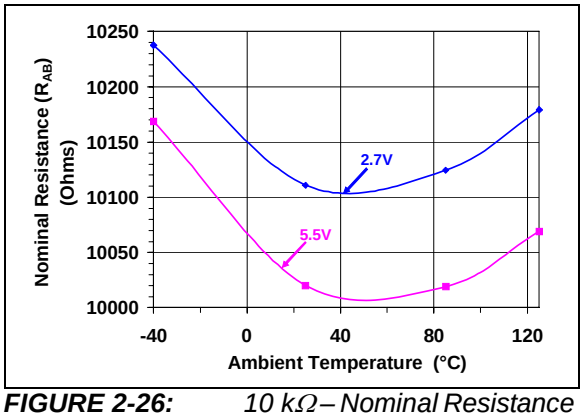



***FIGURE 2-26:*** *10 kΩ – Nominal Resistance ($R_{AB}$) (Ω) vs. Ambient Temperature and $V_{DD}$.*

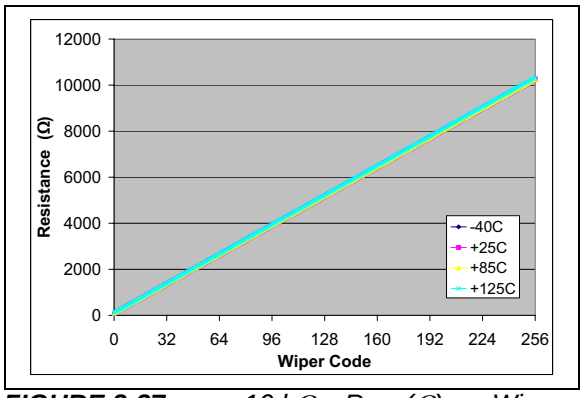



***FIGURE 2-27:*** *10 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V, $I_W$ = 150 µA).*

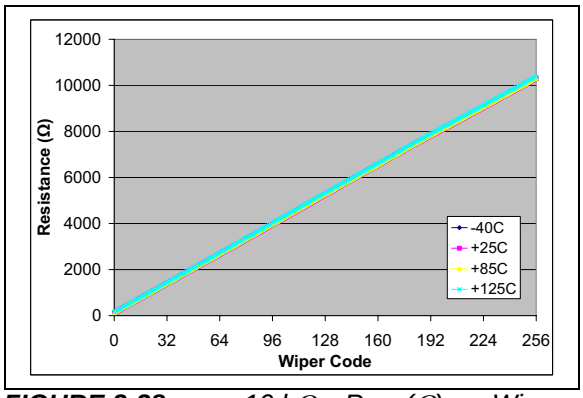



***FIGURE 2-28:*** *10 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V, $I_W$ = 150 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

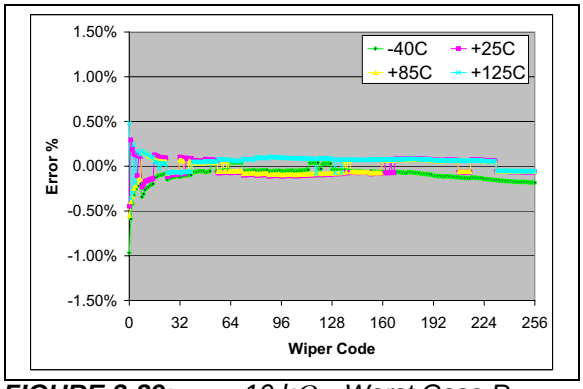



***FIGURE 2-29:*** *10 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 5.5V, $I_W$ = 150 µA).*

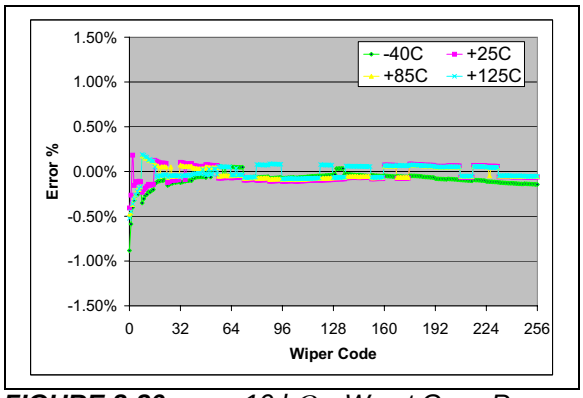



***FIGURE 2-30:*** *10 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 3.0V, $I_W$ = 150 µA).*

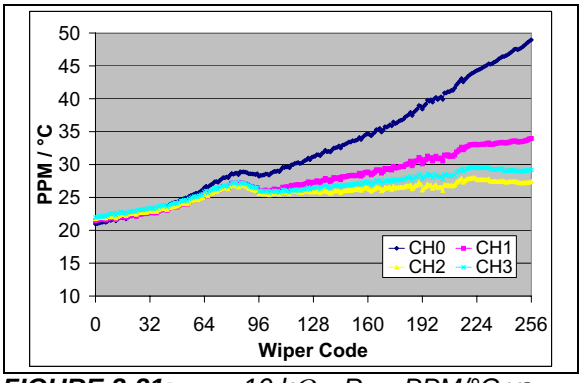



***FIGURE 2-31:*** *10 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, $I_W$ = 150 µA).*

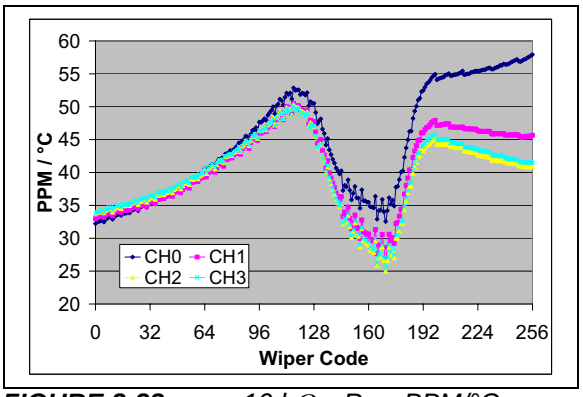



***FIGURE 2-32:*** *10 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, $I_W$ = 150 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

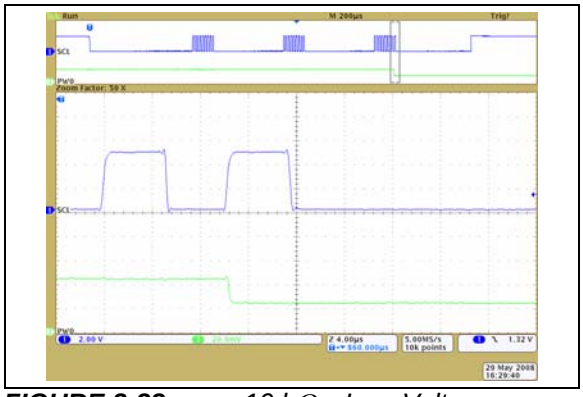


***FIGURE 2-33:*** *10 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

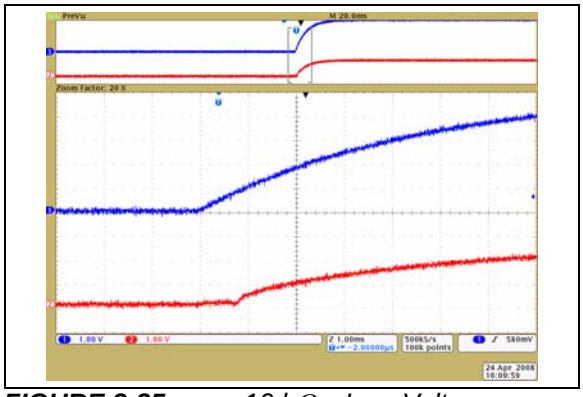


***FIGURE 2-35:*** *10 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

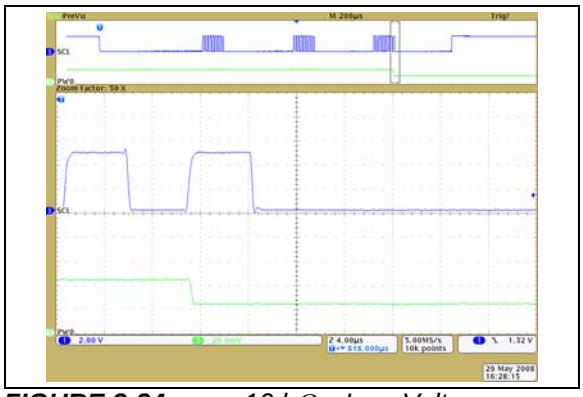


***FIGURE 2-34:*** *10 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

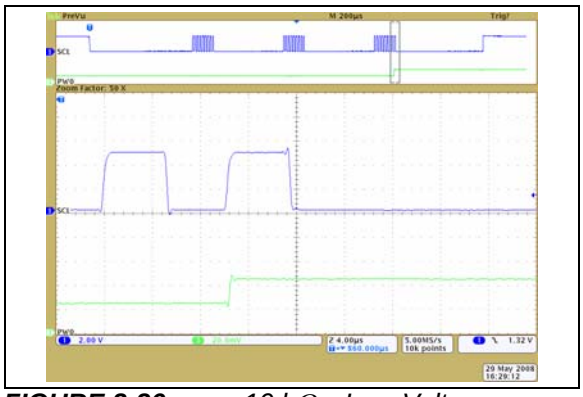


***FIGURE 2-36:*** *10 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

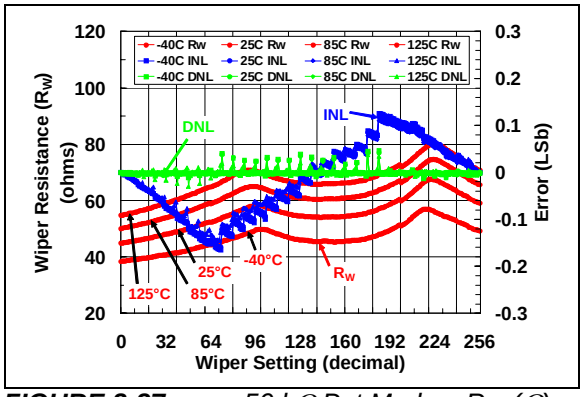



***FIGURE 2-37:*** *50 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

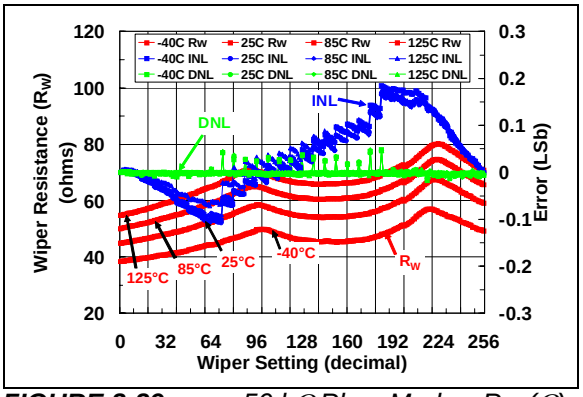



***FIGURE 2-39:*** *50 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

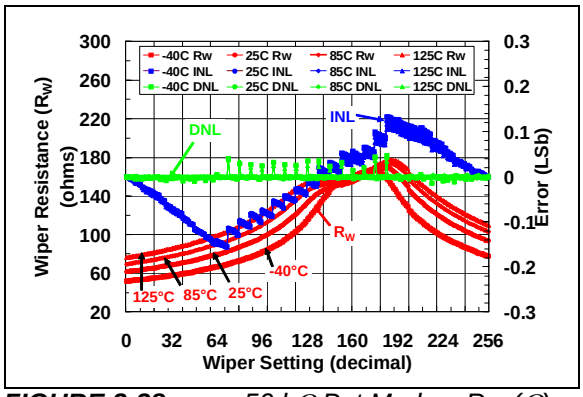



***FIGURE 2-38:*** *50 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

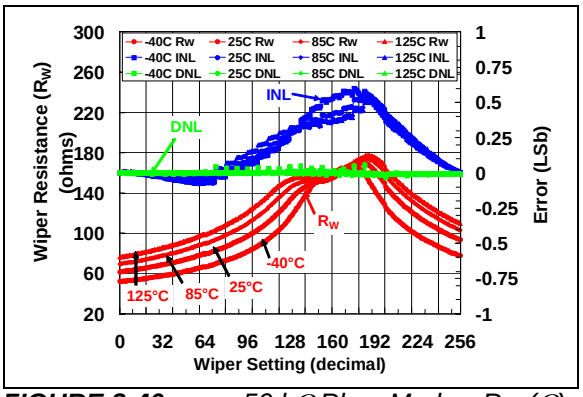



***FIGURE 2-40:*** *50 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

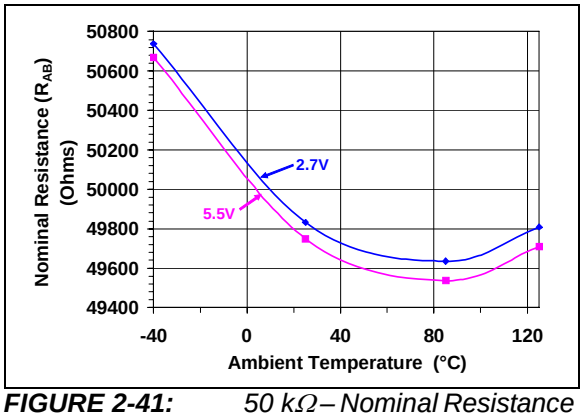



***FIGURE 2-41:*** *50 kΩ – Nominal Resistance ($R_{AB}$) (Ω) vs. Ambient Temperature and $V_{DD}$.*

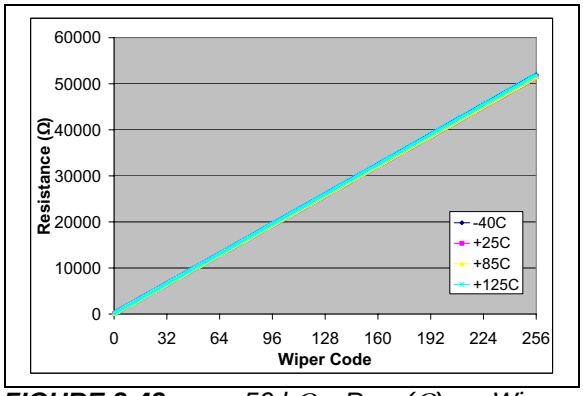



***FIGURE 2-42:*** *50 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V, $I_W$ = 90 µA).*

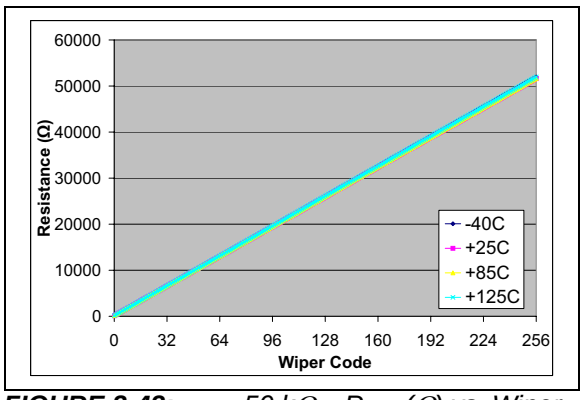



***FIGURE 2-43:*** *50 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V, $I_W$ = 48 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

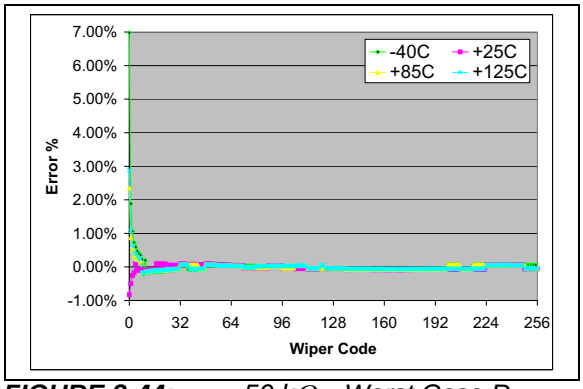



***FIGURE 2-44:*** *50 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 5.5V, $I_W$ = 90 µA).*

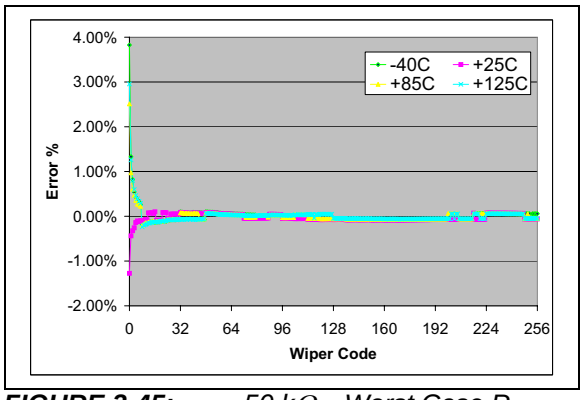



***FIGURE 2-45:*** *50 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 3.0V, $I_W$ = 48 µA).*

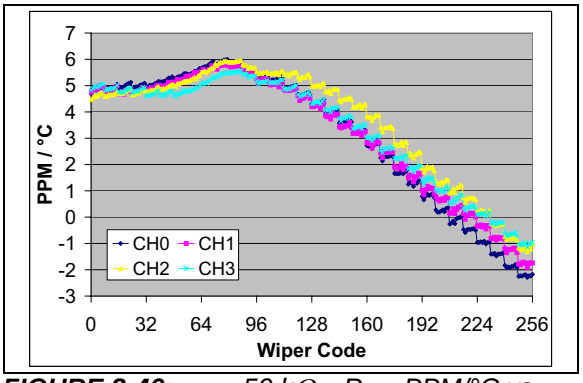



***FIGURE 2-46:*** *50 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, $I_W$ = 90 µA).*

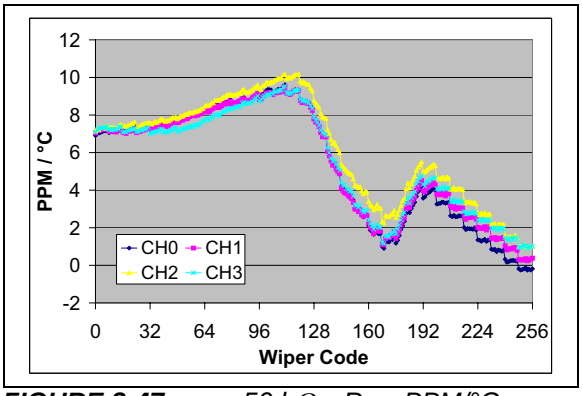



***FIGURE 2-47:*** *50 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, $I_W$ = 48 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

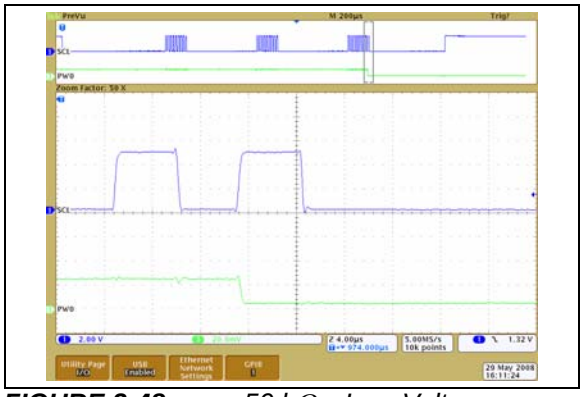


***FIGURE 2-48:*** *50 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

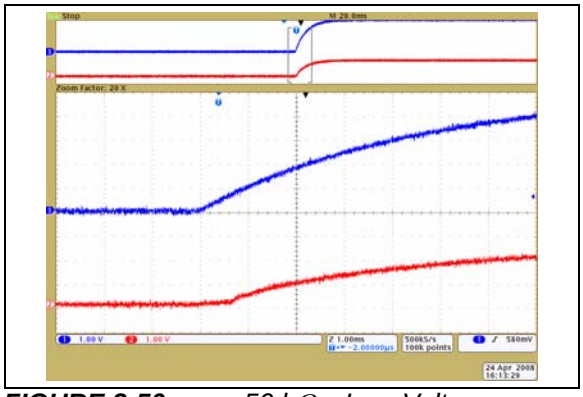


***FIGURE 2-50:*** *50 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

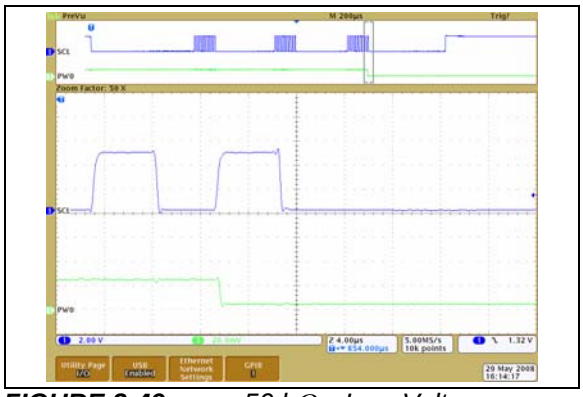


***FIGURE 2-49:*** *50 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

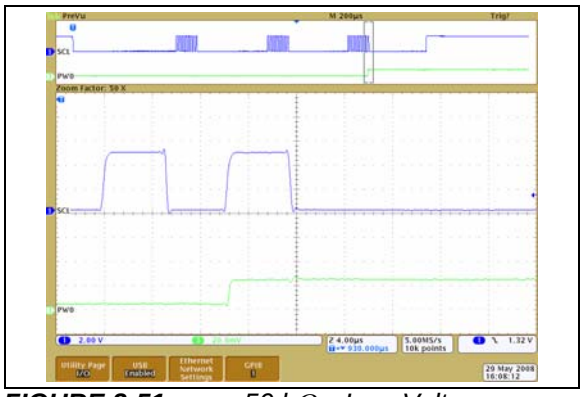


***FIGURE 2-51:*** *50 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

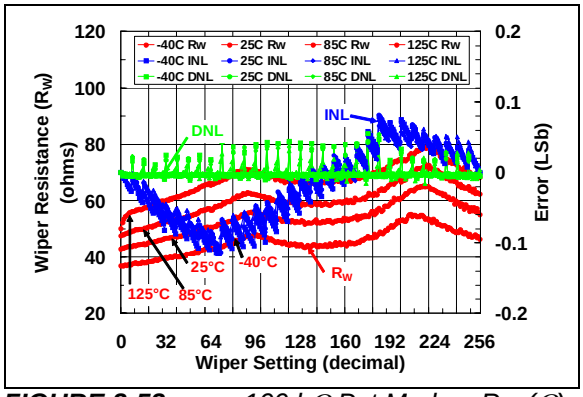



***FIGURE 2-52:*** *100 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

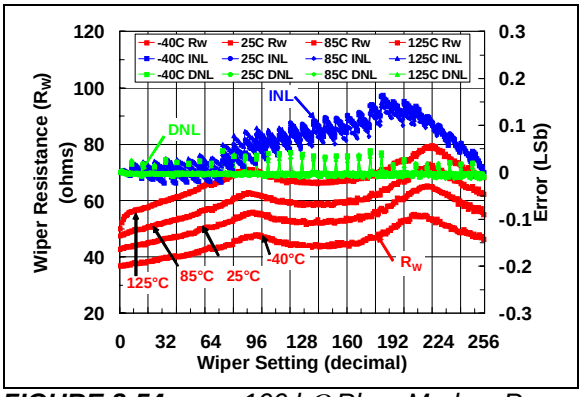



***FIGURE 2-54:*** *100 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

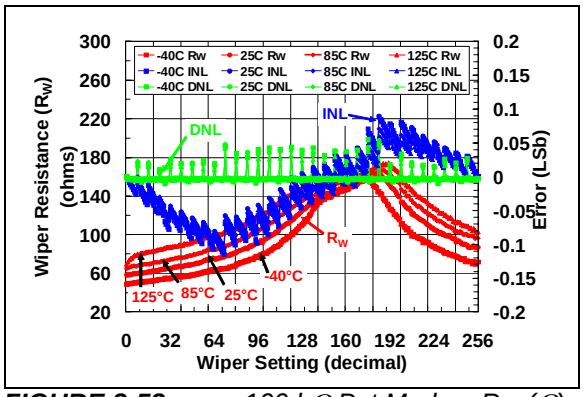



***FIGURE 2-53:*** *100 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

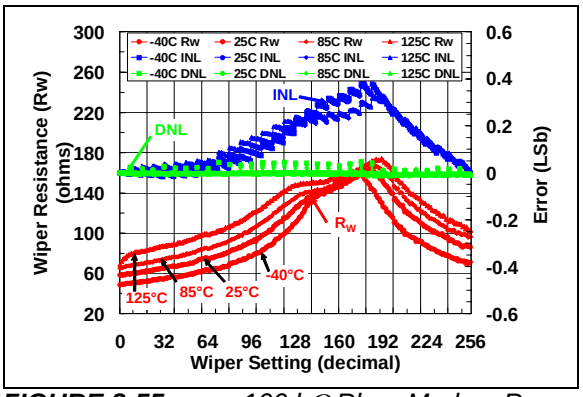



***FIGURE 2-55:*** *100 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

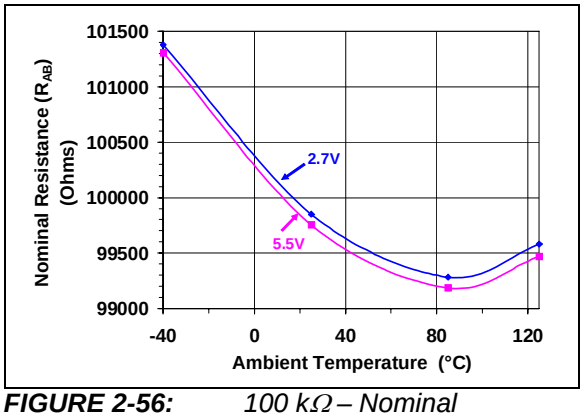



***FIGURE 2-56:*** *100 kΩ – Nominal Resistance ($R_{AB}$) (Ω) vs. Ambient Temperature and $V_{DD}$.*

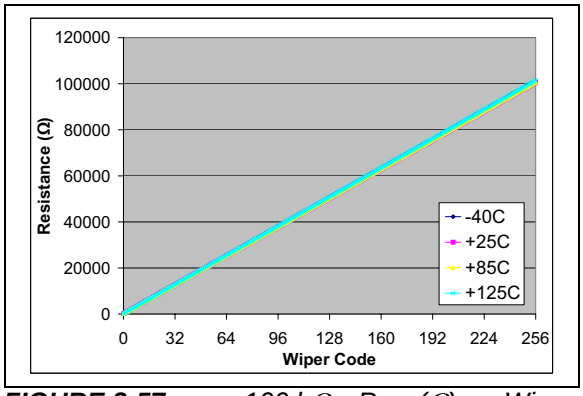



***FIGURE 2-57:*** *100 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V, $I_W$ = 45 µA).*

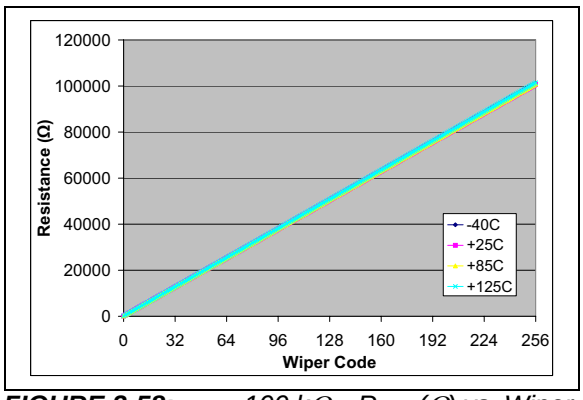



***FIGURE 2-58:*** *100 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V, $I_W$ = 24 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

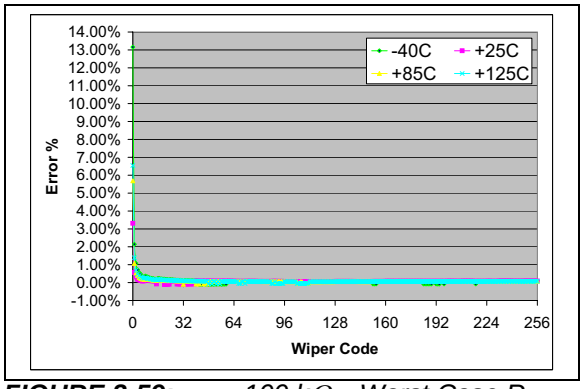



***FIGURE 2-59:*** *100 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 5.5V, $I_W$ = 45 µA).*

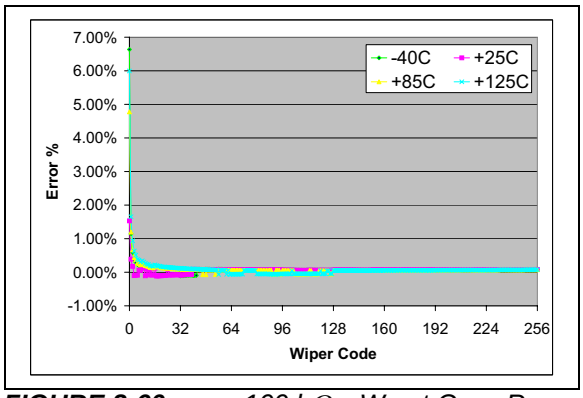



***FIGURE 2-60:*** *100 kΩ – Worst Case $R_{BW}$ from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) Error (%) vs. Wiper Setting and Temperature ($V_{DD}$ = 3.0V, $I_W$ = 24 µA).*

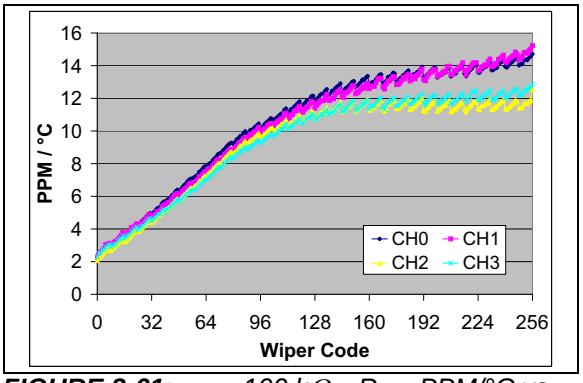



***FIGURE 2-61:*** *100 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, $I_W$ = 45 µA).*

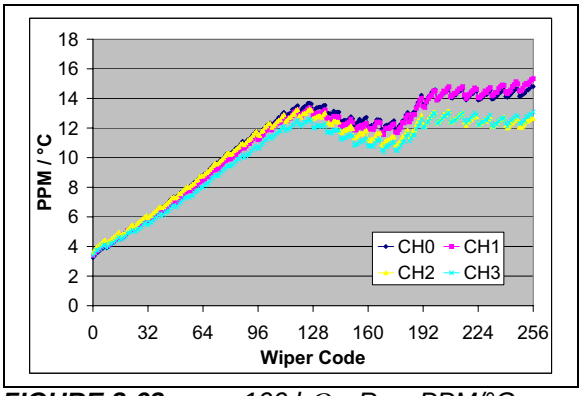



***FIGURE 2-62:*** *100 kΩ – $R_{WB}$ PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$ )/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, $I_W$ = 24 µA).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

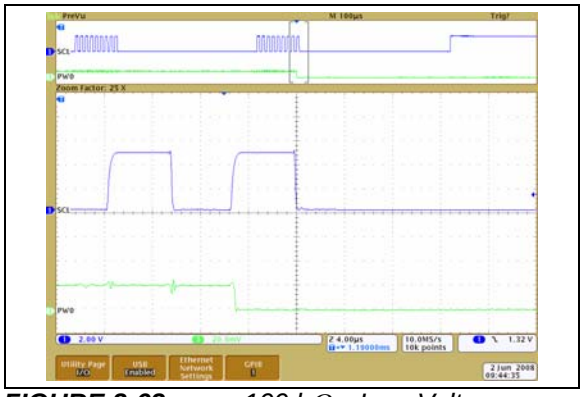


***FIGURE 2-63:*** *100 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

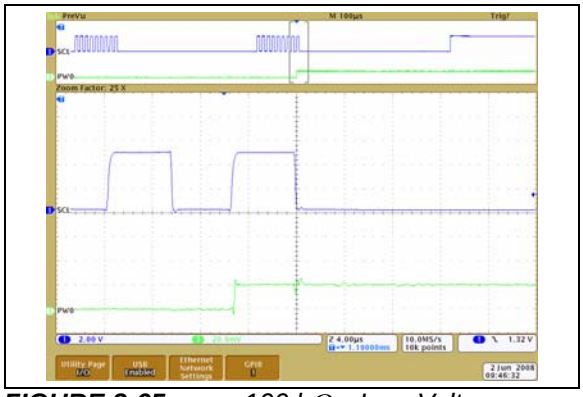


***FIGURE 2-65:*** *100 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

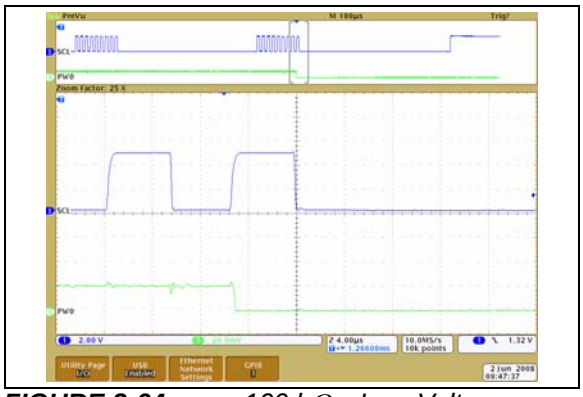


***FIGURE 2-64:*** *100 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

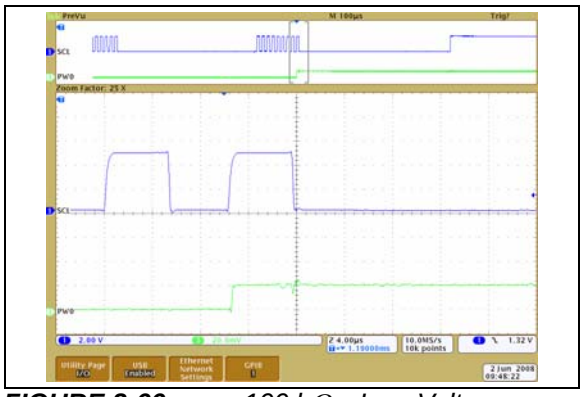


***FIGURE 2-66:*** *100 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

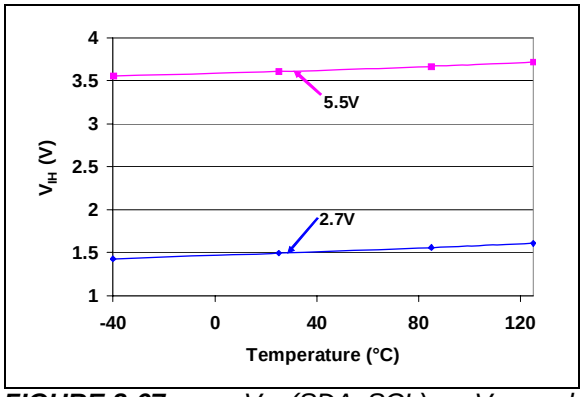



***FIGURE 2-67:*** *$V_{IH}$ (SDA, SCL) vs. $V_{DD}$ and Temperature.*

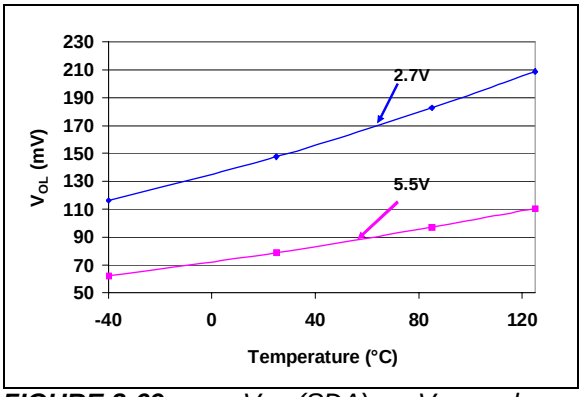



***FIGURE 2-69:*** *$V_{OL}$ (SDA) vs. $V_{DD}$ and Temperature ($I_{OL}$ = 3 mA).*

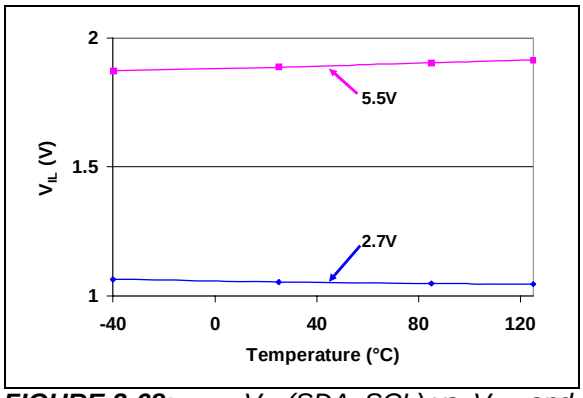



***FIGURE 2-68:*** *$V_{IL}$ (SDA, SCL) vs. $V_{DD}$ and Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

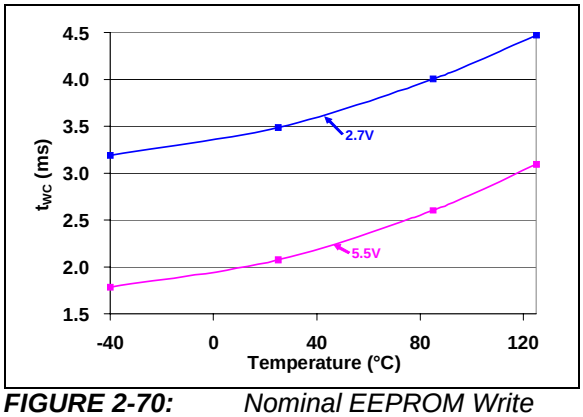



***FIGURE 2-70:*** *Nominal EEPROM Write Cycle Time vs. $V_{DD}$ and Temperature.*

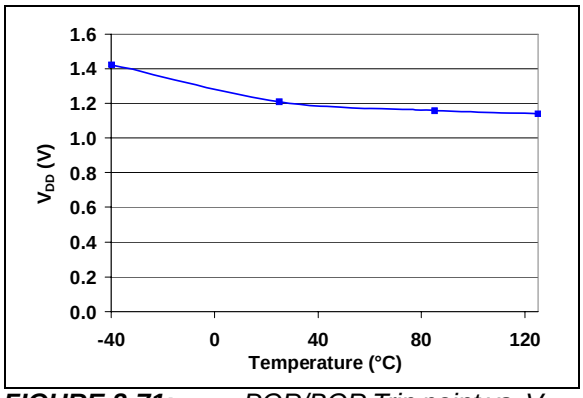



***FIGURE 2-71:*** *POR/BOR Trip point vs. $V_{DD}$ and Temperature.*

## 2.1 Test Circuits

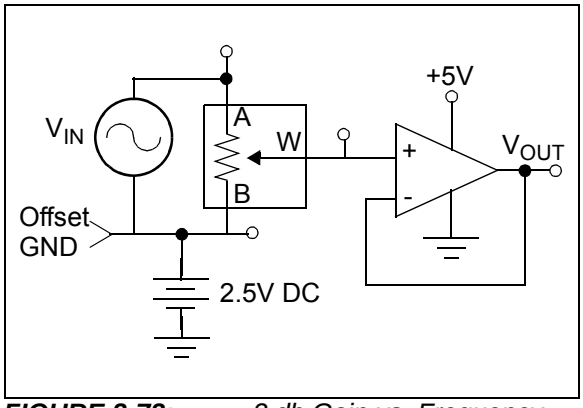



***FIGURE 2-72:*** *-3 db Gain vs. Frequency Test.*

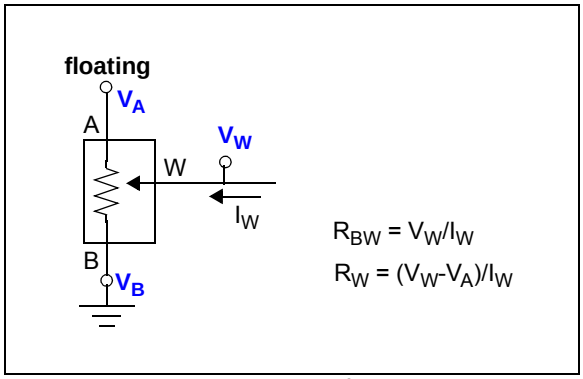



***FIGURE 2-73:*** *$R_{BW}$ and $R_W$ Measurement.*

**NOTES:**

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follows.

**TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP444X/446X**

| Pin | | | Symbol | I/O | Buffer Type | Weak Pull-up/ down (Note 1) | Standard Function |
|---|---|---|---|---|---|---|---|
| TSSOP | | QFN | | | | | |
| 14L | 20L | 20L | | | | | |
| — | 1 | 19 | P3A | A | Analog | No | Potentiometer 3 Terminal A |
| 1 | 2 | 20 | P3W | A | Analog | No | Potentiometer 3 Wiper Terminal |
| 2 | 3 | 1 | P3B | A | Analog | No | Potentiometer 3 Terminal B |
| 3 | 4 | 2 | HVC/A0 | I | HV w/ST | “smart” | High Voltage Command / $I^2C$ Address 0 |
| 4 | 5 | 3 | SCL | I | HV w/ST | No | $I^2C$ Clock Input |
| 5 | 6 | 4 | SDA | I | HV w/ST | No | $I^2C$ Serial Data I/O. Open Drain output |
| 6 | 7 | 5 | $V_{SS}$ | — | P | — | Ground |
| 7 | 8 | 6 | P1B | A | Analog | No | Potentiometer 1 Terminal B |
| 8 | 9 | 7 | P1W | A | Analog | No | Potentiometer 1 Wiper Terminal |
| — | 10 | 8 | P1A | A | Analog | No | Potentiometer 1 Terminal A |
| — | 11 | 9 | P0A | A | Analog | No | Potentiometer 0 Terminal A |
| 9 | 12 | 10 | P0W | A | Analog | No | Potentiometer 0 Wiper Terminal |
| 10 | 13 | 11 | P0B | A | Analog | No | Potentiometer 0 Terminal B |
| — | 14 | 12 | $\overline{WP}$ | I | HV w/ST | “smart” | Hardware EEPROM Write Protect |
| — | 15 | 13 | $\overline{RESET}$ | I | HV w/ST | Yes | Hardware Reset Pin |
| 11 | 16 | 14 | A1 | I | HV w/ST | “smart” | $I^2C$ Address 1 |
| 12 | 17 | 15 | $V_{DD}$ | — | P | — | Positive Power Supply Input |
| 13 | 18 | 16 | P2B | A | Analog | No | Potentiometer 2 Terminal B |
| 14 | 19 | 17 | P2W | A | Analog | No | Potentiometer 2 Wiper Terminal |
| — | 20 | 18 | P2A | A | Analog | No | Potentiometer 2 Terminal A |
| — | — | 21 | EP | — | — | — | Exposed Pad. (Note 2) |

**Legend:** HV w/ST = High Voltage tolerant input (with Schmidtt trigger input)
A = Analog pins (Potentiometer terminals) I = digital input (high Z)
O = digital output I/O = Input / Output
P = Power

**Note 1:** The pin’s “smart” pull-up shuts off while the pin is forced low. This is done to reduce the standby and shut-down current.

**2:** The QFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device’s $V_{SS}$ pin.

### 3.1 High Voltage Command / Address 0 (HVC/A0)

The HVC/A0 pin is the Address 0 input for the $I^2C$ interface as well as the High Voltage Command pin. At the device's POR/BOR the value of the A0 address bit is latched. This input along with the A1 pin completes the device address. This allows up to 4 MCP44XX devices to be on a single $I^2C$ bus.

During normal operation, the voltage on this pin determines whether the $I^2C$ command is a normal command or a High Voltage command (when HVC/A0 = $V_{IHH}$).

### 3.2 Serial Clock (SCL)

The SCL pin is the serial interfaces Serial Clock pin. This pin is connected to the Host Controllers SCL pin. The MCP44XX is a slave device, so its SCL pin accepts only external clock signals.

### 3.3 Serial Data (SDA)

The SDA pin is the serial interfaces Serial Data pin. This pin is connected to the Host Controllers SDA pin. The SDA pin is an open-drain N-channel driver.

### 3.4 Ground ($V_{SS}$)

The $V_{SS}$ pin is the device ground reference.

### 3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the Zero Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between $V_{SS}$ and $V_{DD}$.

MCP44XX devices have four terminal B pins, one for each resistor network.

### 3.6 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between $V_{SS}$ and $V_{DD}$.

MCP44XX devices have four terminal W pins, one for each resistor network.

### 3.7 Potentiometer Terminal A

The terminal A pin is available on the MCP44X1 devices, and is connected to the internal potentiometer's terminal A.

The potentiometer's terminal A is the fixed connection to the Full Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x100 for 8-bit devices or 0x80 for 7-bit devices.

The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between $V_{SS}$ and $V_{DD}$.

The terminal A pin is not available on the MCP44X2 devices, and the internally terminal A signal is floating.

MCP44X1 devices have four terminal A pins, one for each resistor network. Terminal A is not available on the MCP44X2 devices.

### 3.8 Write Protect ($\overline{WP}$)

The $\overline{WP}$ pin is used to force the nonvolatile memory to be write protected.

### 3.9 Reset ($\overline{RESET}$)

The $\overline{RESET}$ pin is used to force the device into the POR/BOR state.

### 3.10 Address 1 (A1)

The A1 pin is the $I^2C$ interface's Address 1 pin. Along with the A0 pins, up to 4 MCP44XX devices can be on a single $I^2C$ bus.

### 3.11 Positive Power Supply Input ($V_{DD}$)

The $V_{DD}$ pin is the device's positive power supply input. The input power supply is relative to $V_{SS}$.

While the device $V_{DD}$ < $V_{min}$ (2.7V), the electrical performance of the device may not meet the data sheet specifications.

### 3.12 No Connect (NC)

These pins should be either connected to $V_{DD}$ or $V_{SS}$.

### 3.13 Exposed Pad (EP)

This pad is conductively connected to the device's substrate. This pad should be tied to the same potential as the $V_{SS}$ pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.

## 4.0 FUNCTIONAL OVERVIEW

This Data Sheet covers a family of four nonvolatile Digital Potentiometer and Rheostat devices that will be referred to as MCP44XX. The MCP44X1 devices are the Potentiometer configuration, while the MCP44X2 devices are the Rheostat configuration.

As the **Device Block Diagram** shows, there are four main functional blocks. These are:

- **POR/BOR and RESET Operation**
- **Memory Map**
- **Resistor Network**
- **Serial Interface ($I^2C$)**

The POR/BOR operation and the Memory Map are discussed in this section and the Resistor Network and $I^2C$ operation are described in their own sections. The **Device Commands** commands are discussed in **Section 7.0**.

## 4.1 POR/BOR and $\overline{\text{RESET}}$ Operation

The Power-on Reset is the case where the device is having power applied to it from $V_{SS}$. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The devices RAM retention voltage ($V_{RAM}$) is lower than the POR/BOR voltage trip point ($V_{POR}/V_{BOR}$). The maximum $V_{POR}/V_{BOR}$ voltage is less then 1.8V.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and incrementing, decrementing, reading and writing to its volatile memory if the proper serial command is executed.

When $V_{DD} < V_{POR}/V_{BOR}$ or the RESET pin is Low, the pin weak pull-ups are enabled.

### 4.1.1 POWER-ON RESET

When the device powers up, the device $V_{DD}$ will cross the $V_{POR}/V_{BOR}$ voltage. Once the $V_{DD}$ voltage crosses the $V_{POR}/V_{BOR}$ voltage, the following happens:

- The volatile wiper register is loaded with value in the corresponding nonvolatile wiper register
- The TCON registers are loaded with their default value
- The device is capable of digital operation

### 4.1.2 BROWN-OUT RESET

When the device powers down, the device $V_{DD}$ will cross the $V_{POR}/V_{BOR}$ voltage.

Once the $V_{DD}$ voltage decreases below the $V_{POR}/V_{BOR}$ voltage, the following happens:

- Serial Interface is disabled
- EEPROM Writes are disabled

If the $V_{DD}$ voltage decreases below the $V_{RAM}$ voltage, the following happens:

- Volatile wiper registers may become corrupted
- TCON registers may become corrupted

As the voltage recovers above the $V_{POR}/V_{BOR}$ voltage, see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and nonvolatile) to become corrupted.

### 4.1.3 $\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin can be used to force the device into the POR/BOR state of the device. When the $\overline{\text{RESET}}$ pin is forced Low, the device is forced into the reset state. This means that the TCON and STATUS registers are forced to their default values and the volatile wiper registers are loaded with the value in the corresponding Nonvolatile wiper register. Also the $I^2C$ interface is disabled. Any nonvolatile write cycle is not interrupted, and allowed to complete.

This feature allows a hardware method for all registers to be updated at the same time.

### 4.1.4 INTERACTION OF $\overline{\text{RESET}}$ PIN AND BOR/POR CIRCUITRY

Figure 4-1 shows how the $\overline{\text{RESET}}$ pin signal and the POR/BOR signal interact to control the hardware reset state of the device.

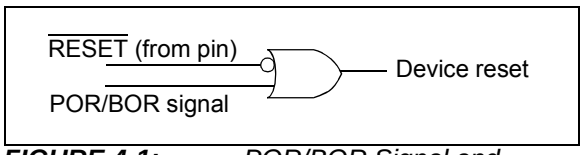



***FIGURE 4-1:*** *POR/BOR Signal and $\overline{\text{RESET}}$ Pin Interaction.*

## 4.2 Memory Map

The device memory has 16 locations that are 9-bit wide (16x9 bits). This memory space contains both volatile and nonvolatile locations (see Table 4-1).

**TABLE 4-1: MEMORY MAP AND THE SUPPORTED COMMANDS**

| Address | Function | Memory Type | Allowed Commands | Disallowed Commands (2) | Factory Initialization | |
|---|---|---|---|---|---|---|
| 00h | Volatile Wiper 0 | RAM | Read, Write, Increment, Decrement | — | — | |
| 01h | Volatile Wiper 1 | RAM | Read, Write, Increment, Decrement | — | — | |
| 02h | Nonvolatile Wiper 0 | EEPROM | Read, Write (1) | Increment, Decrement | 8-bit | 80h |
| | | | | | 7-bit | 40h |
| 03h | Nonvolatile Wiper 1 | EEPROM | Read, Write (1) | Increment, Decrement | 8-bit | 80h |
| | | | | | 7-bit | 40h |
| 04h | Volatile TCON0 Register | RAM | Read, Write | Increment, Decrement | — | |
| 05h | Status Register | RAM | Read | Write, Increment, Decrement | — | |
| 06h | Volatile Wiper 2 | RAM | Read, Write, Increment, Decrement | — | — | |
| 07h | Volatile Wiper 3 | RAM | Read, Write, Increment, Decrement | — | — | |
| 08h | Nonvolatile Wiper 2 | EEPROM | Read, Write (1) | Increment, Decrement | 8-bit | 80h |
| | | | | | 7-bit | 40h |
| 09h | Nonvolatile Wiper 3 | EEPROM | Read, Write (1) | Increment, Decrement | 8-bit | 80h |
| | | | | | 7-bit | 40h |
| 0Ah | Volatile TCON1 Register | RAM | Read, Write | Increment, Decrement | — | |
| 0Bh | Data EEPROM | EEPROM | Read, Write (1) | Increment, Decrement | 000h | |
| 0Ch | Data EEPROM | EEPROM | Read, Write (1) | Increment, Decrement | 000h | |
| 0Dh | Data EEPROM | EEPROM | Read, Write (1) | Increment, Decrement | 000h | |
| 0Eh | Data EEPROM | EEPROM | Read, Write (1) | Increment, Decrement | 000h | |
| 0Fh | Data EEPROM | EEPROM | Read, Write (1) | Increment, Decrement | 000h | |

**Note 1:** When an EEPROM write is active, these are invalid commands and will generate an error condition. The user should use a read of the Status register to determine when the write cycle has completed. To exit the error condition, the user must take the HVC pin to the $V_{IH}$ level and then back to the active state ($V_{IL}$ or $V_{IHH}$).

**2:** This command on this address will generate an error condition. To exit the error condition, the user must take the HVC pin to the $V_{IH}$ level and then back to the active state ($V_{IL}$ or $V_{IHH}$).

### 4.2.1 NONVOLATILE MEMORY (EEPROM)

This memory can be grouped into two uses of nonvolatile memory. These are:

- **General Purpose Registers**
- **Nonvolatile Wiper Registers**

The nonvolatile wipers start functioning below the devices $V_{POR}/V_{BOR}$ trip point.

#### 4.2.1.1 General Purpose Registers

These locations allow the user to store up to 5 (9-bit) locations worth of information.

#### 4.2.1.2 Nonvolatile Wiper Registers

These locations contain the wiper values that are loaded into the corresponding volatile wiper register whenever the device has a POR/BOR event. There are four registers, one for each resistor network.

The nonvolatile wiper register enables stand-alone operation of the device (without Microcontroller control) after being programmed to the desired value.

#### 4.2.1.3 Factory Initialization of Nonvolatile Memory (EEPROM)

The Nonvolatile Wiper values will be initialized to mid-scale value. This is shown in Table 4-2.

The General purpose EEPROM memory will be programmed to a default value of 0x000.

It is good practice in the manufacturing flow to configure the device to your desired settings.

**TABLE 4-2: DEFAULT FACTORY SETTINGS SELECTION**

| Resistance Code | Typical $R_{AB}$ Value | Default POR Wiper Setting | Wiper Code | | WiperLock™ Technology and Write Protect Setting |
|---|---|---|---|---|---|
| | | | 8-bit | 7-bit | |
| -502 | 5.0 kΩ | Mid scale | 80h | 40h | Disabled |
| -103 | 10.0 kΩ | Mid scale | 80h | 40h | Disabled |
| -503 | 50.0 kΩ | Mid scale | 80h | 40h | Disabled |
| -104 | 100.0 kΩ | Mid scale | 80h | 40h | Disabled |

#### 4.2.1.4 Special Features

There are 5 nonvolatile bits that are not directly mapped into the address space. These bits control the following functions:

- EEPROM Write Protect
- WiperLock Technology for Nonvolatile Wiper 0
- WiperLock Technology for Nonvolatile Wiper 1
- WiperLock Technology for Nonvolatile Wiper 2
- WiperLock Technology for Nonvolatile Wiper 3

The operation of WiperLock Technology is discussed in **Section 5.3**. The state of the WL0, WL1, WL2, WL3, and WP bits is reflected in the STATUS register (see Register 4-1).

## EEPROM Write Protect

All internal EEPROM memory can be Write Protected. When EEPROM memory is Write Protected, Write commands to the internal EEPROM are prevented.

Write Protect ($\overline{WP}$) can be enabled/disabled by two methods. These are:

- External $\overline{WP}$ Hardware pin (MCP44X1 devices only)
- Nonvolatile configuration bit (WP)

High Voltage commands are required to enable and disable the nonvolatile WP bit. These commands are shown in **Section 7.8 "Modify Write Protect or WiperLock Technology (High Voltage)"**.

To write to EEPROM, both the external $\overline{WP}$ pin and the internal WP EEPROM bit must be disabled. Write Protect does not block commands to the volatile registers.

### 4.2.2 VOLATILE MEMORY (RAM)

There are seven Volatile Memory locations. These are:

- Volatile Wiper 0
- Volatile Wiper 1
- Volatile Wiper 2
- Volatile Wiper 3
- Status Register
- Terminal Control (TCON0) Register 0
- Terminal Control (TCON)1 Register 1

The volatile memory starts functioning at the RAM retention voltage ($V_{RAM}$).

#### 4.2.2.1 Status (STATUS) Register

This register contains 7 status bits. These bits show the state of the WiperLock bits, the Write Protect bit, and if an EEPROM write cycle is active. The STATUS register can be accessed via the READ commands. Register 4-1 describes each STATUS register bit.

The STATUS register is placed at Address 05h.

**REGISTER 4-1: STATUS REGISTER**

| R-1 | R-1 | R-1 | R-1 | R-0 | R-x | R-x | R-1 | R-x |
|---|---|---|---|---|---|---|---|---|
| D8:D7 | | WL3 (1) | WL2 (1) | EEWA | WL1 (1) | WL0 (1) | — | WP (1) |
| bit 7 | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 8-7 **D8:D7:** Reserved. Forced to "1"

bit 6 **WL3:** WiperLock Status bit for Resistor Network 3 (Refer to **Section 5.3 "WiperLock Technology"** for further information)

The WiperLock Technology bit (WL3) prevents the Volatile and Nonvolatile Wiper 3 addresses and the TCON1 register bits R3HW, R3A, R3W, and R3B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON1 register bits R3HW, R3A, R3W, and R3B of Resistor Network 3 (Pot 3) are "Locked" (Write Protected)

0 = Wiper and TCON1 of Resistor Network 3 (Pot 3) can be modified

**Note:** The WL3 bit always reflects the result of the last programming cycle to the nonvolatile WL3 bit. After a POR/BOR or $\overline{\text{RESET}}$ pin event, the WL3 bit is loaded with the nonvolatile WL3 bit value.

bit 5 **WL2:** WiperLock Status bit for Resistor Network 2 (Refer to **Section 5.3 "WiperLock Technology"** for further information)

The WiperLock Technology bit (WL2) prevents the Volatile and Nonvolatile Wiper 2 addresses and the TCON1 register bits R2HW, R2A, R2W, and R2B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON1 register bits R2HW, R2A, R2W, and R2B of Resistor Network 2 (Pot 2) are "Locked" (Write Protected)

0 = Wiper and TCON1 of Resistor Network 2 (Pot 2) can be modified

**Note:** The WL0 bit always reflects the result of the last programming cycle to the nonvolatile WL0 bit. After a POR/BOR or $\overline{\text{RESET}}$ pin event, the WL0 bit is loaded with the nonvolatile WL0 bit value.

bit 4 **EEWA:** EEPROM Write Active Status bit

This bit indicates if the EEPROM Write Cycle is occurring.

1 = An EEPROM Write cycle is currently occurring. Only serial commands to the Volatile memory locations are allowed (addresses 00h, 01h, 04h, and 05h)

0 = An EEPROM Write cycle is NOT currently occurring

**Note 1:** Requires a High Voltage command to modify the state of this bit (for Nonvolatile devices only). This bit is not directly written, but reflects the system state (for this feature).

**REGISTER 4-1: STATUS REGISTER (CONTINUED)**

bit 3 **WL1:** WiperLock Status bit for Resistor Network 1 (Refer to **Section 5.3 "WiperLock Technology"** for further information)

The WiperLock Technology bit (WL1) prevents the Volatile and Nonvolatile Wiper 1 addresses and the TCON0 register bits R1HW, R1A, R1W, and R1B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON0 register bits R1HW, R1A, R1W, and R1B of Resistor Network 1 (Pot 1) are "Locked" (Write Protected)

0 = Wiper and TCON0 of Resistor Network 1 (Pot 1) can be modified

**Note:** The WL1 bit always reflects the result of the last programming cycle to the nonvolatile WL1 bit. After a POR/BOR or $\overline{\text{RESET}}$ pin event, the WL1 bit is loaded with the nonvolatile WL1 bit value.

bit 2 **WL0:** WiperLock Status bit for Resistor Network 0 (Refer to **Section 5.3 "WiperLock Technology"** for further information)

The WiperLock Technology bit (WL0) prevents the Volatile and Nonvolatile Wiper 0 addresses and the TCON0 register bits R0HW, R0A, R0W, and R0B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON0 register bits R0HW, R0A, R0W, and R0B of Resistor Network 0 (Pot 0) are "Locked" (Write Protected)

0 = Wiper and TCON0 of Resistor Network 0 (Pot 0) can be modified

**Note:** The WL0 bit always reflects the result of the last programming cycle to the nonvolatile WL0 bit. After a POR/BOR or $\overline{\text{RESET}}$ pin event, the WL0 bit is loaded with the nonvolatile WL0 bit value.

bit 1 **Reserved:** Forced to "1"

bit 0 **WP:** EEPROM Write Protect Status bit (Refer to **Section "EEPROM Write Protect"** for further information)

This bit indicates the status of the write protection on the EEPROM memory. When Write Protect is enabled, writes to all nonvolatile memory are prevented. This includes the General Purpose EEPROM memory, and the nonvolatile Wiper registers. Write Protect does not block modification of the volatile wiper register values or the volatile TCON0 and TCON1 register values (via Increment, Decrement, or Write commands).

This status bit is an OR of the devices Write Protect pin ($\overline{\text{WP}}$) and the internal nonvolatile WP bit. High Voltage commands are required to enable and disable the internal WP EEPROM bit.

1 = EEPROM memory is Write Protected

0 = EEPROM memory can be written

**Note 1:** Requires a High Voltage command to modify the state of this bit (for Nonvolatile devices only). This bit is not directly written, but reflects the system state (for this feature).

#### 4.2.2.2 Terminal Control (TCON) Registers

There are two Terminal Control (TCON) Registers. These are called TCON0 and TCON1. Each register contains 8 control bits, four bits for each Wiper. Register 4-2 describes each bit of the TCON0 register, while Register 4-3 describes each bit of the TCON1 register.

The state of each resistor network terminal connection is individually controlled. That is, each terminal connection (A, B and W) can be individually connected/disconnected from the resistor network. This allows the system to minimize the currents through the digital potentiometer.

The value that is written to the specified TCON register will appear on the appropriate resistor network terminals when the serial command has completed.

When the WL1 bit is enabled, writes to the TCON0 register bits R1HW, R1A, R1W, and R1B are inhibited.

When the WL0 bit is enabled, writes to the TCON0 register bits R0HW, R0A, R0W, and R0B are inhibited.

When the WL3 bit is enabled, writes to the TCON1 register bits R3HW, R3A, R3W, and R3B are inhibited.

When the WL2 bit is enabled, writes to the TCON1 register bits R2HW, R2A, R2W, and R2B are inhibited.

On a POR/BOR these registers are loaded with 1FFh (9-bit), for all terminals connected. The Host Controller needs to detect the POR/BOR event and then update the Volatile TCON register values.

**REGISTER 4-2: TCON0 BITS (1)**

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|---|
| D8 | R1HW | R1A | R1W | R1B | R0HW | R0A | R0W | R0B |
| bit 8 | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 8 **D8:** Reserved. Forced to "1"

bit 7 **R1HW:** Resistor 1 Hardware Configuration Control bit

This bit forces Resistor 1 into the "shutdown" configuration of the Hardware pin
1 = Resistor 1 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 1 is forced to the hardware pin "shutdown" configuration

bit 6 **R1A:** Resistor 1 Terminal A (P1A pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Terminal A to the Resistor 1 Network
1 = P1A pin is connected to the Resistor 1 Network
0 = P1A pin is disconnected from the Resistor 1 Network

bit 5 **R1W:** Resistor 1 Wiper (P1W pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Wiper to the Resistor 1 Network
1 = P1W pin is connected to the Resistor 1 Network
0 = P1W pin is disconnected from the Resistor 1 Network

bit 4 **R1B:** Resistor 1 Terminal B (P1B pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Terminal B to the Resistor 1 Network
1 = P1B pin is connected to the Resistor 1 Network
0 = P1B pin is disconnected from the Resistor 1 Network

bit 3 **R0HW:** Resistor 0 Hardware Configuration Control bit

This bit forces Resistor 0 into the "shutdown" configuration of the Hardware pin
1 = Resistor 0 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 0 is forced to the hardware pin "shutdown" configuration

bit 2 **R0A:** Resistor 0 Terminal A (P0A pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Terminal A to the Resistor 0 Network
1 = P0A pin is connected to the Resistor 0 Network
0 = P0A pin is disconnected from the Resistor 0 Network

bit 1 **R0W:** Resistor 0 Wiper (P0W pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Wiper to the Resistor 0 Network
1 = P0W pin is connected to the Resistor 0 Network
0 = P0W pin is disconnected from the Resistor 0 Network

bit 0 **R0B:** Resistor 0 Terminal B (P0B pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Terminal B to the Resistor 0 Network
1 = P0B pin is connected to the Resistor 0 Network
0 = P0B pin is disconnected from the Resistor 0 Network

**Note 1:** These bits do not affect the wiper register values.

**REGISTER 4-3: TCON1 BITS (1)**

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|---|
| D8 | R3HW | R3A | R3W | R3B | R2HW | R2A | R2W | R2B |
| bit 8 | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 8 **D8:** Reserved. Forced to "1"

bit 7 **R3HW:** Resistor 3 Hardware Configuration Control bit

This bit forces Resistor 3 into the "shutdown" configuration of the Hardware pin
1 = Resistor 3 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 3 is forced to the hardware pin "shutdown" configuration

bit 6 **R3A:** Resistor 3 Terminal A (P3A pin) Connect Control bit

This bit connects/disconnects the Resistor 3 Terminal A to the Resistor 3 Network
1 = P3A pin is connected to the Resistor 3 Network
0 = P3A pin is disconnected from the Resistor 3 Network

bit 5 **R3W:** Resistor 3 Wiper (P3W pin) Connect Control bit

This bit connects/disconnects the Resistor 3 Wiper to the Resistor 3 Network
1 = P3W pin is connected to the Resistor 3 Network
0 = P3W pin is disconnected from the Resistor 3 Network

bit 4 **R3B:** Resistor 3 Terminal B (P3B pin) Connect Control bit

This bit connects/disconnects the Resistor 3 Terminal B to the Resistor 3 Network
1 = P3B pin is connected to the Resistor 3 Network
0 = P3B pin is disconnected from the Resistor 3 Network

bit 3 **R2HW:** Resistor 2 Hardware Configuration Control bit

This bit forces Resistor 2 into the "shutdown" configuration of the Hardware pin
1 = Resistor 2 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 2 is forced to the hardware pin "shutdown" configuration

bit 2 **R2A:** Resistor 2 Terminal A (P0A pin) Connect Control bit

This bit connects/disconnects the Resistor 2 Terminal A to the Resistor 2 Network
1 = P2A pin is connected to the Resistor 2 Network
0 = P2A pin is disconnected from the Resistor 2 Network

bit 1 **R2W:** Resistor 2 Wiper (P0W pin) Connect Control bit

This bit connects/disconnects the Resistor 2 Wiper to the Resistor 2 Network
1 = P2W pin is connected to the Resistor 2 Network
0 = P2W pin is disconnected from the Resistor 2 Network

bit 0 **R2B:** Resistor 2 Terminal B (P2B pin) Connect Control bit

This bit connects/disconnects the Resistor 2 Terminal B to the Resistor 2 Network
1 = P2B pin is connected to the Resistor 2 Network
0 = P2B pin is disconnected from the Resistor 2 Network

**Note 1:** These bits do not affect the wiper register values.

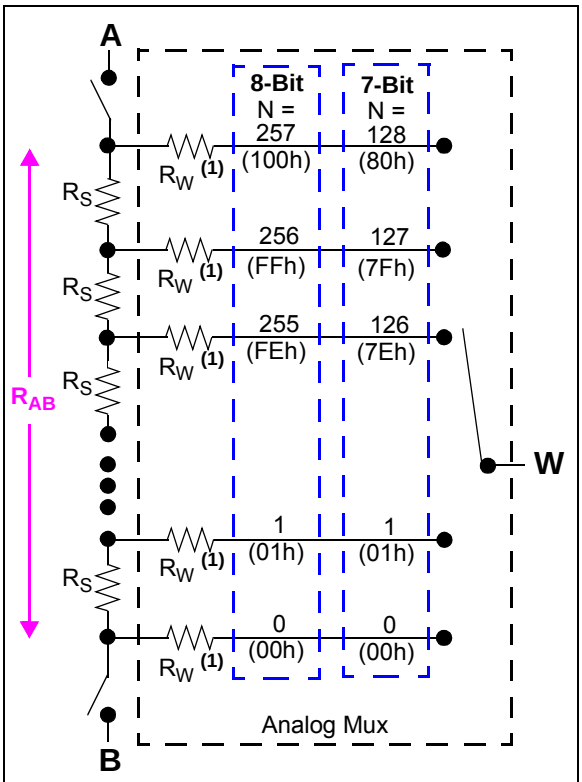
## 5.0 RESISTOR NETWORK

The Resistor Network has either 7-bit or 8-bit resolution. Each Resistor Network allows zero scale to full scale connections. Figure 5-1 shows a block diagram for the resistive network of a device.

The Resistor Network is made up of several parts. These include:

- Resistor Ladder
- Wiper
- Shutdown (Terminal Connections)

Devices have four resistor networks. These are referred to as Pot 0, Pot 1 Pot 2, and Pot 3.




**Note 1:** The wiper resistance is dependent on several factors including, wiper code, device $V_{DD}$, Terminal voltages (on A, B, and W), and temperature.
Also for the same conditions, each tap selection resistance has a small variation. This $R_W$ variation has greater effects on some specifications (such as INL) for the smaller resistance devices (5.0 kΩ) compared to larger resistance devices (100.0 kΩ).

***FIGURE 5-1:*** *Resistor Block Diagram.*

### 5.1 Resistor Ladder Module

The resistor ladder is a series of equal value resistors ($R_S$) with a connection point (tap) between the two resistors. The total number of resistors in the series (ladder) determines the $R_{AB}$ resistance (see Figure 5-1). The end points of the resistor ladder are connected to analog switches which are connected to the device Terminal A and Terminal B pins. The $R_{AB}$ (and $R_S$) resistance has small variations over voltage and temperature.

For an 8-bit device, there are 256 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 256 resistors, thus providing 257 possible settings (including terminal A and terminal B).

For a 7-bit device, there are 128 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 128 resistors, thus providing 129 possible settings (including terminal A and terminal B).

Equation 5-1 shows the calculation for the step resistance.

**EQUATION 5-1: $R_S$ CALCULATION**

$$R_S = \frac{R_{AB}}{(256)} \quad \text{8-bit Device}$$

$$R_S = \frac{R_{AB}}{(128)} \quad \text{7-bit Device}$$

## 5.2 Wiper

Each tap point (between the $R_S$ resistors) is a connection point for an analog switch. The opposite side of the analog switch is connected to a common signal which is connected to the Terminal W (Wiper) pin.

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The wiper can connect directly to Terminal B or to Terminal A. A zero scale connections, connects the Terminal W (wiper) to Terminal B (wiper setting of 000h). A full scale connection, connects the Terminal W (wiper) to Terminal A (wiper setting of 100h or 80h). In these configurations, the only resistance between the Terminal W and the other Terminal (A or B) is that of the analog switches.

A wiper setting value greater than full scale (wiper setting of 100h for 8-bit device or 80h for 7-bit devices) will also be a Full Scale setting (Terminal W (wiper) connected to Terminal A). Table 5-1 illustrates the full wiper setting map.

Equation 5-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.

**EQUATION 5-2: $R_{WB}$ CALCULATION**

$$R_{WB} = \frac{R_{AB}N}{(256)} + R_W \quad \text{8-bit Device}$$

N = 0 to 256 (decimal)

$$R_{WB} = \frac{R_{AB}N}{(128)} + R_W \quad \text{7-bit Device}$$

N = 0 to 128 (decimal)

**TABLE 5-1: VOLATILE WIPER VALUE VS. WIPER POSITION MAP**

| Wiper Setting | | Properties |
|---|---|---|
| 7-bit | 8-bit | |
| 3FFh – 081h | 3FFh – 101h | Reserved (Full Scale (W = A)), Increment and Decrement commands ignored |
| 080h | 100h | Full Scale (W = A), Increment commands ignored |
| 07Fh – 041h | 0FFh – 081h | W = N |
| 040h | 080h | W = N (Mid Scale) |
| 03Fh – 001h | 07Fh – 001h | W = N |
| 000h | 000h | Zero Scale (W = B) Decrement command ignored |

## 5.3 WiperLock Technology

The MCP44XX device's WiperLock technology allows application-specific calibration settings to be secured in the EEPROM without requiring the use of an additional write-protect pin. There are four WiperLock Technology configuration bits (WL0, WL1, WL2, and WL3). These bits prevent the Nonvolatile and Volatile addresses and bits for the specified resistor network from being written.

The WiperLock technology prevents the serial commands from doing the following:

- Changing a volatile wiper value
- Writing to the specified nonvolatile wiper memory location
- Changing the related volatile TCON register bits

For either Resistor Network 0, Resistor Network 1, Resistor Network 2, or Resistor Network 3 (Potx), the WLx bit controls the following:

- Nonvolatile Wiper Register
- Volatile Wiper Register
- Volatile TCON register bits RxHW, RxA, RxW, and RxB

High Voltage commands are required to enable and disable WiperLock. Please refer to the **Modify Write Protect or WiperLock Technology (High Voltage)** command for operation.

### 5.3.1 POR/BOR OPERATION WHEN WIPERLOCK TECHNOLOGY ENABLED

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the Volatile Wiper register value with the Nonvolatile Wiper register value, refer to **Section 4.1**.

## 5.4 Shutdown

Shutdown is used to minimize the device's current consumption. The MCP44XX has one method to achieve this. This is:

- **Terminal Control Register (TCON)**

This is different from the MCP42XXX devices in that the Hardware Shutdown Pin ($\overline{SHDN}$) has been replaced by a $\overline{RESET}$ pin. The Hardware Shutdown Pin function is still available via software commands to the TCON register.

### 5.4.1 TERMINAL CONTROL REGISTER (TCON)

The Terminal Control (TCON) register is a volatile register used to configure the connection of each resistor network terminal pin (A, B, and W) to the Resistor Network. These registers are shown in Register 4-2 and Register 4-3.

The RxHW bits forces the selected resistor network into the same state as the MCP42X1's $\overline{SHDN}$ pin. Alternate low power configurations may be achieved with the RxA, RxW, and RxB bits.

When the RxHW bit is "0":

- The P0A, P1A, P2A, and P3A terminals are disconnected
- The P0W, P1W, P2W, and P3W terminals are simultaneously connect to the P0B, P1B, P2B, and P3B terminals, respectively (see Figure 5-2)

| | |
|---|---|
| **Note:** | When the RxHW bit forces the resistor network into the hardware $\overline{SHDN}$ state, the state of the TCON0 or TCON1 register's RxA, RxW, and RxB bits is overridden (ignored). When the state of the RxHW bit no longer forces the resistor network into the hardware $\overline{SHDN}$ state, the TCON0 or TCON1 register's RxA, RxW, and RxB bits return to controlling the terminal connection state. In other words, the RxHW bit does not corrupt the state of the RxA, RxW, and RxB bits. |

The RxHW bit does NOT corrupt the values in the Volatile Wiper Registers nor the TCON register. When the Shutdown mode is exited (RxHW bit = "1"):

- The device returns to the Wiper setting specified by the Volatile Wiper value
- The TCON register bits return to controlling the terminal connection state

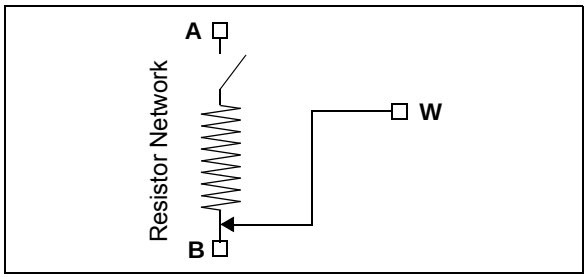



***FIGURE 5-2:*** *Resistor Network Shutdown State (RxHW = '0').*

**NOTES:**

## 6.0 SERIAL INTERFACE ($I^2C$)

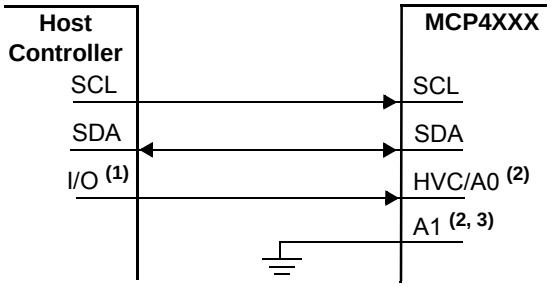
The MCP44XX devices support the $I^2C$ serial protocol. The MCP44XX $I^2C$'s module operates in Slave mode (does not generate the serial clock).

Figure 6-1 shows a typical $I^2C$ Interface connection. All $I^2C$ interface signals are high-voltage tolerant.

The MCP44XX devices use the two-wire $I^2C$ serial interface. This interface can operate in standard, fast or High-Speed mode. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. The MCP44XX device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the START bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the R/$\overline{W}$ bit.

Refer to the Phillips $I^2C$ document for more details of the $I^2C$ specifications.

**Typical $I^2C$ Interface Connections**




**Note 1:** If High voltage commands are desired, some type of external circuitry needs to be implemented.

**2:** These pins have internal pull-ups. If faster rise times are required, then external pull-ups should be added.

**3:** This pin could be tied high, low, or connected to an I/O pin of the Host Controller.

***FIGURE 6-1:*** *Typical $I^2C$ Interface Block Diagram.*

### 6.1 Signal Descriptions

The $I^2C$ interface uses up to four pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)
- A0 (Address 0 bit)
- A1 (Address 1 bit)

#### 6.1.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the START and STOP conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is HIGH will be interpreted as a START or a STOP condition.

#### 6.1.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin. The MCP44XX supports three $I^2C$ interface clock modes:

- Standard Mode: clock rates up to 100 kHz
- Fast Mode: clock rates up to 400 kHz
- High-Speed Mode (HS mode): clock rates up to 3.4 MHz

The MCP44XX will not stretch the clock signal (SCL) since memory read access occur fast enough.

Depending on the clock rate mode, the interface will display different characteristics.

#### 6.1.3 THE ADDRESS BITS (A1:A0)

There are up to two hardware pins used to specify the device address. The number of address pins is determined by the part number.

Address 0 is multiplexed with the High Voltage Command (HVC) function. So the state of A0 is latched on the MCP4XXX's POR/BOR event.

The state of the A1 pin should be static, that is they should be tied high or tied low.

##### 6.1.3.1 The High Voltage Command (HVC) Signal

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

The HVC pin has an internal resistor connection to the MCP44XXs internal $V_{DD}$ signal.

## 6.2 I²C Operation

The MCP44XX's I²C module is compatible with the Philips I²C specification. The following lists some of the modules features:

- 7-bit slave addressing
- Supports three clock rate modes:
  - Standard mode, clock rates up to 100 kHz
  - Fast mode, clock rates up to 400 kHz
  - High-speed mode (HS mode), clock rates up to 3.4 MHz
- Support Multi-Master Applications
- General call addressing
- Internal weak pull-ups on interface signals

The I²C 10-bit addressing mode is not supported.

The Philips I²C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content for the MCP44XX is defined in **Section 7.0**.

### 6.2.1 I²C BIT STATES AND SEQUENCE

Figure 6-8 shows the I²C transfer sequence. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low) / No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

#### 6.2.1.1 Start Bit

The Start bit (see Figure 6-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is "High".

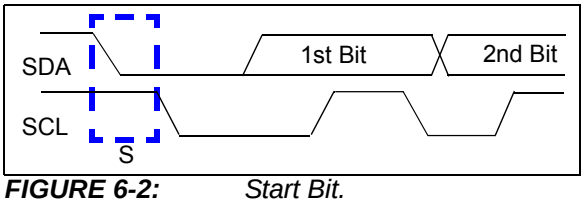



***FIGURE 6-2:*** *Start Bit.*

#### 6.2.1.2 Data Bit

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 6-5).

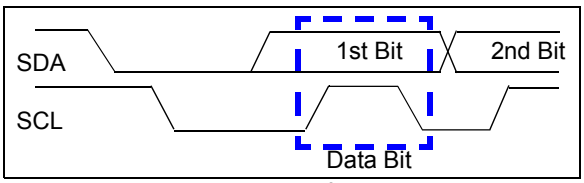



***FIGURE 6-3:*** *Data Bit.*

#### 6.2.1.3 Acknowledge (A) Bit

The A bit (see Figure 6-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically the Slave device will supply an A response after the Start bit and 8 "data" bits have been received. an A bit has the SDA signal low.

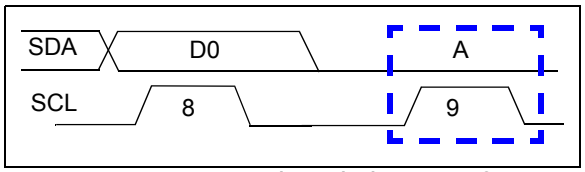



***FIGURE 6-4:*** *Acknowledge Waveform.*

### Not A ($\overline{A}$) Response

The $\overline{A}$ bit has the SDA signal high. Table 6-1 shows some of the conditions where the Slave Device will issue a Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then an START bit must be issued to reset the command state machine.

**TABLE 6-1: MCP45XX/MCP46XX A / $\overline{A}$ RESPONSES**

| Event | Acknowledge Bit Response | Comment |
|---|---|---|
| General Call | A | Only if GCEN bit is set |
| Slave Address valid | A | |
| Slave Address not valid | $\overline{A}$ | |
| Device Memory Address and specified command (AD3:AD0 and C1:C0) are an invalid combination | $\overline{A}$ | After device has received address and command |
| Communication during EEPROM write cycle | A | After device has received address and command, and valid conditions for EEPROM write |
| Bus Collision | N.A. | I²C Module Resets, or a "Don't Care" if the collision occurs on the Master's "Start bit" |

#### 6.2.1.4 Repeated Start Bit

The Repeated Start bit (see Figure 6-5) indicates the current Master Device wishes to continue communicating with the current Slave Device without releasing the $I^2C$ bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “High”.

**Note 1:** A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

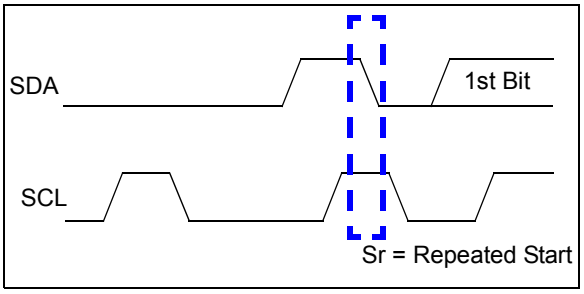



***FIGURE 6-5:*** *Repeat Start Condition Waveform.*

#### 6.2.1.5 Stop Bit

The Stop bit (see Figure 6-6) Indicates the end of the $I^2C$ Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “High”.

A Stop bit resets the $I^2C$ interface of all MCP44XX devices.

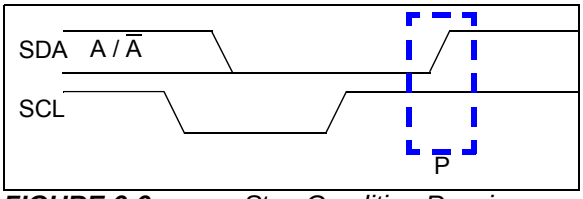



***FIGURE 6-6:*** *Stop Condition Receive or Transmit Mode.*

### 6.2.2 CLOCK STRETCHING

“Clock Stretching” is something that the receiving Device can do, to allow additional time to “respond” to the “data” that has been received.

The MCP44XX will not stretch the clock signal (SCL) since memory read access occur fast enough.

### 6.2.3 ABORTING A TRANSMISSION

If any part of the $I^2C$ transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a START or STOP condition. This is done so that noisy transmissions (usually an extra START or STOP condition) are aborted before they corrupt the device.

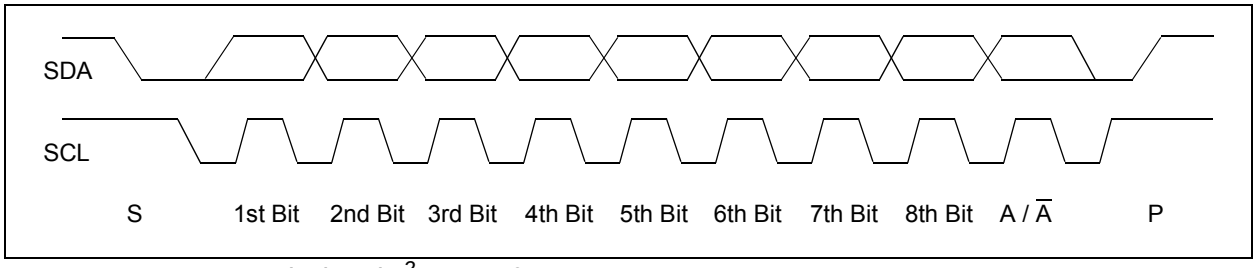



***FIGURE 6-7:*** *Typical 8-Bit $I^2C$ Waveform Format.*

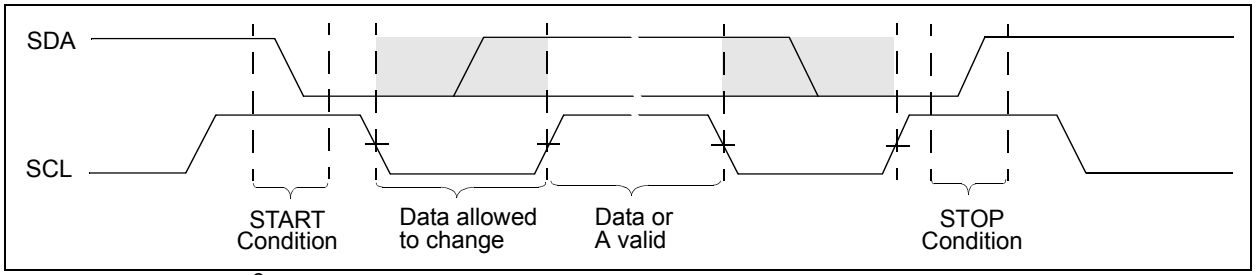



***FIGURE 6-8:*** *$I^2C$ Data States and Bit Sequence.*

### 6.2.4 ADDRESSING

The address byte is the first byte received following the START condition from the master device. The address contains four (or more) fixed bits and (up to) three user defined hardware address bits (pins A1 and A0). These 7-bits address the desired $I^2C$ device. The A6:A2 address bits are fixed to "01011" and the device appends the value of following two address pins (A1 and A0).

Since there are address bits controlled by hardware pins, there may be up to four MCP44XX devices on the same $I^2C$ bus.

Figure 6-9 shows the slave address byte format, which contains the seven address bits. There is also a read/write (R/$\overline{W}$) bit. Table 6-2 shows the fixed address for device.

#### Hardware Address Pins

The hardware address bits (A1, and A0) correspond to the logic level on the associated address pins. This allows up to eight devices on the bus.

These pins have a weak pull-up enabled when the $V_{DD} < V_{BOR}$. The weak pull-up utilizes the "smart" pull-up technology and exhibits the same characteristics as the High-voltage tolerant I/O structure.

The state of the A0 address pin is latch on POR/BOR. This is required since High Voltage commands force this pin (HVC/A0) to the $V_{IHH}$ level.

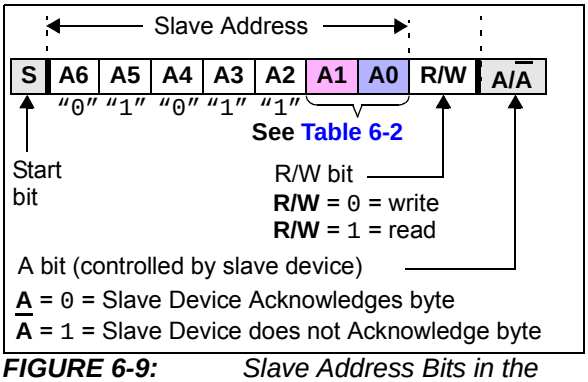



***FIGURE 6-9:*** *Slave Address Bits in the $I^2C$ Control Byte.*

**TABLE 6-2: DEVICE SLAVE ADDRESSES**

| Device | Address | Comment |
|---|---|---|
| MCP44XX | '0101 1'b + A1:A0 | Supports up to 4 devices. **(Note 1)** |

**Note 1:** A0 is used for High-Voltage commands (HVC/A0) and the value is latched at POR/BOR.

### 6.2.5 SLOPE CONTROL

The MCP44XX implements slope control on the SDA output.

As the device transitions from HS mode to FS mode, the slope control parameter will change from the HS specification to the FS specification.

For Fast (FS) and High-Speed (HS) modes, the device has a spike suppression and a Schmidt trigger at SDA and SCL inputs.

### 6.2.6 HS MODE

The $I^2C$ specification requires that a high-speed mode device must be 'activated' to operate in high-speed (3.4 Mbit/s) mode. This is done by the Master sending a special address byte following the START bit. This byte is referred to as the high-speed Master Mode Code (HSMMC).

The MCP44XX device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode. The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

The master code is sent as follows:

1. START condition (S)
2. High-Speed Master Mode Code (0000 1XXX), The XXX bits are unique to the high-speed (HS) mode Master.
3. No Acknowledge ($\overline{A}$)

After switching to the High-Speed mode, the next transferred byte is the $I^2C$ control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgements. The Master Device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other Master Device (in a Multi-Master system) can arbitrate for the $I^2C$ bus.

See Figure 6-10 for illustration of HS mode command sequence.

For more information on the HS mode, or other $I^2C$ modes, please refer to the Phillips $I^2C$ specification.

#### 6.2.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

#### 6.2.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

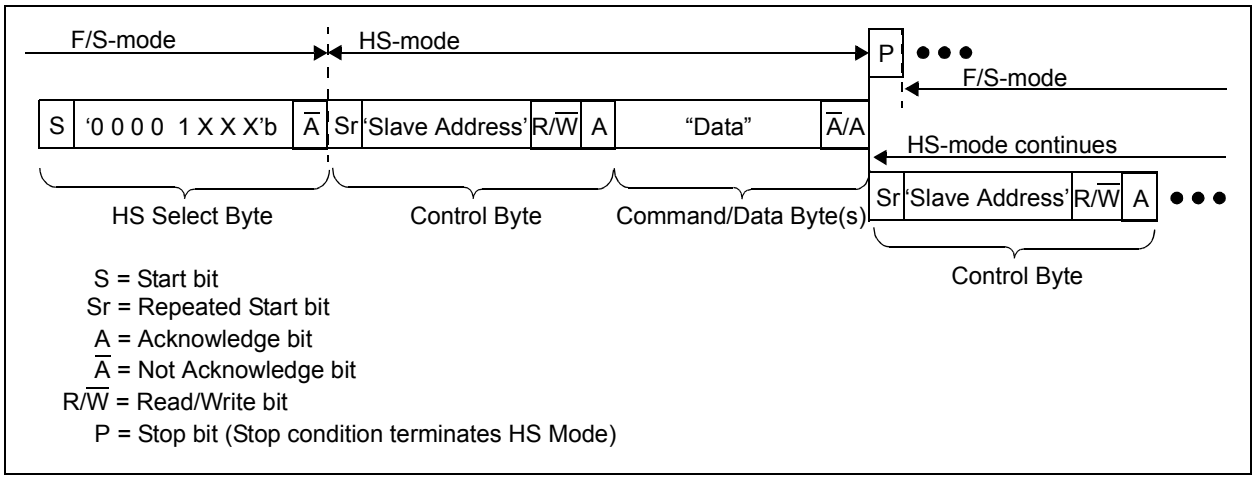



***FIGURE 6-10:*** *HS Mode Sequence.*

### 6.2.7 GENERAL CALL

The General Call is a method that the “Master” device can communicate with all other “Slave” devices. In a Multi-Master application, the other Master devices are operating in Slave mode. The General Call address has two documented formats. These are shown in Figure 6-11. We have added a MCP44XX format in this figure as well.

This will allow customers to have multiple $I^2C$ Digital Potentiometers on the bus and have them operate in a synchronous fashion (analogous to the DAC Sync pin functionality). If these MCP44XX 7-bit commands conflict with other $I^2C$ devices on the bus, then the customer will need two $I^2C$ busses and ensure that the devices are on the correct bus for their desired application functionality.

Dual Pot devices can not update both Pot0 and Pot1 from a single command. To address this, there are General Call commands for the Wiper 0, Wiper 1, and the TCON registers.

Table 6-3 shows the General Call Commands. Three commands are specified by the $I^2C$ specification and are not applicable to the MCP44XX (so command is Not Acknowledged) The MCP44XX General Call Commands are Acknowledge. Any other command is Not Acknowledged.

| **Note:** | Only one General Call command per issue of the General Call control byte. Any additional General Call commands are ignored and Not Acknowledged. |
|---|---|

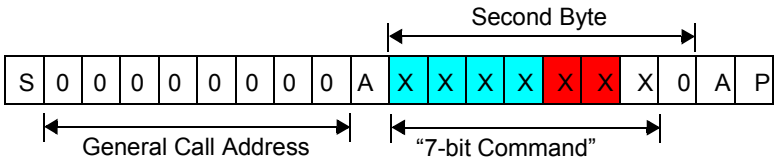
**TABLE 6-3: GENERAL CALL COMMANDS**

| **7-bit Command (1, 2, 3)** | **Comment** |
|---|---|
| ‘1000 00d’b | Write Next Byte (Third Byte) to Volatile Wiper 0 Register |
| ‘1001 00d’b | Write Next Byte (Third Byte) to Volatile Wiper 1 Register |
| ‘1100 00d’b | Write Next Byte (Third Byte) to TCON Register |
| ‘1000 010’b or ‘1000 011’b | Increment Wiper 0 Register |
| ‘1001 010’b or ‘1001 011’b | Increment Wiper 1 Register |
| ‘1000 100’b or ‘1000 101’b | Decrement Wiper 0 Register |
| ‘1001 100’b or ‘1001 101’b | Decrement Wiper 1 Register |

**Note 1:** Any other code is Not Acknowledged. These codes may be used by other devices on the $I^2C$ bus.

**2:** The 7-bit command always appends a “0” to form 8-bits.

**3:** “d” is the D8 bit for the 9-bit write value.



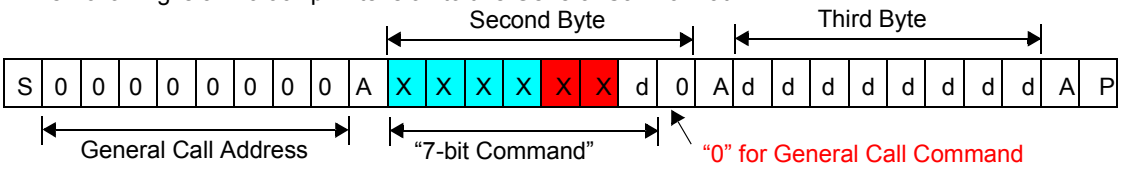

Reserved 7-bit Commands (By $I^2C$ Specification - Philips # 9398 393 40011, Ver. 2.1 January 2000)

- '0000 011'b - Reset and write programmable part of slave address by hardware.
- '0000 010'b - Write programmable part of slave address by hardware.
- '0000 000'b - NOT Allowed

MCP44XX 7-bit Commands

- '1000 01x'b - Increment Wiper 0 Register.
- '1001 01x'b - Increment Wiper 1 Register.
- '1000 10x'b - Decrement Wiper 0 Register.
- '1001 10x'b - Decrement Wiper 1 Register.

The Following is a Microchip Extension to this General Call Format




MCP44XX 7-bit Commands

- '1000 00d'b - Write Next Byte (Third Byte) to Volatile Wiper 0 Register.
- '1001 00d'b - Write Next Byte (Third Byte) to Volatile Wiper 1 Register.
- '1100 00d'b - Write Next Byte (Third Byte) to TCON Register.

The Following is a "Hardware General Call" Format

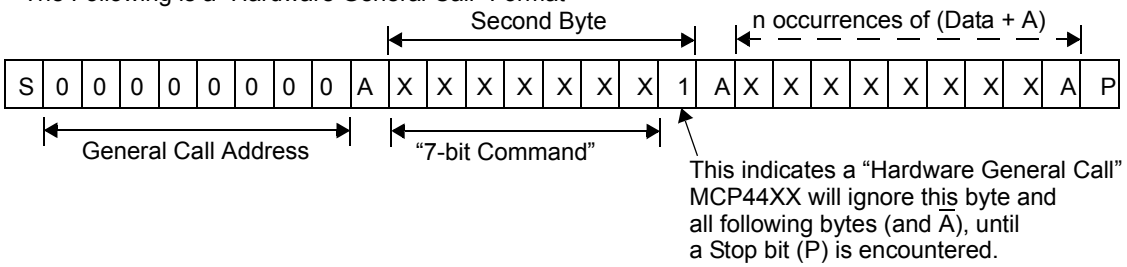



***FIGURE 6-11:*** *General Call Formats.*

**NOTES:**

## 7.0 DEVICE COMMANDS

The MCP44XX's $I^2C$ command formats are specified in this section. The $I^2C$ protocol does not specify how commands are formatted.

The MCP44XX supports four basic commands. The location accessed determines the commands that are supported.

For the Volatile Wiper Registers, these commands are:

- Write Data
- Read Data
- Increment Data
- Decrement Data

For the Nonvolatile wiper EEPROM, general purpose data EEPROM, and the TCON Register, these commands are:

- Write Data
- Read Data

These commands have formats for both a single command or continuous commands. These commands are shown in Table 7-1.

Each command has two operational states. The operational state determines if the device commands control the special features (Write Protect and WiperLock Technology). These operational states are referred to as:

- Normal Serial Commands
- High-Voltage Serial Commands

**TABLE 7-1: $I^2C$ COMMANDS**

| Command | | # of Bit Clocks (1) | Operates on Volatile/ Nonvolatile memory |
|---|---|---|---|
| **Operation** | **Mode** | | |
| Write Data | Single | 29 | Both |
| | Continuous | 18n + 11 | Volatile Only |
| Read Data | Single | 29 | Both |
| | Random | 48 | Both |
| | Continuous | 18n + 11 | Both (2) |
| Increment (3) | Single | 20 | Volatile Only |
| | Continuous | 9n + 11 | Volatile Only |
| Decrement (3) | Single | 20 | Volatile Only |
| | Continuous | 9n + 11 | Volatile Only |

**Note 1:** "n" indicates the number of times the command operation is to be repeated.

**2:** This command is useful to determine if a nonvolatile memory write cycle has completed.

**3:** High Voltage Increment and Decrement commands on select nonvolatile memory locations enable/disable WiperLock Technology and the software Write Protect feature.

Normal serial commands are those where the HVC pin is driven to $V_{IH}$ or $V_{IL}$. With High-Voltage Serial Commands, the HVC pin is driven to $V_{IHH}$. In each mode, there are four possible commands.

Additionally, there are two commands used to enable or disable the special features (Write Protect and Wiper Lock Technology) of the device. The commands are special cases of the Increment and Decrement High-Voltage Serial Command.

Table 7-2 shows the supported commands for each memory location.

Table 7-3 shows an overview of all the device commands and their interaction with other device features.

### 7.1 Command Byte

The MCP44XX's Command Byte has three fields: the Address, the Command Operation, and 2 Data bits (see Figure 7-1). Currently only one of the data bits is defined (D8).

The device memory is accessed when the Master sends a proper Command Byte to select the desired operation. The memory location getting accessed is contained in the Command Byte's AD3:AD0 bits. The action desired is contained in the Command Byte's C1:C0 bits, see Figure 7-1. C1:C0 determines if the desired memory location will be read, written, Incremented (wiper setting +1) or Decremented (wiper setting -1). The Increment and Decrement commands are only valid on the volatile wiper registers, and in High Voltage commands to enable/disable WiperLock Technology and Software Write Protect.

If the Address bits and Command bits are not a valid combination, then the MCP44XX will generate a Not Acknowledge pulse to indicate the invalid combination. The $I^2C$ Master device must then force a Start Condition to reset the MCP44XX's $I^2C$ module.

D9 and D8 are the most significant bits for the digital potentiometer's wiper setting. The 8-bit devices utilize D8 as their MSb while the 7-bit devices utilize D7 (from the data byte) as their MSb.

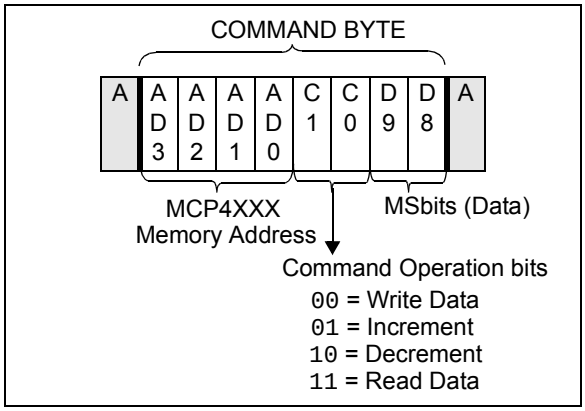



***FIGURE 7-1:*** *Command Byte Format.*

**TABLE 7-2: MEMORY MAP AND THE SUPPORTED COMMANDS**

| Address | | Command | Data (10-bits) (1) | Comment |
|---|---|---|---|---|
| Value | Function | | | |
| 00h | Volatile Wiper 0 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | Increment Wiper | — | |
| | | Decrement Wiper | — | |
| 01h | Volatile Wiper 1 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | Increment Wiper | — | |
| | | Decrement Wiper | — | |
| 02h | NV Wiper 0 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | High Voltage Increment | — | Wiper Lock 0 Disable (4) |
| | | High Voltage Decrement | — | Wiper Lock 0 Enable (5) |
| 03h | NV Wiper 1 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | High Voltage Increment | — | Wiper Lock 1 Disable (4) |
| | | High Voltage Decrement | — | Wiper Lock 1 Enable (5) |
| 04h (2) | Volatile TCON 0 Register | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 05h (2) | Status Register | Read Data (3) | nn nnnn nnnn | |
| 06h | Volatile Wiper 2 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | Increment Wiper | — | |
| | | Decrement Wiper | — | |
| 07h | Volatile Wiper 3 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | Increment Wiper | — | |
| | | Decrement Wiper | — | |
| 08h | NV Wiper 2 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | High Voltage Increment | — | Wiper Lock 2 Disable (4) |
| | | High Voltage Decrement | — | Wiper Lock 2 Enable (5) |
| 09h | NV Wiper 3 | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | High Voltage Increment | — | Wiper Lock 3 Disable (4) |
| | | High Voltage Decrement | — | Wiper Lock 3 Enable (5) |
| 0Ah (2) | Volatile TCON 1 Register | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 0Bh (2) | Data EEPROM | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 0Ch (2) | Data EEPROM | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 0Dh (2) | Data EEPROM | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 0Eh (2) | Data EEPROM | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| 0Fh | Data EEPROM | Write Data | nn nnnn nnnn | |
| | | Read Data (3) | nn nnnn nnnn | |
| | | High Voltage Increment | — | Write Protect Disable (4) |
| | | High Voltage Decrement | — | Write Protect Enable (5) |

**Note 1:** The Data Memory is only 9-bits wide, so the MSb is ignored by the device.
**2:** Increment or Decrement commands are invalid for these addresses.
**3:** $I^2C$ read operation will read 2 bytes, of which the 10-bits of data are contained within.
**4:** Disables WiperLock Technology for wiper 0, wiper 1, wiper 2, wiper3, or disables Write Protect.
**5:** Enables WiperLock Technology for wiper 0, wiper 1, wiper 2, wiper3, or enables Write Protect.

## 7.2 Data Byte

Only the Read Command and the Write Command have Data Byte(s).

The Write command concatenates the 8 bits of the Data Byte with the one data bit (D8) contained in the Command Byte to form 9 bits of data (D8:D0). The Command Byte format supports up to 9 bits of data so that the 8-bit resistor network can be set to Full-Scale (100h or greater). This allows wiper connections to Terminal A and to Terminal B. The D9 bit is currently unused.

## 7.3 Error Condition

If the four address bits received (AD3:AD0) and the two command bits received (C1:C0) are a valid combination, the MCP44XX will Acknowledge the $I^2C$ bus.

If the address bits and command bits are an invalid combination, then the MCP44XX will Not Acknowledge the $I^2C$ bus.

Once an error condition has occurred, any following commands are ignored until the $I^2C$ bus is reset with a Start Condition.

### 7.3.1 ABORTING A TRANSMISSION

A Restart or Stop condition in the expected data bit position will abort the current command sequence and data will not be written to the MCP44XX.

**TABLE 7-3: COMMANDS**

| Command Name | Writes Value in EEPROM | Operates on Volatile/ Nonvolatile memory | High Voltage ($V_{IHH}$) on HVC pin? | Impact on WiperLock or Write Protect | Works when Wiper is "locked"? |
|---|---|---|---|---|---|
| **Write Data** | Yes (1) | Both | — | unlocked (1) | No |
| **Read Data** | — | Both | — | unlocked (1) | No |
| **Increment Wiper** | — | Volatile Only | — | unlocked (1) | No |
| **Decrement Wiper** | — | Volatile Only | — | unlocked (1) | No |
| High Voltage **Write Data** | Yes | Both | Yes | unchanged | No |
| High Voltage **Read Data** | — | Both | Yes | unchanged | Yes |
| High Voltage **Increment Wiper** | — | Volatile Only | Yes | unchanged | No |
| High Voltage **Decrement Wiper** | — | Volatile Only | Yes | unchanged | No |
| **Modify Write Protect or WiperLock Technology (High Voltage)** - Enable | — (2) | Nonvolatile Only (2) | Yes | locked/ protected (2) | Yes |
| **Modify Write Protect or WiperLock Technology (High Voltage)** - Disable | — (3) | Nonvolatile Only (3) | Yes | unlocked/ unprotected (3) | Yes |

**Note 1:** This command will only complete, if wiper is "unlocked" (WiperLock Technology is Disabled).

**2:** If the command is executed using address 02h, 03h 08h, or 09h; that corresponding wiper is locked or if with address 0Fh, then Write Protect is enabled.

**3:** If the command is executed using with address 02h, 03h 08h, or 09h; that corresponding wiper is unlocked or if with address 0Fh, then Write Protect is disabled.

## 7.4 Write Data Normal and High Voltage

The Write Command can be issued to both the Volatile and Nonvolatile memory locations. The format of the command, see Figure 7-2, includes the $I^2C$ Control Byte, an A bit, the MCP44XX Command Byte, an A bit, the MCP44XX Data Byte, an A bit, and a Stop (or Restart) condition. The MCP44XX generates the A / $\overline{A}$ bits.

A Write command to a Volatile memory location changes that location after a properly formatted Write Command and the A / $\overline{A}$ clock have been received.

A Write command to a Nonvolatile memory location will only start a write cycle after a properly formatted Write Command have been received and the Stop condition has occurred.

| **Note:** | Writes to certain memory locations will be dependant on the state of the WiperLock Technology bits and the Write Protect bit. |
|---|---|

### 7.4.1 SINGLE WRITE TO VOLATILE MEMORY

For volatile memory locations, data is written to the MCP44XX after every byte transfer (during the Acknowledge). If a Stop or Restart condition is generated during a data transfer (before the A), the data will not be written to the MCP44XX. After the A bit, the master can initiate the next sequence with a Stop or Restart condition.

Refer to Figure 7-2 for the byte write sequence.

### 7.4.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that the EEPROM write cycle ($t_{WC}$) is started after a properly formatted command, including the Stop bit, is received. After the Stop condition occurs, the serial interface may immediately be re-enabled by initiating a Start condition.

During an EEPROM write cycle, access to the volatile memory (addresses 00h, 01h, 04h, 05h, 06h, 07h, and 0Ah) is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the EEPROM write cycle ($t_{WC}$) completes. This allows the Host Controller to operate on the Volatile Wiper registers, the TCON register, and to Read the Status Register. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

Once a write command to a Nonvolatile memory location has been received, no other commands should be received before the Stop condition occurs.

Figure 7-2 shows the waveform for a single write.

### 7.4.3 CONTINUOUS WRITES TO VOLATILE MEMORY

A continuous write mode of operation is possible when writing to the volatile memory registers (address 00h, 01h, 04h, 06h, 07h, and 0Ah). This continuous write mode allows writes without a Stop or Restart condition or repeated transmissions of the $I^2C$ Control Byte. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the master sending a STOP or RESTART condition.

### 7.4.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

If a continuous write is attempted on Nonvolatile memory, the missing Stop condition will cause the command to be an error condition ($\overline{A}$). A Start bit is required to reset the command state machine.

### 7.4.5 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage operational state. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

The HVC pin has an internal resistor connection to the MCP44XXs internal $V_{DD}$ signal.

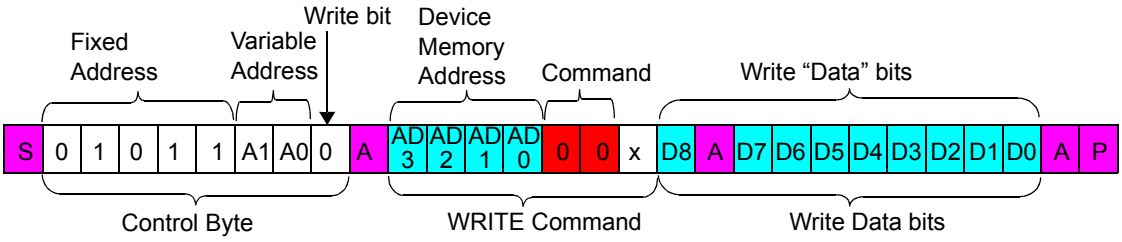
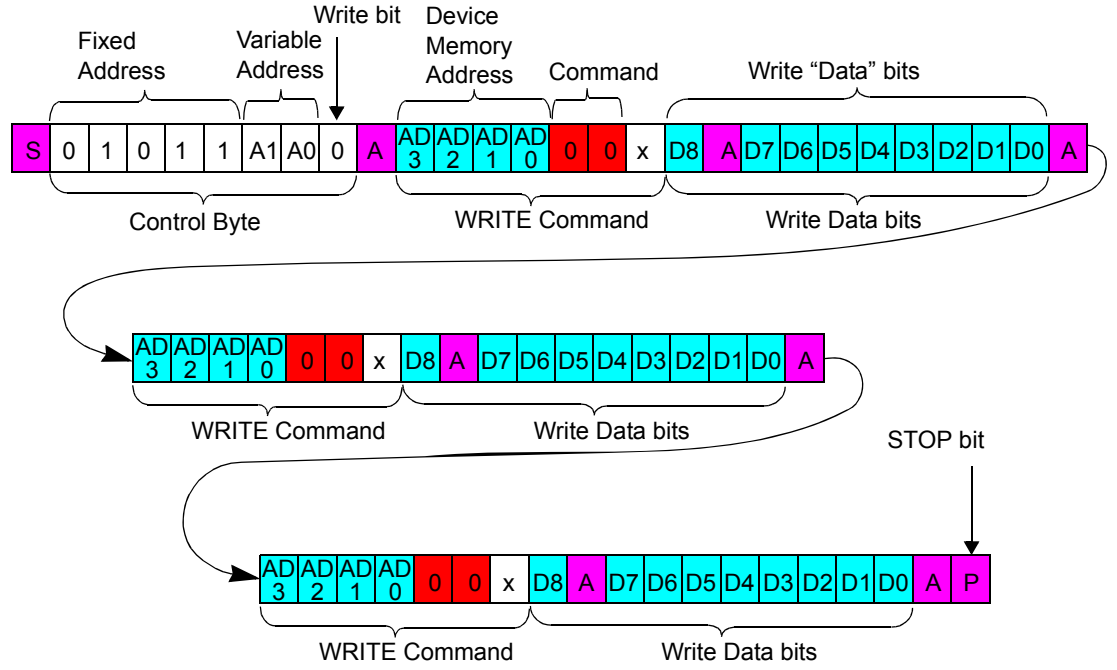



***FIGURE 7-2:*** *$I^2C$ Write Sequence.*




**Note:** Only functions when writing the volatile wiper registers (AD3:AD0 = 00h, 01h, 06h, and 07h) or the TCON registers (AD3:AD0 = 04h and 0Ah)

***FIGURE 7-3:*** *$I^2C$ Continuous Volatile Wiper Write.*

## 7.5 Read Data Normal and High Voltage

The Read Command can be issued to both the Volatile and Nonvolatile memory locations. The format of the command (see Figure 7-4), includes the Start condition, $I^2C$ Control Byte (with R/W bit set to “0”), A bit, MCP44XX Command Byte, A bit, followed by a Repeated Start bit, $I^2C$ Control Byte (with R/W bit set to “1”), and the MCP44XX transmitting the requested Data High Byte, and A bit, the Data Low Byte, the Master generating the $\overline{A}$, and Stop condition.

The $I^2C$ Control Byte requires the R/W bit equal to a logic one (R/W = 1) to generate a read sequence. The memory location read will be the last address contained in a valid write MCP44XX Command Byte or address 00h if no write operations have occurred since the device was reset (Power-on Reset or Brown-out Reset).

During a write cycle (Write or High Voltage Write to a Nonvolatile memory location) the Read command can only read the Volatile memory locations. By reading the Status Register (05h), the Host Controller can determine when the write cycle has completed (via the state of the EEWA bit).

Read operations initially include the same address byte sequence as the write sequence (shown in Figure 6-9). This sequence is followed by another control byte (including the Start condition and Acknowledge) with the R/W bit equal to a logic one (R/W = 1) to indicate a read. The MCP44XX will then transmit the data contained in the addressed register. This is followed by the master generating an A bit in preparation for more data, or an $\overline{A}$ bit followed by a Stop. The sequence is ended with the master generating a Stop or Restart condition.

The internal address pointer is maintained. If this address pointer is for a nonvolatile memory address and the read control byte addresses the device during a Nonvolatile Write Cycle ($t_{WC}$) the device will respond with an $\overline{A}$ bit.

### 7.5.1 SINGLE READ

Figure 7-4 show the waveforms for a single read.

For ***single reads*** the master sends a STOP or RESTART condition after the data byte is sent from the slave.

#### 7.5.1.1 Random Read

Figure 7-5 shows the sequence for a Random Reads.

Refer to Figure 7-5 for the random byte read sequence.

### 7.5.2 CONTINUOUS READS

Continuous reads allows the devices memory to be read quickly. Continuous reads are possible to all memory locations. If a nonvolatile memory write cycle is occurring, then Read commands may only access the volatile memory locations.

Figure 7-6 shows the sequence for three continuous reads.

For ***continuous reads***, instead of transmitting a Stop or Restart condition after the data transfer, the master reads the next data byte. The sequence ends with the master Not Acknowledging and then sending a Stop or Restart.

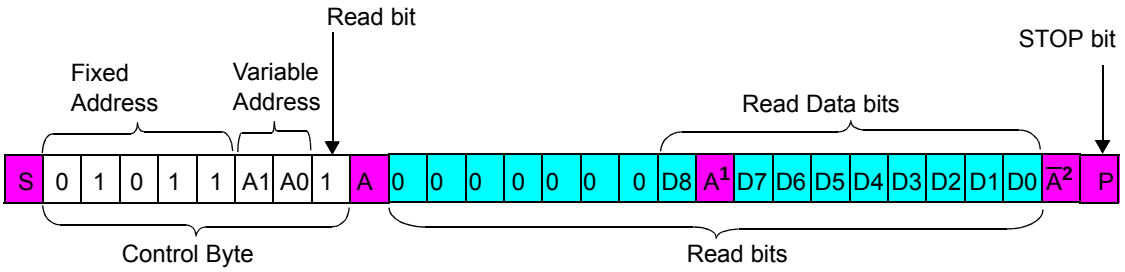
### 7.5.3 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. High Voltage commands allow the device’s WiperLock Technology and write protect features to be enabled and disabled.

The HVC pin has an internal resistor connection to the MCP44XX’s internal $V_{DD}$ signal.

### 7.5.4 IGNORING AN $I^2C$ TRANSMISSION AND “FALLING OFF” THE BUS

The MCP44XX expects to receive complete, valid $I^2C$ commands and will assume any command not defined as a valid command is due to a bus corruption and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and Control Byte are received.



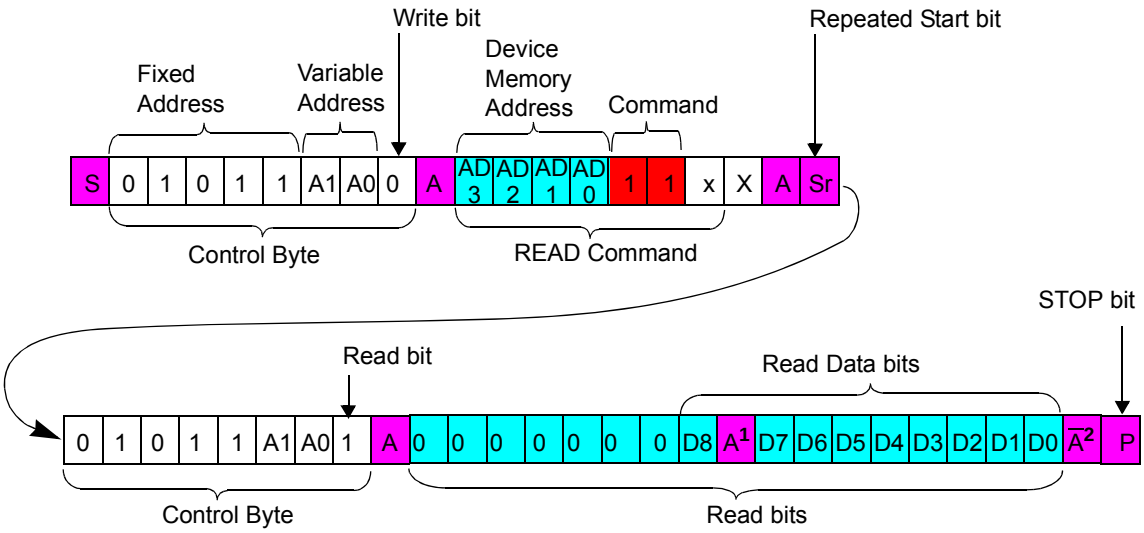

**Note 1:** Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP44XX will abort this transfer and release the bus.

**2:** The Master Device will Not Acknowledge, and the MCP44XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

**3:** The MCP44XX retains the last “Device Memory Address” that it has received. This is the MCP44XX does not “corrupt” the “Device Memory Address” after Repeated Start or Stop conditions.

**4:** The Device Memory Address pointer defaults to 00h on POR and BOR conditions.

***FIGURE 7-4:*** *$I^2C$ Read (Last Memory Address Accessed).*

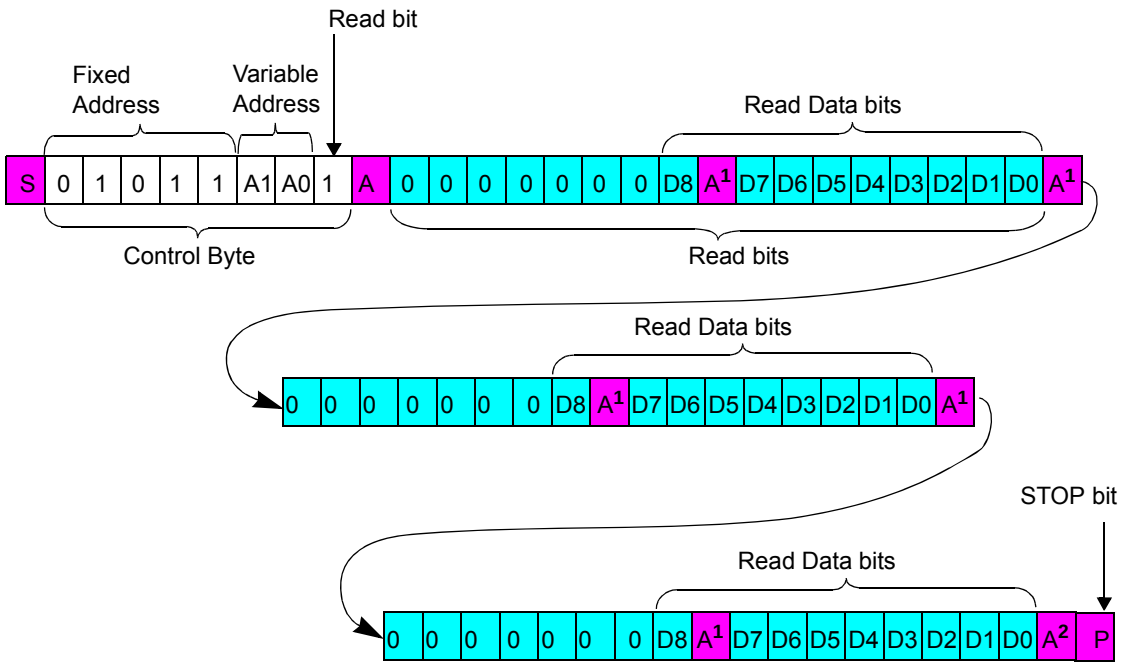



**Note 1:** Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP44XX will abort this transfer and release the bus.

**2:** The Master Device will Not Acknowledge, and the MCP44XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

**3:** The MCP44XX retains the last “Device Memory Address” that it has received. This is the MCP44XX does not “corrupt” the “Device Memory Address” after Repeated Start or Stop conditions.

***FIGURE 7-5:*** *$I^2C$ Random Read.*




**Note 1:** Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP44XX will abort this transfer and release the bus.

**2:** The Master Device will Not Acknowledge, and the MCP44XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

***FIGURE 7-6:*** *$I^2C$ Continuos Reads.*

## 7.6 Increment Wiper Normal and High Voltage

The Increment Command provides a quick and easy method to modify the potentiometer's wiper by +1 with minimal overhead. The Increment Command will only function on the volatile wiper setting memory locations 00h, 01h, 06h and 07h. The Increment Command to Nonvolatile addresses will be ignored and will generate a $\overline{A}$.

**Note:** Table 7-4 shows the valid addresses for the Increment Wiper command. Other addresses are invalid.

When executing an Increment Command, the volatile wiper setting will be altered from n to n+1 for each Increment Command received. The value will increment up to 100h max on 8-bit devices and 80h on 7-bit devices. If multiple Increment Commands are received after the value has reached 100h (or 80h), the value will not be incremented further. Table 7-4 shows the Increment Command versus the current volatile wiper value.

The Increment Command will most commonly be performed on the Volatile Wiper locations until a desired condition is met. The value in the Volatile Wiper register would need to be read using a Read operation in order to write the new setting to the corresponding Nonvolatile wiper memory using a Write operation. The MCP44XX is responsible for generating the A bits.

Refer to Figure 7-7 for the Increment Command sequence. The sequence is terminated by the Stop condition. So when executing a continuous command string, the Increment command can be followed by any other valid command. This means that writes do not need to be to the same volatile memory address.

**Note:** The command sequence can go from an increment to any other valid command for the specified address. Issuing an increment or decrement to a nonvolatile location will cause an error condition ($\overline{A}$ will be generated).

The advantage of using an Increment Command instead of a read-modify-write series of commands is speed and simplicity. The wiper will transition after each Command Acknowledge when accessing the volatile wiper registers.

**TABLE 7-4: INCREMENT OPERATION VS. VOLATILE WIPER VALUE**

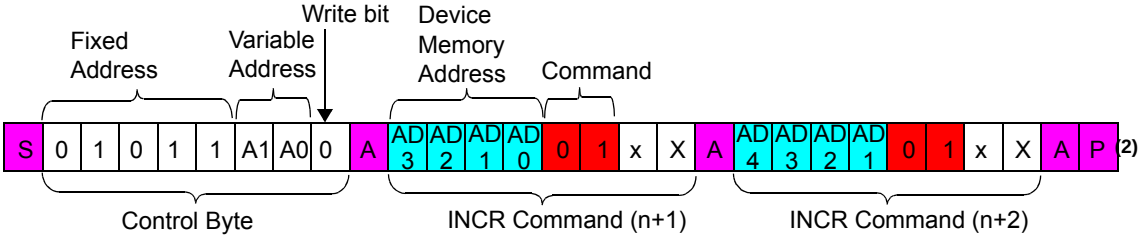
| Current Wiper Setting | | Wiper (W) Properties | Increment Command Operates? |
|---|---|---|---|
| 7-bit Pot | 8-bit Pot | | |
| 3FFh<br>081h | 3FFh<br>101h | Reserved<br>(Full-Scale (W = A)) | No |
| 080h | 100h | Full-Scale (W = A) | No |
| 07Fh<br>041h | 0FFh<br>081 | W = N | Yes |
| 040h | 080h | W = N (Mid-Scale) | |
| 03Fh<br>001h | 07Fh<br>001 | W = N | |
| 000h | 000h | Zero Scale (W = B) | Yes |

### 7.6.1 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. Signals > $V_{IHH}$ (~8.5V) on the HVC/A0 pin puts MCP44XX devices into High Voltage mode. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

**Note:** There is a required delay after the HVC pin is driven to the $V_{IHH}$ level to the 1st edge of the SCL pin.

The HVC pin has an internal resistor connection to the MCP44XX's internal $V_{DD}$ signal.




**Note1:** Increment Command (INCR) only functions when accessing the volatile wiper registers (AD3:AD0 = 00h, 01h, 06h, and 07h).

**2:** This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (Increment, Read, or Write).

***FIGURE 7-7:*** *$I^2C$ Increment Command Sequence.*

## 7.7 Decrement Wiper Normal and High Voltage

The Decrement Command provides a quick and easy method to modify the potentiometer's wiper by -1 with minimal overhead. The Decrement Command will only function on the volatile wiper setting memory locations 00h and 01h. Decrement Commands to Nonvolatile addresses will be ignored and will generate an $\overline{A}$ bit.

**Note:** Table 7-5 shows the valid addresses for the Decrement Wiper command. Other addresses are invalid.

When executing a Decrement Command, the volatile wiper setting will be altered from n to n-1 for each Decrement Command received. The value will decrement down to 000h min. If multiple Decrement Commands are received after the value has reached 000h, the value will not be decremented further. Table 7-5 shows the Increment Command versus the current volatile wiper value.

The Decrement Command will most commonly be performed on the Volatile Wiper locations until a desired condition is met. The value in the Volatile Wiper register would need to be read using a Read operation in order to write the new setting to the corresponding Nonvolatile wiper memory using a Write operation. The MCP44XX is responsible for generating the A bits.

Refer to Figure 7-8 for the Decrement Command sequence. The sequence is terminated by the Stop condition. So when executing a continuous command string, the Increment command can be followed by any other valid command. This means that writes do not need to be to the same volatile memory address.

**Note:** The command sequence can go from an increment to any other valid command for the specified address. Issuing an increment or decrement to a nonvolatile location will cause an error condition ($\overline{A}$ will be generated).

The advantage of using a Decrement Command instead of a read-modify-write series of commands is speed and simplicity. The wiper will transition after each Command Acknowledge when accessing the volatile wiper registers.

**TABLE 7-5: DECREMENT OPERATION VS. VOLATILE WIPER VALUE**

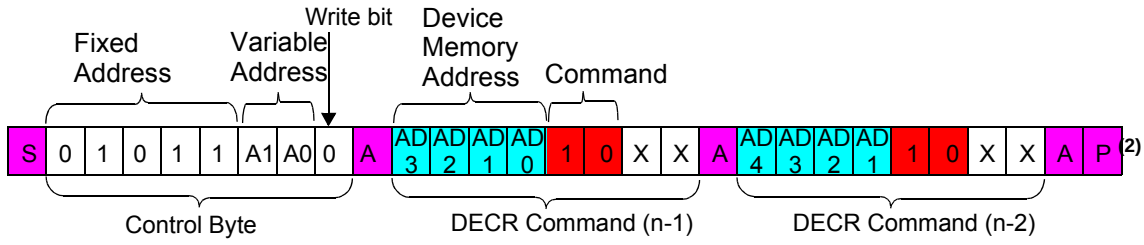
| Current Wiper Setting | | Wiper (W) Properties | Decrement Command Operates? |
|---|---|---|---|
| 7-bit Pot | 8-bit Pot | | |
| 3FFh 081h | 3FFh 101h | Reserved (Full-Scale (W = A)) | No |
| 080h | 100h | Full-Scale (W = A) | Yes |
| 07Fh 041h | 0FFh 081 | W = N | Yes |
| 040h | 080h | W = N (Mid-Scale) | |
| 03Fh 001h | 07Fh 001 | W = N | |
| 000h | 000h | Zero Scale (W = B) | No |

### 7.7.1 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. Signals > $V_{IHH}$ (~8.5V) on the HVC/A0 pin puts MCP44XX devices into High Voltage mode. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

**Note:** There is a required delay after the HVC pin is driven to the $V_{IHH}$ level to the 1st edge of the SCL pin.

The HVC pin has an internal resistor connection to the MCP44XX's internal $V_{DD}$ signal.




**Note1:** Decrement Command (DECR) only functions when accessing the volatile wiper registers (AD3:AD0 = 00h, 01h, 06h, and 07h).

**2:** This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (INCR, Read, or Write).

***FIGURE 7-8:*** *$I^2C$ Decrement Command Sequence.*

## 7.8 Modify Write Protect or WiperLock Technology (High Voltage) Enable and Disable

These commands are special cases of the High Voltage **Decrement Wiper** and the High Voltage **Increment Wiper** commands to the nonvolatile memory locations 02h, 03h, 08h, 09h, and 0Fh. This command is used to enable or disable either the software Write Protect, wiper 0 WiperLock Technology, wiper 1 WiperLock Technology, wiper 2 WiperLock Technology, or wiper 3 WiperLock Technology. Table 7-6 shows the memory addresses, the High Voltage command and the result of those commands on the nonvolatile WP, WL0, or WL1 bits.

### 7.8.1 SINGLE MODIFY (ENABLE OR DISABLE) WRITE PROTECT OR WIPERLOCK TECHNOLOGY (HIGH VOLTAGE)

Figure 7-9 (Disable) and Figure 7-10 (Enable) show the formats for a single Modify Write Protect or Wiper-Lock Technology command.

A Modify Write Protect or WiperLock Technology Command will only start an EEPROM write cycle ($t_{WC}$) after a properly formatted Command has been received and the Stop condition occurs.

During an EEPROM write cycle, only serial commands to Volatile memory (addresses 00h, 01h, 04h, and 05h) are accepted. All other serial commands are ignored until the EEPROM write cycle ($t_{WC}$) completes. This allows the Host Controller to operate on the Volatile Wiper registers and the TCON register, and to Read the Status Register. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

**TABLE 7-6: ADDRESS MAP TO MODIFY WRITE PROTECT AND WIPERLOCK TECHNOLOGY**

| Memory Address | Commands and Results | |
|---|---|---|
| | **High Voltage Decrement Wiper** | **High Voltage Increment Wiper** |
| 00h | Wiper 0 register is decremented | Wiper 0 register is incremented |
| 01h | Wiper 1 register is decremented | Wiper 1 register is incremented |
| 02h | WL0 is enabled | WL0 is disabled |
| 03h | WL1 is enabled | WL1 is disabled |
| 04h (1) | TCON0 register not changed | TCON0 register not changed |
| 05h (1) | STATUS register not changed | STATUS register not changed |
| 06h | Wiper 2 register is decremented | Wiper 2 register is incremented |
| 07h | Wiper 3 register is decremented | Wiper 3 register is incremented |
| 08h | WL2 is enabled | WL2 is disabled |
| 09h | WL3 is enabled | WL3 is disabled |
| 0Ah (1) | TCON1 register not changed | TCON1 register not changed |
| 0Bh - 0Eh (1) | Reserved | Reserved |
| 0Fh | WP is enabled | WP is disabled |

**Note 1: Reserved addresses:** Increment or Decrement commands are invalid for these addresses.

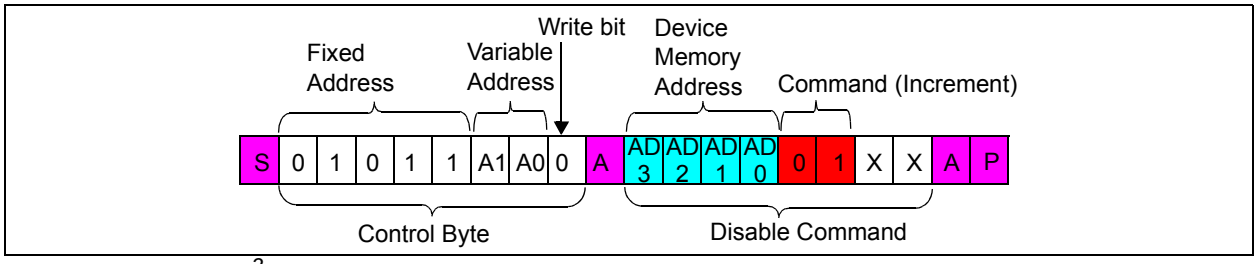



***FIGURE 7-9:*** *$I^2C$ Disable Command Sequence.*

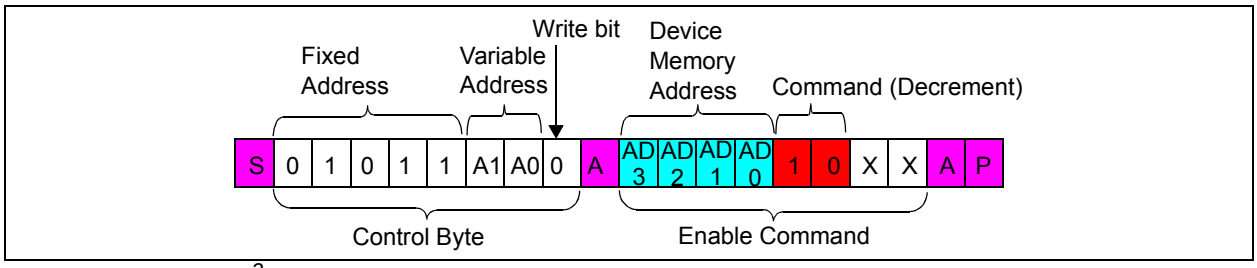



***FIGURE 7-10:*** *$I^2C$ Enable Command Sequence.*

## 8.0 APPLICATIONS EXAMPLES

Nonvolatile digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP44XX devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations ($V_{DD}$ = 2.7V to 5.5V).

### 8.1 Techniques to Force the HVC/A0 Pin to $V_{IHH}$

The circuit in Figure 8-1 shows a method using the TC1240A doubling charge pump. When the SHDN pin is high, the TC1240A is off, and the level on the HVC/A0 pin is controlled by the PIC® microcontrollers (MCUs) IO2 pin.

When the SHDN pin is low, the TC1240A is on and the $V_{OUT}$ voltage is 2 * $V_{DD}$. The resistor $R_1$ allows the HVC/A0 pin to go higher than the voltage such that the PIC MCU's IO2 pin "clamps" at approximately $V_{DD}$.

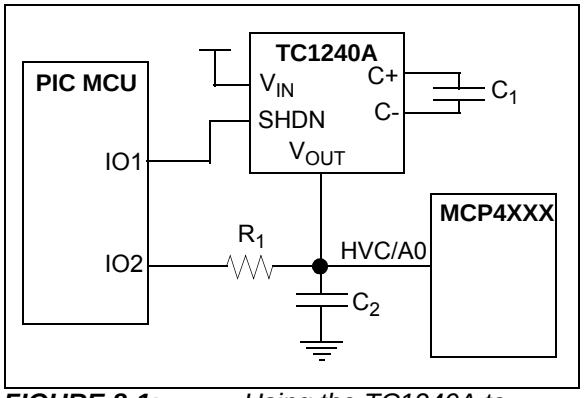



***FIGURE 8-1:*** *Using the TC1240A to Generate the $V_{IHH}$ Voltage.*

The circuit in Figure 8-2 shows the method used on the MCP402X Nonvolatile Digital Potentiometer Evaluation Board (Part Number: MCP402XEV). This method requires that the system voltage be approximately 5V. This ensures that when the PIC10F206 enters a brown-out condition, there is an insufficient voltage level on the HVC/A0 pin to change the stored value of the wiper. The MCP402X Nonvolatile Digital Potentiometer Evaluation Board User's Guide (DS51546) contains a complete schematic.

GP0 is a general purpose I/O pin, while GP2 can either be a general purpose I/O pin or it can output the internal clock.

For the serial commands, configure the GP2 pin as an input (high impedance). The output state of the GP0 pin will determine the voltage on the HVC/A0 pin ($V_{IL}$ or $V_{IH}$).

For high-voltage serial commands, force the GP0 output pin to output a high level ($V_{OH}$) and configure the GP2 pin to output the internal clock. This will form a charge pump and increase the voltage on the $\overline{CS}$ pin (when the system voltage is approximately 5V).

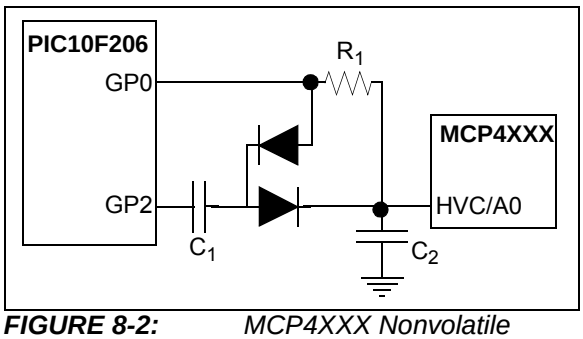



***FIGURE 8-2:*** *MCP4XXX Nonvolatile Digital Potentiometer Evaluation Board (MCP402XEV) implementation to generate the $V_{IHH}$ voltage.*

## 8.2 Using Shutdown Modes

Figure 8-3 shows a possible application circuit where the independent terminals could be used. Disconnecting the wiper allows the transistor input to be taken to the Bias voltage level (disconnecting A and or B may be desired to reduce system current). Disconnecting Terminal A modifies the transistor input by the $R_{BW}$ rheostat value to the Common B. Disconnecting Terminal B modifies the transistor input by the $R_{AW}$ rheostat value to the Common A. The Common A and Common B connections could be connected to $V_{DD}$ and $V_{SS}$.

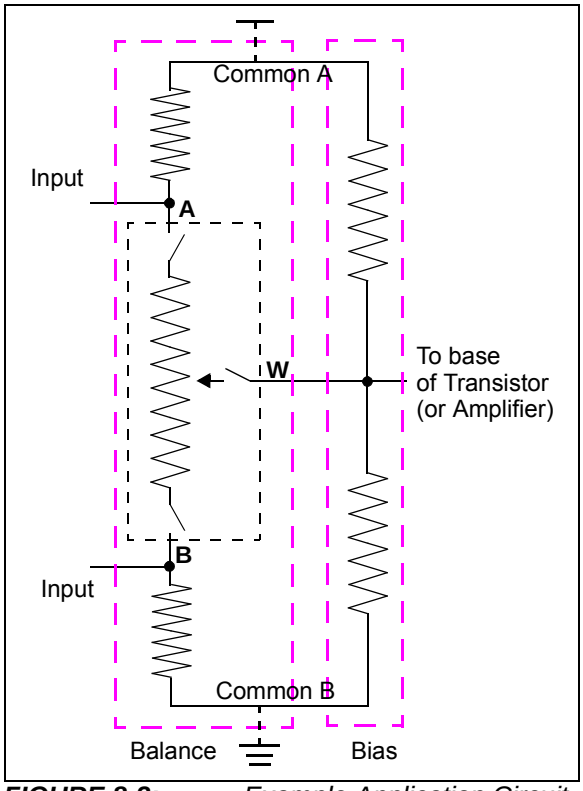



***FIGURE 8-3:*** *Example Application Circuit using Terminal Disconnects.*

## 8.3 Software Reset Sequence

**Note:** This technique is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP44XX device is in a correct and known $I^2C$ Interface state. This technique only resets the $I^2C$ state machine.

This is useful if the MCP44XX device powers up in an incorrect state (due to excessive bus noise, etc), or if the Master Device is reset during communication. Figure 8-4 shows the communication sequence to software reset the device.

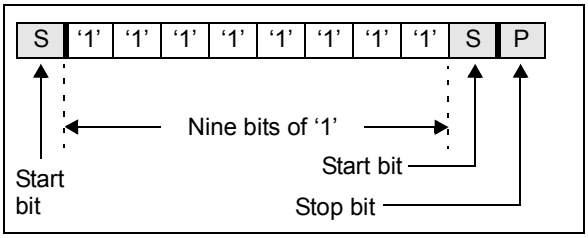



***FIGURE 8-4:*** *Software Reset Sequence Format.*

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master Device. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP44XX is driving an A bit on the $I^2C$ bus, or is in output mode (from a Read command) and is driving a data bit of '0' onto the $I^2C$ bus. In both of these cases, the previous Start bit could not be generated due to the MCP44XX holding the bus low. By sending out nine '1' bits, it is ensured that the device will see a $\overline{A}$ bit (the Master Device does not drive the $I^2C$ bus low to acknowledge the data sent by the MCP44XX), which also forces the MCP44XX to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master Device was reset while sending a Write command to the MCP44XX, AND then as the Master Device returns to normal operation and issues a Start condition while the MCP44XX is issuing an Acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP44XX could initiate a write cycle.

**Note:** The potential for this erroneous write ONLY occurs if the Master Device is reset while sending a Write command to the MCP44XX.

The Stop bit terminates the current $I^2C$ bus activity. The MCP44XX waits to detect the next Start condition.

This sequence does not effect any other $I^2C$ devices which may be on the bus, as they should disregard this as an invalid command.

## 8.4 Using the General Call Command

The use of the General Call Address Increment, Decrement, or Write commands is analogous to the "Load" feature (LDAC pin) on some DACs (such as the MCP4921). This allows all the devices to "Update" the output level "at the same time".

For some applications, the ability to update the wiper values "at the same time" may be a requirement, since they delay from writing to one wiper value and then the next may cause application issues. A possible example would be a "tuned" circuit that uses several MCP44XX in rheostat configuration. As the system condition changes (temperature, load, etc.) these devices need to be changed (incremented/decremented) to adjust for the system change. These changes will either be in the same direction or in opposite directions. With the Potentiometer device, the customer can either select the PxB terminals (same direction) or the PxA terminal(s) (opposite direction).

Figure 8-6 shows that the update of six devices takes $6*T_{I2CDLY}$ time in "normal" operation, but only $1*T_{I2CDLY}$ time in "General Call" operation.

| **Note:** | The application system may need to partition the $I^2C$ bus into multiple busses to ensure that the MCP44XX General Call commands do not conflict with the General Call commands that the other $I^2C$ devices may have defined. Also if only a portion of the MCP44XX devices are to require this synchronous operation, then the devices that should not receive these commands should be on the second $I^2C$ bus. |
|---|---|

Figure 8-5 shows two $I^2C$ bus configurations. In many cases, the single $I^2C$ bus configuration will be adequate. For applications that do not want all the MCP44XX devices to do General Call support or have a conflict with General Call commands, the multiple $I^2C$ bus configuration would be used.

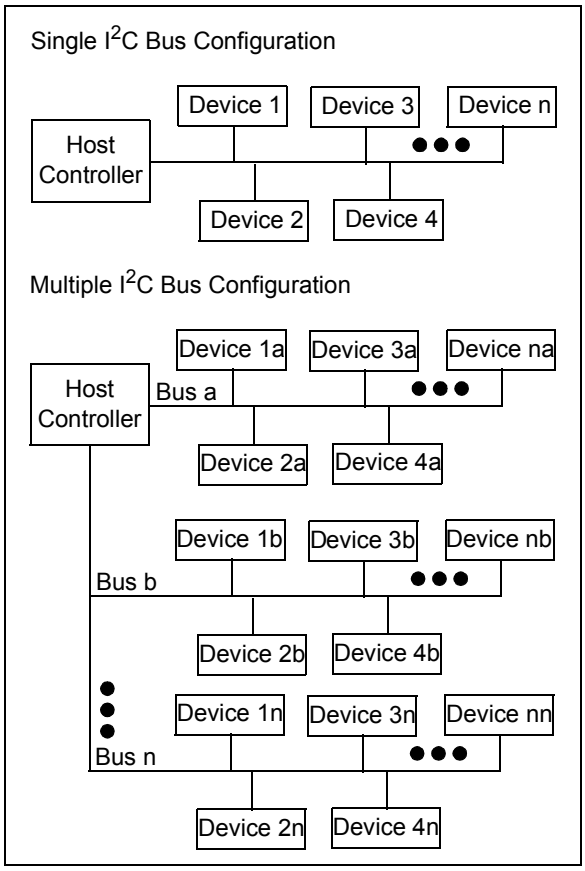



***FIGURE 8-5:*** *Typical Application $I^2C$ Bus Configurations.*

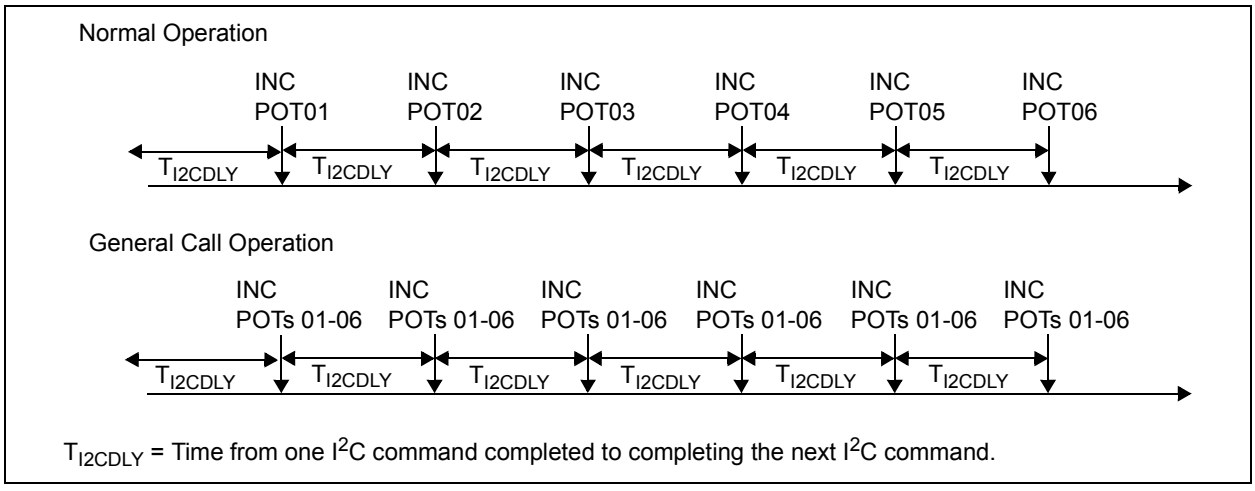



***FIGURE 8-6:*** *Example Comparison of "Normal Operation" vs. "General Call Operation" Wiper Updates.*

## 8.5 Implementing Log Steps with a Linear Digital Potentiometer

In audio volume control applications, the use of logarithmic steps is desirable since the human ear hears in a logarithmic manner. The use of a linear potentiometer can approximate a log potentiometer, but with fewer steps. An 8-bit potentiometer can achieve fourteen 3 dB log steps plus a 100% (0 dB) and a mute setting.

Figure 8-7 shows a block diagram of one of the MCP44x1 resistor networks being used to attenuate an input signal. In this case, the attenuation will be ground referenced. Terminal B can be connected to a common mode voltage, but the voltages on the A, B and Wiper terminals must not exceed the MCP44x1's $V_{DD}/V_{SS}$ voltage limits.

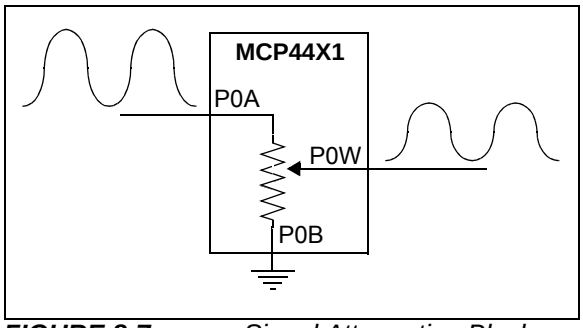



***FIGURE 8-7:*** *Signal Attenuation Block Diagram - Ground Referenced.*

Equation 8-1 shows the equation to calculate voltage dB gain ratios for the digital potentiometer, while Equation 8-2 shows the equation to calculate resistance dB gain ratios. These two equations assume that the B terminal is connected to ground.

If terminal B is not directly resistively connected to ground, then this terminal B to ground resistance ($R_{B2GND}$) must be included into the calculation. Equation 8-3 shows this equation.

**EQUATION 8-1: dB CALCULATIONS (VOLTAGE)**

$$L = 20 * \log_{10} (V_{OUT} / V_{IN})$$

| dB | $V_{OUT} / V_{IN}$ Ratio |
|---|---|
| -3 | 0.70795 |
| -2 | 0.79433 |
| -1 | 0.89125 |

**EQUATION 8-2: dB CALCULATIONS (RESISTANCE) - CASE 1**

Terminal B connected to Ground (see Figure 8-7)

$$L = 20 * \log_{10} (R_{BW} / R_{AB})$$

**EQUATION 8-3: dB CALCULATIONS (RESISTANCE) - CASE 2**

Terminal B through $R_{B2GND}$ to Ground

$$L = 20 * \log_{10} ( (R_{BW} + R_{B2GND}) / (R_{AB} + R_{B2GND}) )$$

Table 8-1 shows the codes that can be used for 8-bit digital potentiometers to implement the log attenuation. The table shows the wiper codes for -3 dB, -2 dB, and -1 dB attenuation steps. This table also shows the calculated attenuation based on the wiper code's linear step. Calculated attenuation values less than the desired attenuation are shown with red text. At lower wiper code values, the attenuation may skip a step, if this occurs the next attenuation value is colored magenta to highlight that a skip occurred. For example, in the -3 dB column the -48 dB value is highlighted since the -45 dB step could not be implemented (there are no wiper codes between 2 and 1).

**TABLE 8-1: LINEAR TO LOG ATTENUATION FOR 8-BIT DIGITAL POTENTIOMETERS**

| # of Steps | -3 dB Steps | | | -2 dB Steps | | | -1 dB Steps | | |
|---|---|---|---|---|---|---|---|---|---|
| | Desired Attenuation | Wiper Code | Calculated Attenuation (1) | Desired Attenuation | Wiper Code | Calculated Attenuation (1) | Desired Attenuation | Wiper Code | Calculated Attenuation (1) |
| 0 | 0 dB | 256 | 0 dB | 0 dB | 256 | 0 dB | 0 dB | 256 | 0 dB |
| 1 | -3 dB | 181 | -3.011 dB | -2 dB | 203 | -2.015 dB | -1 dB | 228 | -1.006 dB |
| 2 | -6 dB | 128 | -6.021 dB | -4 dB | 162 | -3.975 dB | -2 dB | 203 | -2.015 dB |
| 3 | -9dB | 91 | -8.984 dB | -6 dB | 128 | -6.021 dB | -3 dB | 181 | -3.011 dB |
| 4 | -12 dB | 64 | -12.041 dB | -8 dB | 102 | -7.993 dB | -4 dB | 162 | -3.975 dB |
| 5 | -15 dB | 46 | -14.910 dB | -10 dB | 81 | -9.995 dB | -5 dB | 144 | -4.998 dB |
| 6 | -18 dB | 32 | -18.062 dB | -12 dB | 64 | -12.041 dB | -6 dB | 128 | -6.021 dB |
| 7 | -21 dB | 23 | -20.930 dB | -14 dB | 51 | -14.013 dB | -7 dB | 114 | -7.027 dB |
| 8 | -24 dB | 16 | -24.082 dB | -16 dB | 41 | -15.909 dB | -8 dB | 102 | -7.993 dB |
| 9 | -27 dB | 11 | -27.337 dB | -18 dB | 32 | -18.062 dB | -9 dB | 91 | -8.984 dB |
| 10 | -30 dB | 8 | -30.103 dB | -20 dB | 26 | -19.865 dB | -10 dB | 81 | -9.995 dB |
| 11 | -33 dB | 6 | -32.602 dB | -22 dB | 20 | -22.144 dB | -11 dB | 72 | -11.018 dB |
| 12 | -36 dB | 4 | -36.124 dB | -24 dB | 16 | -24.082 dB | -12 dB | 64 | -12.041 dB |
| 13 | -39 dB | 3 | -38.622 dB | -26 dB | 13 | -25.886 dB | -13 dB | 57 | -13.047 dB |
| 14 | -42 dB | 2 | -42.144 dB | -28 dB | 10 | -28.165 dB | -14 dB | 51 | -14.013 dB |
| 15 | -48 dB | 1 | -48.165 dB | -30 dB | 8 | -30.103 dB | -15 dB | 46 | - 14.910 dB |
| 16 | Mute | 0 | Mute | -32 dB | 6 | -32.602 dB | -16 dB | 41 | -15.909 dB |
| 17 | | | | -34 dB | 5 | -34.185 dB | -17 dB | 36 | -17.039 dB |
| 18 | | | | -36 dB | 4 | -36.124 dB | -18 dB | 32 | -18.062 dB |
| 19 | | | | -38 dB | 3 | -38.622 dB | -19 dB | 29 | -18.917 dB |
| 20 | | | | -42 dB | 2 | -42.144 dB | -20 dB | 26 | -19.865 dB |
| 21 | | | | -48 dB | 1 | -48.165 dB | -21 dB | 23 | - 20.930 dB |
| 22 | | | | Mute | 0 | Mute | -22 dB | 20 | -22.144 dB |
| 23 | | | | | | | -23 dB | 18 | -23.059 dB |
| 24 | | | | | | | -24 dB | 16 | -24.082 dB |
| 25 | | | | | | | -25 dB | 14 | -25.242 dB |
| 26 | | | | | | | -26 dB | 13 | -25.886 dB |
| 27 | | | | | | | -27dB | 11 | -27.337 dB |
| 28 | | | | | | | -28 dB | 10 | -28.165 dB |
| 29 | | | | | | | -29 dB | 9 | -29.080 dB |
| 30 | | | | | | | -30 dB | 8 | -30.103 dB |
| 31 | | | | | | | -31 dB | 7 | -31.263 dB |
| 32 | | | | | | | -33 dB | 6 | -32.602 dB |
| 33 | | | | | | | -34 dB | 5 | -34.185 dB |
| 34 | | | | | | | -36 dB | 4 | -36.124 dB |
| 35 | | | | | | | -39 dB | 3 | -38.622 dB |
| 36 | | | | | | | -42 dB | 2 | -42.144 dB |
| 37 | | | | | | | -48 dB | 1 | -48.165 dB |
| 38 | | | | | | | Mute | 0 | Mute |

**Note 1:** Attenuation values do not include errors from Digital Potentiometer errors, such as Full Scale Error or Zero Scale Error.

## 8.6 Design Considerations

In the design of a system with the MCP44XX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

### 8.6.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-8 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin ($V_{DD}$) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, $V_{DD}$ and $V_{SS}$ should reside on the analog plane.

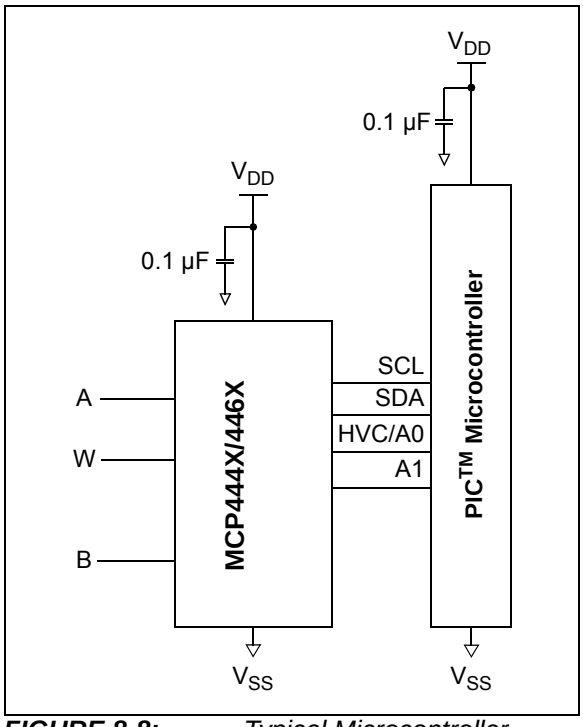



***FIGURE 8-8:*** *Typical Microcontroller Connections.*

### 8.6.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **Footprint Compatibility**
- **PCB Area Requirements**

#### 8.6.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP44XX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

#### 8.6.2.2 Footprint Compatibility

The specification of the MCP44XX pinouts was done to allow systems to be designed to easily support the use of either the dual (MCP46XX) or quad (MCP44XX) device.

Figure 8-9 shows how the dual pinout devices fit on the quad device footprint. For the Rheostat devices, the dual device is in the MSOP package, so the footprints would need to be offset from each other.

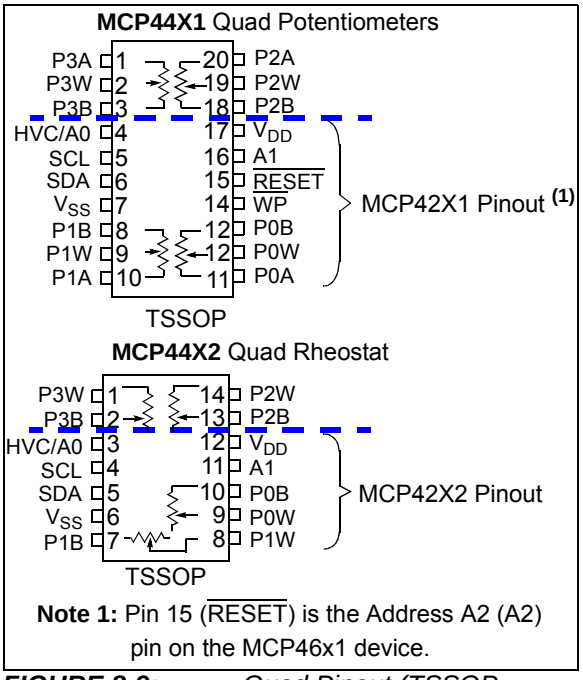



***FIGURE 8-9:*** *Quad Pinout (TSSOP Package) vs. Dual Pinout.*

Figure 8-10 shows possible layout implementations for an application to support the quad and dual options on the same PCB.

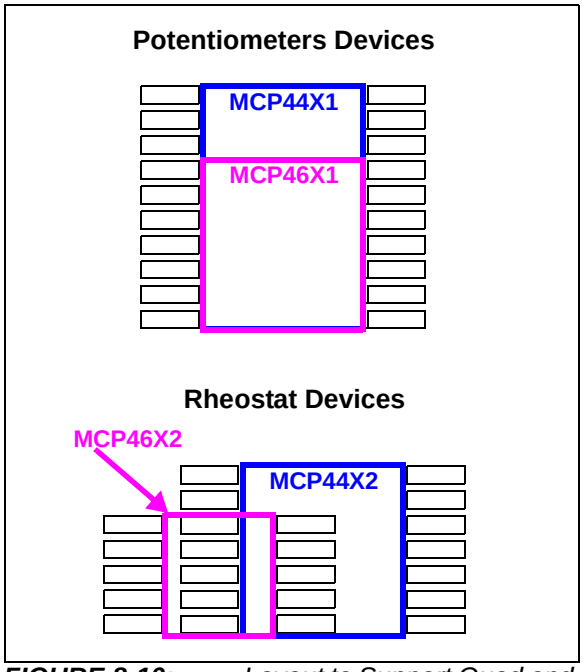



***FIGURE 8-10:*** *Layout to Support Quad and Dual Devices.*

### 8.6.2.3 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the package dimensions and area for the different package options. The table also shows the relative area factor compared to the smallest area. For space critical applications, the QFN package would be the suggested package.

**TABLE 8-2: PACKAGE FOOTPRINT (1)**

| Package | | | Package Footprint | | | |
|---|---|---|---|---|---|---|
| Pins | Type | Code | Dimensions (mm) | | Area ($mm^2$) | Relative Area |
| | | | X | Y | | |
| 14 | TSSOP | ST | 5.10 | 6.40 | 32.64 | 2.04 |
| 20 | QFN | ML | 4.00 | 4.00 | 16.00 | 1 |
| | TSSOP | ST | 6.60 | 6.40 | 42.24 | 2.64 |

**Note 1:** Does not include recommended land pattern dimensions.

### 8.6.3 RESISTOR TEMPCO

Characterization curves of the resistor temperature coefficient (Tempco) are shown in Figure 2-10, Figure 2-26, Figure 2-41, and Figure 2-56.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end to end change is $R_{AB}$ resistance.

### 8.6.4 HIGH VOLTAGE TOLERANT PINS

High Voltage support ($V_{IHH}$) on the Serial Interface pins supports two features. These are:

- In-Circuit Accommodation of split rail applications and power supply sync issues
- User configuration of the Nonvolatile EEPROM, Write Protect, and WiperLock feature

**Note:** In many applications, the High Voltage will only be present at the manufacturing stage so as to “lock” the Nonvolatile wiper value (after calibration) and the contents of the EEPROM. This ensures that since High Voltage is not present under normal operating conditions, these values can not be modified.

# 9.0 DEVELOPMENT SUPPORT

## 9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP44XX devices. The currently available tools are shown in Table 9-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

## 9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

**TABLE 9-1: DEVELOPMENT TOOLS**

| Board Name | Part # | Supported Devices |
|---|---|---|
| 20-pin TSSOP and SSOP Evaluation Board | TSSOP20EV | MCP44XX |
| MCP46XX Digital Potentiometer PICtail Plus Demo Board (1, 2) | MCP46XXDM-PTPLS | MCP46XX |
| MCP46XX Digital Potentiometer Evaluation Board (2) | MCP46XXEV | MCP46X1 |

**Note 1:** Requires a PICDEM Demo board. See the User's Guide for additional information and requirements.

**2:** Requires a PICkit Serial Analyzer. See the User's Guide for additional information and requirements.

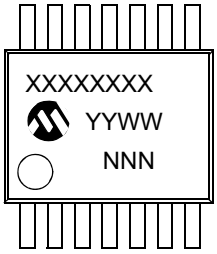
**TABLE 9-2: TECHNICAL DOCUMENTATION**

| Application Note Number | Title | Literature # |
|---|---|---|
| AN1316 | Using Digital Potentiometers for Programmable Amplifier Gain | DS01316 |
| AN1080 | Understanding Digital Potentiometers Resistor Variations | DS01080 |
| AN737 | Using Digital Potentiometers to Design Low-Pass Adjustable Filters | DS00737 |
| AN692 | Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect | DS00692 |
| AN691 | Optimizing the Digital Potentiometer in Precision Circuits | DS00691 |
| AN219 | Comparing Digital Potentiometers to Mechanical Potentiometers | DS00219 |
| — | Digital Potentiometer Design Guide | DS22017 |
| — | Signal Chain Design Guide | DS21825 |

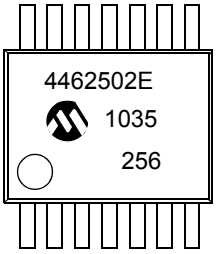
## 10.0 PACKAGING INFORMATION

### 10.1 Package Marking Information

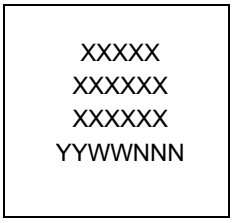
14-Lead TSSOP



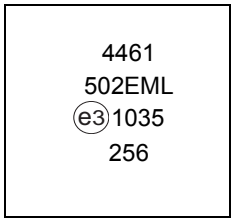

Example



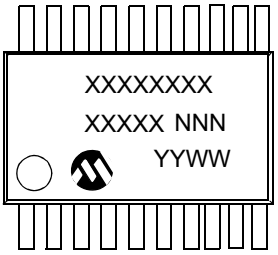

20-Lead QFN (4x4)



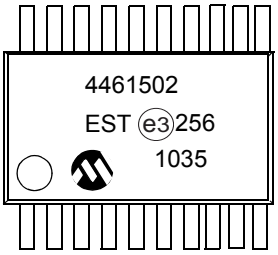

Example




20-Lead TSSOP




Example

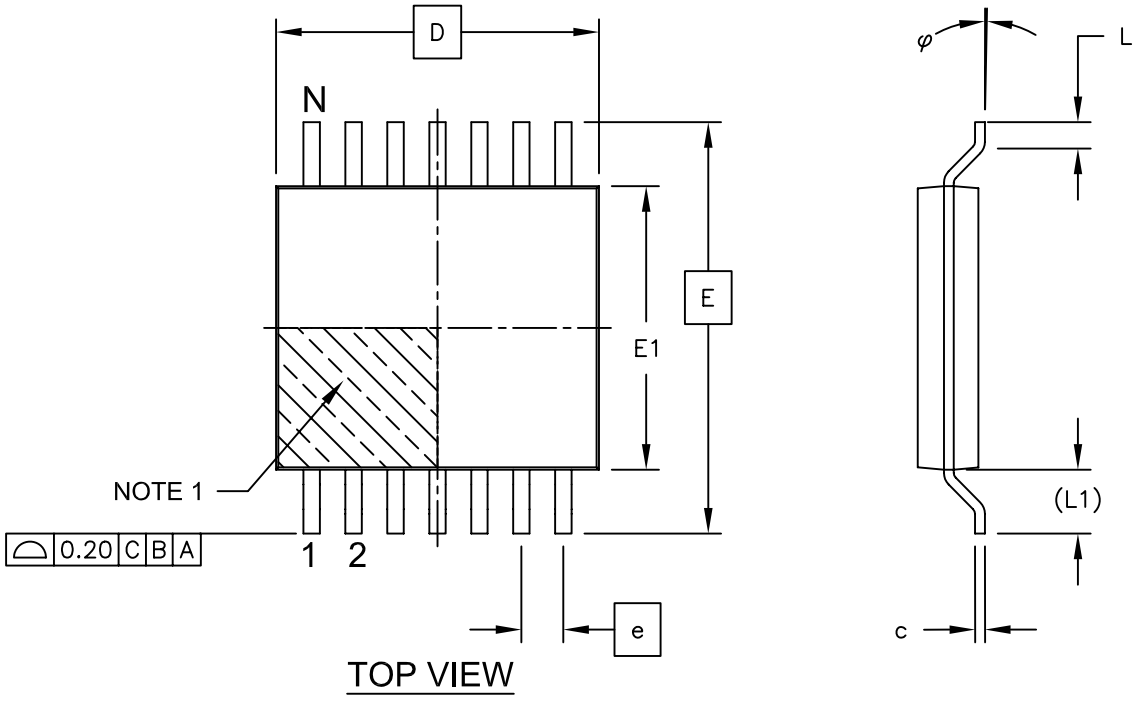


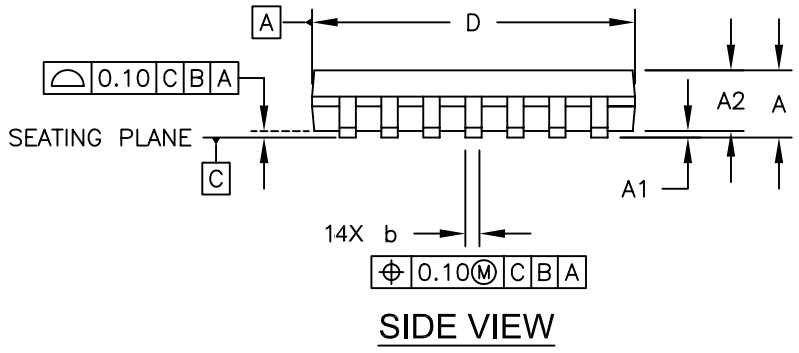

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

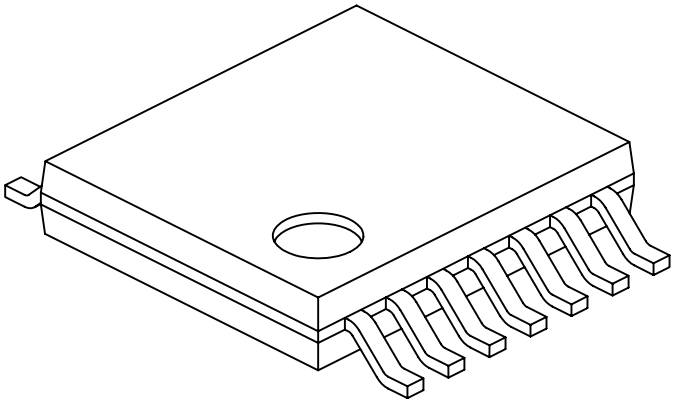



Microchip Technology Drawing C04-087C Sheet 1 of 2

## 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 4.90 | 5.00 | 5.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | (L1) | | 1.00 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

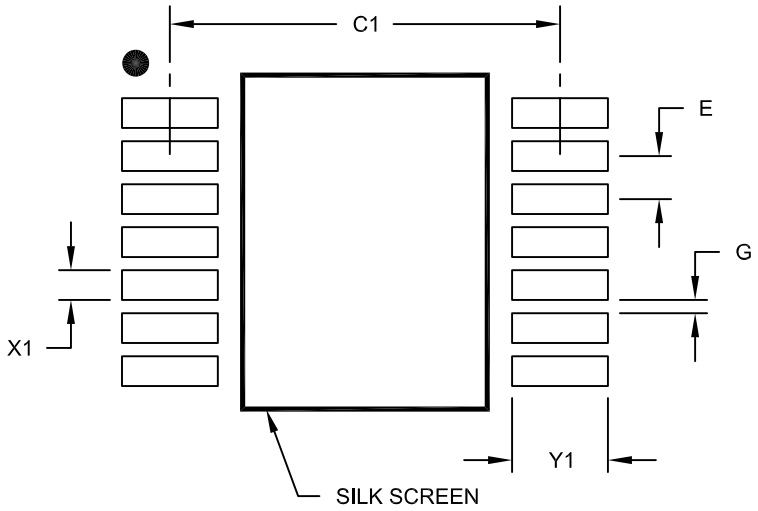
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C1 | | 5.90 | |
| Contact Pad Width (X14) | X1 | | | 0.45 |
| Contact Pad Length (X14) | Y1 | | | 1.45 |
| Distance Between Pads | G | 0.20 | | |

Notes:

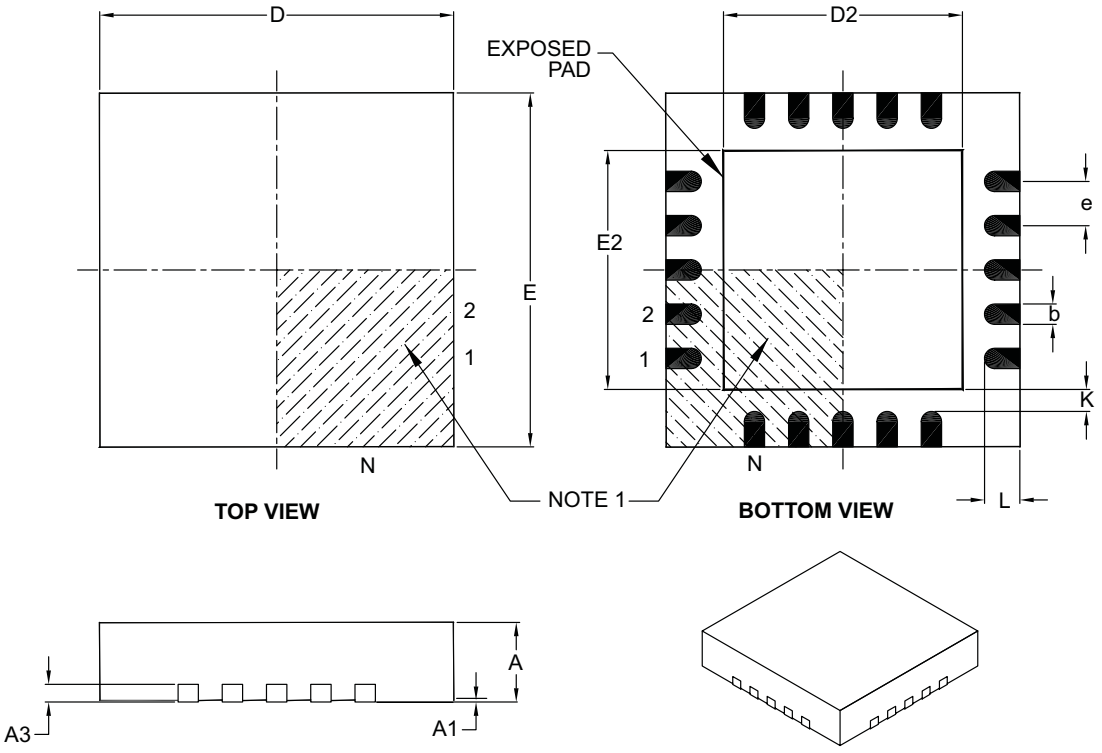
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

## 20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.60 | 2.70 | 2.80 |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Length | D2 | 2.60 | 2.70 | 2.80 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

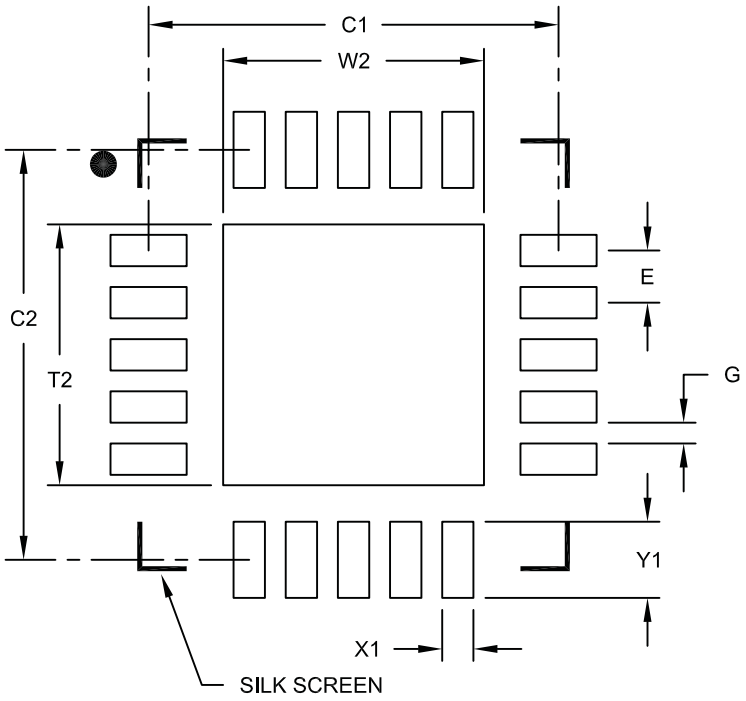
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 2.50 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 3.93 | |
| Contact Pad Spacing | C2 | | 3.93 | |
| Contact Pad Width | X1 | | | 0.30 |
| Contact Pad Length | Y1 | | | 0.73 |
| Distance Between Pads | G | 0.20 | | |

Notes:

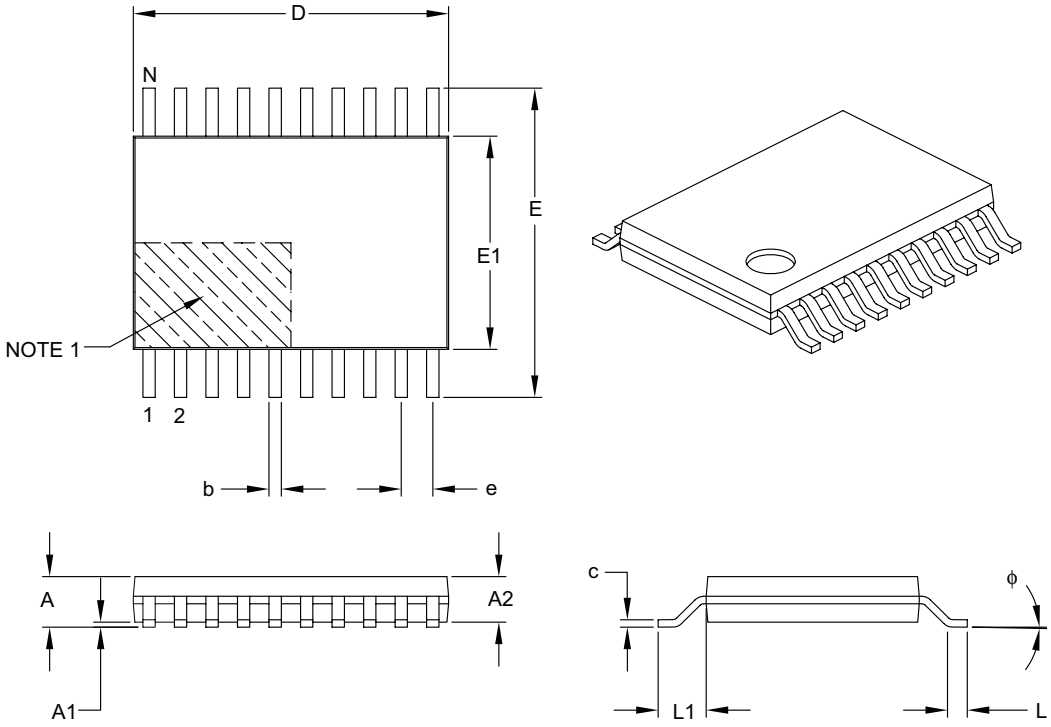
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

## 20-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 6.40 | 6.50 | 6.60 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

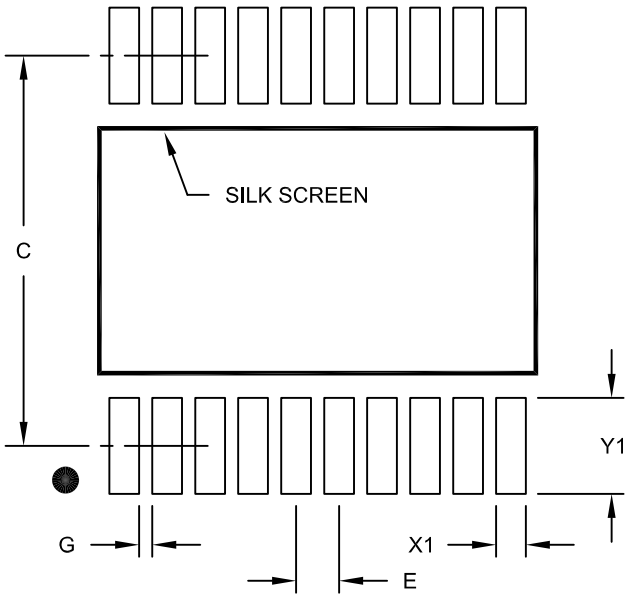
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088B

### 20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 5.90 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.45 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

# APPENDIX A: REVISION HISTORY

## Revision A (September 2010)

- Original Release of this Document.

**NOTES:**

# APPENDIX B: CHARACTERIZATION DATA ANALYSIS

Some designers may want to understand the device operational characteristics outside of the specified operating conditions of the device.

Applications where the knowledge of the resistor network characteristics could be useful include battery powered devices and applications that experience brown-out conditions.

In battery applications, the application voltage decays over time until new batteries are installed. As the voltage decays, the system will continue to operate. At some voltage level, the application will be below its specified operating voltage range. This is dependent on the individual components used in the design. It is still useful to understand the device characteristics to expect when this low-voltage range is encountered. Unlike a microcontroller, which can use an external supervisor device to force the controller into the Reset state, a digital potentiometer's resistance characteristic is not specified. But understanding the operational characteristics can be important in the design of the applications circuit for this low-voltage condition.

Other application system scenarios where understanding the low-voltage characteristics of the resistor network could be important is for system brown out conditions.

For the MCP444X/446X devices, the analog operation is specified at a minimum of 2.7V. Device testing has Terminal A connected to the device $V_{DD}$ (for the potentiometer configuration only) and Terminal B connected to $V_{SS}$.

## B.1 Low-Voltage Operation

This appendix gives an overview of CMOS semiconductor characteristics at lower voltages. This is important so that the 1.8V resistor network characterization graphs of the MCP444X/446X devices can be better understood.

For this discussion, we will use the 5 kΩ device data. This data was chosen since the variations of wiper resistance have much greater implications for devices with smaller $R_{AB}$ resistances.

Figure B-1 shows the worst case $R_{BW}$ error from the average $R_{BW}$ as a percentage, while Figure B-2 shows the $R_{BW}$ resistance versus the wiper code graph. Non-linear behavior occurs at approximately wiper code 160. This is better shown in Figure B-2, where the $R_{BW}$ resistance changes from a linear slope. This change is due to the change in the wiper resistance.

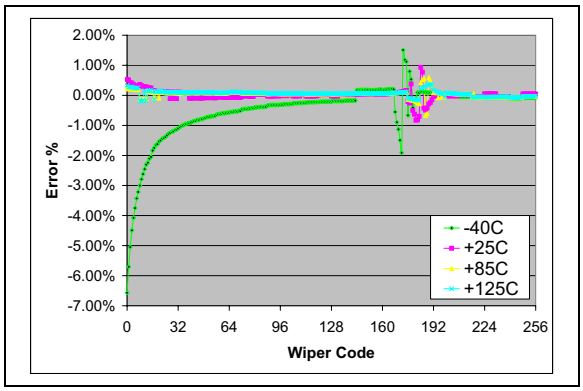



***FIGURE B-1:*** *1.8V Worst Case $R_{BW}$ Error from Average $R_{BW}$ ($R_{BW0}$-$R_{BW3}$) vs. Wiper Code and Temperature ($V_{DD}$ = 1.8V, $I_W$ = 190 µA).*

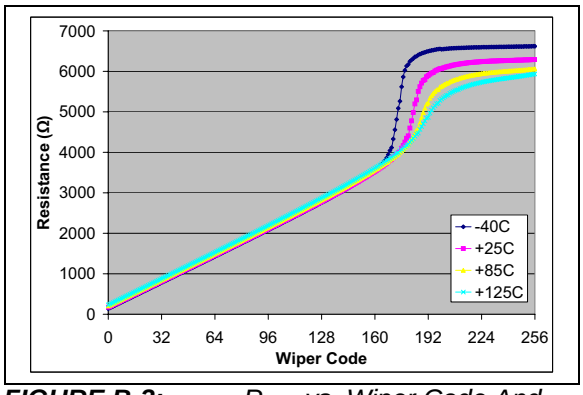



***FIGURE B-2:*** *$R_{BW}$ vs. Wiper Code And Temperature ($V_{DD}$ = 1.8V, $I_W$ = 190 µA).*

Figure B-3 and Figure B-4 show the wiper resistance for $V_{DD}$ voltages of 5.5, 3.0, 1.8 Volts. These graphs show that as the resistor ladder wiper node voltage ($V_{WCn}$) approaches the $V_{DD}/2$ voltage, the wiper resistance increases. These graphs also show the different resistance characteristics of the NMOS and PMOS transistors that make up the wiper switch. This is demonstrated by the wiper code resistance curve, which does not mirror itself around the mid-scale code (wiper code = 128).

So why are the $R_W$ graphs showing the maximum resistance at about mid-scale (wiper code = 128) and the $R_{BW}$ graphs showing the issue at code 160?

This requires understanding low-voltage transistor characteristics as well as how the data was measured.

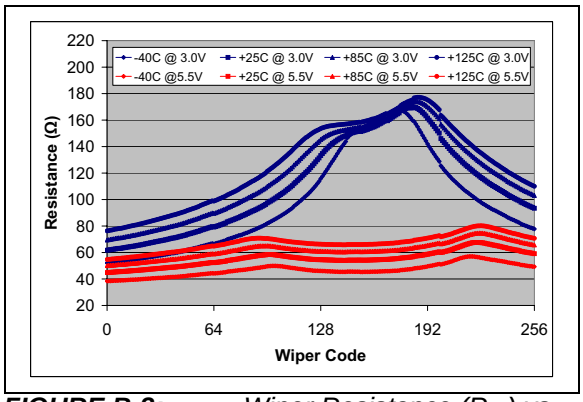



***FIGURE B-3:*** *Wiper Resistance ($R_W$) vs. Wiper Code and Temperature ($V_{DD}$ = 5.5V, $I_W$ = 900 µA; $V_{DD}$ = 3.0V, $I_W$ = 480 µA).*

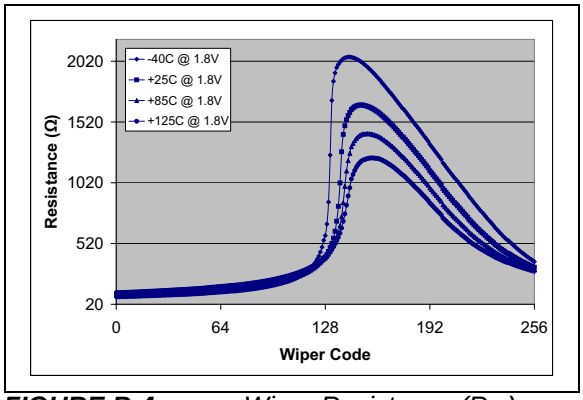



***FIGURE B-4:*** *Wiper Resistance ($R_W$) vs. Wiper Code and Temperature ($V_{DD}$ = 1.8V, $I_W$ = 260 µA).*

The method in which the data was collected is important to understand. Figure B-5 shows the technique that was used to measure the $R_{BW}$ and $R_W$ resistance. In this technique, Terminal A is floating and Terminal B is connected to ground. A fixed current is then forced into the wiper ($I_W$) and the corresponding wiper voltage ($V_W$) is measured. Forcing a known current through $R_{BW}$ ($I_W$) and then measuring the voltage difference between the wiper ($V_W$) and Terminal A ($V_A$), the wiper resistance ($R_W$) can be calculated, see Figure B-5. Changes in $I_W$ current will change the wiper voltage ($V_W$). This may affect the device's wiper resistance ($R_W$).

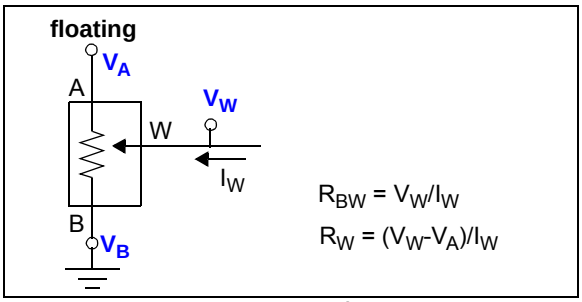
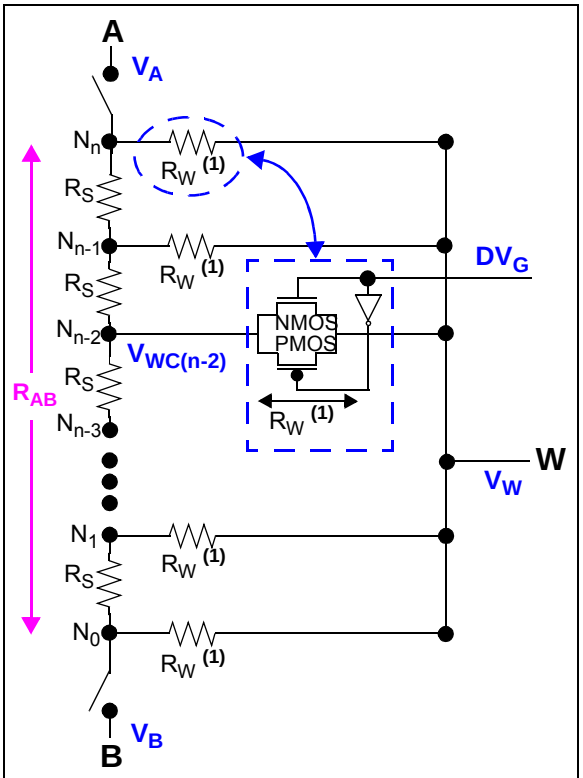



***FIGURE B-5:*** *$R_{BW}$ and $R_W$ Measurement.*

Figure B-6 shows a block diagram of the resistor network where the $R_{AB}$ resistor is a series of 256 $R_S$ resistors. These resistors are polysilicon devices. Each wiper switch is an analog switch made up of an NMOS and PMOS transistor. A more detailed figure of the wiper switch is shown in Figure B-7. The wiper resistance is influenced by the voltage on the wiper switches nodes ($V_G$, $V_W$ and $V_{WCn}$). Temperature also influences the characteristics of the wiper switch, see Figure B-4.

The NMOS transistor and PMOS transistor have different characteristics. These characteristics, as well as the wiper switch node voltages, determine the $R_W$ resistance at each wiper code. The variation of each wiper switch's characteristics in the resistor network is greater then the variation of the $R_S$ resistors.

The voltage on the resistor network node ($V_{WCn}$) is dependent upon the wiper code selected and the voltages applied to $V_A$, $V_B$ and $V_W$. The wiper switch $V_G$ voltage to $V_W$ or $V_{WCn}$ voltage determines how strongly the transistor is turned on. When the transistor is weakly turned on, the wiper resistance $R_W$ will be high. When the transistor is strongly turned on, the wiper resistance ($R_W$) will be in the typical range.

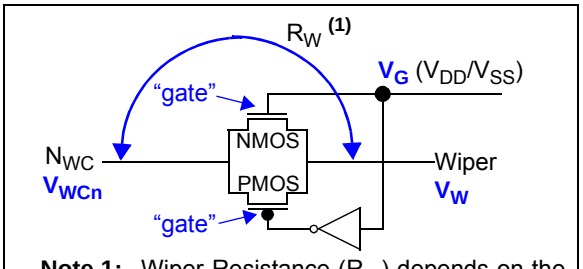



**Note 1:** The wiper resistance is dependent on several factors including, wiper code, device $V_{DD}$, Terminal voltages (on A, B and W), and temperature.

***FIGURE B-6:*** *Resistor Network Block Diagram.*

The characteristics of the wiper are determined by the characteristics of the wiper switch at each of the resistor networks tap points. Figure B-7 shows an example of a wiper switch. As the device operational voltage becomes lower, the characteristics of the wiper switch change due to a lower voltage on the $V_G$ signal.

Figure B-7 shows an implementation of a wiper switch. When the transistor is turned off, the switch resistance is in the Giga Ωs. When the transistor is turned on, the switch resistance is dependent on the $V_G$, $V_W$ and $V_{WCn}$ voltages. This resistance is referred to as $R_W$.




**Note 1:** Wiper Resistance ($R_W$) depends on the voltages at the wiper switch nodes ($V_G$, $V_W$ and $V_{WCn}$).

***FIGURE B-7:*** *Wiper Switch.*

So looking at the wiper voltage ($V_W$) for the 3.0V and 1.8V data gives the graphs in Figure B-8 and Figure B-9. In the 1.8V graph, as the $V_W$ approaches 0.8V, the voltage increases nonlinearly. Since V = I * R, and the current ($I_W$) is constant, it means that the device resistance increased nonlinearly at around wiper code 160.

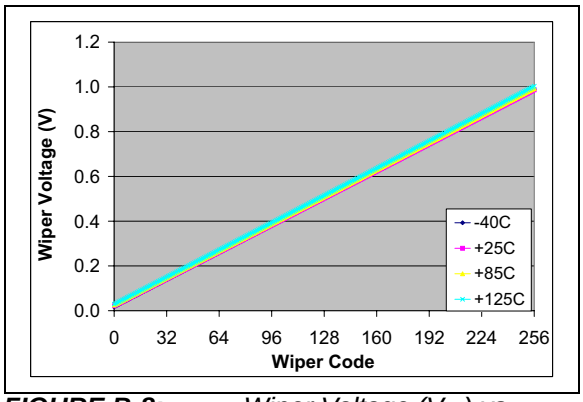



***FIGURE B-8:*** *Wiper Voltage ($V_W$) vs. Wiper Code ($V_{DD}$ = 3.0V, $I_W$ = 190 µA).*

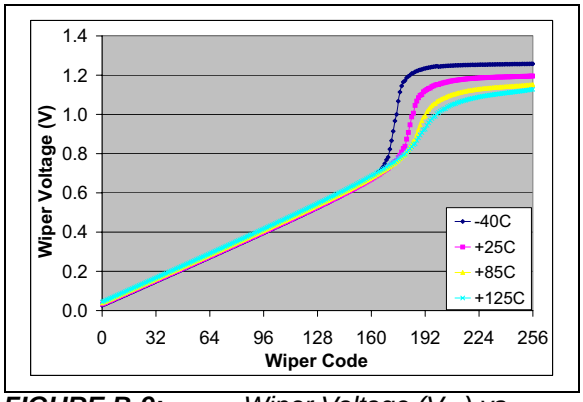



***FIGURE B-9:*** *Wiper Voltage ($V_W$) vs. Wiper Code ($V_{DD}$ = 1.8V, $I_W$ = 190 µA).*

Using the simulation models of the NMOS and PMOS devices for the MCP44XX analog switch (Figure B-10), we plot the device resistance when the devices are turned on. Figure B-11 and Figure B-12 show the resistances of the NMOS and PMOS devices as the $V_{IN}$ voltage is increased. The wiper resistance ($R_W$) is simply the parallel resistance on the NMOS and PMOS devices ($R_W = R_{NMOS} \parallel R_{PMOS}$). Below the threshold voltage for the NMOS ad PMOS devices, the resistance becomes very large (Gigaohms). In the transistors active region, the resistance is much lower. For these graphs, the resistances are on different scales. Figure B-13 and Figure B-14 only plot the NMOS and PMOS device resistance for their active region and the resulting wiper resistance. For these graphs, all resistances are on the same scale.

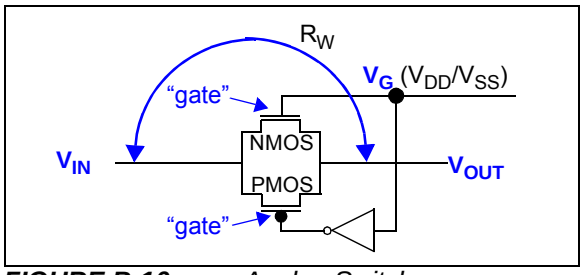



***FIGURE B-10:*** *Analog Switch.*

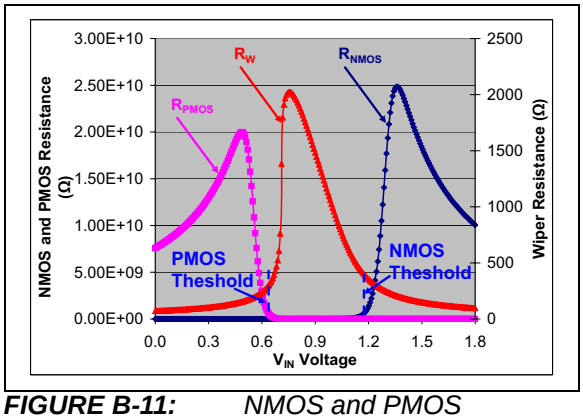



***FIGURE B-11:*** *NMOS and PMOS Transistor Resistance ($R_{NMOS}$, $R_{PMOS}$) and Wiper Resistance ($R_W$) VS. $V_{IN}$ ($V_{DD}$ = 3.0V).*

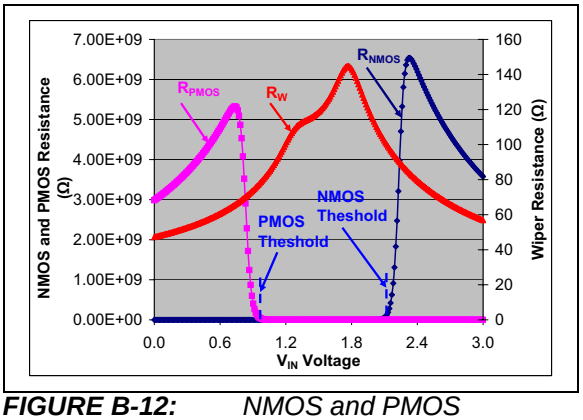



***FIGURE B-12:*** *NMOS and PMOS Transistor Resistance ($R_{NMOS}$, $R_{PMOS}$) and Wiper Resistance ($R_W$) VS. $V_{IN}$ ($V_{DD}$ = 1.8V).*

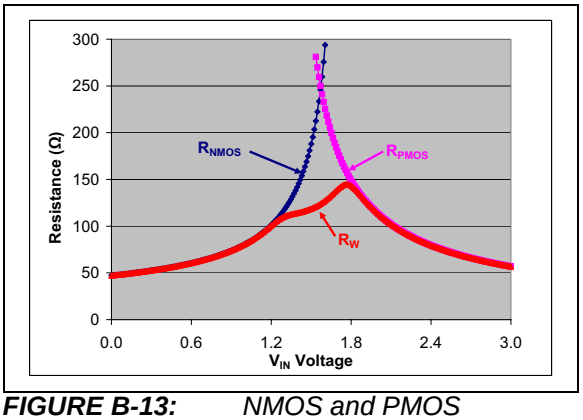



***FIGURE B-13:*** *NMOS and PMOS Transistor Resistance ($R_{NMOS}$, $R_{PMOS}$) and Wiper Resistance ($R_W$) VS. $V_{IN}$ ($V_{DD}$ = 3.0V).*

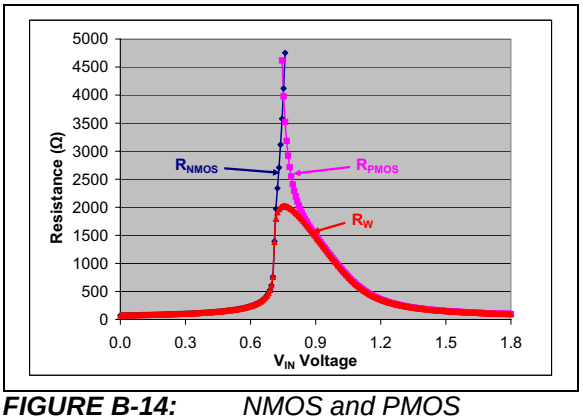



***FIGURE B-14:*** *NMOS and PMOS Transistor Resistance ($R_{NMOS}$, $R_{PMOS}$) and Wiper Resistance ($R_W$) VS. $V_{IN}$ ($V_{DD}$ = 1.8V).*

## B.2 Optimizing Circuit Design for Low-Voltage Characteristics

The low-voltage nonlinear characteristics can be minimized by application design. The section will show two application circuits that can be used to control a programmable reference voltage ($V_{OUT}$).

Minimizing the low-voltage nonlinear characteristics is done by keeping the voltages on the wiper switch nodes at a voltage where either the NMOS or PMOS transistor is turned on.

An example of this is if we are using a digital potentiometer for a voltage reference ($V_{OUT}$). Let's say that we want $V_{OUT}$ to range from 0.5 * $V_{DD}$ to 0.6 * $V_{DD}$.

In example implementation #1 (Figure B-15), we window the digital potentiometer using resistors R1 and R2. When the wiper code is at full scale, the $V_{OUT}$ voltage will be ≥ 0.6 * $V_{DD}$, and when the wiper code is at zero scale the $V_{OUT}$ voltage will be ≤ 0.5 * $V_{DD}$. Remember that the digital potentiometers $R_{AB}$ variation must be included. Table B-1 shows that the $V_{OUT}$ voltage can be selected to be between 0.455 * $V_{DD}$ and 0.727 * $V_{DD}$, which includes the desired range. With respect to the voltages on the resistor network node, at 1.8V the $V_A$ voltage would range from 1.29V to 1.31V while the $V_B$ voltage would range from 0.82V to 0.86V. These voltages cause the wiper resistance to be in the nonlinear region (see Figure B-12). In Potentiometer mode, the variation of the wiper resistance is typically not an issue, as shown by the INL/DNL graph (Figure 2-7).

In example implementation #2 (Figure B-16) we use the digital potentiometer in Rheostat mode. The resistor ladder uses resistors R1 and R2 with $R_{BW}$ at the bottom of the ladder. When the wiper code is at full scale, the $V_{OUT}$ voltage will be ≥ 0.6 * $V_{DD}$ and when the wiper code is at full scale the $V_{OUT}$ voltage will be ≤ 0.5 * $V_{DD}$. Remember that the digital potentiometers $R_{AB}$ variation must be included. Table B-2 shows that the $V_{OUT}$ voltage can be selected to be between 0.50 * $V_{DD}$ and 0.687 * $V_{DD}$, which includes the desired range. With respect to the voltages on the resistor network node, at 1.8V the $V_W$ voltage would range from 0.29V to 0.38V. These voltages cause the wiper resistance to be in the linear region (see Figure B-12).

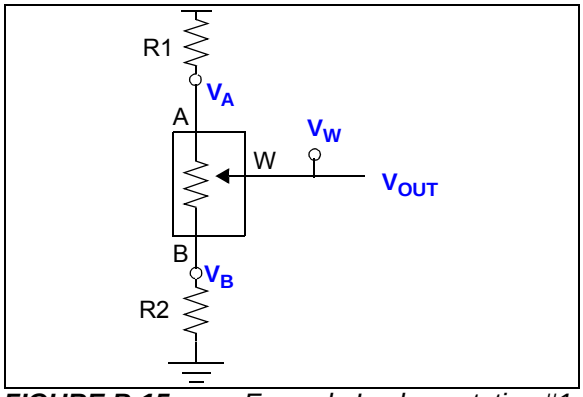



***FIGURE B-15:*** *Example Implementation #1.*

**TABLE B-1: EXAMPLE #1 VOLTAGE CALCULATIONS**

| | Variation | | |
|---|---|---|---|
| | **Min** | **Typ** | **Max** |
| R1 | 12,000 | 12,000 | 12,000 |
| R2 | 20,000 | 20,000 | 20,000 |
| $R_{AB}$ | 8,000 | 10,000 | 12,000 |
| $V_{OUT}$ (@ FS) | 0.714 $V_{DD}$ | 0.70 $V_{DD}$ | 0.727 $V_{DD}$ |
| $V_{OUT}$ (@ ZS) | 0.476 $V_{DD}$ | 0.50 $V_{DD}$ | 0.455 $V_{DD}$ |
| $V_A$ | 0.714 $V_{DD}$ | 0.70 $V_{DD}$ | 0.727 $V_{DD}$ |
| $V_B$ | 0.476 $V_{DD}$ | 0.50 $V_{DD}$ | 0.455 $V_{DD}$ |

**Legend:** FS – Full Scale, ZS – Zero Scale

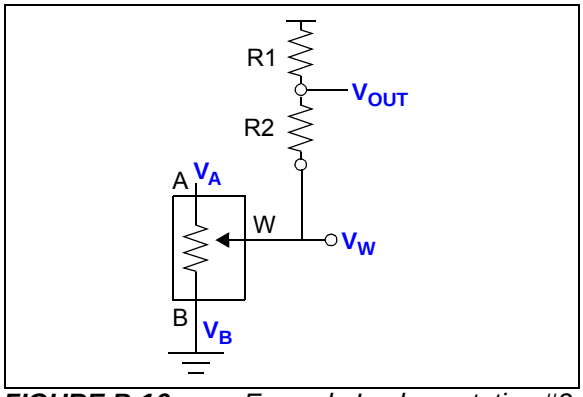



***FIGURE B-16:*** *Example Implementation #2.*

**TABLE B-2: EXAMPLE #2 VOLTAGE CALCULATIONS**

| | Variation | | |
|---|---|---|---|
| | **Min** | **Typ** | **Max** |
| R1 | 10,000 | 10,000 | 10,000 |
| R2 | 10,000 | 10,000 | 10,000 |
| $R_{BW}$ (max) | 8,000 | 10,000 | 12,000 |
| $V_{OUT}$ (@ FS) | 0.667 $V_{DD}$ | 0.643 $V_{DD}$ | 0.687 $V_{DD}$ |
| $V_{OUT}$(@ ZS) | 0.50 $V_{DD}$ | 0.50 $V_{DD}$ | 0.50 $V_{DD}$ |
| $V_W$ (@ FS) | 0.333 $V_{DD}$ | 0.286 $V_{DD}$ | 0.375 $V_{DD}$ |
| $V_W$ (@ ZS) | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |

**Legend:** FS – Full Scale, ZS – Zero Scale

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | -XXX | X | /XX |
|---|---|---|---|
| Device | Resistance Version | Temperature Range | Package |

| | | |
|---|---|---|
| Device | MCP4441: | Quad Nonvolatile 7-bit Potentiometer |
| | MCP4441T: | Quad Nonvolatile 7-bit Potentiometer (Tape and Reel) |
| | MCP4442: | Quad Nonvolatile 7-bit Rheostat |
| | MCP4442T: | Quad Nonvolatile 7-bit Rheostat (Tape and Reel) |
| | MCP4461: | Quad Nonvolatile 8-bit Potentiometer |
| | MCP4461T: | Quad Nonvolatile 8-bit Potentiometer (Tape and Reel) |
| | MCP4462: | Quad Nonvolatile 8-bit Rheostat |
| | MCP4462T: | Quad Nonvolatile 8-bit Rheostat (Tape and Reel) |
| Resistance Version: | 502 = 5 kΩ | |
| | 103 = 10 kΩ | |
| | 503 = 50 kΩ | |
| | 104 = 100 kΩ | |
| Temperature Range | E = -40°C to +125°C (Extended) | |
| Package | ST = Plastic Thin Shrink Small Outline (TSSOP), 14/20-lead | |
| | ML = Plastic Quad Flat No-lead (4x4 QFN), 20-lead | |

**Examples:**

| | | |
|---|---|---|
| a) | MCP4441-502E/XX: | 5 kΩ, 20-LD Device |
| b) | MCP4441T-502E/XX: | T/R, 5 kΩ, 20-LD Device |
| c) | MCP4441-103E/XX: | 10 kΩ, 20-LD Device |
| d) | MCP4441T-103E/XX: | T/R, 10 kΩ, 20-LD Device |
| e) | MCP4441-503E/XX: | 50 kΩ, 20-LD Device |
| f) | MCP4441T-503E/XX: | T/R, 50 kΩ, 20-LD Device |
| g) | MCP4441-104E/XX: | 100 kΩ, 20-LD Device |
| h) | MCP4441T-104E/XX: | T/R, 100 kΩ, 20-LD Device |
| a) | MCP4442-502E/XX: | 5 kΩ, 14-LD Device |
| b) | MCP4442T-502E/XX: | T/R, 5 kΩ, 14-LD Device |
| c) | MCP4442-103E/XX: | 10 kΩ, 14-LD Device |
| d) | MCP4442T-103E/XX: | T/R, 10 kΩ, 14-LD Device |
| e) | MCP4442-503E/XX: | 50 kΩ, 8LD Device |
| f) | MCP4442T-503E/XX: | T/R, 50 kΩ, 14-LD Device |
| g) | MCP4442-104E/XX: | 100 kΩ, 14-LD Device |
| h) | MCP4442T-104E/XX: | T/R, 100 kΩ, 14-LD Device |
| a) | MCP4461-502E/XX: | 5 kΩ, 20-LD Device |
| b) | MCP4461T-502E/XX: | T/R, 5 kΩ, 20-LD Device |
| c) | MCP4461-103E/XX: | 10 kΩ, 20-LD Device |
| d) | MCP4461T-103E/XX: | T/R, 10 kΩ, 20-LD Device |
| e) | MCP4461-503E/XX: | 50 kΩ, 20-LD Device |
| f) | MCP4461T-503E/XX: | T/R, 50 kΩ, 20-LD Device |
| g) | MCP4461-104E/XX: | 100 kΩ, 20-LD Device |
| h) | MCP4461T-104E/XX: | T/R, 100 kΩ, 20-LD Device |
| a) | MCP4462-502E/XX: | 5 kΩ, 14-LD Device |
| b) | MCP4462T-502E/XX: | T/R, 5 kΩ, 14-LD Device |
| c) | MCP4462-103E/XX: | 10 kΩ, 14-LD Device |
| d) | MCP4462T-103E/XX: | T/R, 10 kΩ, 14-LD Device |
| e) | MCP4462-503E/XX: | 50 kΩ, 14-LD Device |
| f) | MCP4462T-503E/XX: | T/R, 50 kΩ, 14-LD Device |
| g) | MCP4462-104E/XX: | 100 kΩ, 14-LD Device |
| h) | MCP4462T-104E/XX: | T/R, 100 kΩ, 14-LD Device |

XX = ST for 14/20-lead TSSOP
= ML for 20-lead QFN

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



**Trademarks**



Printed on recycled paper.

ISBN: 978-1-60932-533-6

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

# Worldwide Sales and Service

## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Cleveland**
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

**Kokomo**
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

**Santa Clara**
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

**Toronto**
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

## ASIA/PACIFIC

**Asia Pacific Office**
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

**Australia - Sydney**
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

**China - Beijing**
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

**China - Chengdu**
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

**China - Chongqing**
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

**China - Hong Kong SAR**
Tel: 852-2401-1200
Fax: 852-2401-3431

**China - Nanjing**
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

**China - Qingdao**
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

**China - Shanghai**
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

**China - Shenyang**
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

**China - Shenzhen**
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

**China - Wuhan**
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

**China - Xian**
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

**China - Xiamen**
Tel: 86-592-2388138
Fax: 86-592-2388130

**China - Zhuhai**
Tel: 86-756-3210040
Fax: 86-756-3210049

## ASIA/PACIFIC

**India - Bangalore**
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

**India - New Delhi**
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

**India - Pune**
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

**Japan - Yokohama**
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

**Korea - Daegu**
Tel: 82-53-744-4301
Fax: 82-53-744-4302

**Korea - Seoul**
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

**Malaysia - Kuala Lumpur**
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

**Malaysia - Penang**
Tel: 60-4-227-8870
Fax: 60-4-227-4068

**Philippines - Manila**
Tel: 63-2-634-9065
Fax: 63-2-634-9069

**Singapore**
Tel: 65-6334-8870
Fax: 65-6334-8850

**Taiwan - Hsin Chu**
Tel: 886-3-6578-300
Fax: 886-3-6578-370

**Taiwan - Kaohsiung**
Tel: 886-7-213-7830
Fax: 886-7-330-9305

**Taiwan - Taipei**
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

**Thailand - Bangkok**
Tel: 66-2-694-1351
Fax: 66-2-694-1350

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4450-2828
Fax: 45-4485-2829

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**UK - Wokingham**
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/04/10