MCP60711/1U/3

10 MHz Precision Op Amps

Features

- Gain Bandwidth Product: 10 MHz (typical)
- Slew Rate: 15 V/µs (typical at V_{DD} = 5.5V)
- THD: -115 dBc (typical) at 1 kHz and 2 V_{P-P}
- Input Offset Voltage: ±105 µV (maximum, V_{CM} = 0.1V)
- Rail-to-Rail: I/O
- Power Supply: 2.2V to 5.5V
  - Single or Dual (Split) Supplies
  - Quiescent Current: 720 µA/chan (typical)
  - Shutdown pins for some packages
- Enhanced EMI Protection:
  - EMIRR: 81 dB at 2.4 GHz (typical)
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Audio
- Test and Measurement
- Communications
- Medical
- Active Filters
- Trans-impedance Amplifiers
- Current Sensing
- ADC Driver
- DAC Buffer

Design Aids

- Analog Demonstration and Evaluation Boards
- Application Notes

Description

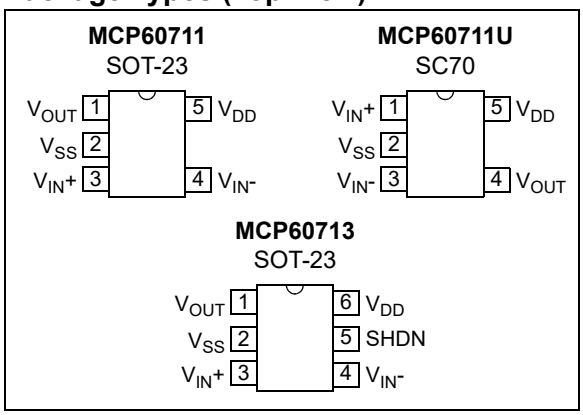
The MCP60711/1U/3 op amps operate on a power supply voltage between 2.2V and 5.5V, and over the E-Temp temperature range (-40°C to +125°C). The input offset voltage is trimmed at 25°C and V_{DD} = 3.5V.

Single op amps are offered in 5L SC70, 5L SOT-23, and 6L SOT-23 (with SHDN pin) packages.

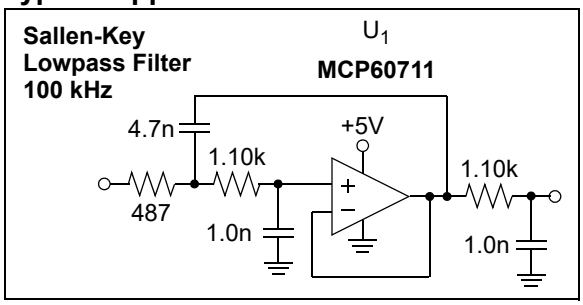
Related Op Amps

- MCP6051/2/4: 385 kHz, Low Input Offset Voltage
- MCP6061/2/4: 730 kHz, Low Input Offset Voltage
- MCP6071/2/4: 1.2 MHz, Low Input Offset Voltage

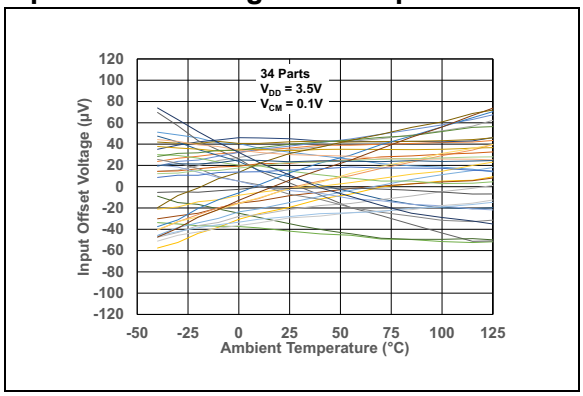
Package Types (Top View)



Typical Application Circuit



Input Offset Voltage vs. Temperature



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ ..... -0.3V to +6.0V
Current at Input Pins ..... ±2 mA
Inputs and Outputs ..... $V_{SS} – 0.5V$ to $V_{DD} + 0.5V$
Input Difference Voltage ($V_{IN}+ – V_{IN}-$) ..... (intermittent) $±V_{DD}$
..... (continuous) ±0.5V
Output Short Circuit Current ..... ±60 mA
Current at Output and Supply Pins ..... (continuous) ±30 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C
ESD Protection (HBM, CDM) ..... ≥ 4 kV, 2 kV

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 5 kΩ to V_L and C_L = 30 pF; see Figure 1-6.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset Voltage						
Input Offset Voltage	V_{OS}	-105	±50	105	µV	V_{CM} = 0.1V
		-150	±75	150		$V_{CM} = V_{DD} – 0.5V$
Input Offset Voltage Aging	ΔV_{OS}	—	±80	—		Dynamic Burn-*in*, V_{CM} = 0.1V, 1008 hr, 125°C, V_{DD} = 5.5V, $\lvert V_{IN}+ – V_{IN}-\rvert$ < 60 mV
		—	±40	—		Dynamic Burn-*in*, V_{CM} = 0.1V, 1008 hr, 125°C, V_{DD} = 5.5V, $\lvert V_{IN}+ – V_{IN}-\rvert$ < 60 mV
Input Offset Drift with Temperature	TC_1	—	±0.4	—	µV/°C	T_A = -40°C to +125°C, V_{CM} = 0.1V
		—	±0.45	—		T_A = -40°C to +125°C, $V_{CM} = V_{DD} – 0.5V$
Input Offset Quadratic Temp. Co.	TC_2	—	±1.5	—	nV/°C^2	T_A = -40°C to +125°C, V_{CM} = 0.1V
		—	±2.1	—		T_A = -40°C to +125°C, $V_{CM} = V_{DD} – 0.5V$
Power Supply Rejection Ratio	PSRR	80	95	—	dB	V_{DD} = 2.2V to 5.5V, V_{CM} = 0.1V
		76	92	—		V_{DD} = 2.2V to 5.5V, $V_{CM} = V_{DD} – 0.5V$
Input Current and Impedance						
Input Bias Current	I_B	-20	±0.4	20	pA	V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= 25°C
		—	40	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +85°C
		—	420	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +125°C
Input Offset Current	I_{OS}	-20	±1	20		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +25°C
		—	±10	—		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +85°C
		-400	±180	400		V_{DD} = 5.5V, V_{CM} = 2.75V, T_A= +125°C
Common Mode Input Impedance	Z_{CM}	—	$10^{11}\|\|6.5$	—	Ω||pF	
Differential Mode Input Impedance	Z_{DM}	—	$10^{11}\|\|2.4$	—		

Note 1: V_{CML}, V_{CMH}, V_{OL} and V_{OH} change with temperature; see Figure 2-19 and Figure 2-21.
2: The POR must be on for the time t_{PON_TR} before SHDN function is enabled; it is disabled when the POR is off.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF; see Figure 1-6.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Common Mode Voltage						
Common Mode Voltage Range (Note 1)	V_{CML}	—	-0.4	-0.3	V	T_A = 25°C
	V_{CMH}	V_{DD} + 0.3	V_{DD} + 0.4	—		T_A = 25°C
Common Mode Rejection Ratio	CMRR	80	95	—	dB	V_{CM} = -0.3V to V_{DD} + 0.3V
Open-Loop Gain						
DC Open-Loop Gain	A_{OL}	97	112	—	µV/V	V_{OUT} = 0.2V to V_{DD} – 0.2V, V_{CM} = 0.1V
		97	112	—		V_{OUT} = 0.2V to V_{DD} – 0.2V, V_{CM} = V_{DD} – 0.5V
Output						
Output Voltage Swing – Low (Note 1)	$V_{OL} – V_{SS}$	—	5	—	mV	Input Overdrive = -0.5V, V_{DD} = 2.2V
		—	8	—		Input Overdrive = -0.5V, V_{DD} = 5.5V
		10	45	200		Input Overdrive = -0.5V, V_{DD} = 5.5V, R_L = 500Ω
Output Voltage Swing – High (Note 1)	$V_{OH} – V_{DD}$	—	-4	—		Input Overdrive = +0.5V, V_{DD} = 2.2V
		—	-7	—		Input Overdrive = +0.5V, V_{DD} = 5.5V
		-180	-40	-10		Input Overdrive = +0.5V, V_{DD} = 5.5V, R_L = 500Ω
Output Short Circuit Current	I_{SCP}	—	12	—	mA	V_{DD} = 2.2V
		—	47	—		V_{DD} = 5.5V
	I_{SCM}	—	-18	—		V_{DD} = 2.2V
		—	-57	—		V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.2	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.65	0.72	0.79	mA	I_O = 0, t > t_{PON_TR}
	I_{Q_TR}	—	1.5	—		I_O = 0, t_{PON} < t < t_{PON_TR} (power-on current)
POR Trip Voltages	V_{PRHL}	1.45	1.61	—	V	POR turns off (V_{DD} ↓), V_L = 0V, not tested in production
	V_{PRLH}	—	1.76	1.95		POR turns on (V_{DD} ↑), V_L = 0V, not tested in production
POR Trip Voltage Drift with Temperature	$\Delta V_{PRHL}/\Delta T_A$	—	0.90	—	mV/°C	
	$\Delta V_{PRLH}/\Delta T_A$	—	0.85	—		
Shutdown Logic Threshold, Low	V_{SDL}	0	—	0.55	V	At SHDN pin
Shutdown Logic Threshold, High	V_{SDH}	1.3	—	V_{DD}		
Shutdown Logic Hysteresis	V_{SDHYST}	—	0.12	—		
Shutdown Current per Amplifier	I_{SS_SD}	-15	-4	-1.5	µA	I_O = 0, t > t_{PON_TR}, SHDN high
Shutdown Pull-Down Resistor	R_{SD}	—	2	—	MΩ	At the SHDN pin

Note 1: V_{CML}, V_{CMH}, V_{OL} and V_{OH} change with temperature; see Figure 2-19 and Figure 2-21.

2: The POR must be on for the time t_{PON_TR} before SHDN function is enabled; it is disabled when the POR is off.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF; see Figure 1-7.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain-Bandwidth Product	GBWP	—	10	—	MHz	V_{OUT} = 0.1 V_{P-P}, G_N > +2
Full Power Bandwidth	FPBW	—	1.1	—		V_{DD} = 5V, V_{CM} = 2.5V, V_{OUT} = 4.6 V_{P-P}, Gain = -1 V/V
Phase Margin	PM	—	65	—	°	G = +1, V_{OUT} = 0.1 V_{P-P}
		—	45	—		G = +1, V_{OUT} = 0.1 V_{P-P}, C_L = 100 pF
Step Response						
Settling Time	t_{settle}	—	110	—	ns	G = +1, V_{CM} = 0.5V, +0.1V step and 1% settling
		—	110	—		G = +1, V_{CM} = V_{DD} – 0.5V, +0.1V step and 1% settling
Slew Rate	SR	—	4.1	—	V/µs	G = +1, V_{DD} = 2.2V
		—	15	—		G = +1, V_{DD} = 5.5V
Output Overdrive Recovery Time (Note 1)	t_{ODR}	—	0.9	—	µs	G = -10, V_{DD} = 3.5V, V_{CM} = V_{DD}/2, ±0.5V output overdrive (V_{IN} = V_{CM} ± 0.225V to V_{CM}), 90% of V_{OUT} change
Noise						
Input Noise Voltage	E_{ni}	—	3.1	—	μV_{P-P}	f = 0.1 Hz to 10 Hz, V_{CM} = 0.1V
		—	5.9	—		f = 0.1 Hz to 10 Hz, V_{CM} = V_{DD} – 0.5V
Input Noise Voltage Density	e_{ni}	—	5.4	—	nV/√Hz	f = 100 kHz, V_{CM} = 0.1V
		—	6.1	—		f = 100 kHz, V_{CM} = V_{DD} – 0.5V
Input Current Noise Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz, V_{CM} = 0.1V
		—	0.6	—		f = 1 kHz, V_{CM} = V_{DD} – 0.5V
Harmonic Distortion – Output Nonlinearity						
Total Harmonic Distortion + Noise	THD+N	—	-115	—	dBc	G_N = 1 V/V, f = 1 kHz, V_{OUT} = 2 V_{P-P}, V_{DD} = 5V, V_{CM} = 2V
EMI Protection						
EMI Rejection Ratio	EMIRR	—	29	—	dB	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	50	—		V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	71	—		V_{IN} = 0.1 V_{PK}, f = 1800 MHz
		—	81	—		V_{IN} = 0.1 V_{PK}, f = 2400 MHz
		—	112	—		V_{IN} = 0.1 V_{PK}, f = 6000 MHz
Shutdown						
Shutdown V_{OUT} Turn On Time	t_{SD_ON}	—	3.1	—	µs	I_O = 0, V_L = 0V, SHDN = 3.5V to 0V step, 90% of V_{OUT} change (Note 2)
Shutdown V_{OUT} Turn Off Time	t_{SD_OFF}	—	0.5	—	µs	I_O = 0, V_L = 0V, SHDN = 0V to 3.5V step, 90% of V_{OUT} change (Note 2)
Shutdown Setup Time	t_{SD_SU}	—	0.5	—	µs	Minimum setup time between SHDN events (Note 2)

Note 1: t_{ODR} includes some uncertainty due to clock edge timing.

2: The POR must be on for the time t_{PON_TR} before SHDN function is enabled; it is disabled when the POR is off.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF; see Figure 1-7.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Up/Down						
POR Off Time	t_{PRHL}	—	1	—	µs	V_L = 0V, V_{DD} = 2.2V to V_{PHL} – 0.1V step, 90% of V_{OUT} change
POR On Time	t_{PRLH}	—	1	—		V_L = 0V, V_{DD} = 0V to V_{PLH} + 0.1V step, 90% of V_{OUT} change
V_{OUT} Power On Time (V_{DD} ↑)	t_{PON}	—	22	—		V_{DD} = 0V to 3.5V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of V_{OUT} change, SHDN is low
		—	52	—		V_{DD} = 0V to 3.5V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of V_{OUT} change, SHDN is low, T_A = -40°C
V_{OUT} Power Off Time (V_{DD} ↓)	t_{POFF}	—	0.2	—		V_{DD} = 3.5V to 0V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of V_{OUT} change, SHDN is low
I_Q Power On Time (V_{DD} ↑)	t_{PONIQ}	—	21	—		V_{DD} = 0V to 3.5V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of I_Q change, SHDN is low
		—	58	—		V_{DD} = 0V to 3.5V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of I_Q change, SHDN is low, T_A = -40°C
I_Q Power Off Time (V_{DD} ↓)	t_{POFFIQ}	—	0.2	—		V_{DD} = 3.5V to 0V, V_{CM} = 0V, V_L = 0V, G_N = 1, 90% of I_Q change, SHDN is low
Trim Power On Time (V_{DD} ↑) (Note 2)	t_{PON_TR}	—	235	285		Singles, V_{DD} = 0V to 3.5V, V_{CM} = 0V, G_N = 1, all trims to 100% (time when I_{DD} changes from ≥ I_{Q_TR} to ≥ I_Q), SHDN is disabled until after this time

Note 1: t_{ODR} includes some uncertainty due to clock edge timing.

2: The POR must be on for the time t_{PON_TR} before SHDN function is enabled; it is disabled when the POR is off.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = 2.2V to 5.5V and V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range		-40	—	+150		(Note 1)
Storage Temperature Range		-65	—	+150		Powered off
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	209	—	°C/W	
Thermal Resistance, 5L-SOT-23		—	201	—		
Thermal Resistance, 6L-SOT-23		—	191	—		

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature Rating (+150°C).

1.3 Timing Diagrams

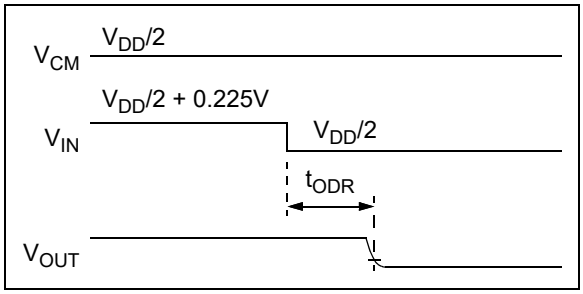


FIGURE 1-1: *Output Overdrive Recovery Timing Diagram.*

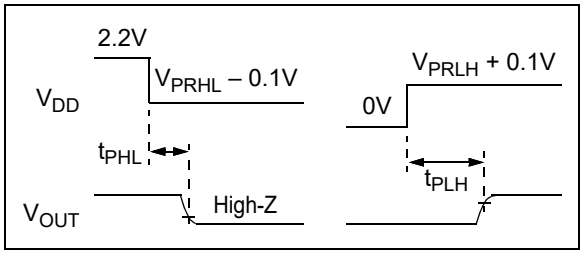


FIGURE 1-2: *POR Timing Diagram.*

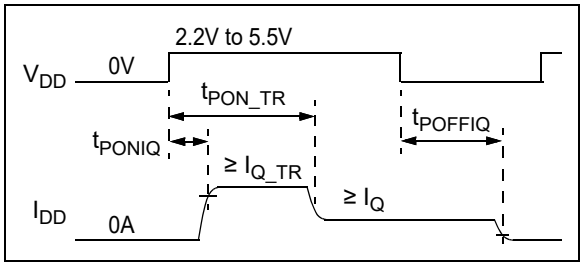


FIGURE 1-3: *Supply Current Power Up/Down Timing Diagram, with SHDN Low.*

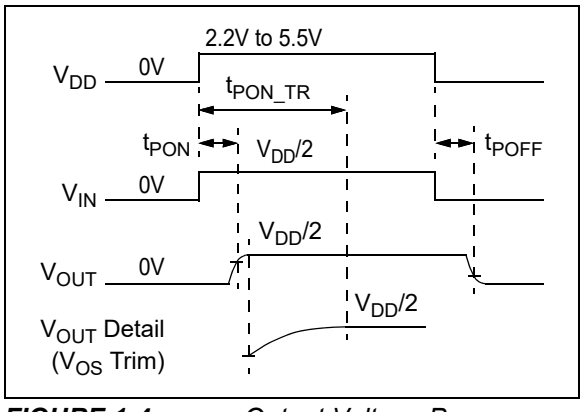


FIGURE 1-4: *Output Voltage Power Up/Down Timing Diagram, with V_L = 0V and SHDN Low.*

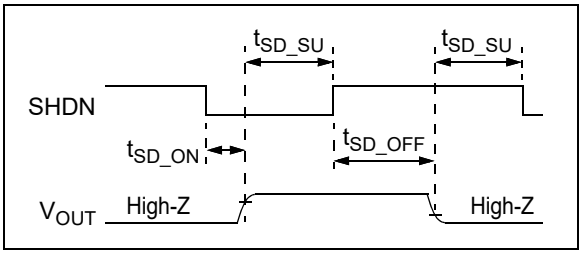


FIGURE 1-5: *SHDN Timing Diagram, with 2.2V ≤ V_{DD} ≤ 5.5V (the POR must be on for the time t_{PON_TR} before SHDN is enabled; see Figure 1-3).*

1.4 Test Circuits

Figure 1-6 shows the circuit used for many DC tests; it sets V_{CM} and V_{OUT} (see Equation 1-1).

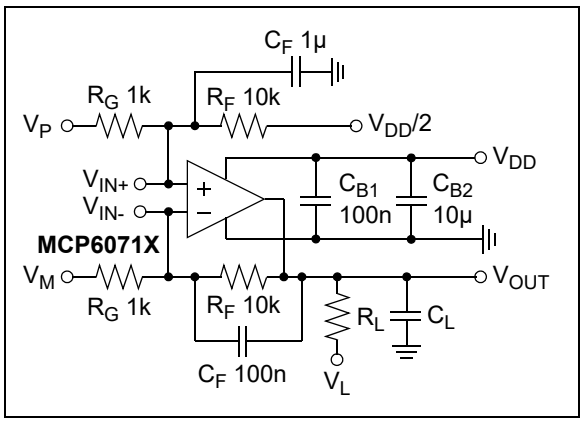


FIGURE 1-6: *DC Bench Test Circuit.*

EQUATION 1-1:

$G_{DM} = R_F/R_G$

$V_{CM} \approx (V_P G_{DM} + V_{DD}/2) / (G_{DM} + 1)$

$V_{OUT} = (V_{DD}/2) + (V_P - V_M)G_{DM} + V_{OST}(G_{DM} + 1)$

Where:

G_{DM} = Differential-Mode Gain (V/V)

$V_{CM} = (V_{IN+} + V_{IN-})/2$

V_{OST} = Op Amp's Total Input Offset Voltage (mV)
$= V_{IN-} - V_{IN+}$

V_{OST} includes V_{OS} plus temperature, CMRR, PSRR and A_{OL} effects. V_{CM} is the op amp's common mode input voltage. The circuit's common-mode input voltage is $V_{CMX} = (V_P + V_M)/2$.

Figure 1-7 shows the circuit used for many AC tests. Ground V_M to make the gain noninverting. Ground V_P to make the gain inverting. Keep the op amp stable and fast by making the R-C poles caused by the input capacitances faster than the designed bandwidth (see Equation 1-2).

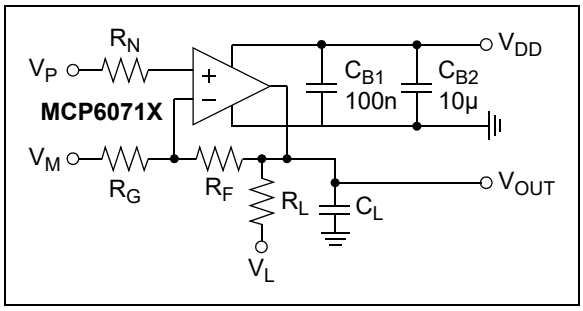


FIGURE 1-7: *AC Bench Test Circuit.*

EQUATION 1-2:

$G_N = 1 + R_F/R_G$

$f_{BW} \approx GBWP/G_N$, bandwidth ($G_N > 2$)

$R_N < 0.5/(2\pi f_{BW} (C_{CM} + C_{DM}))$, for speed

$(R_F||R_G) < 0.5/(2\pi f_{BW} (C_{CM} + C_{DM}))$, for stability

Where:

C_{CM} = Common Mode Input Capacitance (F)

C_{DM} = Differential Mode Input Capacitance (F)

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

2.1 DC Input Precision

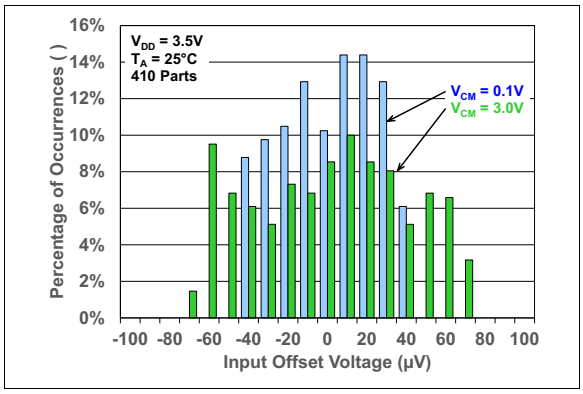


FIGURE 2-1: *Input Offset Voltage.*

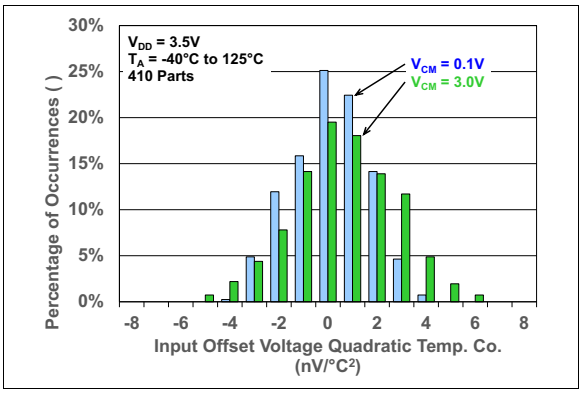


FIGURE 2-3: *Input Offset Voltage Quadratic Temp. Co.*

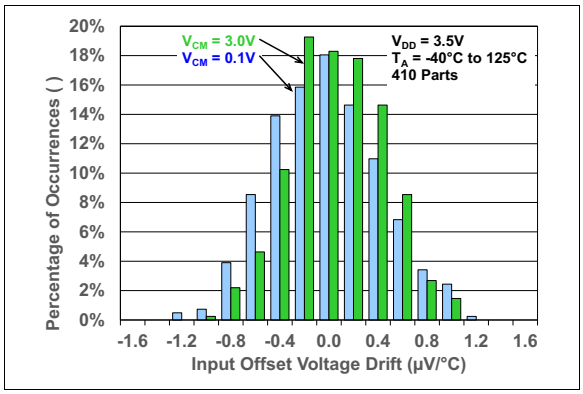


FIGURE 2-2: *Input Offset Voltage Drift.*

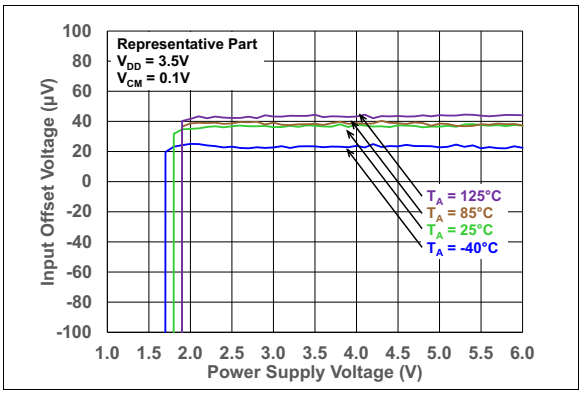


FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0.1V.*

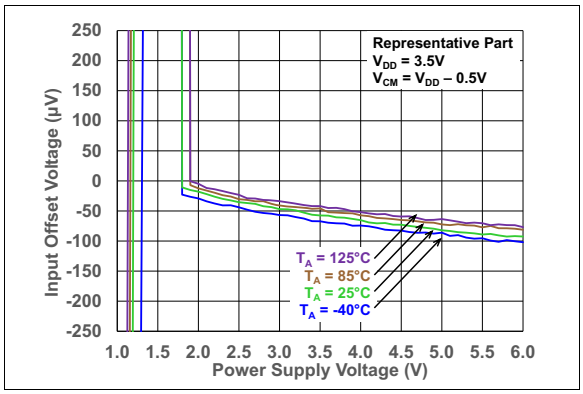


FIGURE 2-5: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} – 0.5V.*

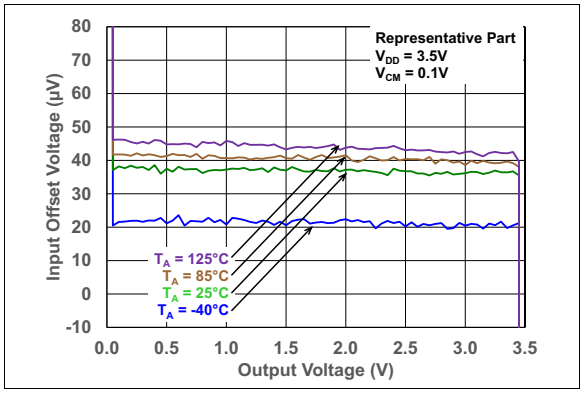


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage, with V_{DD} = 3.5V.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

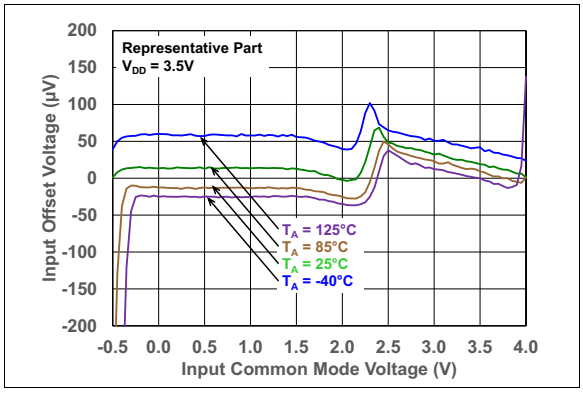


FIGURE 2-7: *Input Offset Voltage vs. Input Common Mode Voltage, with V_{DD} = 3.5V.*

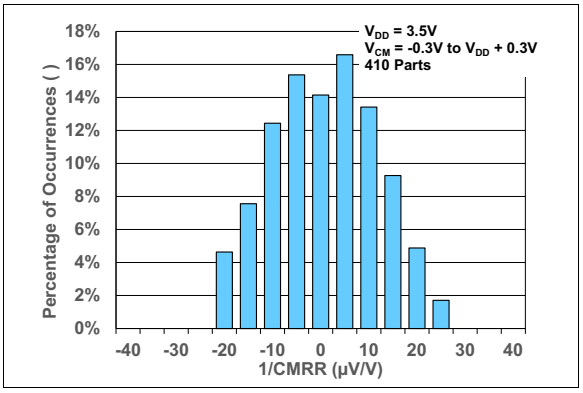


FIGURE 2-10: *Common Mode Rejection Ratio, with V_{DD} = 3.5V.*

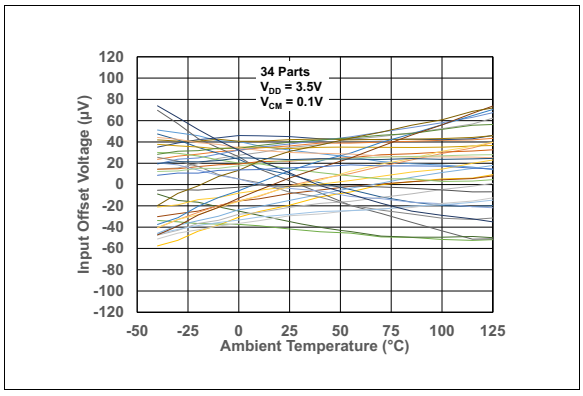


FIGURE 2-8: *Input Offset Voltage vs. Temperature, with V_{DD} = 3.5V and V_{CM} = 0.1V.*

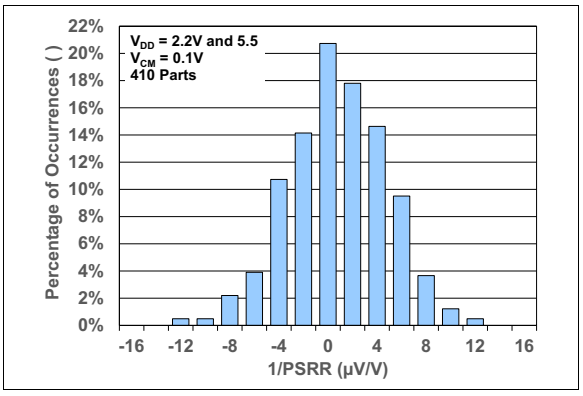


FIGURE 2-11: *Power Supply Rejection Ratio, with V_{CM} = 0.1V.*

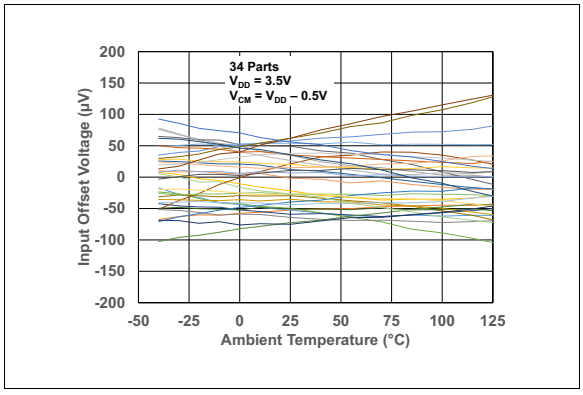


FIGURE 2-9: *Input Offset Voltage vs. Temperature, with V_{DD} = 3.5V and V_{CM} = V_{DD} – 0.5V.*

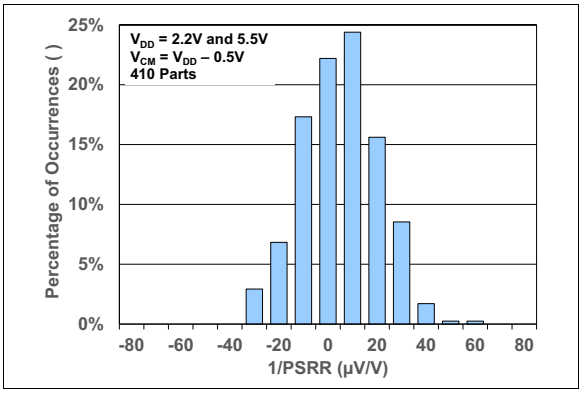


FIGURE 2-12: *Power Supply Rejection Ratio, with V_{CM} = V_{DD} – 0.5V.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

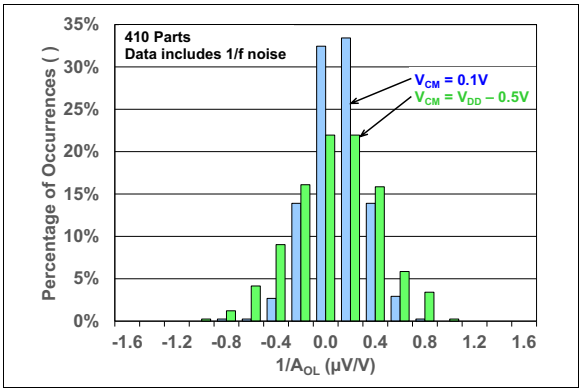


FIGURE 2-13: *DC Open-Loop Gain, with V_{CM} = 0.1V and V_{DD} – 0.5V.*

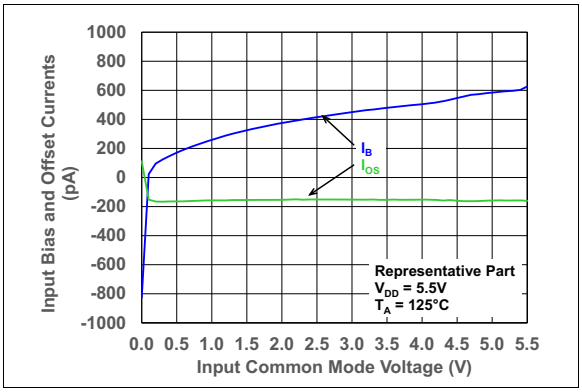


FIGURE 2-16: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +125°C.*

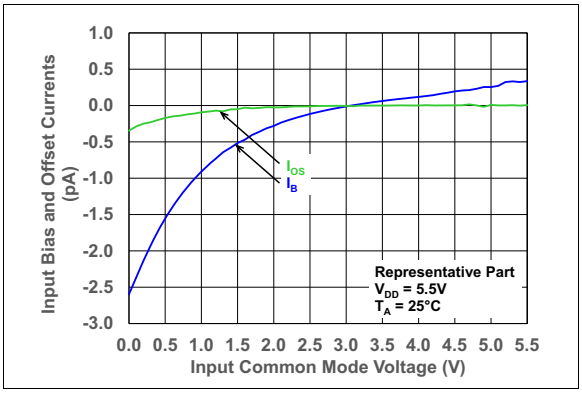


FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +25°C.*

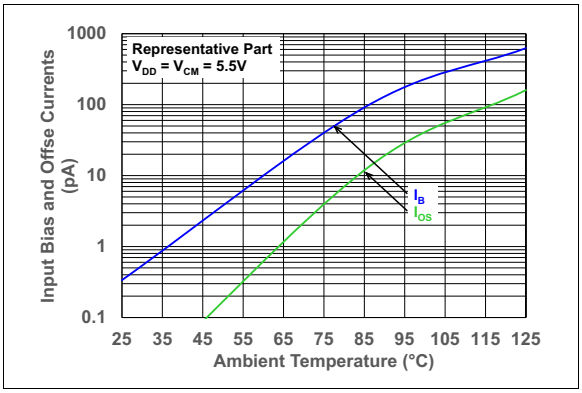


FIGURE 2-17: *Input Bias and Offset Currents vs. Ambient Temperature, with V_{DD} = 5.5V.*

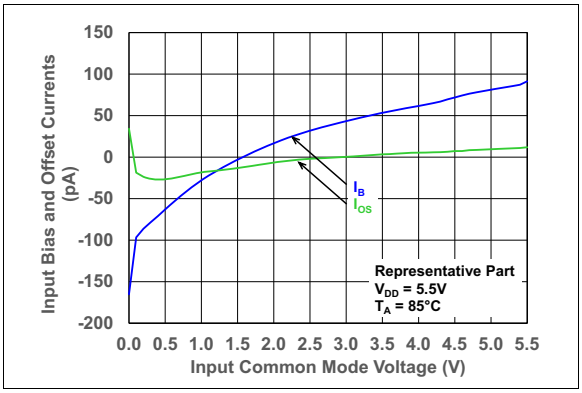


FIGURE 2-15: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +85°C.*

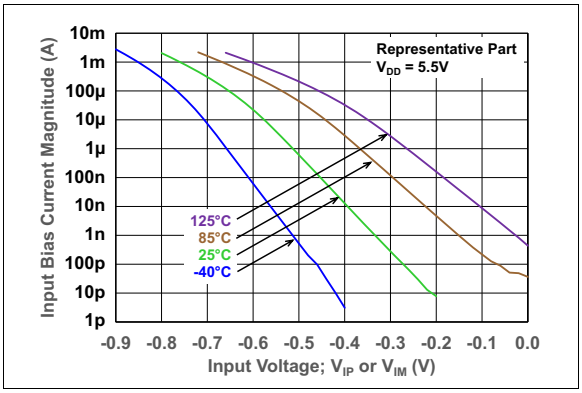


FIGURE 2-18: *Input Bias Current vs. Input Voltage (below V_{SS}).*

2.2 Other DC Voltages and Currents

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

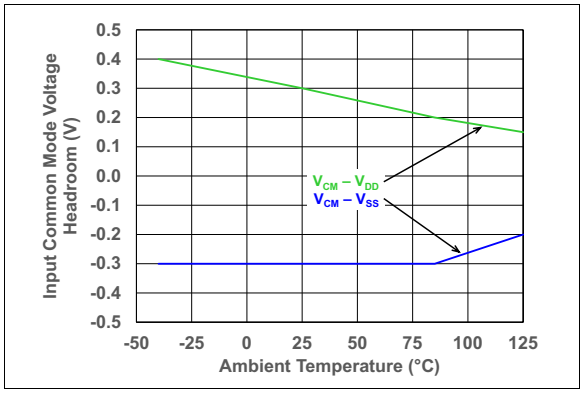


FIGURE 2-19: *Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.*

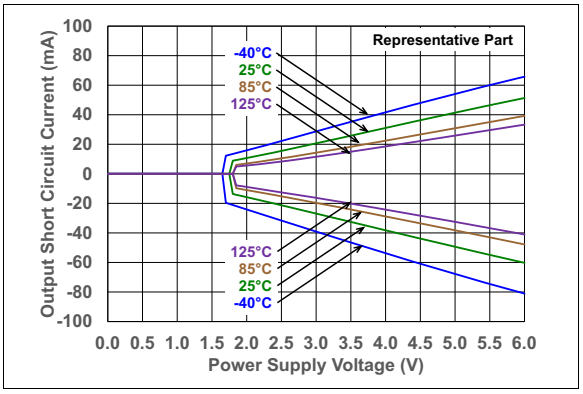


FIGURE 2-22: *Output Short Circuit Current vs. Power Supply Voltage.*

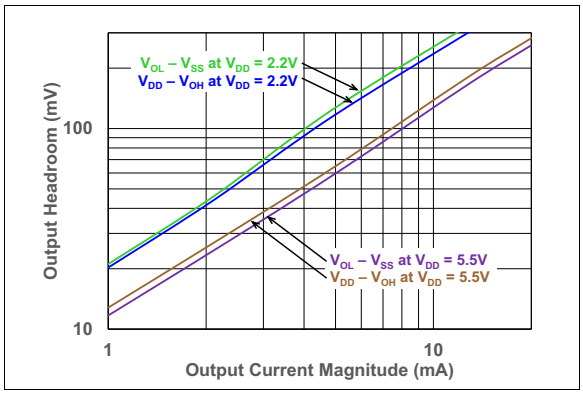


FIGURE 2-20: *Output Voltage Headroom vs. Output Current.*

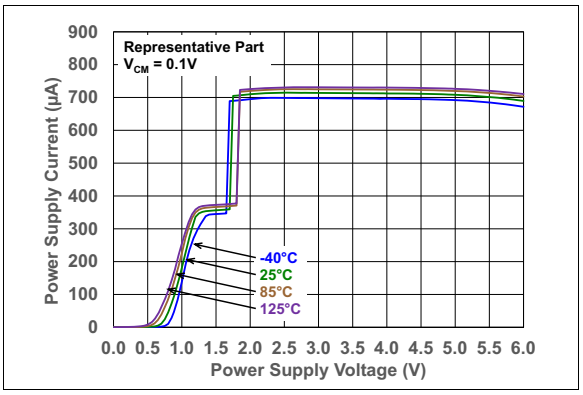


FIGURE 2-23: *Power Supply Current vs. Power Supply Voltage.*

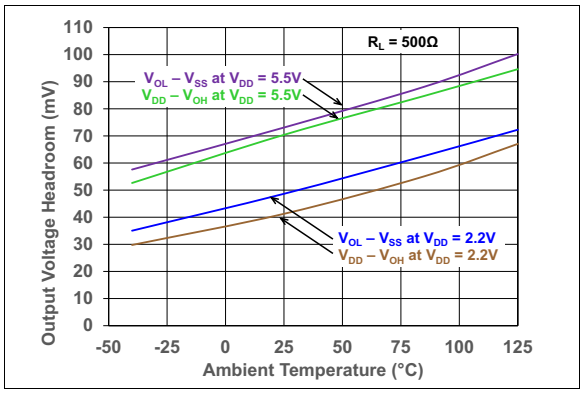


FIGURE 2-21: *Output Voltage Headroom vs. Ambient Temperature.*

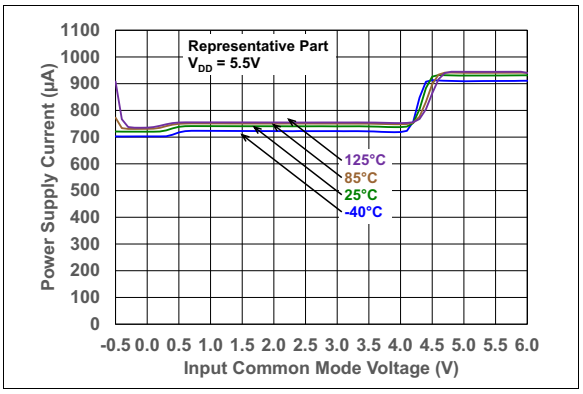


FIGURE 2-24: *Supply Current vs. Input Common Mode Voltage, with V_{DD} = 5.5V.*

2.3 Frequency Response

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

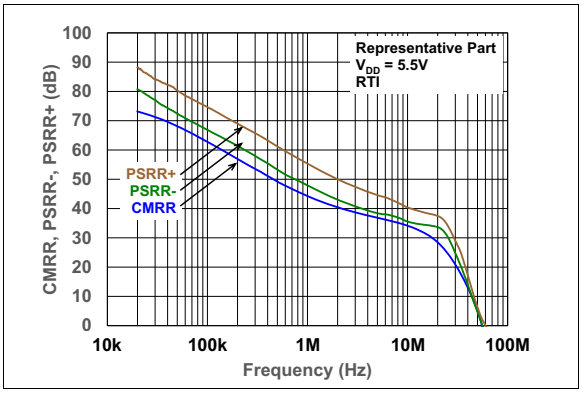


FIGURE 2-25: *CMRR and PSRR vs. Frequency.*

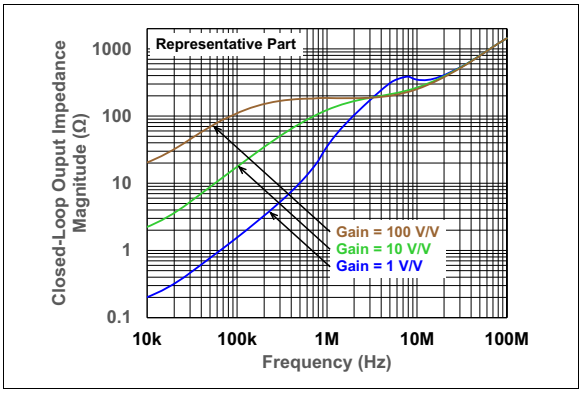


FIGURE 2-28: *Closed-Loop Output Impedance vs. Frequency.*

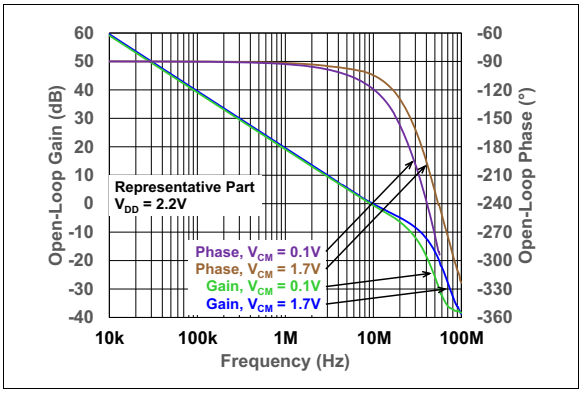


FIGURE 2-26: *Open-Loop Gain vs. Frequency, with V_{DD} = 2.2V.*

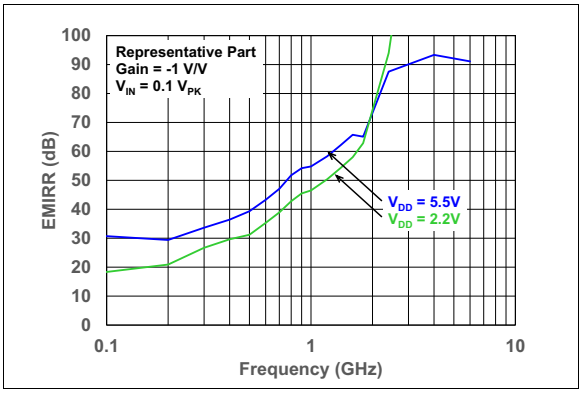


FIGURE 2-29: *EMIRR vs. Frequency.*

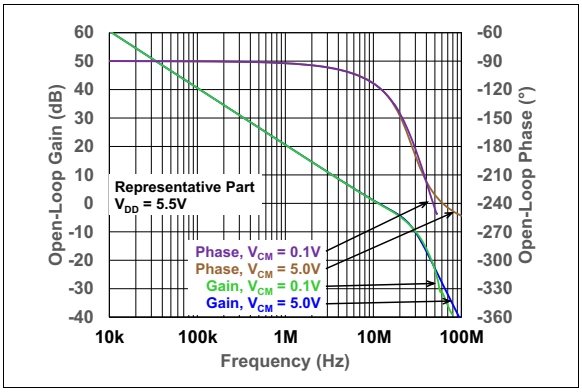


FIGURE 2-27: *Open-Loop Gain vs. Frequency, with V_{DD} = 5.5V.*

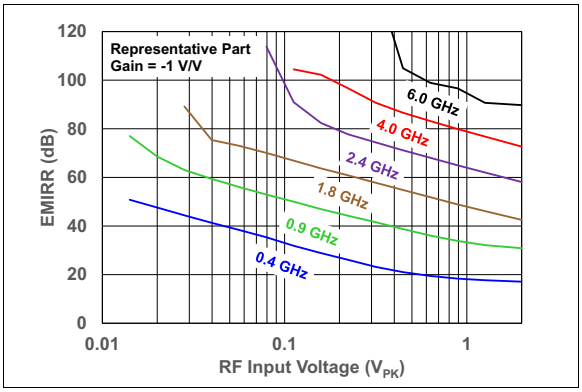


FIGURE 2-30: *EMIRR vs. RF Input Voltage.*

2.4 Input Noise and Distortion

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

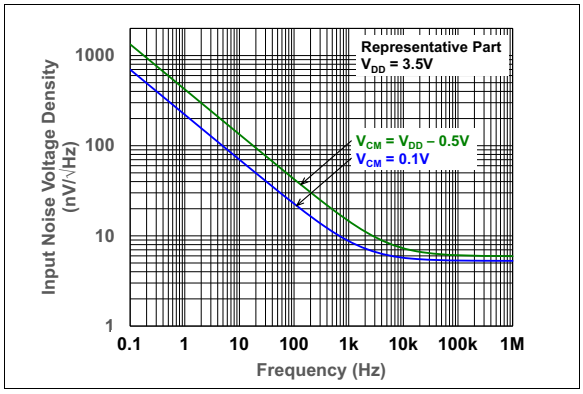


FIGURE 2-31: *Input Noise Voltage Density vs. Frequency.*

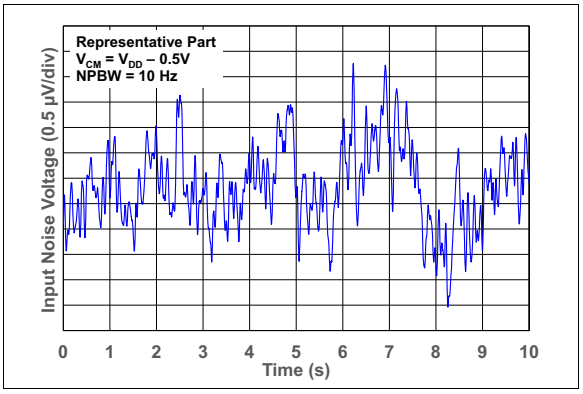


FIGURE 2-33: *Input Noise vs. Time, with a 0.1 Hz to 10 Hz Low-pass Filter and V_{CM} = V_{DD} – 0.5V.*

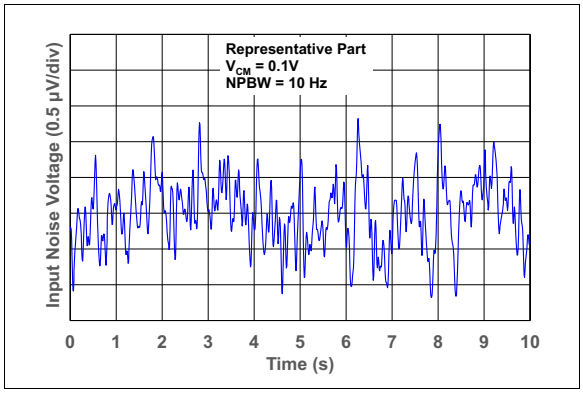


FIGURE 2-32: *Input Noise vs. Time, with a 0.1 Hz to 10 Hz Low-pass Filter and V_{CM} = 0.1V.*

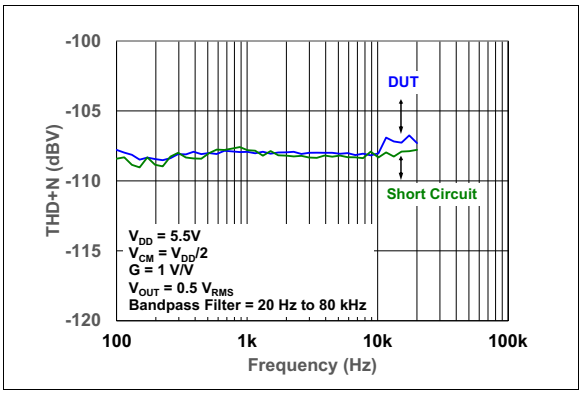


FIGURE 2-34: *Total Harmonic Distortion plus Noise vs. Frequency.*

2.5 Time Response

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

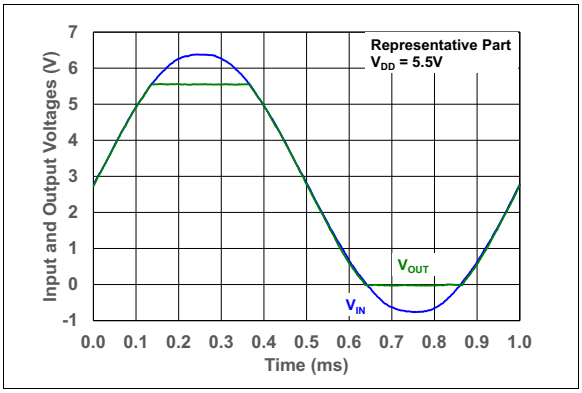


FIGURE 2-35: *The MCP60711/1U/3 Family Shows no Input Phase Reversal with Overdrive.*

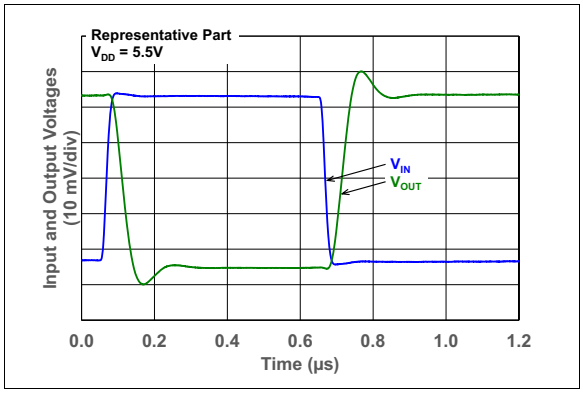


FIGURE 2-38: *Inverting Small Signal Step Response.*

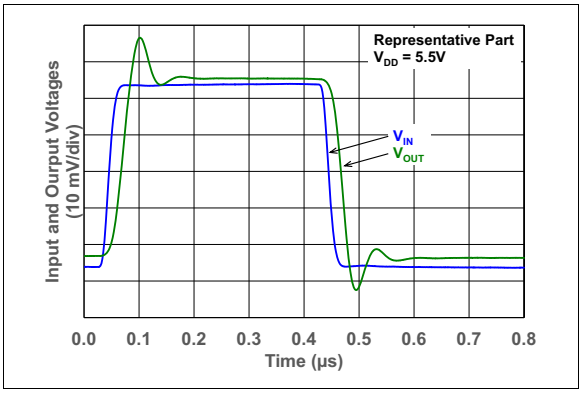


FIGURE 2-36: *Noninverting Small Signal Step Response.*

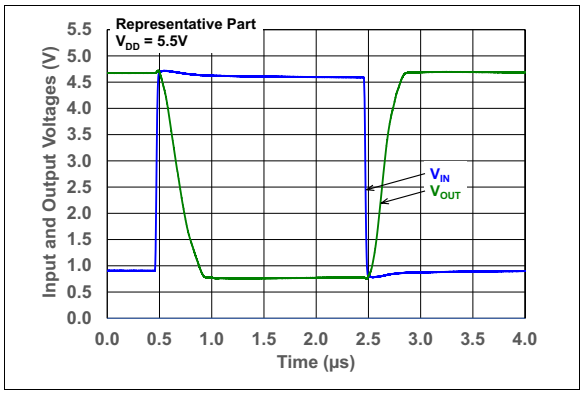


FIGURE 2-39: *Inverting Large Signal Step Response.*

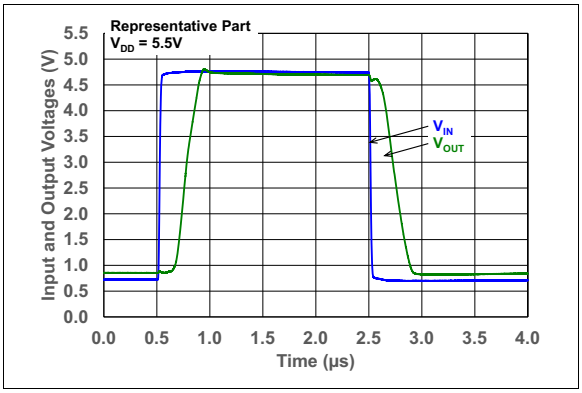


FIGURE 2-37: *Noninverting Large Signal Step Response.*

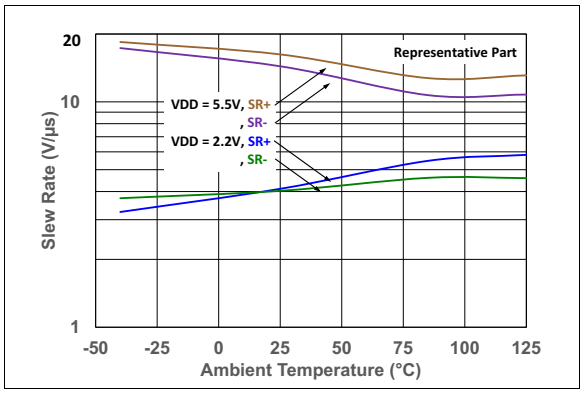


FIGURE 2-40: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

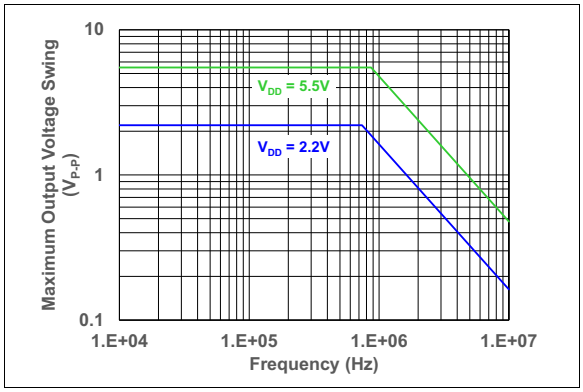


FIGURE 2-41: *Maximum Output Voltage Swing vs. Frequency.*

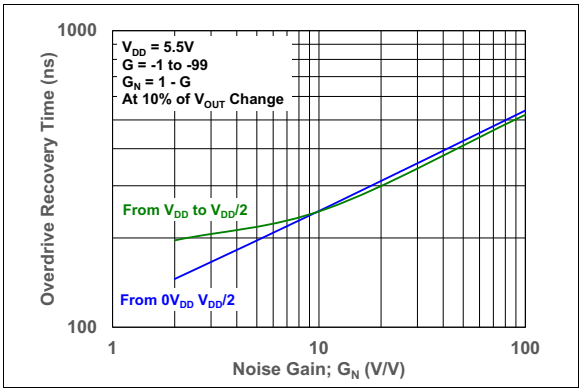


FIGURE 2-42: *Output Overdrive Recovery Time vs. Noise Gain.*

2.6 Capacitive Loads

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = 3.5V, V_{SS} = GND, V_{CM} = 0.1V, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 5 kΩ to V_L and C_L = 30 pF.

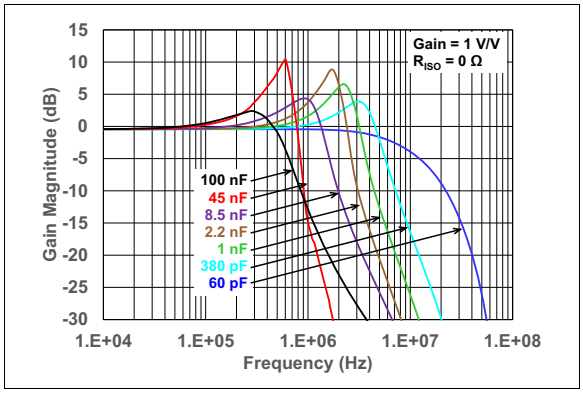


FIGURE 2-43: *Gain Magnitude vs. Frequency, with Uncompensated Capacitive Loads and Gain = 1 V/V.*

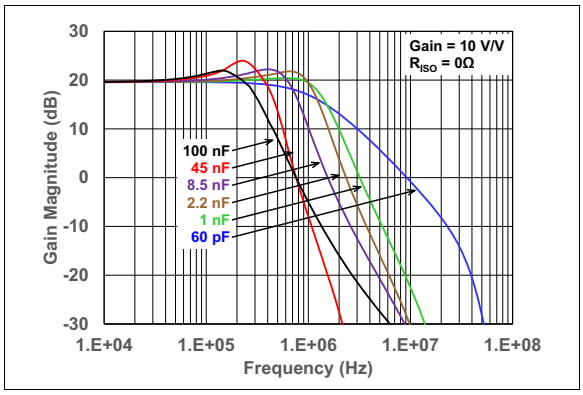


FIGURE 2-44: *Gain Magnitude vs. Frequency, with Uncompensated Capacitive Loads and Gain = 10 V/V.*

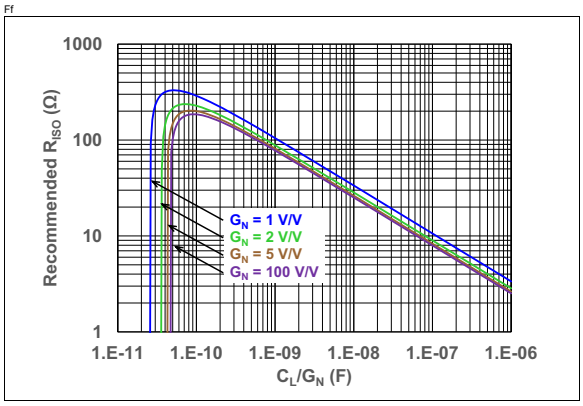


FIGURE 2-45: *Recommended R_{ISO} vs. Normalized Capacitive Load (see Section 4.2.4).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP60711	MCP60711U	MCP60713	Symbol	Description
SOT-23	SC70	SOT-23		
1	4	1	V_{OUT}	Output
4	3	4	V_{IN}-	Inverting Input
3	1	3	V_{IN}+	Noninverting Input
5	5	6	V_{DD}	Positive Power Supply
2	2	2	V_{SS}	Negative Power Supply
—	—	5	SHDN	Shut Down

3.1 Analog Outputs

The output pin is a low-impedance voltage source.

3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Shutdown Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a Low-Power standby mode. The internal trim values are kept active, but the op amp is disabled. The POR must be on (power is up) for the time t_{PON_TR} before SHDN is enabled (see Figure 1-3). $\overline{SHDN}$ is disabled once the POR is off (power is down).

3.4 Power Supply Pins

For normal operation, the positive power supply (V_{DD}) is 2.2V to 5.5V higher than the negative power supply (V_{SS}). Also, the output (V_{OUT}) is between V_{SS} and V_{DD}, while the V_{CM} range is larger (see the V_{CML} and V_{CMH} specs and Figure 2-19).

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} needs a bypass capacitor.

Dual (or split) supply configurations connect the V_{DD} and V_{SS} pins to their respective supply voltages; the supply also has a circuit ground connection. Both V_{DD} and V_{SS} need bypass capacitors.

4.0 APPLICATION INFORMATION

This family of op amps is manufactured using a state-of-the-art CMOS process and is specifically designed for low-cost, high speed and DC precision.

4.1 Op Amp Operation

4.1.1 ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings (see Section 1.1, Absolute Maximum Ratings †) are independent of each other; all of them must be enforced by the user. Being at, or near, two or more Absolute Maximum Ratings at the same time may increase risk.

4.1.2 RAIL-TO-RAIL INPUTS

4.1.2.1 Phase Reversal

The MCP60711/1U/3 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-35 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2.2 Input Voltage and Current Limits

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} or more than one diode drop above V_{DD}.

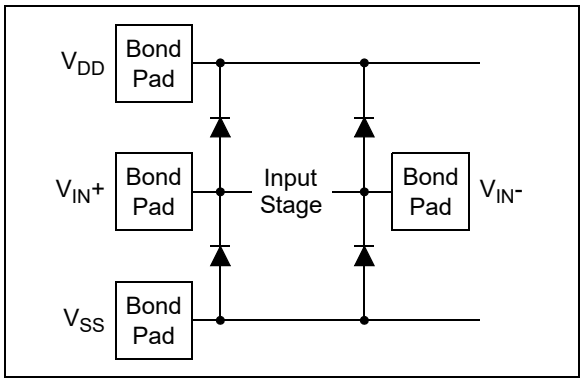


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see Section 1.1, Absolute Maximum Ratings †). Figure 4-2 shows the recommended approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents at the input pins.

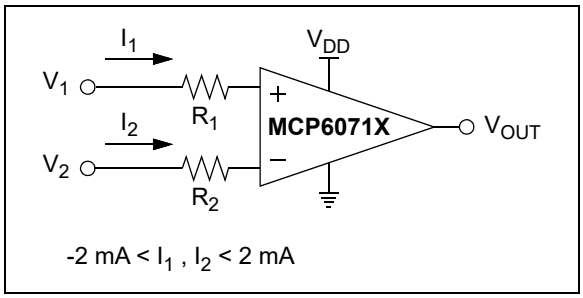


FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-18.

The differential input voltage ($V_{DM} = V_{IN}+ – V_{IN}-$) needs to be limited for normal operations; keep its magnitude below 0.5V. Reasons that this limit may be exceeded include operating voltages outside of their operating limits and input signals with very fast rise or fall rates.

4.1.3 INPUT ERRORS

The input offset voltage (V_{OS}) is trimmed at V_{CM} = 0.1V and $V_{CM} = V_{DD} – 0.5V$, which gives good V_{OS} and CMRR.

Reducing stresses (mechanical, thermal and electrical) improves input offset aging. Applications with long life-times and calibration requirements will benefit.

The input bias current (I_B) and input offset current (I_{OS}) are low across temperature; they will support many applications.

4.1.4 RAIL-TO-RAIL OUTPUTS

4.1.4.1 Output Voltage Limits

Figure 2-20 and Figure 2-21 show typical values of output headroom versus output current and temperature. Also, Figure 2-42 shows the output overdrive vs. temperature behavior of these parts

4.1.4.2 Output Current Limits

For reliable operations, limit the output current (see Section 1.1, Absolute Maximum Ratings †). These op amps' output short circuit current will help, but the circuit may also need to limit the output current.

Large output currents, in some cases, may increase the internal junction temperature (T_J) of the output stage too high (see Section 1.1, Absolute Maximum Ratings †).

Figure 4-3 show the quantities used in the following power calculations for a single op amp. R_{SER} is 0 Ω in most applications; higher values can be used to limit I_{OUT}. V_{OUT} is the op amp's output voltage, V_L is the

voltage at the load, and V_{LG} is the load's ground point. V_{SS} is usually ground (0V). The input currents are assumed to be negligible.

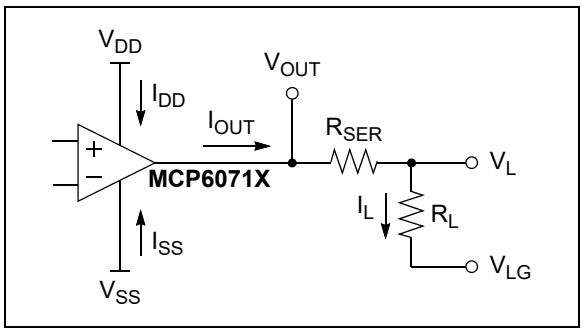


FIGURE 4-3: *Diagram for Power Calculations.*

The currents shown are approximately:

EQUATION 4-1:

$$I_{OUT} = I_L = \frac{V_{OUT} - V_{LG}}{R_{SER} + R_L}$$

$$I_{DD} \approx I_Q + max(0, I_{OUT})$$

$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = Quiescent supply current

The instantaneous op amp power ($P_{OA}(t)$), R_{SER} power ($P_{RSER}(t)$) and load power ($P_L(t)$) are:

EQUATION 4-2:

$$P_{OA}(t) = I_{DD}\,(V_{DD} - V_{OUT}) + I_{SS}\,(V_{SS} - V_{OUT})$$

$$P_{RSER}(t) = I_{OUT}^2 R_{SER}$$

$$P_L(t) = I_L^2 R_L$$

The maximum op amp power dissipation, with resistive loads, occurs when V_{OUT} is halfway between V_{DD} and V_{LG} or halfway between V_{SS} and V_{LG}:

EQUATION 4-3:

$$P_{OAmax} \leq \frac{max^2(V_{DD} - V_{LG}\,,\, V_{LG} - V_{SS})}{4(R_{SER} + R_L)}$$

The maximum ambient to junction temperature rise (ΔT_{JA}) and junction temperature (T_J) is calculated using the sum P_{OAmax} for all op amps in the same package (ΣP_{OAmax}), ambient temperature (T_A), and the package thermal resistance (θ_{JA}) found in Table 1-3:

EQUATION 4-4:

$$\Delta T_{JA} = (\Sigma P_{OAmax})\,\theta_{JA}$$

$$T_J = T_A + \Delta T_{JA}$$

4.1.5 TRIMMED I_Q

The quiescent current (I_Q) is trimmed and is reasonably flat across temperature (T_A) and supply voltage ($V_{DD} - V_{SS}$); see Figure 2-23. This reduces the maximum power dissipation in an application. I_Q does increase at higher V_{CM} levels; see Figure 2-24.

4.1.6 EMI REJECTION RATIO (EMIRR)

Electromagnetic interference (EMI) is the disturbance that affects an electrical circuit, due to either electromagnetic induction or radiation, emitted from an external source.

EMIRR helps describe the EMI robustness of an op amp to an interfering RF signal. The common errors caused by EMI in circuits are a shift in input offset voltage (V_{OS}), due to nonlinearities at the input, and interference at high frequencies. EMIRR compares the change in V_{OS} to the RF signal's peak voltage.

EQUATION 4-5:

$$EMIRR(dB) = 20\,log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

V_{RF} = Interfering RF Signal's peak voltage (V_{PK})

ΔV_{OS} = Input Offset Voltage Shift (V)

Internal passive filters improve EMIRR, but good PCB layout techniques are also necessary for best overall performance.

4.2 Circuit Design

4.2.1 SUPPLY BYPASS

For a positive single supply (V_{SS} = 0V and $V_{DD} > V_{SS}$), the V_{DD} pin needs a local bypass capacitor (usually 10 nF to 100 nF) within 2 mm of the V_{DD} pin; this gives good high-frequency performance. It also needs a bulk capacitor (usually 1 µF or larger) within 10 mm; this provides for large, slow currents. In some cases, but not all, this bulk capacitor can be shared with nearby analog parts.

For split or dual supplies ($V_{SS} < 0V < V_{DD}$), both the V_{DD} pin and the V_{SS} pin need bypass capacitors as described in the previous paragraph.

4.2.2 PCB SURFACE LEAKAGE

In applications where maintaining low input currents is critical, Printed Circuit Board (PCB) leakage currents must be minimized. These PCB leakage currents are mainly caused by humidity, dust or other contaminants on the PCB surfaces.

The following techniques can help to reduce PCB leakage currents:

- Place critical input traces in inner layers
- Use conformal coating
- Use guard rings where possible (packages with tightly spaced pins can limit this approach)

4.2.3 LOW OFFSETS

4.2.3.1 Input Offset Voltage Errors

The data sheet parameters that describe DC voltage errors at the op amp's input, act as an increase of the voltage at the noninverting input (see Figure 4-4). These parameters are: V_{OS}, TC_1, TC_2, CMRR, PSRR and A_{OL} (see the DC Electrical Specifications table).

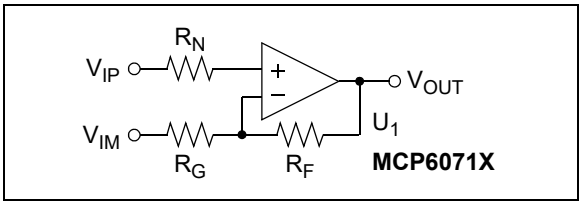


FIGURE 4-4: *Op Amp Feedback Network.*

The combined errors are:

EQUATION 4-6:

$$V_{OST} = V_{OS} + TC_1(T_A - 25°C) + TC_2(T_A - 25°C)^2 + \Delta V_{CM}/CMRR + \Delta V_{OUT}/A_{OL} + \Delta(V_{DD} - V_{SS})/PSRR$$

Where:

V_{OST} = total input offset voltage (error)

1/CMRR, $1/A_{OL}$ and 1/PSRR have units of µV/V (e.g., ±100 µV/V corresponds to 80 dB)

The error referred to V_{OUT} is:

EQUATION 4-7:

$$V_{OERR} = G_N V_{OST}$$

Where:

V_{OERR} = total output offset voltage (error)

G_N = the circuit's DC "Noise Gain" $= 1 + R_F/R_G$, in Figure 4-4

Mechanical stresses on an op amp will change the input offset voltage. Standard techniques to minimize stresses on the PCB will minimize this issue.

4.2.3.2 Input Bias Current Errors

The Input Bias Current (I_B) and Input Offset Current (I_{OS}) cause voltage drops across resistors in the circuit, increasing the voltage errors. These currents are positive when they go into the op amp, so the circuit in Figure 4-4 gives:

EQUATION 4-8:

$$V_{TIBE} = (I_B - I_{OS}/2)(R_F||R_G) - (I_B + I_{OS}/2) R_N$$

$$V_{TOBE} = G_N V_{TIBE}$$

Where:

V_{TIBE} = total input bias current error

V_{TOBE} = total output bias current error

G_N is defined in Equation 4-7

Note that the PCB leakage currents discussed in Section 4.2.2, PCB Surface Leakage add additional DC errors to the circuit. These errors depend on where these currents are injected into the circuit. Standard circuit analysis techniques will give the output error.

4.2.4 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the signal's frequency response (see Figure 2-43 and Figure 2-44) and overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior. See Section 2.6, Capacitive Loads for plots of typical behavior.

When driving large capacitive loads (e.g., C_L > 30 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

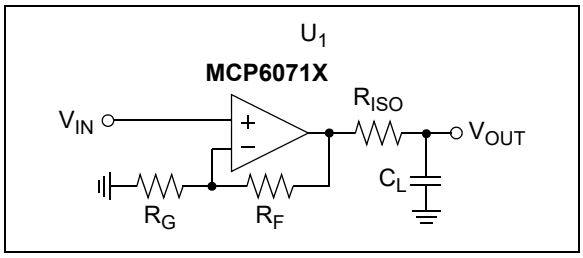


FIGURE 4-5: *Compensating a Capacitive Load (C_L) with R_{ISO}.*

Figure 2-45 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the

circuit's noise gain. For noninverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1 + |Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation of R_{ISO}'s effect on a specific design is important.

4.2.5 ESTIMATING THE BANDWIDTH

The three most common op amp circuits are represented by Figure 4-6: noninverting gain (R_{PF} = open and V_{IM} grounded), inverting gain (R_{PF} = open and V_{IP} grounded) and differential (difference) gain.

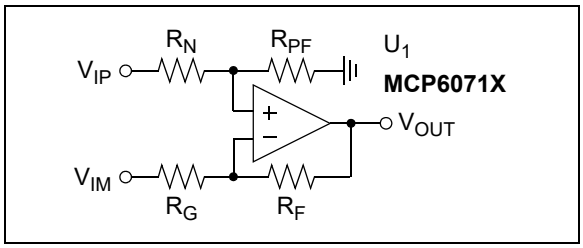


FIGURE 4-6: *Common Op Amp Configurations.*

The Noise Gain and Small Signal Bandwidth are:

EQUATION 4-9:

$$G_N = 1 + R_F/R_G$$
$$BW \approx GBWP/G_N, \quad G_N > 2$$

The Full Power Bandwidth (FPBW) is the frequency where a large output sine wave's maximum slope equals the Slew Rate (SR):

EQUATION 4-10:

V_{OPP} = Peak-to-Peak Output Voltage, (V_{P-P})

$$FPBW \approx |SR|/(\pi V_{OPP}), \quad (Hz)$$

For accurate AC gains, set BW higher than the input signal's bandwidth (e.g., a 10 to 1 ratio). For low harmonic distortion, set FPBW higher than BW (e.g., a 3 to 1 ratio).

4.2.6 GAIN PEAKING

Figure 4-7 shows an op amp circuit that represents noninverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's Common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel.

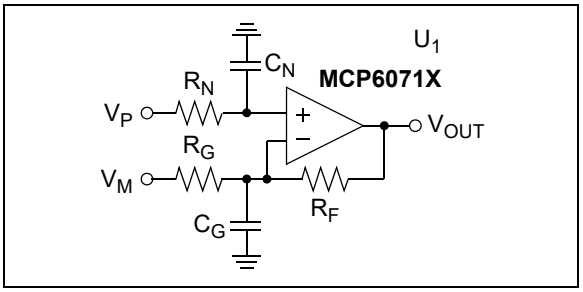


FIGURE 4-7: *Amplifier with Parasitic Capacitance.*

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G and/or $R_F||R_G$ so that:

EQUATION 4-11:

$$2\,BW \le 1 / (2\pi(R_F||R_G)C_G)$$

C_N and R_N form a low-pass filter that affects the signal at V_{IP}. This filter has a single real pole at $1/(2\pi R_N C_N)$. Usually, this pole should be faster than the BW:

EQUATION 4-12:

$$2\,BW \le 1 / (2\pi R_N C_N)$$

It is also possible to add a capacitor (C_F) in parallel with R_F to compensate for the destabilizing effect of C_G, making it possible to use larger values of R_F. This will also reduce the bandwidth at higher gain. The conditions for stability are shown in Figure 4-13.

It pays to simulate the circuit after making these changes. Be sure to include all of the significant capacitances and inductances, including parasitic ones.

EQUATION 4-13:

Given:

$$G_{N1} = 1 + R_F/R_G$$
$$G_{N2} = 1 + C_G/C_F$$
$$f_F = 1 / (2\pi R_F C_F), \quad \text{response pole}$$
$$f_Z = f_F\,(G_{N1}/G_{N2}), \quad \text{response zero}$$

We need:

$$f_F \le GBWP/(2G_{N2}), \quad G_{N1} < G_{N2}$$
$$f_F \le GBWP/(4G_{N1}), \quad G_{N1} > G_{N2}$$

4.2.7 POWER UP/DOWN

The "Power Up/Down" section of Table 1-2 specifies how I_Q and V_{OUT} behave when power pin (V_{DD}) turns the part on and off, using the internal POR circuit.

When powered up, the part quickly becomes operational (t_{PONIQ} and t_{PON}). It will use extra current (I_{Q_TR}) for a short time (t_{PON_TR}) to complete the internal trims. During this time, V_{OS} and I_Q settle to their final values.

When powered down, the part quickly turns off (t_{POFFIQ} and t_{POFF}). Once off, I_Q = 0 µA (since $V_{DD} = V_{SS}$).

When powering up and down, make sure that V_{DD} ramps up and down smoothly and quickly between 0V and 2.2V. This helps the internal digital circuitry to operate as specified.

4.2.8 SHUTDOWN PIN

The “Shutdown” section of Table 1-2 specifies how I_Q and V_{OUT} behave when the Shutdown Pin (SHDN) is high (V_{OUT} is off and I_{DD} is very low) and low (V_{OUT} is on and I_Q is normal).

At initial power up, the part is kept in the enabled state (for the time t_{PON_TR}; see Figure 1-3), in order to load all of the internal trim registers from nonvolatile memory. Once this happens, control is passed to the SHDN pin. At power down, the shutdown function is disabled and the internal trim registers lose their values.

When SHDN turns the part off, the quiescent current reaches a very low level (I_{SS_SD}), which helps with saving power.

When SHDN turns the part on, the part quickly reaches normal operation (all trims are complete) without needing extra current (I_{Q_TR}) or time (t_{PON_TR}) to complete the internal trims. For these reasons, using the SHDN pin may be preferred in some applications.

4.2.9 NOISE

Figure 2-31 shows the Input Noise Voltage Density across frequency ($e_{ni}(f)$). The corresponding Integrated Output Noise Voltage (E_{no}) is the RMS noise seen at the output due to $e_{ni}(f)$ and the Noise Gain across frequency ($G_N(f)$), which is the gain from the op amp's noninverting input to its output). E_{no} is calculated as follows:

EQUATION 4-14:

$$E_{ni}^2(f_L, f_H) = \int_{f_L}^{f_H} e_{ni}^2(f)\, G_N^2(f)\, df$$

E_{ni} has units of nV/√Hz. E_{ni} has two common units: μV_{RMS} (RMS value) and μV_{P-P} (Peak-to-Peak value). The E_{ni} specification (in Table 1-2) has units of μV_{P-P} and a value 6.6 times larger than the RMS value.

4.3 Typical Applications

4.3.1 LOW-PASS FILTER

Figure 4-8 is a low-pass active filter using the Sallen-Key topology. It has a bandwidth of 100 kHz, which takes advantage of the MCP6071x’s speed. It also has low sensitivity to component variations. This and other active filters can be easily designed using Microchip’s FilterLab® design tool.

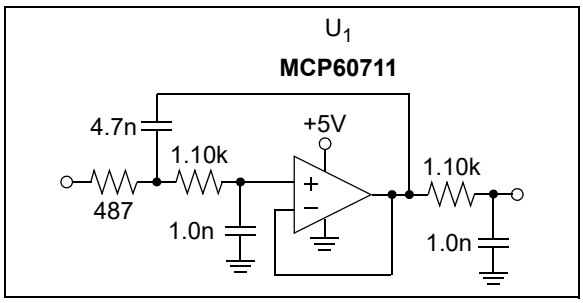


FIGURE 4-8: *Sallen-Key Low-pass Filter.*

4.3.2 EDGE DETECTOR

Figure 4-9 shows an edge detector based on a high-pass Sallen-Key filter and a low-pass R-C filter. At low frequencies, the high-pass filter produces a gain proportional to f^2 (or the second time derivative of V_{IN}), which emphasizes the time points when there are large changes in V_{IN}’s slope. The low-pass filter limits the impact of random noise and interference.

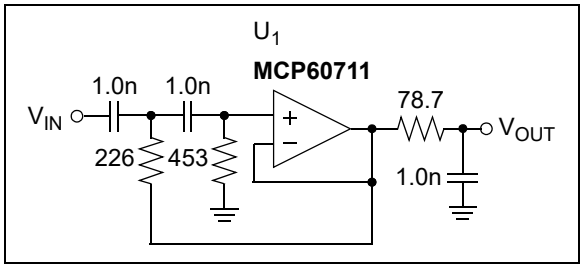


FIGURE 4-9: *Edge Detector Circuit.*

The high-pass filter has a second order Butterworth response, with low step response overshoot. Its cutoff frequency is 0.5 MHz, which supports detection of rise and fall times of about 0.7 µs and longer.

The low-pass filter has a cutoff frequency of 2 MHz, which supports detection of rise and fall times of 0.7 µs and longer.

4.3.3 PHOTO-DIODE DETECTOR

The circuit in Figure 4-10 has a photo-diode detector (D), which has parasitic capacitance C_D and produces an output current (I_D). V_{DB} biases D so that it’s either in photo-voltaic mode (at 0V, like U_1’s noninverting input) or photo-conductive mode (less than 0V). Photo-voltaic mode has a linear response to light, while photo-conductive mode is faster.

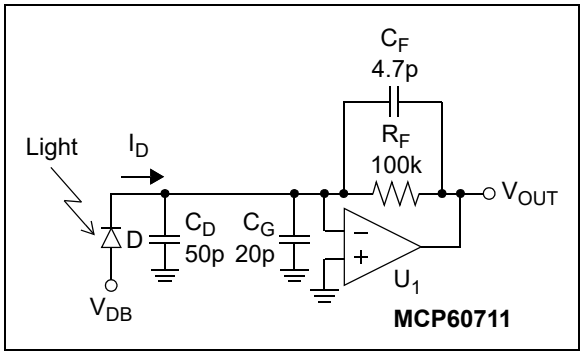


FIGURE 4-10: *Photo-diode Detector Circuit.*

The op amp (U_1) provides gain. The capacitance C_G represents parasitic board capacitance plus U_1's input capacitance (C_{CM}).

The gain resistor (R_F) converts I_D to a voltage at V_{OUT}. The combination of R_F, C_D and C_G create a noise gain zero at 22.7 kHz, which would destabilize the feedback loop without an appropriate value of C_F. C_F stabilizes the feedback loop by adding a noise gain pole at 339 kHz and sets the high frequency noise gain to 15.9 V/V.

The feedback loop's crossover frequency is U_1's GBWP divided by the high frequency noise gain, or 629 kHz. Since this is roughly two times larger than the noise gain pole, the feedback loop is robustly stable.

The signal gain has one pole at 339 kHz, which is set by R_F and C_F (the same as the noise gain pole).

Use simulations and bench testing to obtain the design goals. Check step response overshoot for stability and output random noise for accuracy.

Other photo-voltaic detector circuits give different trade-offs. This circuit is faster than a circuit that doesn't need C_F, but requires a much faster op amp. Other implementation details can vary too.

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP60711/1U/3 op amps.

5.1 Analog Demonstration Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchipdirect.com.

5.2 Application Notes

The following Microchip Analog Design Notes and Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **ADN003** – *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **A**N722 – *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723** – *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884** – *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990** – *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1177** – *"Op Amp Precision Design: DC Errors"*, DS01177
- **AN1228** – *"Op Amp Precision Design: Random Noise"*, DS01228
- **AN1297** – *"Microchip's Op Amp SPICE Macro Models"*, DS01297
- **AN1332** – *"Current Sensing Circuit Concepts and Fundamentals"*, DS01332
- **AN1494** – *"Using MCP6491 Op Amps for Photo-detection Applications"*, DS01494

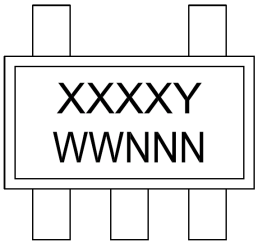
These applications notes and others are listed in the design guide:

- *"Signal Chain Design Guide"*, DS21825

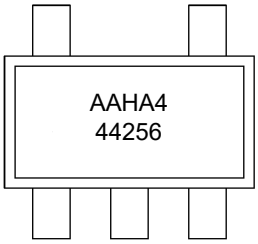
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

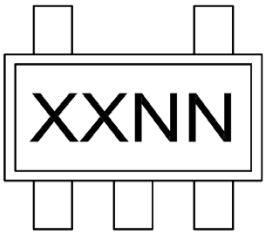
5 Lead SOT-23 (MCP60711)



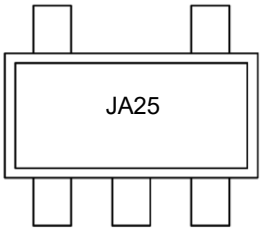
Example:



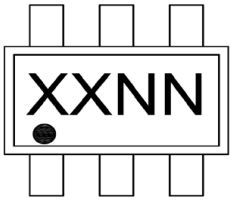
5 Lead SC70 (MCP60711U)



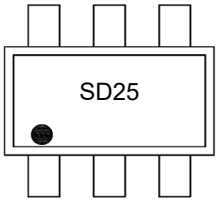
Example:



6 Lead SOT-23 (MCP60713)



Example:

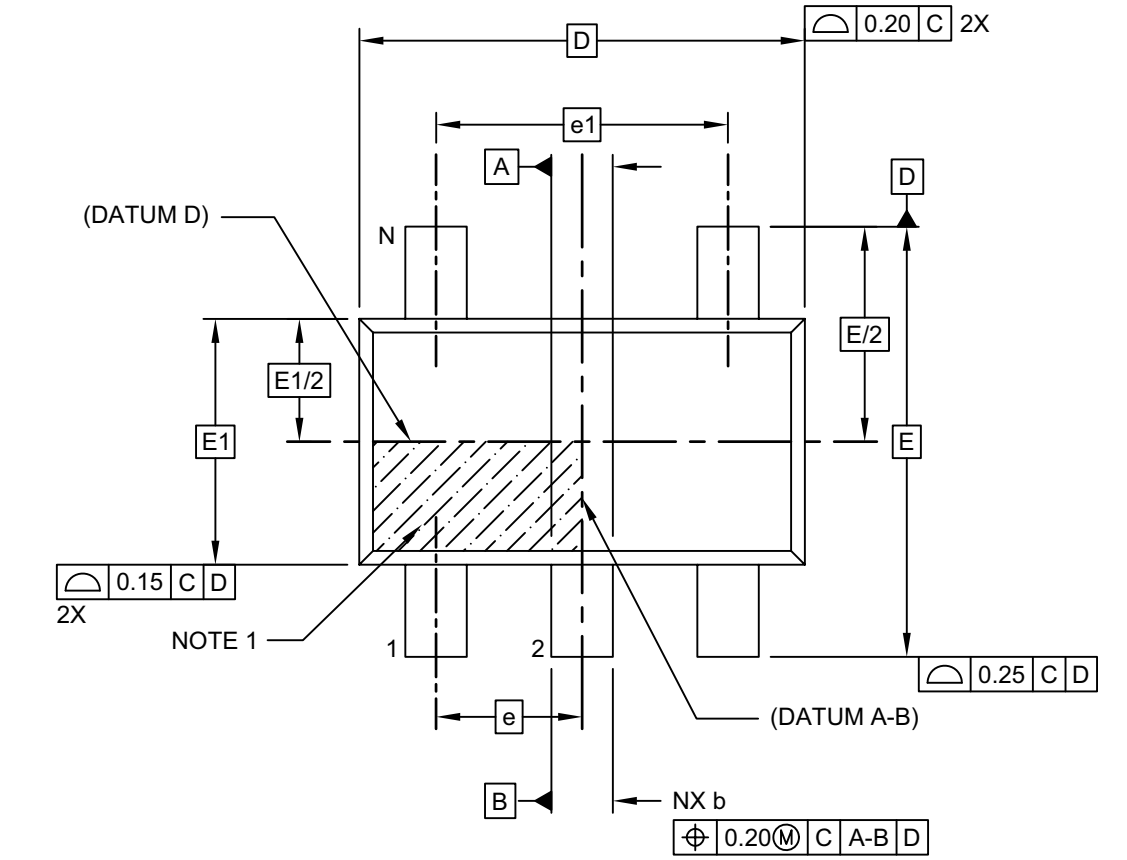


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

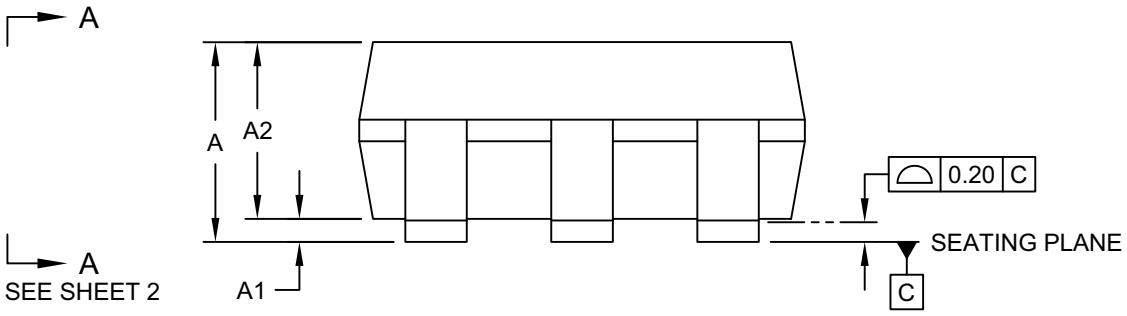
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

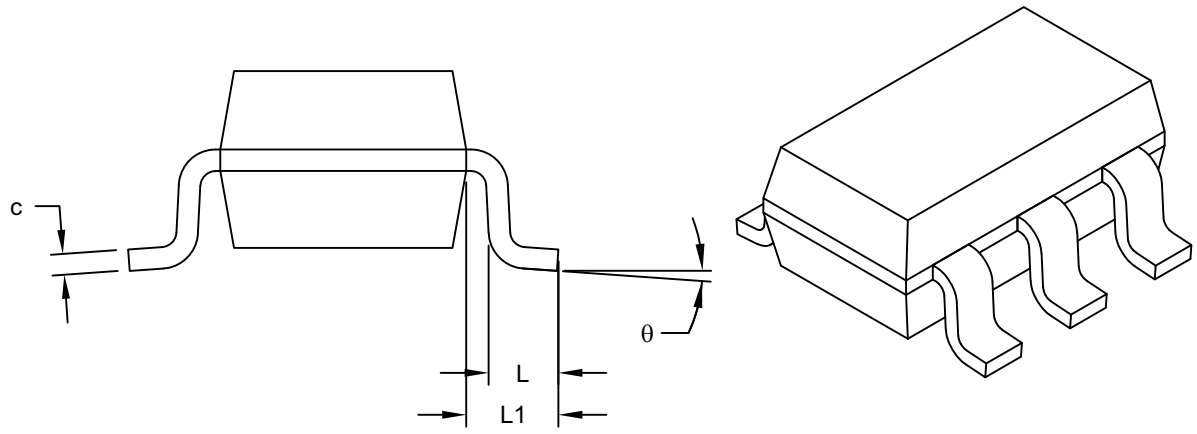


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

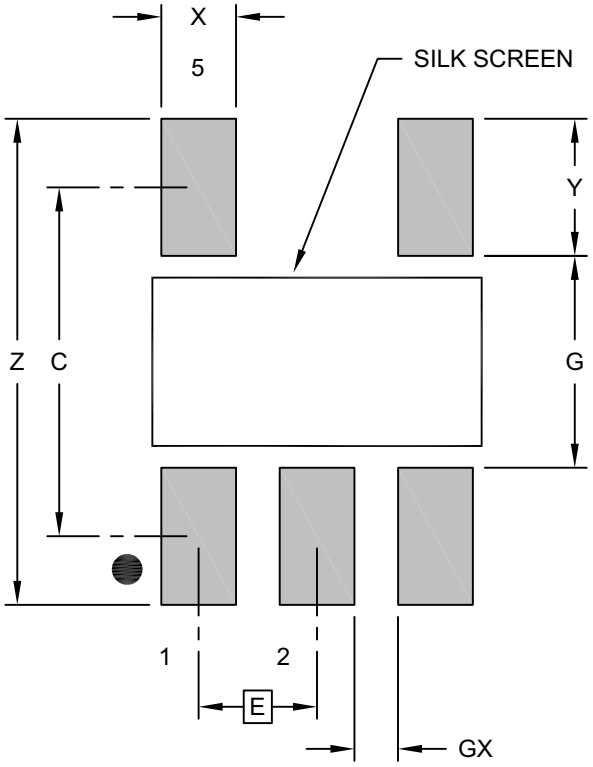
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

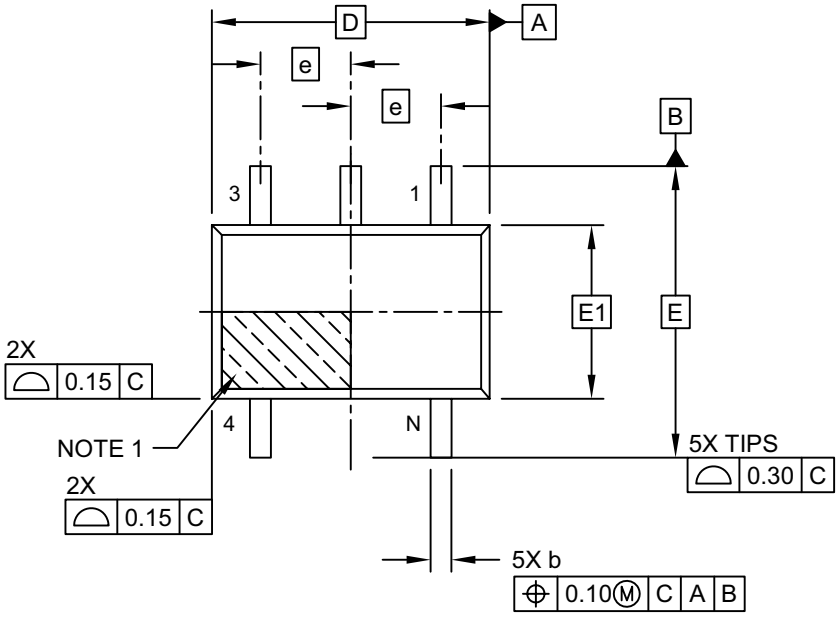
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

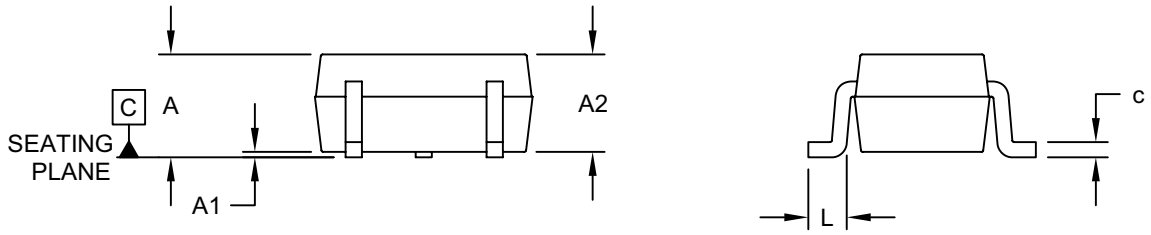
Microchip Technology Drawing No. C04-2091-OT Rev H

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

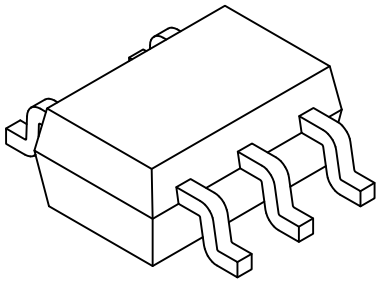


SIDE VIEW END VIEW

Microchip Technology Drawing C04-061-LTY Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

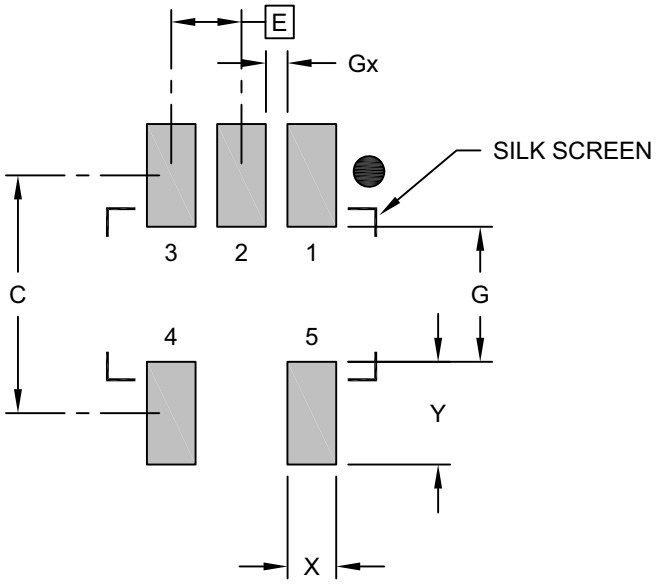
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LTY Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

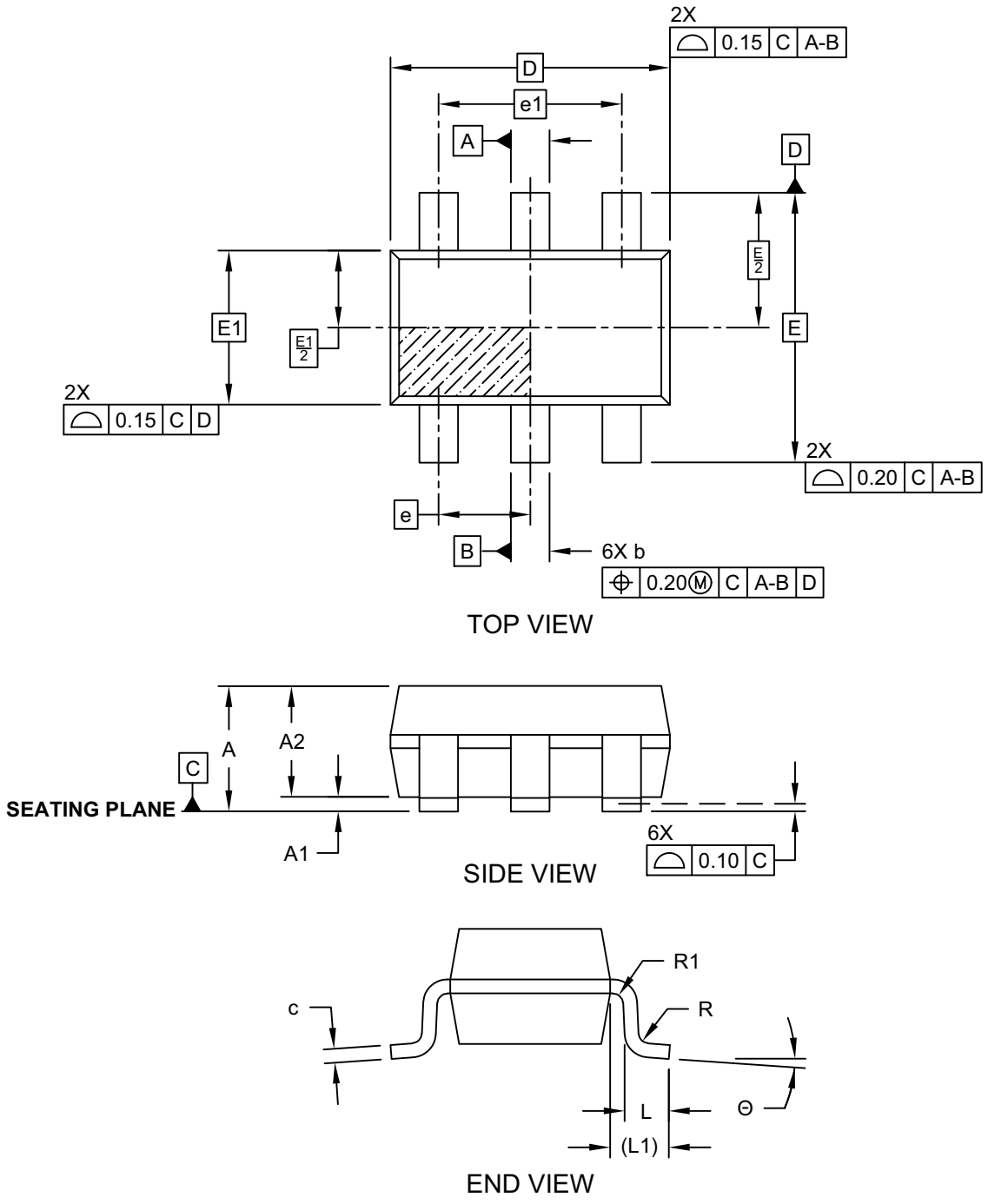
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LTY Rev E

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

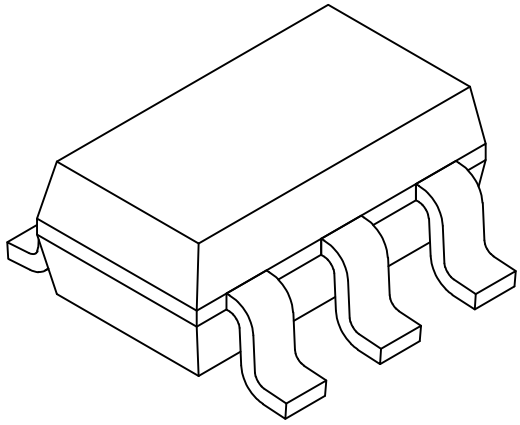
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-028D (CH) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

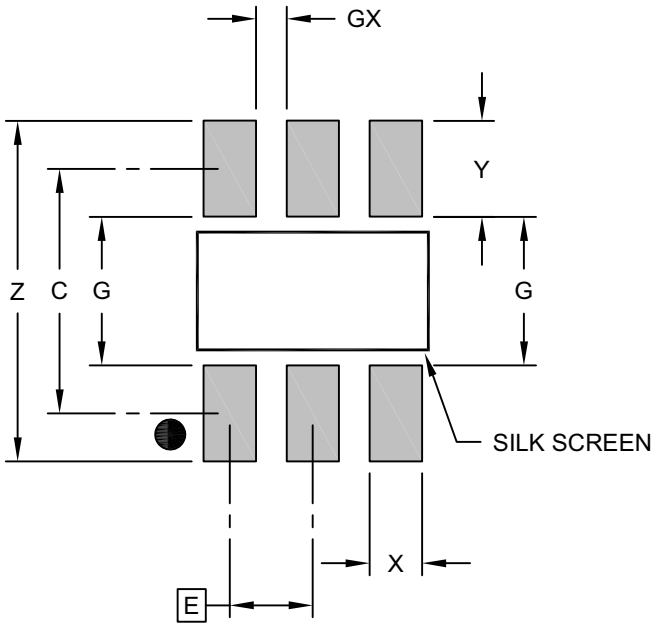
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028D (CH) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028D (CH)

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP60711T	Single Op Amp (Tape and Reel)
	MCP60711UT	Single Op Amp (Tape and Reel)
	MCP60713T	Single Op Amp (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C
Package:	LTY =	Plastic Package (SC70), 5-lead *
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead
	CH =	Plastic Small Outline Transistor (SOT-23), 6-lead

* Y = nickel palladium gold manufacturing designator.

Examples:

a) MCP60711T-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23

b) MCP60711UT-E/LTY: Tape and Reel, Extended temperature, 5LD SC70

c) MCP60713T-E/CH: Tape and Reel, Extended temperature, 6LD SOT-23

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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